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Renesas Electronics Corporation

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## 1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

The data flash ROM (2 KB X 2 blocks) is embedded.

### 1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

## 1.2 Performance Overview

Table 1.1. lists the performance outline of this MCU.

**Table 1.1 Performance outline**

| Item                       |                                     | Performance                                                                                                                                                                                                                                                   |
|----------------------------|-------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CPU                        | Number of basic instructions        | 89 instructions                                                                                                                                                                                                                                               |
|                            | Minimum instruction execution time  | 50 ns (f(X <sub>IN</sub> ) = 20 MHz, V <sub>CC</sub> = 3.0 to 5.5 V)<br>100 ns (f(X <sub>IN</sub> ) = 10 MHz, V <sub>CC</sub> = 2.7 to 5.5 V)                                                                                                                 |
|                            | Operating mode                      | Single-chip                                                                                                                                                                                                                                                   |
|                            | Address space                       | 1M bytes                                                                                                                                                                                                                                                      |
|                            | Memory capacity                     | See Table 1.2.                                                                                                                                                                                                                                                |
| Peripheral function        | Port                                | Input/Output: 22 (including LED drive port), Input: 2                                                                                                                                                                                                         |
|                            | LED drive port                      | I/O port: 8                                                                                                                                                                                                                                                   |
|                            | Timer                               | Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel,<br>Timer Z: 8 bits x 1 channel<br>(Each timer equipped with 8-bit prescaler)<br>Timer C: 16 bits x 1 channel<br>(Circuits of input capture and output compare)                                      |
|                            | Serial interface                    | •1 channel<br>Clock synchronous, UART<br>•1 channel<br>UART                                                                                                                                                                                                   |
|                            | A/D converter                       | 10-bit A/D converter: 1 circuit, 12 channels                                                                                                                                                                                                                  |
|                            | Watchdog timer                      | 15 bits x 1 (with prescaler)<br>Reset start function selectable                                                                                                                                                                                               |
|                            | Interrupt                           | Internal: 11 factors, External: 5 factors,<br>Software: 4 factors, Priority level: 7 levels                                                                                                                                                                   |
|                            | Clock generation circuit            | 2 circuits<br>•Main clock generation circuit (Equipped with a built-in feedback resistor)<br>•On-chip oscillator (high-speed, low-speed)<br>On high-speed on-chip oscillator the frequency adjustment function is usable.                                     |
|                            | Oscillation stop detection function | Main clock oscillation stop detection function                                                                                                                                                                                                                |
|                            | Voltage detection circuit           | Included                                                                                                                                                                                                                                                      |
|                            | Power on reset circuit              | Included                                                                                                                                                                                                                                                      |
| Electrical characteristics | Supply voltage                      | V <sub>CC</sub> = 3.0 to 5.5V (f(X <sub>IN</sub> ) = 20MHz)<br>V <sub>CC</sub> = 2.7 to 5.5V (f(X <sub>IN</sub> ) = 10MHz)                                                                                                                                    |
|                            | Power consumption                   | Typ.9 mA (V <sub>CC</sub> = 5.0V, (f(X <sub>IN</sub> ) = 20MHz)<br>Typ.5 mA (V <sub>CC</sub> = 3.0V, (f(X <sub>IN</sub> ) = 10MHz)<br>Typ.35 μA (V <sub>CC</sub> = 3.0V, Wait mode, Peripheral clock stops)<br>Typ.0.7 μA (V <sub>CC</sub> = 3.0V, Stop mode) |
| Flash memory               | Program/erase supply voltage        | V <sub>CC</sub> = 2.7 to 5.5 V                                                                                                                                                                                                                                |
|                            | Program/erase endurance             | 10,000 times (Data flash)<br>1,000 times (Program ROM)                                                                                                                                                                                                        |
|                            |                                     | Operating ambient temperature                                                                                                                                                                                                                                 |
|                            |                                     | -20 to 85°C<br>-40 to 85°C (D-version)                                                                                                                                                                                                                        |
| Package                    |                                     | 32-pin plastic mold LOFP                                                                                                                                                                                                                                      |

### 1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

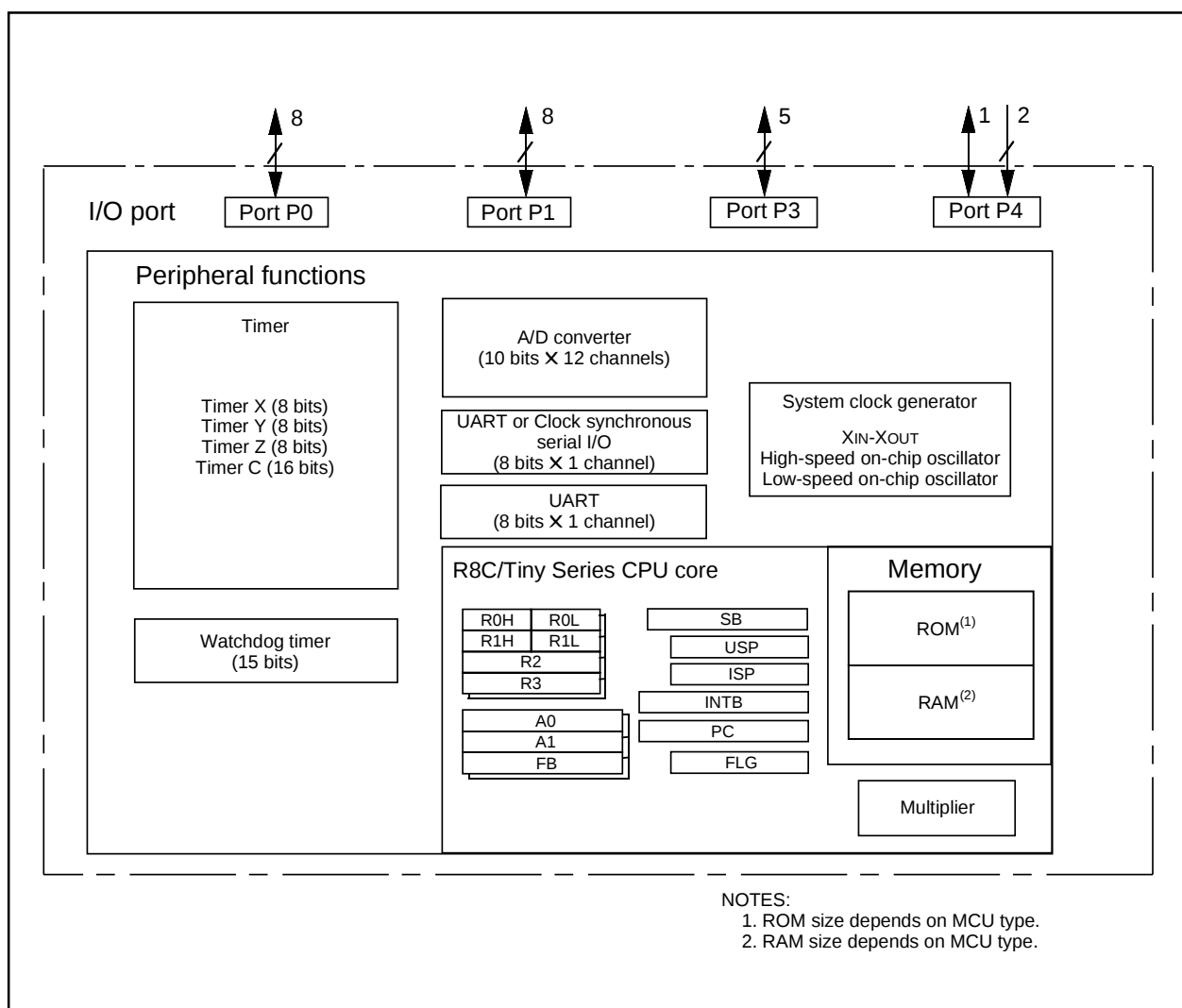


Figure 1.1 Block Diagram

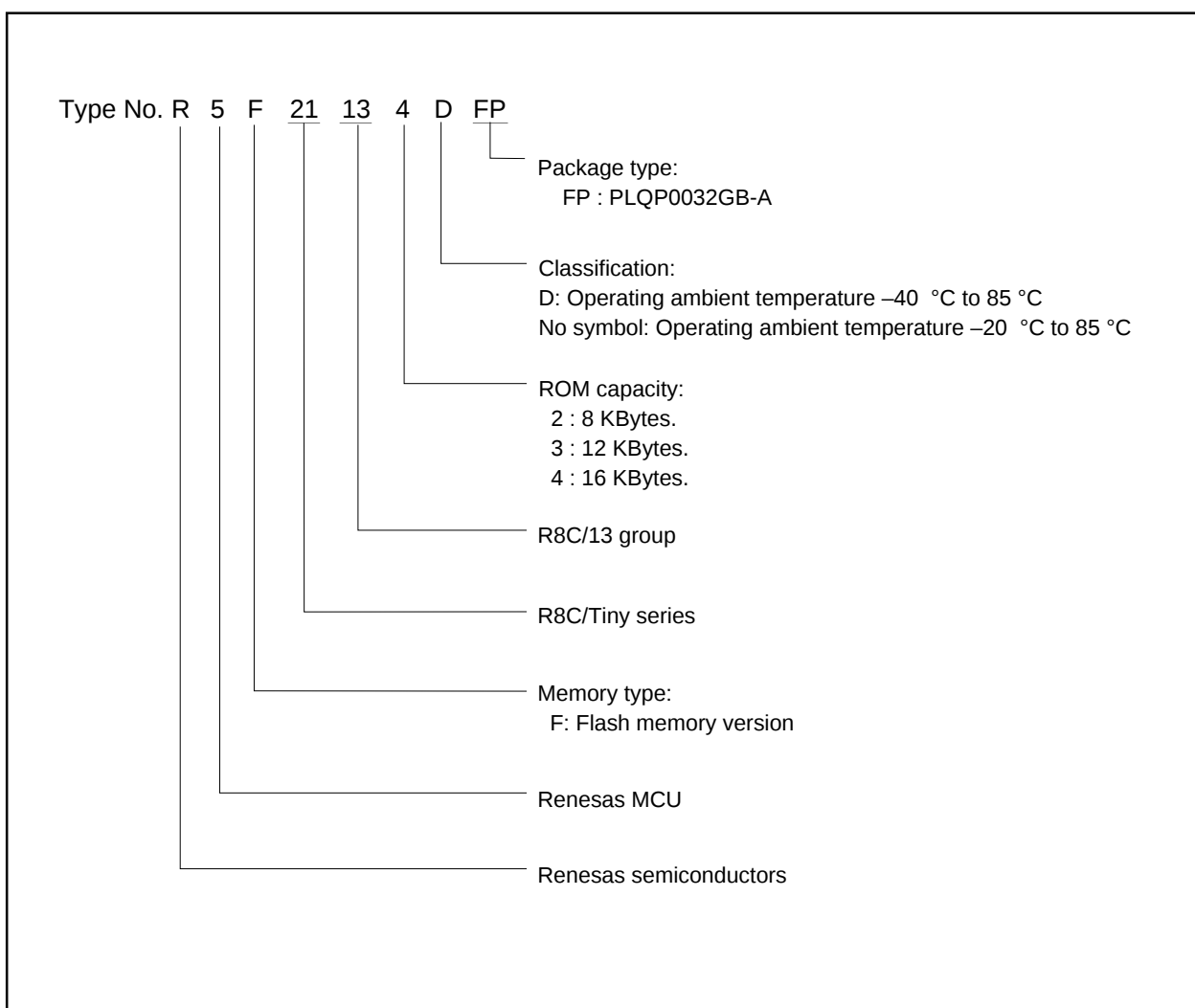
## 1.4 Product Information

Table 1.2 lists the product information.

**Table 1.2 Product Information**

As of January 2006

| Type No.    | ROM capacity |              | RAM capacity | Package type | Remarks              |
|-------------|--------------|--------------|--------------|--------------|----------------------|
|             | Program ROM  | Data flash   |              |              |                      |
| R5F21132FP  | 8K bytes     | 2K bytes x 2 | 512 bytes    | PLQP0032GB-A | Flash memory version |
| R5F21133FP  | 12K bytes    | 2K bytes x 2 | 768 bytes    | PLQP0032GB-A |                      |
| R5F21134FP  | 16K bytes    | 2K bytes x 2 | 1K bytes     | PLQP0032GB-A |                      |
| R5F21132DFP | 8K bytes     | 2K bytes x 2 | 512 bytes    | PLQP0032GB-A | D version            |
| R5F21133DFP | 12K bytes    | 2K bytes x 2 | 768 bytes    | PLQP0032GB-A |                      |
| R5F21134DFP | 16K bytes    | 2K bytes x 2 | 1K bytes     | PLQP0032GB-A |                      |



**Figure 1.2 Type No., Memory Size, and Package**

## 1.5 Pin Assignments

Figure 1.3 shows the pin configuration (top view).

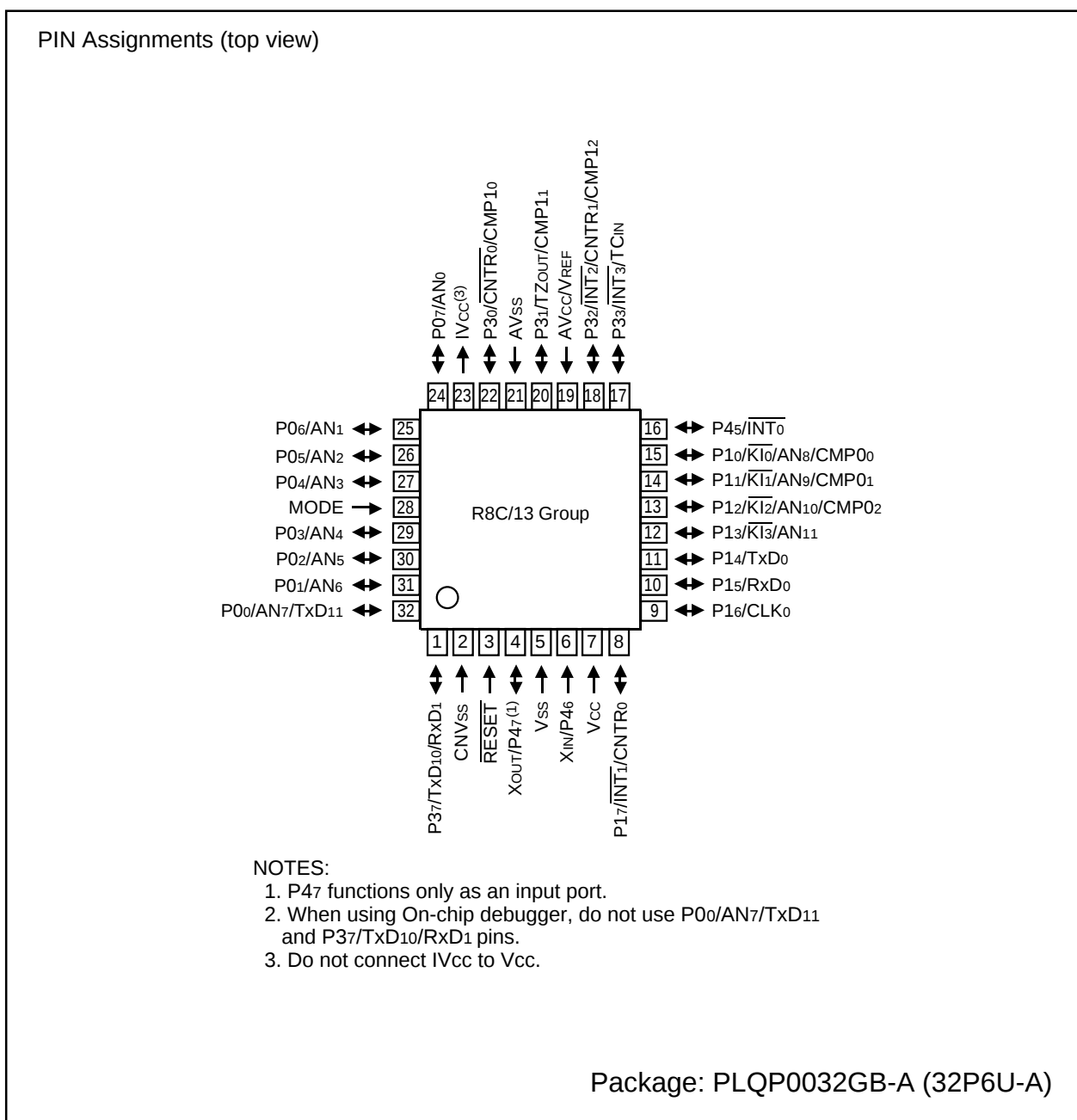


Figure 1.3 Pin Assignments (Top View)

## 1.6 Pin Description

Table 1.3 shows the pin description

**Table 1.3 Pin description**

| Signal name               | Pin name                                     | I/O type | Function                                                                                                                                                                                                                                                                                           |
|---------------------------|----------------------------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Power supply input        | Vcc, Vss                                     | I        | Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.                                                                                                                                                                                                                                     |
| IVcc                      | IVcc                                         | O        | This pin is to stabilize internal power supply. Connect this pin to Vss via a capacitor (0.1 $\mu$ F). Do not connect to Vcc.                                                                                                                                                                      |
| Analog power supply input | AVcc, AVss                                   | I        | Power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.                                                                                                                                               |
| Reset input               | $\overline{\text{RESET}}$                    | I        | Input "L" on this pin resets the MCU.                                                                                                                                                                                                                                                              |
| CNVss                     | CNVss                                        | I        | Connect this pin to Vss via a resistor.                                                                                                                                                                                                                                                            |
| MODE                      | MODE                                         | I        | Connect this pin to Vcc via a resistor.                                                                                                                                                                                                                                                            |
| Main clock input          | XIN                                          | I        | These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.                                                     |
| Main clock output         | XOUT                                         | O        |                                                                                                                                                                                                                                                                                                    |
| INT interrupt input       | INT0 to INT3                                 | I        | INT interrupt input pins.                                                                                                                                                                                                                                                                          |
| Key input interrupt input | KI0 to KI3                                   | I        | Key input interrupt pins.                                                                                                                                                                                                                                                                          |
| Timer X                   | CNTR0                                        | I/O      | Timer X I/O pin                                                                                                                                                                                                                                                                                    |
|                           | CNTR0                                        | O        | Timer X output pin                                                                                                                                                                                                                                                                                 |
| Timer Y                   | CNTR1                                        | I/O      | Timer Y I/O pin                                                                                                                                                                                                                                                                                    |
| Timer Z                   | TZOUT                                        | O        | Timer Z output pin                                                                                                                                                                                                                                                                                 |
| Timer C                   | TCIN                                         | I        | Timer C input pin                                                                                                                                                                                                                                                                                  |
|                           | CMP00 to CMP02, CMP10 to CMP12               | O        | The timer C output pins                                                                                                                                                                                                                                                                            |
| Serial interface          | CLK0                                         | I/O      | Transfer clock I/O pin.                                                                                                                                                                                                                                                                            |
|                           | RxD0, RxD1                                   | I        | Serial data input pins.                                                                                                                                                                                                                                                                            |
|                           | TxD0, TxD10, TxD11                           | O        | Serial data output pins.                                                                                                                                                                                                                                                                           |
| Reference voltage input   | VREF                                         | I        | Reference voltage input pin for A/D converter. Connect the VREF pin to Vcc.                                                                                                                                                                                                                        |
| A/D converter             | AN0 to AN11                                  | I        | Analog input pins for A/D converter                                                                                                                                                                                                                                                                |
| I/O port                  | P00 to P07, P10 to P17, P30 to P33, P37, P45 | I/O      | These are 8-bit CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports. |
| Input port                | P46, P47                                     | I        | Port for input-only                                                                                                                                                                                                                                                                                |

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Register. The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. Two sets of register banks are provided.

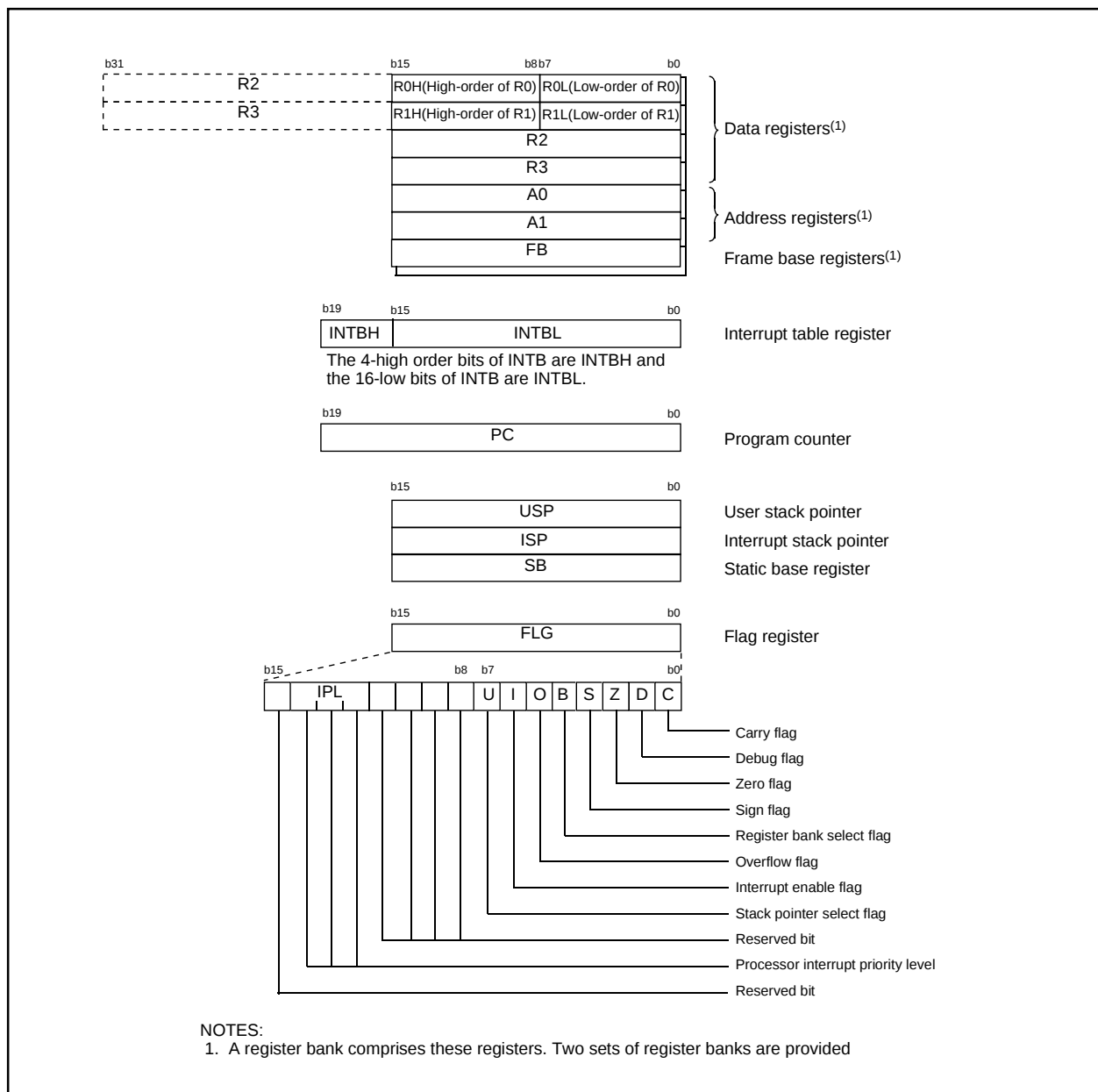


Figure 2.1 CPU Register

### 2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A1 to be used as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each.

The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

### 2.8.3 Zero Flag (Z)

The Z flag is set to "1" when an arithmetic operation resulted in 0; otherwise, "0".

### 2.8.4 Sign Flag (S)

The S flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, "0".

### 2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is "0". The register bank 1 is selected when this flag is set to "1".

### 2.8.6 Overflow Flag (O)

The O flag is set to "1" when the operation resulted in an overflow; otherwise, "0".

### 2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0", and are enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt request is acknowledged.

### 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0", USP is selected when the U flag is set to "1".

The U flag is set to "0" when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

### 2.8.10 Reserved Bit

When write to this bit, set to "0". When read, its content is indeterminate.

### 3. Memory

Figure 3.1 is a memory map of this MCU. This MCU provides 1-Mbyte address space from addresses 00000<sub>16</sub> to FFFFF<sub>16</sub>.

The internal ROM (program ROM) is allocated lower addresses beginning with address 0FFFF<sub>16</sub>. For example, a 16-Kbyte internal ROM is allocated addresses from 0C000<sub>16</sub> to 0FFFF<sub>16</sub>.

The fixed interrupt vector table is allocated addresses 0FFDC<sub>16</sub> to 0FFFF<sub>16</sub>. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses from 02000<sub>16</sub> to 02FFF<sub>16</sub>.

The internal RAM is allocated higher addresses beginning with address 00400<sub>16</sub>. For example, a 1-Kbyte internal RAM is allocated addresses 00400<sub>16</sub> to 007FF<sub>16</sub>. The internal RAM is used not only for storing data, but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000<sub>16</sub> to 002FF<sub>16</sub>. The peripheral function control registers are located there. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.

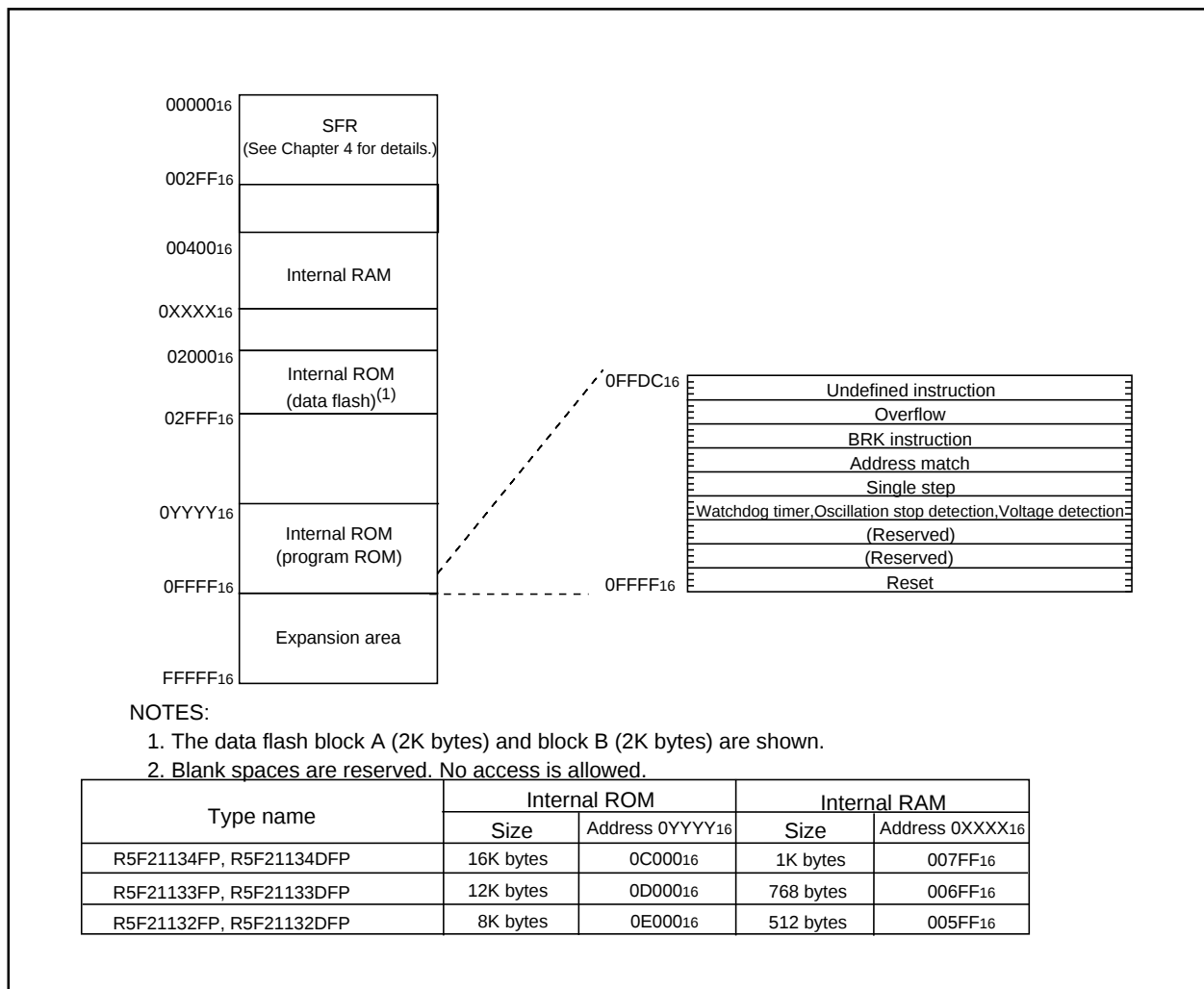


Figure 3.1 Memory Map

## 4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

**Table 4.1 SFR Information(1)(1)**

| Address            | Register                                            | Symbol | After reset                                     |
|--------------------|-----------------------------------------------------|--------|-------------------------------------------------|
| 0000 <sub>16</sub> |                                                     |        |                                                 |
| 0001 <sub>16</sub> |                                                     |        |                                                 |
| 0002 <sub>16</sub> |                                                     |        |                                                 |
| 0003 <sub>16</sub> |                                                     |        |                                                 |
| 0004 <sub>16</sub> | Processor mode register 0 <sup>(1)</sup>            | PM0    | 0016                                            |
| 0005 <sub>16</sub> | Processor mode register 1                           | PM1    | 0016                                            |
| 0006 <sub>16</sub> | System clock control register 0                     | CM0    | 011010002                                       |
| 0007 <sub>16</sub> | System clock control register 1                     | CM1    | 001000002                                       |
| 0008 <sub>16</sub> | High-speed on-chip oscillator control register 0    | HR0    | 0016                                            |
| 0009 <sub>16</sub> | Address match interrupt enable register             | AIER   | XXXXXX002                                       |
| 000A <sub>16</sub> | Protect register                                    | PRCR   | 00XXX0002                                       |
| 000B <sub>16</sub> | High-speed on-chip oscillator control register 1    | HR1    | 4016                                            |
| 000C <sub>16</sub> | Oscillation stop detection register                 | OCD    | 000001002                                       |
| 000D <sub>16</sub> | Watchdog timer reset register                       | WDTR   | XX16                                            |
| 000E <sub>16</sub> | Watchdog timer start register                       | WDTs   | XX16                                            |
| 000F <sub>16</sub> | Watchdog timer control register                     | WDC    | 000111112                                       |
| 0010 <sub>16</sub> | Address match interrupt register 0                  | RMAD0  | 0016                                            |
| 0011 <sub>16</sub> |                                                     |        | 0016                                            |
| 0012 <sub>16</sub> |                                                     |        | X016                                            |
| 0013 <sub>16</sub> |                                                     |        |                                                 |
| 0014 <sub>16</sub> | Address match interrupt register 1                  | RMAD1  | 0016                                            |
| 0015 <sub>16</sub> |                                                     |        | 0016                                            |
| 0016 <sub>16</sub> |                                                     |        | X016                                            |
| 0017 <sub>16</sub> |                                                     |        |                                                 |
| 0018 <sub>16</sub> |                                                     |        |                                                 |
| 0019 <sub>16</sub> | Voltage detection register 1 <sup>(2)</sup>         | VCR1   | 000010002                                       |
| 001A <sub>16</sub> | Voltage detection register 2 <sup>(2)</sup>         | VCR2   | 0016 <sup>(3)</sup><br>100000002 <sup>(4)</sup> |
| 001B <sub>16</sub> |                                                     |        |                                                 |
| 001C <sub>16</sub> |                                                     |        |                                                 |
| 001D <sub>16</sub> |                                                     |        |                                                 |
| 001E <sub>16</sub> | INT0 input filter select register                   | INT0F  | XXXXX0002                                       |
| 001F <sub>16</sub> | Voltage detection interrupt register <sup>(2)</sup> | D4INT  | 0016 <sup>(3)</sup><br>010000012 <sup>(4)</sup> |
| 0020 <sub>16</sub> |                                                     |        |                                                 |
| 0021 <sub>16</sub> |                                                     |        |                                                 |
| 0022 <sub>16</sub> |                                                     |        |                                                 |
| 0023 <sub>16</sub> |                                                     |        |                                                 |
| 0024 <sub>16</sub> |                                                     |        |                                                 |
| 0025 <sub>16</sub> |                                                     |        |                                                 |
| 0026 <sub>16</sub> |                                                     |        |                                                 |
| 0027 <sub>16</sub> |                                                     |        |                                                 |
| 0028 <sub>16</sub> |                                                     |        |                                                 |
| 0029 <sub>16</sub> |                                                     |        |                                                 |
| 002A <sub>16</sub> |                                                     |        |                                                 |
| 002B <sub>16</sub> |                                                     |        |                                                 |
| 002C <sub>16</sub> |                                                     |        |                                                 |
| 002D <sub>16</sub> |                                                     |        |                                                 |
| 002E <sub>16</sub> |                                                     |        |                                                 |
| 002F <sub>16</sub> |                                                     |        |                                                 |
| 0030 <sub>16</sub> |                                                     |        |                                                 |
| 0031 <sub>16</sub> |                                                     |        |                                                 |
| 0032 <sub>16</sub> |                                                     |        |                                                 |
| 0033 <sub>16</sub> |                                                     |        |                                                 |
| 0034 <sub>16</sub> |                                                     |        |                                                 |
| 0035 <sub>16</sub> |                                                     |        |                                                 |
| 0036 <sub>16</sub> |                                                     |        |                                                 |
| 0037 <sub>16</sub> |                                                     |        |                                                 |
| 0038 <sub>16</sub> |                                                     |        |                                                 |
| 0039 <sub>16</sub> |                                                     |        |                                                 |
| 003A <sub>16</sub> |                                                     |        |                                                 |
| 003B <sub>16</sub> |                                                     |        |                                                 |
| 003C <sub>16</sub> |                                                     |        |                                                 |
| 003D <sub>16</sub> |                                                     |        |                                                 |
| 003E <sub>16</sub> |                                                     |        |                                                 |
| 003F <sub>16</sub> |                                                     |        |                                                 |

X : Undefined

NOTES:

- Blank spaces are reserved. No access is allowed.
- Software reset or the watchdog timer reset does not affect this register.
- Owing to Reset input.
- In the case of RESET pin = H retaining.

**Table 4.2 SFR Information(2)<sup>(1)</sup>**

| Address            | Register                                  | Symbol | After reset |
|--------------------|-------------------------------------------|--------|-------------|
| 0040 <sub>16</sub> |                                           |        |             |
| 0041 <sub>16</sub> |                                           |        |             |
| 0042 <sub>16</sub> |                                           |        |             |
| 0043 <sub>16</sub> |                                           |        |             |
| 0044 <sub>16</sub> |                                           |        |             |
| 0045 <sub>16</sub> |                                           |        |             |
| 0046 <sub>16</sub> |                                           |        |             |
| 0047 <sub>16</sub> |                                           |        |             |
| 0048 <sub>16</sub> |                                           |        |             |
| 0049 <sub>16</sub> |                                           |        |             |
| 004A <sub>16</sub> |                                           |        |             |
| 004B <sub>16</sub> |                                           |        |             |
| 004C <sub>16</sub> |                                           |        |             |
| 004D <sub>16</sub> | Key input interrupt control register      | KUPIC  | XXXXX0002   |
| 004E <sub>16</sub> | AD conversion interrupt control register  | ADIC   | XXXXX0002   |
| 004F <sub>16</sub> |                                           |        |             |
| 0050 <sub>16</sub> | Compare 1 interrupt control register      | CMP1IC | XXXXX0002   |
| 0051 <sub>16</sub> | UART0 transmit interrupt control register | S0TIC  | XXXXX0002   |
| 0052 <sub>16</sub> | UART0 receive interrupt control register  | S0RIC  | XXXXX0002   |
| 0053 <sub>16</sub> | UART1 transmit interrupt control register | S1TIC  | XXXXX0002   |
| 0054 <sub>16</sub> | UART1 receive interrupt control register  | S1RIC  | XXXXX0002   |
| 0055 <sub>16</sub> | INT2 interrupt control register           | INT2IC | XXXXX0002   |
| 0056 <sub>16</sub> | Timer X interrupt control register        | TXIC   | XXXXX0002   |
| 0057 <sub>16</sub> | Timer Y interrupt control register        | TYIC   | XXXXX0002   |
| 0058 <sub>16</sub> | Timer Z interrupt control register        | TZIC   | XXXXX0002   |
| 0059 <sub>16</sub> | INT1 interrupt control register           | INT1IC | XXXXX0002   |
| 005A <sub>16</sub> | INT3 interrupt control register           | INT3IC | XXXXX0002   |
| 005B <sub>16</sub> | Timer C interrupt control register        | TCIC   | XXXXX0002   |
| 005C <sub>16</sub> | Compare 0 interrupt control register      | CMP0IC | XXXXX0002   |
| 005D <sub>16</sub> | INT0 interrupt control register           | INT0IC | XX00X0002   |
| 005E <sub>16</sub> |                                           |        |             |
| 005F <sub>16</sub> |                                           |        |             |
| 0060 <sub>16</sub> |                                           |        |             |
| 0061 <sub>16</sub> |                                           |        |             |
| 0062 <sub>16</sub> |                                           |        |             |
| 0063 <sub>16</sub> |                                           |        |             |
| 0064 <sub>16</sub> |                                           |        |             |
| 0065 <sub>16</sub> |                                           |        |             |
| 0066 <sub>16</sub> |                                           |        |             |
| 0067 <sub>16</sub> |                                           |        |             |
| 0068 <sub>16</sub> |                                           |        |             |
| 0069 <sub>16</sub> |                                           |        |             |
| 006A <sub>16</sub> |                                           |        |             |
| 006B <sub>16</sub> |                                           |        |             |
| 006C <sub>16</sub> |                                           |        |             |
| 006D <sub>16</sub> |                                           |        |             |
| 006E <sub>16</sub> |                                           |        |             |
| 006F <sub>16</sub> |                                           |        |             |
| 0070 <sub>16</sub> |                                           |        |             |
| 0071 <sub>16</sub> |                                           |        |             |
| 0072 <sub>16</sub> |                                           |        |             |
| 0073 <sub>16</sub> |                                           |        |             |
| 0074 <sub>16</sub> |                                           |        |             |
| 0075 <sub>16</sub> |                                           |        |             |
| 0076 <sub>16</sub> |                                           |        |             |
| 0077 <sub>16</sub> |                                           |        |             |
| 0078 <sub>16</sub> |                                           |        |             |
| 0079 <sub>16</sub> |                                           |        |             |
| 007A <sub>16</sub> |                                           |        |             |
| 007B <sub>16</sub> |                                           |        |             |
| 007C <sub>16</sub> |                                           |        |             |
| 007D <sub>16</sub> |                                           |        |             |
| 007E <sub>16</sub> |                                           |        |             |
| 007F <sub>16</sub> |                                           |        |             |

X : Undefined

NOTES:

1. Blank spaces are reserved. No access is allowed.

Table 4.3 SFR Information(3)(1)

| Address            | Register                                    | Symbol | After reset         |
|--------------------|---------------------------------------------|--------|---------------------|
| 0080 <sub>16</sub> | Timer Y, Z mode register                    | TYZMR  | 0016                |
| 0081 <sub>16</sub> | Prescaler Y register                        | PREY   | FF16                |
| 0082 <sub>16</sub> | Timer Y secondary register                  | TYSC   | FF16                |
| 0083 <sub>16</sub> | Timer Y primary register                    | TYPR   | FF16                |
| 0084 <sub>16</sub> | Timer Y, Z waveform output control register | PUM    | 0016                |
| 0085 <sub>16</sub> | Prescaler Z register                        | PREZ   | FF16                |
| 0086 <sub>16</sub> | Timer Z secondary register                  | TZSC   | FF16                |
| 0087 <sub>16</sub> | Timer Z primary register                    | TZPR   | FF16                |
| 0088 <sub>16</sub> |                                             |        |                     |
| 0089 <sub>16</sub> |                                             |        |                     |
| 008A <sub>16</sub> | Timer Y, Z output control register          | TYZOC  | 0016                |
| 008B <sub>16</sub> | Timer X mode register                       | TXMR   | 0016                |
| 008C <sub>16</sub> | Prescaler X register                        | PREX   | FF16                |
| 008D <sub>16</sub> | Timer X register                            | TX     | FF16                |
| 008E <sub>16</sub> | Count source set register                   | TCSS   | 0016                |
| 008F <sub>16</sub> |                                             |        |                     |
| 0090 <sub>16</sub> | Timer C register                            | TC     | 0016                |
| 0091 <sub>16</sub> |                                             |        | 0016                |
| 0092 <sub>16</sub> |                                             |        |                     |
| 0093 <sub>16</sub> |                                             |        |                     |
| 0094 <sub>16</sub> |                                             |        |                     |
| 0095 <sub>16</sub> |                                             |        |                     |
| 0096 <sub>16</sub> | External input enable register              | INTEN  | 0016                |
| 0097 <sub>16</sub> |                                             |        |                     |
| 0098 <sub>16</sub> | Key input enable register                   | KIEN   | 0016                |
| 0099 <sub>16</sub> |                                             |        |                     |
| 009A <sub>16</sub> | Timer C control register 0                  | TCC0   | 0016                |
| 009B <sub>16</sub> | Timer C control register 1                  | TCC1   | 0016                |
| 009C <sub>16</sub> | Capture, compare 0 register                 | TM0    | 0016                |
| 009D <sub>16</sub> |                                             |        | 0016 <sup>(2)</sup> |
| 009E <sub>16</sub> | Compare 1 register                          | TM1    | FF16                |
| 009F <sub>16</sub> |                                             |        | FF16                |
| 00A0 <sub>16</sub> | UART0 transmit/receive mode register        | U0MR   | 0016                |
| 00A1 <sub>16</sub> | UART0 bit rate register                     | U0BRG  | XX16                |
| 00A2 <sub>16</sub> | UART0 transmit buffer register              | U0TB   | XX16                |
| 00A3 <sub>16</sub> |                                             |        | XX16                |
| 00A4 <sub>16</sub> | UART0 transmit/receive control register 0   | U0C0   | 000010002           |
| 00A5 <sub>16</sub> | UART0 transmit/receive control register 1   | U0C1   | 000000102           |
| 00A6 <sub>16</sub> | UART0 receive buffer register               | U0RB   | XX16                |
| 00A7 <sub>16</sub> |                                             |        | XX16                |
| 00A8 <sub>16</sub> | UART1 transmit/receive mode register        | U1MR   | 0016                |
| 00A9 <sub>16</sub> | UART1 bit rate register                     | U1BRG  | XX16                |
| 00AA <sub>16</sub> | UART1 transmit buffer register              | U1TB   | XX16                |
| 00AB <sub>16</sub> |                                             |        | XX16                |
| 00AC <sub>16</sub> | UART1 transmit/receive control register 0   | U1C0   | 000010002           |
| 00AD <sub>16</sub> | UART1 transmit/receive control register 1   | U1C1   | 000000102           |
| 00AE <sub>16</sub> | UART1 receive buffer register               | U1RB   | XX16                |
| 00AF <sub>16</sub> |                                             |        | XX16                |
| 00B0 <sub>16</sub> | UART transmit/receive control register 2    | UCON   | 0016                |
| 00B1 <sub>16</sub> |                                             |        |                     |
| 00B2 <sub>16</sub> |                                             |        |                     |
| 00B3 <sub>16</sub> |                                             |        |                     |
| 00B4 <sub>16</sub> |                                             |        |                     |
| 00B5 <sub>16</sub> |                                             |        |                     |
| 00B6 <sub>16</sub> |                                             |        |                     |
| 00B7 <sub>16</sub> |                                             |        |                     |
| 00B8 <sub>16</sub> |                                             |        |                     |
| 00B9 <sub>16</sub> |                                             |        |                     |
| 00BA <sub>16</sub> |                                             |        |                     |
| 00BB <sub>16</sub> |                                             |        |                     |
| 00BC <sub>16</sub> |                                             |        |                     |
| 00BD <sub>16</sub> |                                             |        |                     |
| 00BE <sub>16</sub> |                                             |        |                     |
| 00BF <sub>16</sub> |                                             |        |                     |

X : Undefined

## NOTES:

1. Blank spaces are reserved. No access is allowed.

2. When output compare mode (the TCC13 bit in the TCC1 register = 1) is selected, the value after reset is set to "FFFF16".

Table 4.4 SFR Information(4)(1)

| Address                                  | Register                                | Symbol | After reset  |
|------------------------------------------|-----------------------------------------|--------|--------------|
| 00C0 <sub>16</sub><br>00C1 <sub>16</sub> | AD register                             | AD     | XX16<br>XX16 |
| 00C2 <sub>16</sub>                       |                                         |        |              |
| 00C3 <sub>16</sub>                       |                                         |        |              |
| 00C4 <sub>16</sub>                       |                                         |        |              |
| 00C5 <sub>16</sub>                       |                                         |        |              |
| 00C6 <sub>16</sub>                       |                                         |        |              |
| 00C7 <sub>16</sub>                       |                                         |        |              |
| 00C8 <sub>16</sub>                       |                                         |        |              |
| 00C9 <sub>16</sub>                       |                                         |        |              |
| 00CA <sub>16</sub>                       |                                         |        |              |
| 00CB <sub>16</sub>                       |                                         |        |              |
| 00CC <sub>16</sub>                       |                                         |        |              |
| 00CD <sub>16</sub>                       |                                         |        |              |
| 00CE <sub>16</sub>                       |                                         |        |              |
| 00CF <sub>16</sub>                       |                                         |        |              |
| 00D0 <sub>16</sub>                       |                                         |        |              |
| 00D1 <sub>16</sub>                       |                                         |        |              |
| 00D2 <sub>16</sub>                       |                                         |        |              |
| 00D3 <sub>16</sub>                       |                                         |        |              |
| 00D4 <sub>16</sub><br>00D5 <sub>16</sub> | AD control register 2                   | ADCON2 | 0016         |
| 00D6 <sub>16</sub><br>00D7 <sub>16</sub> | AD control register 0                   | ADCON0 | 00000XXX2    |
| 00D8 <sub>16</sub><br>00D9 <sub>16</sub> | AD control register 1                   | ADCON1 | 0016         |
| 00DA <sub>16</sub>                       |                                         |        |              |
| 00DB <sub>16</sub>                       |                                         |        |              |
| 00DC <sub>16</sub>                       |                                         |        |              |
| 00DD <sub>16</sub>                       |                                         |        |              |
| 00DE <sub>16</sub>                       |                                         |        |              |
| 00DF <sub>16</sub>                       |                                         |        |              |
| 00E0 <sub>16</sub><br>00E1 <sub>16</sub> | Port P0 register                        | P0     | XX16         |
| 00E2 <sub>16</sub><br>00E3 <sub>16</sub> | Port P1 register                        | P1     | XX16         |
| 00E4 <sub>16</sub><br>00E5 <sub>16</sub> | Port P0 direction register              | PD0    | 0016         |
| 00E6 <sub>16</sub><br>00E7 <sub>16</sub> | Port P1 direction register              | PD1    | 0016         |
| 00E8 <sub>16</sub>                       |                                         |        |              |
| 00E9 <sub>16</sub><br>00EA <sub>16</sub> | Port P3 register                        | P3     | XX16         |
| 00EB <sub>16</sub><br>00EC <sub>16</sub> |                                         |        |              |
| 00ED <sub>16</sub><br>00EE <sub>16</sub> | Port P3 direction register              | PD3    | 0016         |
| 00EF <sub>16</sub><br>00F0 <sub>16</sub> | Port P4 register                        | P4     | XX16         |
| 00F1 <sub>16</sub><br>00F2 <sub>16</sub> |                                         |        |              |
| 00F3 <sub>16</sub><br>00F4 <sub>16</sub> | Port P4 direction register              | PD4    | 0016         |
| 00F5 <sub>16</sub>                       |                                         |        |              |
| 00F6 <sub>16</sub>                       |                                         |        |              |
| 00F7 <sub>16</sub>                       |                                         |        |              |
| 00F8 <sub>16</sub>                       |                                         |        |              |
| 00F9 <sub>16</sub>                       |                                         |        |              |
| 03FA <sub>16</sub>                       |                                         |        |              |
| 00FB <sub>16</sub>                       |                                         |        |              |
| 00FC <sub>16</sub><br>00FD <sub>16</sub> | Pull-up control register 0              | PUR0   | 00XX00002    |
| 00FE <sub>16</sub><br>00FF <sub>16</sub> | Pull-up control register 1              | PUR1   | XXXXXX0X2    |
|                                          | Port P1 drive capacity control register | DRR    | 0016         |
|                                          | Timer C output control register         | TCOUT  | 0016         |
|                                          |                                         |        |              |
| 01B3 <sub>16</sub><br>01B4 <sub>16</sub> | Flash memory control register 4         | FMR4   | 010000002    |
| 01B5 <sub>16</sub><br>01B6 <sub>16</sub> | Flash memory control register 1         | FMR1   | 1000000X2    |
| 01B7 <sub>16</sub>                       | Flash memory control register 0         | FMR0   | 000000012    |
| 0FFF <sub>16</sub>                       | Option function select register(2)      | OFS    | (Note 2)     |

X : Undefined

## NOTES:

1. Blank columns, 0100<sub>16</sub> to 01B2<sub>16</sub> and 01B8<sub>16</sub> to 02FF<sub>16</sub> are all reserved. No access is allowed.

2. The watchdog timer control bit is assigned. Refer to "Figure11.2 OFS, WDC, WDTR and WDTS registers" of Hardware Manual for details

## 5. Electrical Characteristics

**Table 5.1 Absolute Maximum Ratings**

| Symbol           | Parameter                     | Condition                         | Rated value                       | Unit |
|------------------|-------------------------------|-----------------------------------|-----------------------------------|------|
| V <sub>CC</sub>  | Supply voltage                | V <sub>CC</sub> =AV <sub>CC</sub> | -0.3 to 6.5                       | V    |
| AV <sub>CC</sub> | Analog supply voltage         | V <sub>CC</sub> =AV <sub>CC</sub> | -0.3 to 6.5                       | V    |
| V <sub>I</sub>   | Input voltage                 |                                   | -0.3 to V <sub>CC</sub> +0.3      | V    |
| V <sub>O</sub>   | Output voltage                |                                   | -0.3 to V <sub>CC</sub> +0.3      | V    |
| P <sub>d</sub>   | Power dissipation             | T <sub>opr</sub> =25 °C           | 300                               | mW   |
| T <sub>opr</sub> | Operating ambient temperature |                                   | -20 to 85 / -40 to 85 (D version) | °C   |
| T <sub>stg</sub> | Storage temperature           |                                   | -65 to 150                        | °C   |

**Table 5.2 Recommended Operating Conditions**

| Symbol                 | Parameter                              | Conditions                              | Standard           |                     |                    | Unit |
|------------------------|----------------------------------------|-----------------------------------------|--------------------|---------------------|--------------------|------|
|                        |                                        |                                         | Min.               | Typ.                | Max.               |      |
| V <sub>CC</sub>        | Supply voltage                         |                                         | 2.7                | —                   | 5.5                | V    |
| AV <sub>CC</sub>       | Analog supply voltage                  |                                         | —                  | V <sub>CC</sub> (3) | —                  | V    |
| V <sub>SS</sub>        | Supply voltage                         |                                         | —                  | 0                   | —                  | V    |
| AV <sub>SS</sub>       | Analog supply voltage                  |                                         | —                  | 0                   | —                  | V    |
| V <sub>IH</sub>        | "H" input voltage                      |                                         | 0.8V <sub>CC</sub> | —                   | V <sub>CC</sub>    | V    |
| V <sub>IL</sub>        | "L" input voltage                      |                                         | 0                  | —                   | 0.2V <sub>CC</sub> | V    |
| I <sub>OH</sub> (sum)  | "H" peak all output currents           | Sum of all pins' I <sub>OH</sub> (peak) | —                  | —                   | -60.0              | mA   |
| I <sub>OH</sub> (peak) | "H" peak output current                |                                         | —                  | —                   | -10.0              | mA   |
| I <sub>OH</sub> (avg)  | "H" average output current             |                                         | —                  | —                   | -5.0               | mA   |
| I <sub>OL</sub> (sum)  | "L" peak all output currents           | Sum of all pins' I <sub>OL</sub> (peak) | —                  | —                   | 60                 | mA   |
| I <sub>OL</sub> (peak) | "L" peak output current                | Except P10 to P17                       | —                  | —                   | 10                 | mA   |
|                        |                                        | P10 to P17                              | —                  | —                   | 30                 | mA   |
|                        |                                        | Drive ability LOW                       | —                  | —                   | 10                 | mA   |
| I <sub>OL</sub> (avg)  | "L" average output current             | Except P10 to P17                       | —                  | —                   | 5                  | mA   |
|                        |                                        | P10 to P17                              | —                  | —                   | 15                 | mA   |
|                        |                                        | Drive ability LOW                       | —                  | —                   | 5                  | mA   |
| f (X <sub>IN</sub> )   | Main clock input oscillation frequency | 3.0V ≤ V <sub>CC</sub> ≤ 5.5V           | 0                  | —                   | 20                 | MHz  |
|                        |                                        | 2.7V ≤ V <sub>CC</sub> < 3.0V           | 0                  | —                   | 10                 | MHz  |

**NOTES:**

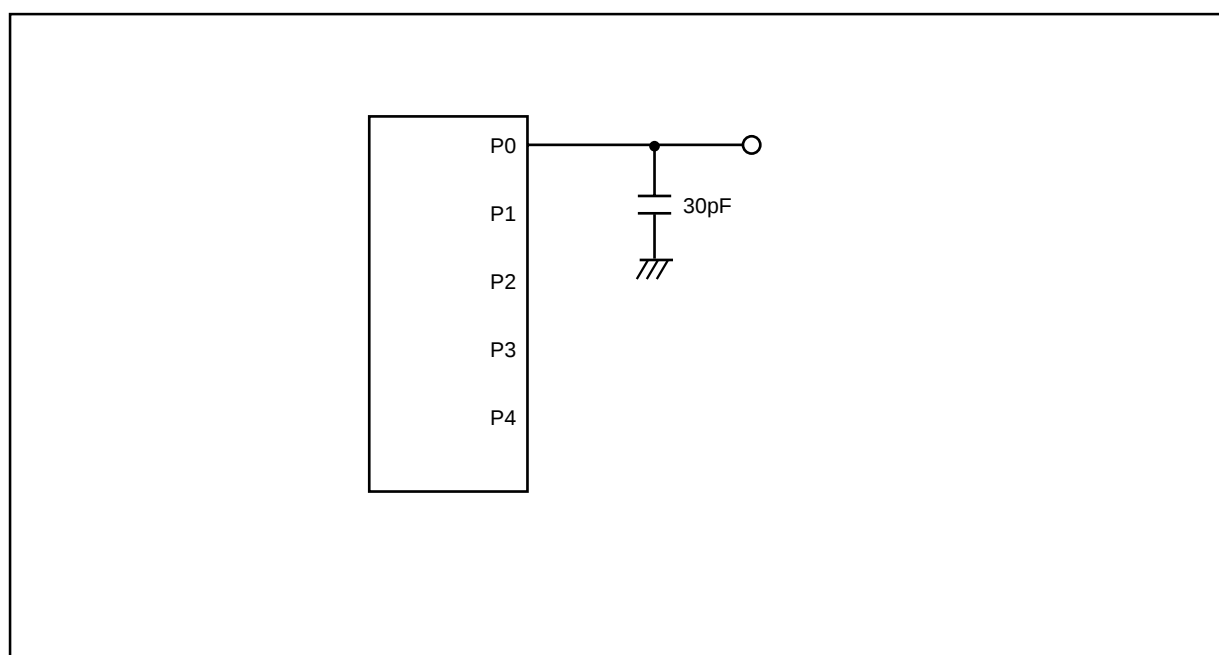
1. V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 to 5.5V at T<sub>opr</sub> = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. The typical values when average output current is 100ms.
3. Hold V<sub>CC</sub>=AV<sub>CC</sub>.

**Table 5.3 A/D Conversion Characteristics**

| Symbol       | Parameter                                    |                       | Measuring condition                                                     | Standard |                |           | Unit          |
|--------------|----------------------------------------------|-----------------------|-------------------------------------------------------------------------|----------|----------------|-----------|---------------|
|              |                                              |                       |                                                                         | Min.     | Typ.           | Max.      |               |
| —            | Resolution                                   |                       | $V_{ref} = V_{CC}$                                                      | —        | —              | 10        | Bit           |
| —            | Absolute accuracy                            | 10 bit mode           | $\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 5.0 \text{ V}$       | —        | —              | $\pm 3$   | LSB           |
|              |                                              | 8 bit mode            | $\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 5.0 \text{ V}$       | —        | —              | $\pm 2$   | LSB           |
|              |                                              | 10 bit mode           | $\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 3.3 \text{ V}^{(3)}$ | —        | —              | $\pm 5$   | LSB           |
|              |                                              | 8 bit mode            | $\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 3.3 \text{ V}^{(3)}$ | —        | —              | $\pm 2$   | LSB           |
| $R_{LADDER}$ | Ladder resistance                            |                       | $V_{REF} = V_{CC}$                                                      | 10       | —              | 40        | $k\Omega$     |
| $t_{CONV}$   | Conversion time                              | 10 bit mode           | $\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 5.0 \text{ V}$       | 3.3      | —              | —         | $\mu\text{s}$ |
|              |                                              | 8 bit mode            | $\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 5.0 \text{ V}$       | 2.8      | —              | —         | $\mu\text{s}$ |
| $V_{REF}$    | Reference voltage                            |                       |                                                                         | —        | $V_{CC}^{(4)}$ | —         | V             |
| $V_{IA}$     | Analog input voltage                         |                       |                                                                         | 0        | —              | $V_{ref}$ | V             |
| —            | A/D operating clock frequency <sup>(2)</sup> | Without sample & hold |                                                                         | 0.25     | —              | 10        | MHz           |
|              |                                              | With sample & hold    |                                                                         | 1.0      | —              | 10        | MHz           |

## NOTES:

1.  $V_{CC} = AV_{CC} = 2.7$  to  $5.5 \text{ V}$  at  $T_{opr} = -20$  to  $85^\circ\text{C}$  /  $-40$  to  $85^\circ\text{C}$ , unless otherwise specified.
2. If  $f_{AD}$  exceeds 10 MHz more, divide the  $f_{AD}$  and hold A/D operating clock frequency ( $\phi_{AD}$ ) 10 MHz or below.
3. If the  $AV_{CC}$  is less than 4.2V, divide the  $f_{AD}$  and hold A/D operating clock frequency ( $\phi_{AD}$ )  $f_{AD}/2$  or below.
4. Hold  $V_{CC} = V_{ref}$ .

**Figure 5.1 Port P0 to P4 measurement circuit**

**Table 5.4 Flash Memory (Program ROM) Electrical Characteristics**

| Symbol                 | Parameter                                           | Measuring condition         | Standard            |      |     | Unit  |
|------------------------|-----------------------------------------------------|-----------------------------|---------------------|------|-----|-------|
|                        |                                                     |                             | Min.                | Typ. | Max |       |
| —                      | Program/Erase endurance <sup>(2)</sup>              |                             | 1000 <sup>(3)</sup> | —    | —   | times |
| —                      | Byte program time                                   |                             | —                   | 50   | —   | μs    |
| —                      | Block erase time                                    |                             | —                   | 0.4  | —   | s     |
| t <sub>d</sub> (SR-ES) | Time delay from Suspend Request until Erase Suspend |                             | —                   | —    | 8   | ms    |
| —                      | Erase Suspend Request Interval                      |                             | 10                  | —    | —   | ms    |
| —                      | Program, Erase Voltage                              |                             | 2.7                 | —    | 5.5 | V     |
| —                      | Read Voltage                                        |                             | 2.7                 | —    | 5.5 | V     |
| —                      | Program, Erase Temperature                          |                             | 0                   | —    | 60  | °C    |
| —                      | Data hold time <sup>(7)</sup>                       | Ambient temperature = 55 °C | 20                  | —    | —   | year  |

**NOTES:**

1. Referenced to V<sub>CC</sub>=A<sub>V</sub>CC=2.7 to 5.5V at T<sub>opr</sub> = 0°C to 60°C unless otherwise specified.

**2. Definition of Program/Erase**

The endurance of Program/Erase shows a time for each block.

If the program/erase number is “n” (n = 1000, 10000), “n” times erase can be performed for each block.

For example, if performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.

However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).

**3. Numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.**

4. To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.

5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.

6. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.

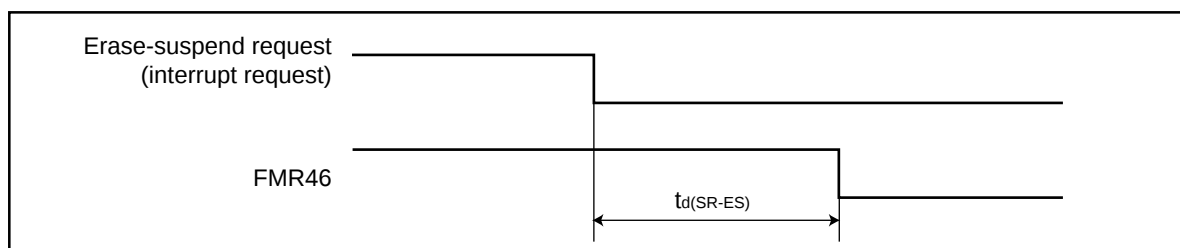
7. The data hold time includes time that the power supply is off or the clock is not supplied.

**Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics<sup>(4)</sup>**

| Symbol                 | Parameter                                              | Measuring condition         | Standard                |      |     | Unit  |
|------------------------|--------------------------------------------------------|-----------------------------|-------------------------|------|-----|-------|
|                        |                                                        |                             | Min.                    | Typ. | Max |       |
| —                      | Program/Erase endurance <sup>(2)</sup>                 |                             | 10000 <sup>(3)</sup>    | —    | —   | times |
| —                      | Byte program time(program/erase endurance ≤1000 times) |                             | —                       | 50   | 400 | μs    |
| —                      | Byte program time(program/erase endurance >1000 times) |                             | —                       | 65   | —   | μs    |
| —                      | Block erase time(program/erase endurance ≤1000 times)  |                             | —                       | 0.2  | 9   | s     |
| —                      | Block erase time(program/erase endurance >1000 times)  |                             | —                       | 0.3  | —   | s     |
| t <sub>d</sub> (SR-ES) | Time delay from Suspend Request until Erase Suspend    |                             | —                       | —    | 8   | ms    |
| —                      | Erase Suspend Request Interval                         |                             | 10                      | —    | —   | ms    |
| —                      | Program, Erase Voltage                                 |                             | 2.7                     | —    | 5.5 | V     |
| —                      | Read Voltage                                           |                             | 2.7                     | —    | 5.5 | V     |
| —                      | Program/Erase Temperature                              |                             | -20(-40) <sup>(8)</sup> | —    | 85  | °C    |
| —                      | Data hold time <sup>(9)</sup>                          | Ambient temperature = 55 °C | 20                      | —    | —   | year  |

## NOTES:

1. Referenced to V<sub>cc</sub>=AV<sub>cc</sub>=2.7 to 5.5V at Topr = -20°C to 85°C / -40°C to 85°C unless otherwise specified.
2. Definition of Program/Erase  
The endurance of Program/Erase shows a time for each block.  
If the program/erase number is “n” (n = 1000, 10000), “n” times erase can be performed for each block.  
For example, if performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.  
However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).
3. Numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.
4. Table 5.5 applies for Block A or B when the Program/Erase cycles are more than 1000. The byte program time up to 1000 cycles are the same as that of the program area (see Table 5.4).
5. To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.
6. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.
7. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
8. -40 °C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

**Figure 5.2 Time delay from Suspend Request until Erase Suspend**

**Table 5.6 Voltage Detection Circuit Electrical Characteristics**

| Symbol  | Parameter                                                                    | Measuring condition | Standard |      |      | Unit |
|---------|------------------------------------------------------------------------------|---------------------|----------|------|------|------|
|         |                                                                              |                     | Min.     | Typ. | Max. |      |
| Vdet    | Voltage detection level                                                      |                     | 3.3      | 3.8  | 4.3  | V    |
|         | Voltage detection interrupt request generating time <sup>(2)</sup>           |                     |          | 40   |      | μs   |
|         | Voltage detection circuit self consumption current                           | VC27=1, VCC=5.0V    |          | 600  |      | nA   |
| td(E-A) | Waiting time until voltage detection circuit operation starts <sup>(3)</sup> |                     |          |      | 20   | μs   |
| Vccmin  | Microcomputer operation voltage minimum value                                |                     | 2.7      |      |      | V    |

## NOTES:

1. The measuring condition is Vcc=AVcc=2.7V to 5.5V and Topr=-40°C to 85°C.
2. This shows the time until the voltage detection interrupt request is generated since the voltage passes Vdet.
3. This shows the required time until the voltage detection circuit operates when setting to "1" again after setting the VC27 bit in the VCR2 register to "0".

**Table 5.7 Reset Circuit Electrical Characteristics (When Using Hardware Reset 2<sup>(1, 3)</sup>)**

| Symbol         | Parameter                                                                 | Measuring condition                               | Standard |      |      | Unit |
|----------------|---------------------------------------------------------------------------|---------------------------------------------------|----------|------|------|------|
|                |                                                                           |                                                   | Min.     | Typ. | Max. |      |
| Vpor2          | Power-on reset valid voltage                                              | -20°C ≤ Topr < 85°C                               | —        | —    | Vdet | V    |
| tw(Vpor2-Vdet) | Supply voltage rising time when power-on reset is canceled <sup>(2)</sup> | -20°C ≤ Topr < 85°C, tw(por2) ≥ 0s <sup>(4)</sup> | —        | —    | 100  | ms   |

## NOTES:

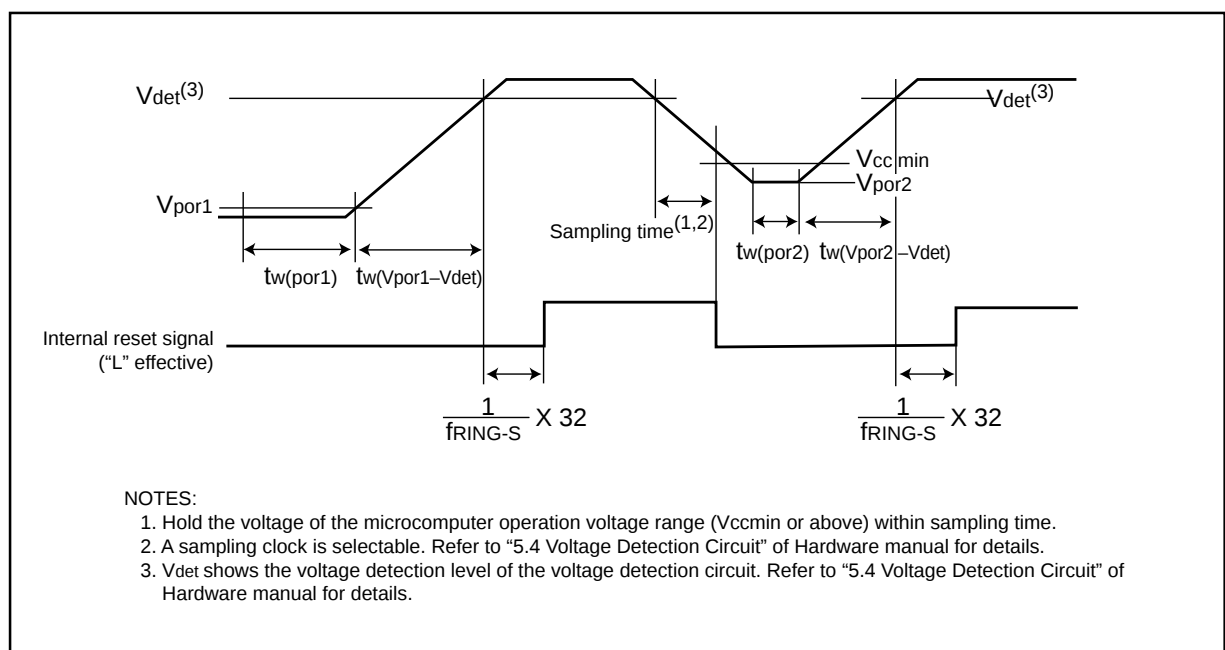
1. The voltage detection circuit which is embedded in a microcomputer is a factor to generate the hardware reset 2. Refer to 5.1.2 Hardware Reset 2 of Hardware Manual for details.
2. This condition is not applicable when using Vcc ≥ 1.0V.
3. When turning power on after the external power has been held below the valid voltage (Vpor1) for greater than 10 seconds, refer to Table 5.8 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2).
4. tw(por2) is time to hold the external power below effective voltage (Vpor2).

**Table 5.8 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2)**

| Symbol         | Parameter                                                  | Measuring condition                               | Standard |      |      | Unit |
|----------------|------------------------------------------------------------|---------------------------------------------------|----------|------|------|------|
|                |                                                            |                                                   | Min.     | Typ. | Max. |      |
| Vpor1          | Power-on reset valid voltage                               | -20°C ≤ Topr < 85°C                               | —        | —    | 0.1  | V    |
| tW(Vpor1-Vdet) | Supply voltage rising time when power-on reset is canceled | 0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 10s <sup>(2)</sup>  | —        | —    | 100  | ms   |
| tW(Vpor1-Vdet) | Supply voltage rising time when power-on reset is canceled | -20°C ≤ Topr < 0°C, tw(por1) ≥ 30s <sup>(2)</sup> | —        | —    | 100  | ms   |
| tW(Vpor1-Vdet) | Supply voltage rising time when power-on reset is canceled | -20°C ≤ Topr < 0°C, tw(por1) ≥ 10s <sup>(2)</sup> | —        | —    | 1    | ms   |
| tW(Vpor1-Vdet) | Supply voltage rising time when power-on reset is canceled | 0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 1s <sup>(2)</sup>   | —        | —    | 0.5  | ms   |

## NOTES:

1. When not using hardware reset 2, use with Vcc ≥ 2.7V.
2. tw(por1) is time to hold the external power below effective voltage (Vpor1).

**Figure 5.3 Reset Circuit Electrical Characteristics**

**Table 5.9 High-speed On-Chip Oscillator Circuit Electrical Characteristics**

| Symbol       | Parameter                                                                                    | Measuring condition                                           | Standard |      |      | Unit |
|--------------|----------------------------------------------------------------------------------------------|---------------------------------------------------------------|----------|------|------|------|
|              |                                                                                              |                                                               | Min.     | Typ. | Max. |      |
| —            | High-speed on-chip oscillator frequency 1 / {td(HRoffset)+td(HR)} when the reset is released | VCC=5.0V, Topr=25 °C<br>Set "4016" in the HR1 register        | —        | 8    | —    | MHz  |
| td(HRoffset) | Settable high-speed on-chip oscillator minimum period                                        | VCC=5.0V, Topr=25 °C<br>Set "0016" in the HR1 register        | —        | 61   | —    | ns   |
| td(HR)       | High-speed on-chip oscillator period adjusted unit                                           | Differences when setting "0116" and "0016" in the HR register | —        | 1    | —    | ns   |
| —            | High-speed on-chip oscillator frequency temperature dependence(1)                            | Frequency fluctuation in temperature range of -10 °C to 50 °C | —        | ±5   | —    | %    |
| —            | High-speed on-chip oscillator frequency temperature dependence(2)                            | Frequency fluctuation in temperature range of -40 °C to 85 °C | —        | ±10  | —    | %    |

NOTES:

1. The measuring condition is Vcc=AVcc=5.0 V and Topr=25 °C.

**Table 5.10 Power Circuit Timing Characteristics**

| Symbol  | Parameter                                                          | Measuring condition | Standard |      |      | Unit |
|---------|--------------------------------------------------------------------|---------------------|----------|------|------|------|
|         |                                                                    |                     | Min.     | Typ. | Max. |      |
| td(P-R) | Time for internal power supply stabilization during powering-on(2) |                     | 1        |      | 2000 | μs   |
| td(R-S) | STOP release time(3)                                               |                     |          |      | 150  | μs   |

NOTES:

1. The measuring condition is Vcc=AVcc=2.7 to 5.5 V and Topr=25 °C.
2. This shows the wait time until the internal power supply generating circuit is stabilized during power-on.
3. This shows the time until BCLK starts from the interrupt acknowledgement to cancel stop mode.

**Table 5.11 Electrical Characteristics (1) [Vcc=5V]**

| Symbol              | Parameter                              |                                                                                 | Measuring condition                         | Standard |      |      | Unit |
|---------------------|----------------------------------------|---------------------------------------------------------------------------------|---------------------------------------------|----------|------|------|------|
|                     |                                        |                                                                                 |                                             | Min.     | Typ. | Max. |      |
| VOH                 | "H" output voltage                     | Except XOUT                                                                     | I <sub>OH</sub> =-5mA                       | Vcc-2.0  | —    | Vcc  | V    |
|                     |                                        |                                                                                 | I <sub>OH</sub> =-200μA                     | Vcc-0.3  | —    | Vcc  | V    |
|                     |                                        | XOUT                                                                            | Drive capacity HIGH I <sub>OH</sub> =-1 mA  | Vcc-2.0  | —    | Vcc  | V    |
|                     |                                        |                                                                                 | Drive capacity LOW I <sub>OH</sub> =-500μA  | Vcc-2.0  | —    | Vcc  | V    |
| VOL                 | "L" output voltage                     | Except P10 to P17, XOUT                                                         | I <sub>OL</sub> = 5 mA                      | —        | —    | 2.0  | V    |
|                     |                                        |                                                                                 | I <sub>OL</sub> = 200 μA                    | —        | —    | 0.45 | V    |
|                     |                                        | P10 to P17                                                                      | Drive capacity HIGH I <sub>OL</sub> = 15 mA | —        | —    | 2.0  | V    |
|                     |                                        |                                                                                 | Drive capacity LOW I <sub>OL</sub> = 5 mA   | —        | —    | 2.0  | V    |
|                     |                                        | XOUT                                                                            | Drive capacity LOW I <sub>OL</sub> = 200 μA | —        | —    | 0.45 | V    |
|                     |                                        |                                                                                 | Drive capacity HIGH I <sub>OL</sub> = 1 mA  | —        | —    | 2.0  | V    |
|                     |                                        |                                                                                 | Drive capacity LOW I <sub>OL</sub> =500 μA  | —        | —    | 2.0  | V    |
|                     |                                        |                                                                                 |                                             | —        | —    | 2.0  | V    |
| VT+-VT-             | Hysteresis                             | INT0, INT1, INT2, INT3, K10, K11, K12, K13, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45 |                                             | 0.2      | —    | 1.0  | V    |
|                     |                                        | RESET                                                                           |                                             | 0.2      | —    | 2.2  | V    |
| I <sub>IH</sub>     | "H" input current                      |                                                                                 | V <sub>I</sub> =5V                          | —        | —    | 5.0  | μA   |
| I <sub>IL</sub>     | "L" input current                      |                                                                                 | V <sub>I</sub> =0V                          | —        | —    | -5.0 | μA   |
| R <sub>PULLUP</sub> | Pull-up resistance                     |                                                                                 | V <sub>I</sub> =0V                          | 30       | 50   | 167  | kΩ   |
| R <sub>XIN</sub>    | Feedback resistance                    | XIN                                                                             |                                             | —        | 1.0  | —    | MΩ   |
| f <sub>RING-S</sub> | Low-speed on-chip oscillator frequency |                                                                                 |                                             | 40       | 125  | 250  | kHz  |
| V <sub>RAM</sub>    | RAM retention voltage                  | At stop mode                                                                    |                                             | 2.0      | —    | —    | V    |

NOTES:

1. Referenced to Vcc = AVcc = 4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN)=20MHz unless otherwise specified.

**Table 5.12 Electrical Characteristics (2) [Vcc=5V]**

| Symbol          | Parameter                                                                                                                                      | Measuring condition                                                                                                                                                                                         | Standard |      |      | Unit |
|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|------|------|------|
|                 |                                                                                                                                                |                                                                                                                                                                                                             | Min.     | Typ. | Max. |      |
| I <sub>CC</sub> | Power supply current<br>(V <sub>CC</sub> =3.3 to 5.5V)<br><br>In single-chip mode, the output pins are open and other pins are V <sub>SS</sub> | High-speed mode<br>X <sub>IN</sub> =20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>No division                                                     | —        | 9    | 15   | mA   |
|                 |                                                                                                                                                | X <sub>IN</sub> =16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>No division                                                                        | —        | 8    | 14   | mA   |
|                 |                                                                                                                                                | X <sub>IN</sub> =10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>No division                                                                        | —        | 5    | —    | mA   |
|                 |                                                                                                                                                | Medium-speed mode<br>X <sub>IN</sub> =20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>Division by 8                                                 | —        | 4    | —    | mA   |
|                 |                                                                                                                                                | X <sub>IN</sub> =16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>Division by 8                                                                      | —        | 3    | —    | mA   |
|                 |                                                                                                                                                | X <sub>IN</sub> =10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>Division by 8                                                                      | —        | 2    | —    | mA   |
|                 |                                                                                                                                                | High-speed on-chip oscillator mode<br>Main clock off<br>High-speed on-chip oscillator on=8 MHz<br>Low-speed on-chip oscillator on=125 kHz<br>No division                                                    | —        | 4    | 8    | mA   |
|                 |                                                                                                                                                | Main clock off<br>High-speed on-chip oscillator on=8 MHz<br>Low-speed on-chip oscillator on=125 kHz<br>Division by 8                                                                                        | —        | 1.5  | —    | mA   |
|                 |                                                                                                                                                | Low-speed on-chip oscillator mode<br>Main clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>Division by 8                                                        | —        | 470  | 900  | μA   |
|                 |                                                                                                                                                | Wait mode<br>Main clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>When a WAIT instruction is executed <sup>(1)</sup><br>Peripheral clock operation<br>VC27="0" | —        | 40   | 80   | μA   |
|                 |                                                                                                                                                | Wait mode<br>Main clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>When a WAIT instruction is executed <sup>(1)</sup><br>Peripheral clock off<br>VC27="0"       | —        | 38   | 76   | μA   |
|                 |                                                                                                                                                | Stop mode<br>Main clock off, T <sub>opr</sub> = -25 °C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10="1"<br>Peripheral clock off<br>VC27="0"                             | —        | 0.8  | 3.0  | μA   |

## NOTES:

1. Timer Y is operated with timer mode.
2. Referenced to V<sub>CC</sub> = AV<sub>CC</sub> = 4.2 to 5.5V at T<sub>opr</sub> = -20 to 85 °C / -40 to 85 °C, f(X<sub>IN</sub>)=20MHz unless otherwise specified.

**Timing requirements [V<sub>CC</sub>=5V] (Unless otherwise noted: V<sub>CC</sub> = 5V, V<sub>SS</sub> = 0V at T<sub>opr</sub> = 25 °C)****Table 5.13 X<sub>IN</sub> input**

| Symbol                             | Parameter                              | Standard |      | Unit |
|------------------------------------|----------------------------------------|----------|------|------|
|                                    |                                        | Min.     | Max. |      |
| t <sub>C</sub> (X <sub>IN</sub> )  | X <sub>IN</sub> input cycle time       | 50       | —    | ns   |
| t <sub>WH</sub> (X <sub>IN</sub> ) | X <sub>IN</sub> input HIGH pulse width | 25       | —    | ns   |
| t <sub>WL</sub> (X <sub>IN</sub> ) | X <sub>IN</sub> input LOW pulse width  | 25       | —    | ns   |

**Table 5.14 CNTR0 input, CNTR1 input,  $\overline{\text{INT2}}$  input**

| Symbol                  | Parameter                    | Standard |      | Unit |
|-------------------------|------------------------------|----------|------|------|
|                         |                              | Min.     | Max. |      |
| t <sub>C</sub> (CNTR0)  | CNTR0 input cycle time       | 100      | —    | ns   |
| t <sub>WH</sub> (CNTR0) | CNTR0 input HIGH pulse width | 40       | —    | ns   |
| t <sub>WL</sub> (CNTR0) | CNTR0 input LOW pulse width  | 40       | —    | ns   |

**Table 5.15 TCIN input,  $\overline{\text{INT3}}$  input**

| Symbol                 | Parameter                   | Standard           |      | Unit |
|------------------------|-----------------------------|--------------------|------|------|
|                        |                             | Min.               | Max. |      |
| t <sub>C</sub> (TCIN)  | TCIN input cycle time       | 400 <sup>(1)</sup> | —    | ns   |
| t <sub>WH</sub> (TCIN) | TCIN input HIGH pulse width | 200 <sup>(2)</sup> | —    | ns   |
| t <sub>WL</sub> (TCIN) | TCIN input LOW pulse width  | 200 <sup>(2)</sup> | —    | ns   |

**NOTES:**

1. When using the Timer C input capture mode, adjust the cycle time above ( 1/ Timer C count source frequency x 3).
2. When using the Timer C input capture mode, adjust the pulse width above ( 1/ Timer C count source frequency x 1.5).

**Table 5.5 Serial Interface**

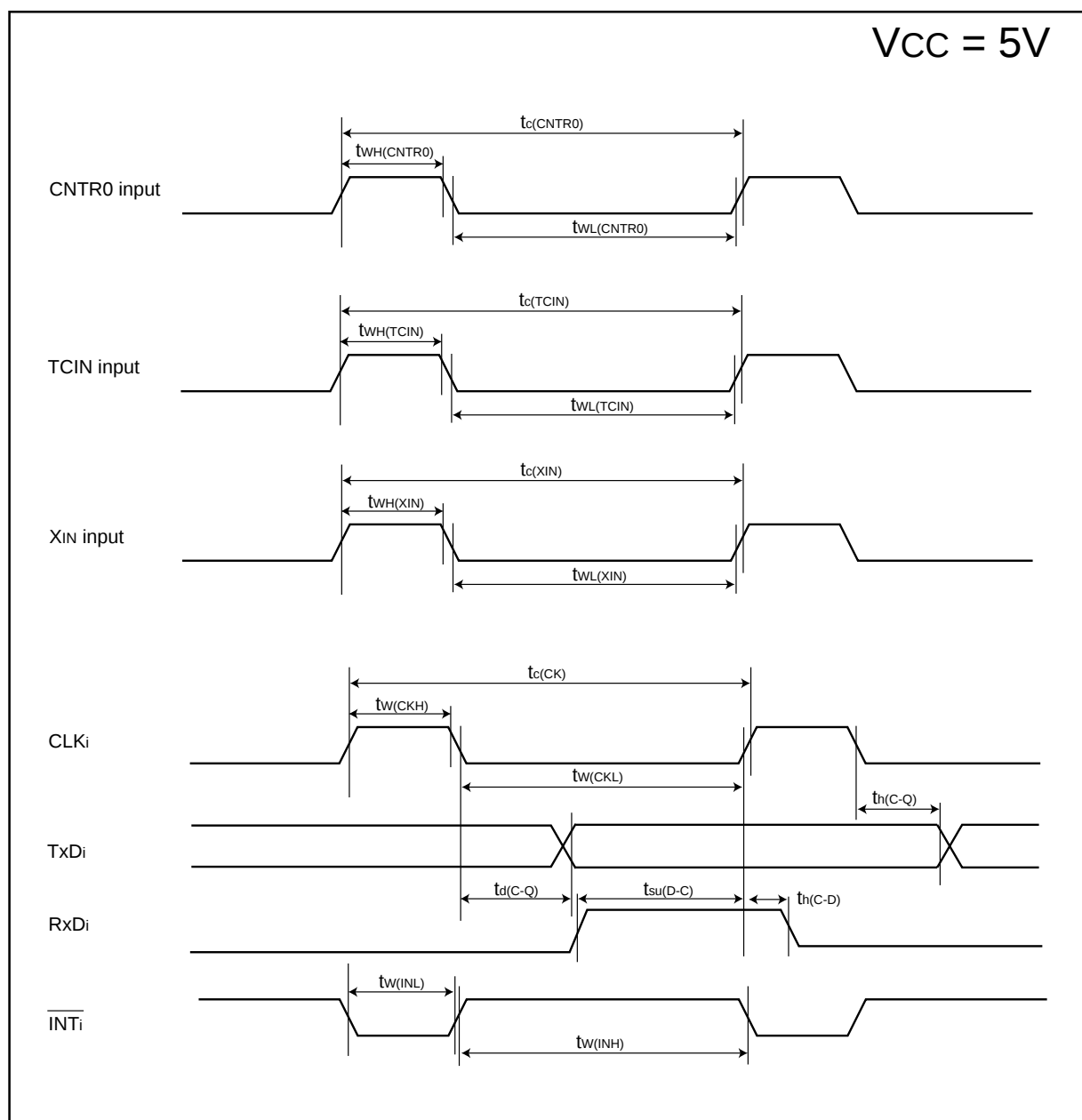
| Symbol                | Parameter                               | Standard |      | Unit |
|-----------------------|-----------------------------------------|----------|------|------|
|                       |                                         | Min.     | Max. |      |
| t <sub>C</sub> (CK)   | CLK <sub>i</sub> input cycle time       | 200      | —    | ns   |
| t <sub>W</sub> (CKH)  | CLK <sub>i</sub> input HIGH pulse width | 100      | —    | ns   |
| t <sub>W</sub> (CKL)  | CLK <sub>i</sub> input LOW pulse width  | 100      | —    | ns   |
| t <sub>d</sub> (C-Q)  | TxD <sub>i</sub> output delay time      | —        | 80   | ns   |
| t <sub>h</sub> (C-Q)  | TxD <sub>i</sub> hold time              | 0        | —    | ns   |
| t <sub>su</sub> (D-C) | RxD <sub>i</sub> input setup time       | 35       | —    | ns   |
| t <sub>h</sub> (C-D)  | RxD <sub>i</sub> input hold time        | 90       | —    | ns   |

**Table 5.17 External interrupt  $\overline{\text{INT0}}$  input**

| Symbol               | Parameter                                       | Standard           |      | Unit |
|----------------------|-------------------------------------------------|--------------------|------|------|
|                      |                                                 | Min.               | Max. |      |
| t <sub>W</sub> (INH) | $\overline{\text{INT0}}$ input HIGH pulse width | 250 <sup>(1)</sup> | —    | ns   |
| t <sub>W</sub> (INL) | $\overline{\text{INT0}}$ input LOW pulse width  | 250 <sup>(2)</sup> | —    | ns   |

**NOTES:**

1. When selecting the digital filter by the  $\overline{\text{INT0}}$  input filter select bit, use the  $\overline{\text{INT0}}$  input HIGH pulse width to the greater value, either ( 1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the  $\overline{\text{INT0}}$  input filter select bit, use the  $\overline{\text{INT0}}$  input LOW pulse width to the greater value, either ( 1/ digital filter clock frequency x 3) or the minimum value of standard.

Figure 5.4  $V_{CC}=5V$  timing diagram

**Table 5.18 Electrical Characteristics (3) [Vcc=3V]**

| Symbol  | Parameter                              |                                                                                 | Measuring condition |             | Standard |      |      | Unit |
|---------|----------------------------------------|---------------------------------------------------------------------------------|---------------------|-------------|----------|------|------|------|
|         |                                        |                                                                                 |                     |             | Min.     | Typ. | Max. |      |
| VOH     | "H" output voltage                     | Except XOUT                                                                     | IOH=-1mA            |             | Vcc-0.5  | —    | Vcc  | V    |
|         |                                        | XOUT                                                                            | Drive capacity HIGH | IOH=-0.1 mA | Vcc-0.5  | —    | Vcc  | V    |
|         |                                        |                                                                                 | Drive capacity LOW  | IOH=-50 μA  | Vcc-0.5  | —    | Vcc  | V    |
| VOL     | "L" output voltage                     | Except P10 to P17, XOUT                                                         | IOL= 1 mA           |             | —        | —    | 0.5  | V    |
|         |                                        | P10 to P17                                                                      | Drive capacity HIGH | IOL= 2 mA   | —        | —    | 0.5  | V    |
|         |                                        |                                                                                 | Drive capacity LOW  | IOL= 1 mA   | —        | —    | 0.5  | V    |
|         |                                        | XOUT                                                                            | Drive capacity HIGH | IOL= 0.1 mA | —        | —    | 0.5  | V    |
|         |                                        |                                                                                 | Drive capacity LOW  | IOL=50 μA   | —        | —    | 0.5  | V    |
| VT+·VT- | Hysteresis                             | INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45 |                     |             | 0.2      | —    | 0.8  | V    |
|         |                                        | RESET                                                                           |                     |             | 0.2      | —    | 1.8  | V    |
| IIH     | "H" input current                      |                                                                                 | VI=3V               |             | —        | —    | 4.0  | μA   |
| IIL     | "L" input current                      |                                                                                 | VI=0V               |             | —        | —    | -4.0 | μA   |
| RPULLUP | Pull-up resistance                     |                                                                                 | VI=0V               |             | 66       | 160  | 500  | kΩ   |
| RXIN    | Feedback resistance                    | XIN                                                                             |                     |             | —        | 3.0  | —    | MΩ   |
| fRING-S | Low-speed on-chip oscillator frequency |                                                                                 |                     |             | 40       | 125  | 250  | kHz  |
| VRAM    | RAM retention voltage                  |                                                                                 | At stop mode        |             | 2.0      | —    | —    | V    |

## NOTES:

1. Referenced to Vcc = AVcc = 2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN)=10MHz unless otherwise specified.

**Table 5.19 Electrical Characteristics (4) [Vcc=3V]**

| Symbol          | Parameter                                                                                                                                  | Measuring condition                                                                                                                                                                                         | Standard |      |      | Unit |
|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|------|------|------|
|                 |                                                                                                                                            |                                                                                                                                                                                                             | Min.     | Typ. | Max. |      |
| I <sub>CC</sub> | Power supply current<br>(V <sub>CC</sub> =2.7 to 3.3V)<br>In single-chip mode, the output pins are open and other pins are V <sub>SS</sub> | High-speed mode<br>X <sub>IN</sub> =20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>No division                                                     | —        | 8    | 13   | mA   |
|                 |                                                                                                                                            | X <sub>IN</sub> =16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>No division                                                                        | —        | 7    | 12   | mA   |
|                 |                                                                                                                                            | X <sub>IN</sub> =10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>No division                                                                        | —        | 5    | —    | mA   |
|                 |                                                                                                                                            | Medium-speed mode<br>X <sub>IN</sub> =20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>Division by 8                                                 | —        | 3    | —    | mA   |
|                 |                                                                                                                                            | X <sub>IN</sub> =16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>Division by 8                                                                      | —        | 2.5  | —    | mA   |
|                 |                                                                                                                                            | X <sub>IN</sub> =10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>Division by 8                                                                      | —        | 1.6  | —    | mA   |
|                 |                                                                                                                                            | High-speed on-chip oscillator mode<br>Main clock off<br>High-speed on-chip oscillator on=8 MHz<br>Low-speed on-chip oscillator on=125 kHz<br>No division                                                    | —        | 3.5  | 7.5  | mA   |
|                 |                                                                                                                                            | Main clock off<br>High-speed on-chip oscillator on=8 MHz<br>Low-speed on-chip oscillator on=125 kHz<br>Division by 8                                                                                        | —        | 1.5  | —    | mA   |
|                 |                                                                                                                                            | Low-speed on-chip oscillator mode<br>Main clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>Division by 8                                                        | —        | 420  | 800  | μA   |
|                 |                                                                                                                                            | Wait mode<br>Main clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>When a WAIT instruction is executed <sup>(1)</sup><br>Peripheral clock operation<br>VC27="0" | —        | 37   | 74   | μA   |
|                 |                                                                                                                                            | Wait mode<br>Main clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on=125 kHz<br>When a WAIT instruction is executed <sup>(1)</sup><br>Peripheral clock off<br>VC27="0"       | —        | 35   | 70   | μA   |
|                 |                                                                                                                                            | Stop mode<br>Main clock off, Topr=-25 °C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10="1"<br>Peripheral clock off<br>VC27="0"                                           | —        | 0.7  | 3.0  | μA   |

## NOTES:

1. Timer Y is operated with timer mode.
2. Referenced to V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(X<sub>IN</sub>)=10MHz unless otherwise specified.

**Timing requirements [ $V_{CC}=3V$ ] (Unless otherwise noted:  $V_{CC} = 3V$ ,  $V_{SS} = 0V$  at  $T_{op} = 25\text{ }^{\circ}C$ )****Table 5.20 XIN input**

| Symbol        | Parameter                  | Standard |      | Unit |
|---------------|----------------------------|----------|------|------|
|               |                            | Min.     | Max. |      |
| $t_c(XIN)$    | XIN input cycle time       | 100      | —    | ns   |
| $t_{WH}(XIN)$ | XIN input HIGH pulse width | 40       | —    | ns   |
| $t_{WL}(XIN)$ | XIN input LOW pulse width  | 40       | —    | ns   |

**Table 5.21 CNTR0 input, CNTR1 input,  $\overline{INT2}$  input**

| Symbol          | Parameter                    | Standard |      | Unit |
|-----------------|------------------------------|----------|------|------|
|                 |                              | Min.     | Max. |      |
| $t_c(CNTR0)$    | CNTR0 input cycle time       | 300      | —    | ns   |
| $t_{WH}(CNTR0)$ | CNTR0 input HIGH pulse width | 120      | —    | ns   |
| $t_{WL}(CNTR0)$ | CNTR0 input LOW pulse width  | 120      | —    | ns   |

**Table 5.22 TCIN input,  $\overline{INT3}$  input**

| Symbol         | Parameter                   | Standard            |      | Unit |
|----------------|-----------------------------|---------------------|------|------|
|                |                             | Min.                | Max. |      |
| $t_c(TCIN)$    | TCIN input cycle time       | 1200 <sup>(1)</sup> | —    | ns   |
| $t_{WH}(TCIN)$ | TCIN input HIGH pulse width | 600 <sup>(2)</sup>  | —    | ns   |
| $t_{WL}(TCIN)$ | TCIN input LOW pulse width  | 600 <sup>(2)</sup>  | —    | ns   |

**NOTES:**

1. When using the Timer C input capture mode, adjust the cycle time above (  $1/\text{Timer C count source frequency} \times 3$  ).
2. When using the Timer C input capture mode, adjust the pulse width above (  $1/\text{Timer C count source frequency} \times 1.5$  ).

**Table 5.23 Serial Interface**

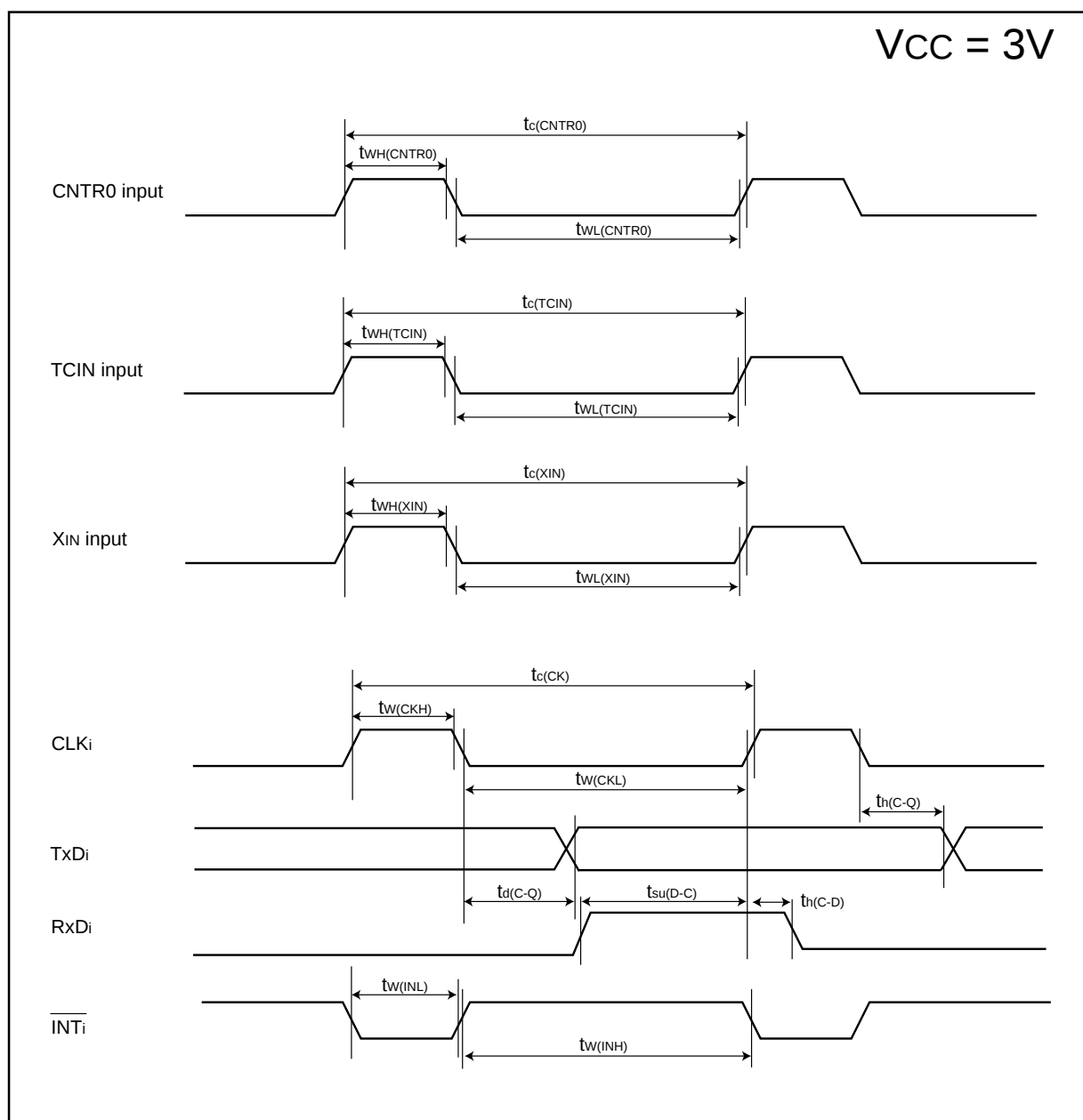
| Symbol        | Parameter                   | Standard |      | Unit |
|---------------|-----------------------------|----------|------|------|
|               |                             | Min.     | Max. |      |
| $t_c(CLKi)$   | CLKi input cycle time       | 300      | —    | ns   |
| $t_{W}(CLKH)$ | CLKi input HIGH pulse width | 150      | —    | ns   |
| $t_{W}(CLKL)$ | CLKi input LOW pulse width  | 150      | —    | ns   |
| $t_d(C-Q)$    | TxDi output delay time      | —        | 160  | ns   |
| $t_h(C-Q)$    | TxDi hold time              | 0        | —    | ns   |
| $t_{su}(D-C)$ | RxDi input setup time       | 55       | —    | ns   |
| $t_h(C-D)$    | RxDi input hold time        | 90       | —    | ns   |

**Table 5.24 External interrupt  $\overline{INT0}$  input**

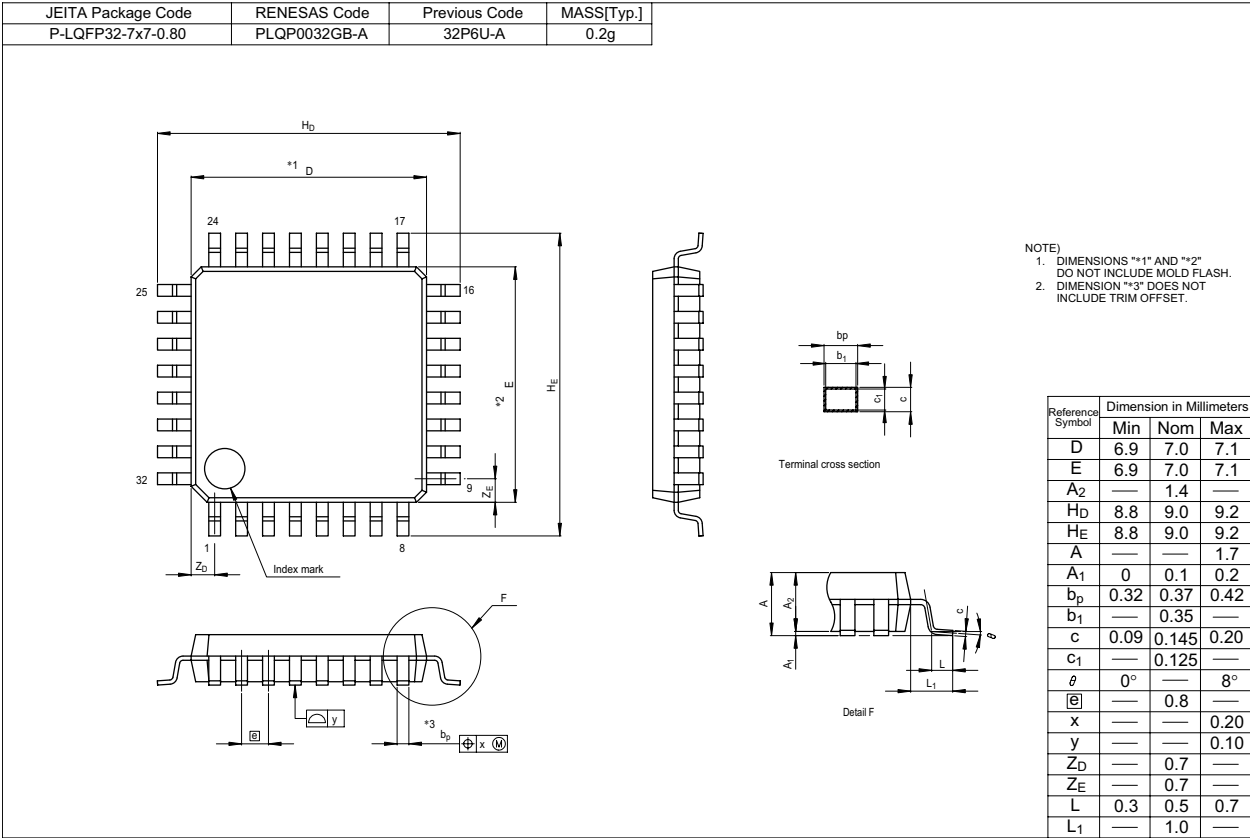
| Symbol                    | Parameter                                | Standard           |      | Unit |
|---------------------------|------------------------------------------|--------------------|------|------|
|                           |                                          | Min.               | Max. |      |
| $t_{W}(\overline{INT0}H)$ | $\overline{INT0}$ input HIGH pulse width | 380 <sup>(1)</sup> | —    | ns   |
| $t_{W}(\overline{INT0}L)$ | $\overline{INT0}$ input LOW pulse width  | 380 <sup>(2)</sup> | —    | ns   |

**NOTES:**

1. When selecting the digital filter by the  $\overline{INT0}$  input filter select bit, use the  $\overline{INT0}$  input HIGH pulse width to the greater value, either (  $1/\text{digital filter clock frequency} \times 3$  ) or the minimum value of standard.
2. When selecting the digital filter by the  $\overline{INT0}$  input filter select bit, use the  $\overline{INT0}$  input LOW pulse width to the greater value, either (  $1/\text{digital filter clock frequency} \times 3$  ) or the minimum value of standard.

Figure 5.5  $V_{CC}=3V$  timing diagram

Package Dimensions



|                  |                        |
|------------------|------------------------|
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| Rev. | Date         | Description |                                                                         |
|------|--------------|-------------|-------------------------------------------------------------------------|
|      |              | Page        | Summary                                                                 |
| 0.10 | Oct 28, 2003 |             | First edition issued                                                    |
| 0.20 | Dec05, 2003  | 5           | Figure 1.3 revised                                                      |
|      |              | 10          | Chapter 4, NOTES revised                                                |
|      |              | 16          | Table 5.4 revised<br>Table 5.5 revised                                  |
|      |              | 17          | Table 5.6 revised<br>Figure 5.3 added                                   |
|      |              | 18          | Table 5.8 revised<br>Table 5.10 revised                                 |
|      |              | 21          | Figure 5.3 revised to Figure 5.4                                        |
|      |              | 22          | Table 5.17 revised                                                      |
|      |              | 25          | Figure 5.4 revised to Figure 5.5                                        |
| 1.00 | Sep 30, 2004 | All pages   | Words standardized (on-chip oscillator, serial interface, A/D)          |
|      |              | 2           | Table 1.1 revised                                                       |
|      |              | 5           | Figure 1.3, NOTES 3 added                                               |
|      |              | 6           | Table 1.3 revised                                                       |
|      |              | 9           | Figure 3.1, NOTES added                                                 |
|      |              | 10-13       | One body sentence in chapter 4 added ; Titles of Table 4.1 to 4.4 added |
|      |              | 12          | Table 4.3 revised ; Table 4.4 revised                                   |
|      |              | 14          | Table 5.2 revised                                                       |
|      |              | 15          | Table 5.3 revised                                                       |
|      |              | 16          | Table 5.4 and Table 5.5 revised                                         |
|      |              | 17          | Table 5.6, 5.7 and 5.8 revised ; Figure 5.3 revised                     |
|      |              | 18          | Table 5.9 and 5.11 revised                                              |
|      |              | 19          | Table 5.12 revised                                                      |
|      |              | 20          | Table 5.13 revised                                                      |
|      |              | 22          | Table 5.18 revised                                                      |
|      |              | 23          | Table 5.19 revised                                                      |
|      |              | 24          | Table 5.20 and Table 5.24 revised                                       |
| 1.10 | Apr.27.2005  | 4           | Table 1.2, Figure 1.2 package name revised                              |
|      |              | 5           | Figure 1.3 package name revised                                         |
|      |              | 10          | Table 4.1 revised                                                       |
|      |              | 12          | Table 4.3 revised                                                       |
|      |              | 15          | Table 5.3 partly revised                                                |
|      |              | 16          | Table 5.4, Table 5.5 partly added                                       |

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| Rev. | Date        | Description |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
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|      |             | Page        | Summary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 1.10 | Apr.27.2005 | 17          | Table 5.7, 5.8 revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|      |             | 18          | Table 5.10, Table 5.11 partly revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|      |             | 22          | Table 5.18 partly revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|      |             | 26          | Package Dimensions revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 1.20 | Jan.27.2006 | 2           | Table 1.1 Performance outline revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|      |             | 3           | Figure 1.1 Block diagram partly revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|      |             | 4           | 1.4 Product Information, title of Table 1.2<br>"Product List" → "Product Informaton" revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|      |             |             | ROM capacity; "Program area" → "Program ROM",<br>"Data area" → "Data flash" revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|      |             |             | Figure 1.2 Type No., Memory Size, and Package partly revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|      |             | 6           | Table 1.3 Pin description revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|      |             | 7-8         | 2 Central Processing Unit (CPU) revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|      |             |             | Figure 2.1 CPU register revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|      |             | 9           | 3 Memory, Figure 3.1 Memory Map;<br>"Program area" → "Program ROM", "Data area" → "Data flash" revised                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|      |             | 10          | Table 4.1 SFR Information(1) NOTES:1 revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|      |             | 11          | Table 4.2 SFR Information(2) NOTES:1 revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|      |             | 12          | Table 4.3 SFR Information(3);<br>0081 <sub>16</sub> : "Prescaler Y" → "Prescaler Y Register"<br>0082 <sub>16</sub> : "Timer Y Secondary" → "Timer Y Secondary Register"<br>0083 <sub>16</sub> : "Timer Y Primary" → "Timer Y Primary Register"<br>0085 <sub>16</sub> : "Prescaler Z" → "Prescaler Z Register"<br>0086 <sub>16</sub> : "Timer Z Secondary" → "Timer Z Secondary Register"<br>0087 <sub>16</sub> : "Timer Z Primary" → "Timer Z Primary Register"<br>008C <sub>16</sub> : "Prescaler X" → "Prescaler X Register" revised<br>NOTES:1, 2 revised |
|      |             | 13          | Table 4.4 SFR Information(4) NOTES:1 revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|      |             | 14          | Table 5.2 Recommended Operating Conditions; NOTES: 1, 2, 3 revised                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|      |             | 15          | Table 5.3 A/D Conversion Characteristics;<br>"A/D operation clock frequency" → "A/D operating clock frequency" revised<br>NOTES: 1, 2, 3, 4 revised                                                                                                                                                                                                                                                                                                                                                                                                          |
|      |             | 16          | Table 5.4 Flash Memory (Program ROM) Electrical Characteristics;<br>"Data retention duration" → "Data hold time" revised<br>"Topr" → "Ambient temperature"<br>NOTES: 1 to 7 added<br>Measuring condition of byte program time and block erase time deleted                                                                                                                                                                                                                                                                                                   |
|      |             | 17          | Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical characteristics<br>"Data retention duration" → "Data hold time" revised<br>"Topr" → "Ambient temperature"<br>NOTES: 1, 3 revised, NOTES: 9 added<br>Measuring condition of byte program time and block erase time deleted                                                                                                                                                                                                                                                                    |
|      |             | 18          | Table 5.7 Reset Circuit Electrical Characteristics (When Using Hardware Reset 2)<br>NOTES: 3 revised                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|      |             | 19          | Table 5.9 High-speed On-Chip Oscillator Circuit Electrical Characteristics;<br>"High-speed on-chip oscillator temperature dependence" →<br>"High-speed on-chip oscillator frequency temperature dependence" revised<br>Table 5.11 Electrical Characteristics (1) [V <sub>CC</sub> =5V];<br>"P1 <sub>0</sub> to P1 <sub>7</sub> Except Xout" → "Except P1 <sub>0</sub> to P1 <sub>7</sub> , Xout" revised                                                                                                                                                     |



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