

# NP50P04SDG

-40V - -50A - P-channel Power MOS FET

R07DS1520EJ0100 Rev.1.00 Jun. 17, 2022

### Application : Automotive

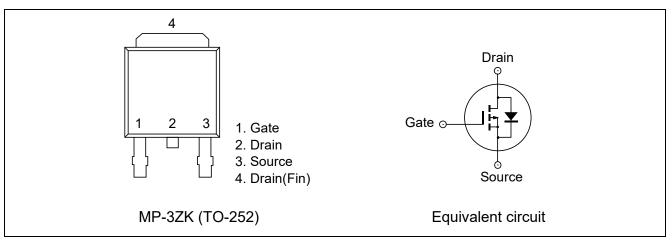
### Description

This product is P-channel MOS Field Effect Transistor designed for high current switching applications.

#### Features

- Super low on-state resistance :  $R_{DS(on)}$  = 9.6 m $\Omega$  Max. (  $V_{GS}$  = -10 V,  $I_D$  = -25 A )
  - $R_{DS(on)}$  = 15 m $\Omega$  Max. (V<sub>GS</sub> = -4.5 V, I<sub>D</sub> = -25 A)
- Low input capacitance : Ciss = 5000 pF Typ.
- Designed for automotive application and AEC-Q101 qualified.
- Pb-free (This product does not contain Pb in the external electrode)

#### Outline



#### **Absolute Maximum Ratings**

			(T <sub>a</sub> =25°C)	
Item	Symbol	Ratings	Unit	
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	-40	V	
Gate to Source Voltage ( $V_{DS} = 0 V$ )	V <sub>GSS</sub>	∓20	V	
Drain Current (DC) $(T_c = 25 \degree C)$	I <sub>D(DC)</sub>	<b>∓</b> 50	А	
Drain Current (pulse)	I <sub>D(pulse)</sub> Notes1	∓150	А	
Total Power Dissipation ( $T_c$ = 25 °C)	P <sub>T1</sub>	84	W	
Total Power Dissipation ( $T_a = 25 \text{ °C}$ )	P <sub>T2</sub>	1.2	W	
Channel Temperature	T <sub>ch</sub>	175	°C	
Storage Temperature	T <sub>stg</sub>	-55 to 175	°C	
Single Avalanche Current	I <sub>AS</sub> Notes2	37	A	
Single Avalanche Energy	E <sub>AS</sub> Notes2	136	mJ	

Notes 1. PW  $\leq$  10  $\mu$ s , Duty Cycle  $\leq$  1%

2. Starting T\_ch=25  $^\circ\!\mathrm{C}$  , V\_DD = -20V , R\_G = 25  $\Omega$  , V\_Gs = -20  $\rightarrow$  0V , L = 100  $\mu\text{H}$ 



#### **Thermal Resistance**

Channel to Case Thermal Resistance	Rth(ch-c) Notes3	1.78	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-a) Notes3	125	°C/W

#### **Electrical Characteristics**

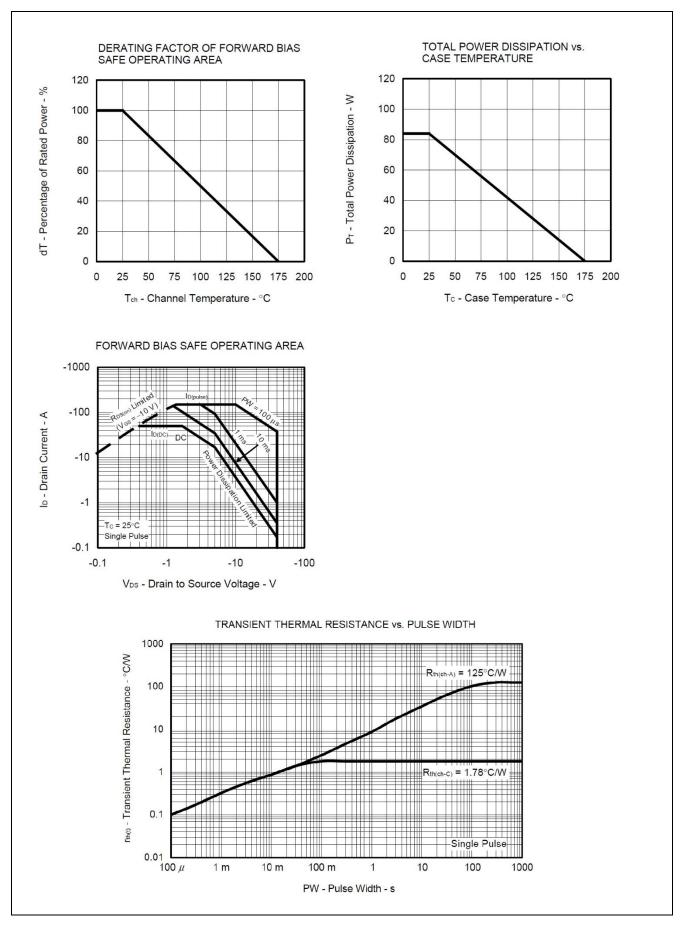
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>		_	-10	μA	V <sub>DS</sub> = -40 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>	_	_	∓100	nA	V <sub>GS</sub> = ∓ 20 V, V <sub>DS</sub> = 0 V
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	-1.0	-1.6	-2.5	V	Vds = Vgs, Id = -250 µ A
Forward Transfer Admittance	yfs   <sup>Notes4</sup>	15	33	_	S	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -25 A
Drain to Source On-state Resistance	R <sub>DS(on)1</sub> Notes4	_	7.7	9.6	mΩ	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -25 A
	R <sub>DS(on)2</sub> Notes4	_	9.3	15	mΩ	Vgs = -4.5 V, Id = -25 A
Input Capacitance	C <sub>iss</sub>	_	5000	_	pF	V <sub>DS</sub> = -10 V
Output Capacitance	C <sub>oss</sub>		770	_	pF	V <sub>GS</sub> = 0 V
Reverse Transfer Capacitance	C <sub>rss</sub>	_	420	_	pF	f = 1 MHz
Turn-on Delay Time	t <sub>d(on)</sub>	_	13	_	ns	V <sub>DD</sub> = -20 V
Rise Time	tr	_	13	_	ns	I⊳ = -25 A
Turn-off Delay Time	t <sub>d(off)</sub>	_	405	_	ns	Vgs = -10 V
Fall Time	t <sub>f</sub>	_	180	_	ns	R <sub>G</sub> = 0 Ω
Total Gate Charge	Qg	_	100	_	nC	V <sub>DD</sub> = -32 V
Gate to Source Charge	Q <sub>gs</sub>	_	12	_	nC	Vgs = -10 V
Gate to Drain Charge	Q <sub>gd</sub>		28	_	nC	I⊳ = -50 A
Body Diode Forward Voltage	V <sub>F(S-D)</sub> <sup>Notes4</sup>		0.95	1.5	V	IF = -50 A, VGS = 0 V
Reverse Recovery Time	t <sub>rr</sub>		48	_	ns	IF = -50 A, VGS = 0 V
Reverse Recovery Charge	Q <sub>rr</sub>		66	_	nC	di/dt = -100 A/µs

Notes 3. Designed target value on Renesas measurement condition. Not subject to production test.

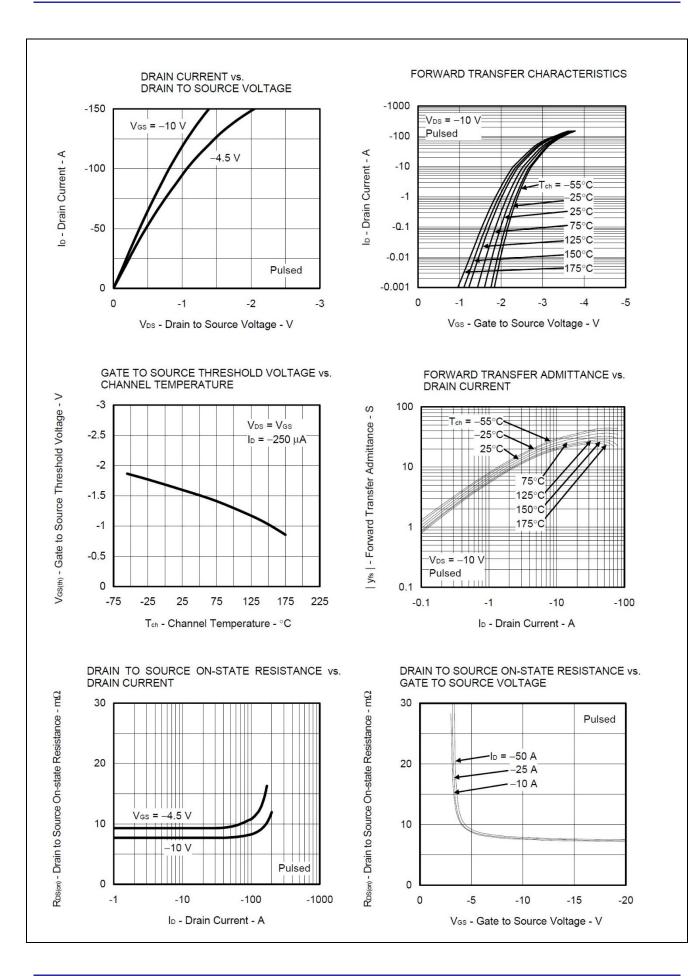
4. Pulse test.

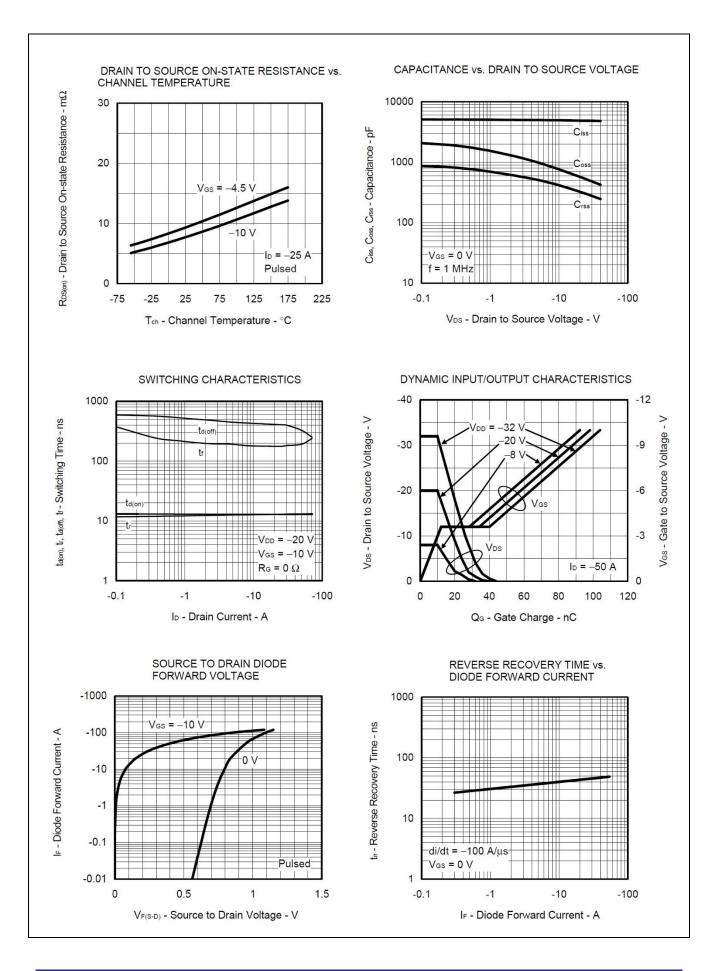
(T<sub>a</sub>=25°C)

#### **Typical Characteristics**



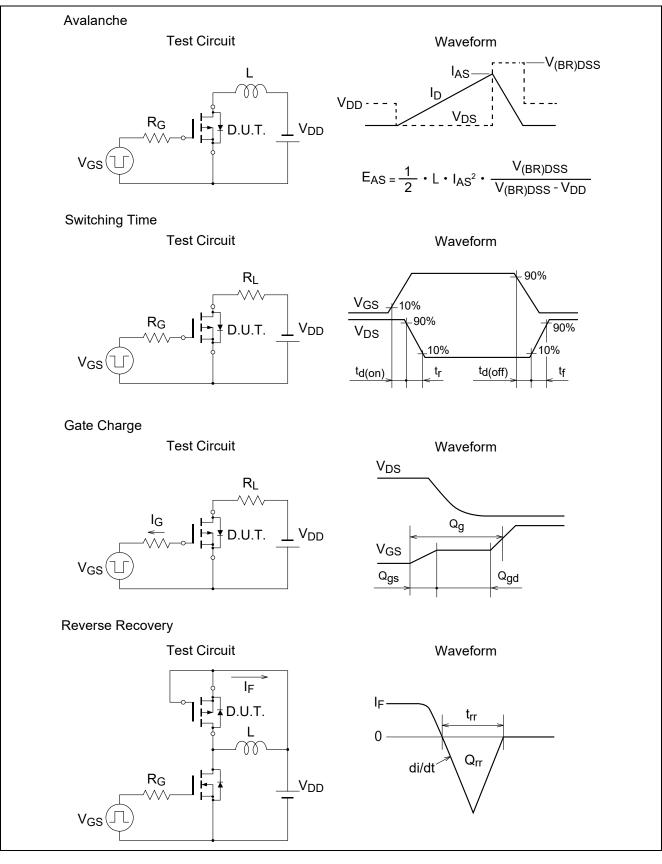




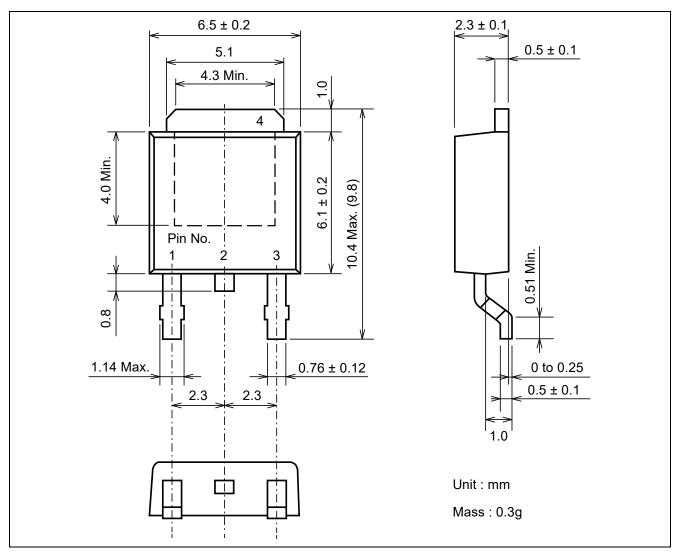


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#### **Test Circuit**



#### **Package Dimensions**



#### **Ordering Information**

Part No.	Quantity	Shipping container
NP50P04SDG-E1-AY	2500pcs/reel	Taping

Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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