RL78/I1C

RENESAS MCU

R01DS0281EJ0230
Rev.2.30
Mar 29, 2024

True Low Power Platform, Independent power supply RTC, Hardware AES, 32-bit MAC, 1.9 V to 5.5 V operation, 64 to 256 Kbyte Flash, for Electric AMI Power Meter Application

1. OUTLINE

1.1 Features

Target application

- Power meters

Ultra-low power consumption technology

- V_{DD} = single power supply voltage of 1.7 to 5.5 V Note 1
- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.03125 μs: @ 32 MHz selection with PLL clock, 0.04167 μs: @ 24 MHz selection with high-speed on-chip oscillator) to ultra-low speed (66.6 μs: @ 15 kHz operation with low-speed on-chip oscillator)
- 16-bit multiplication, 16-bit multiply-accumulation, and 32-bit division are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 6 KB to 16 KB

Code flash memory

- Code flash memory: 64 KB to 256 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data flash memory

- Data flash memory: 2 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 1.9 to 5.5 V

PLL clock Note 2

- 32 MHz is selectable (ΔΣ A/D converter is operable even when the PLL clock is selected as a CPU clock.)

High-speed on-chip oscillator

- Select from 1 to 24 MHz (TYP.). However when it is used as a clock for the ΔΣ A/D converter, select from 24 MHz (TYP.), 12 MHz (TYP.), 6 MHz (TYP.), or 3 MHz (TYP.).
- High accuracy: ±1.0% (V_{DD} = 1.9 to 5.5 V, T_A = –20 to +85°C)
- On-chip high-speed on-chip oscillator clock frequency correction function

Middle-speed on-chip oscillator

- Select from 4 MHz/2 MHz/1 MHz (However ΔΣ A/D converter is disabled.)

Operating ambient temperature

- T_A = -40 to +85°C

Power management and reset function

- On-chip power-on-reset (POR) circuit for Internal V_{DD} Note 3 power supply
- On-chip RTC power-on-reset (RTCPOR) circuit for VRTC power supply
- On-chip voltage detector (LVD) (Select interrupt and reset from 13 levels)

Voltage detective circuit

- Detective voltage for V_{DD} pin (Select interrupt from 6 levels)
- Detective voltage for VBAT pin (Select interrupt from 7 levels)
- Detective voltage for VRTC pin (Select interrupt from 4 levels)
- Detective voltage for EXLVD pin (Select interrupt from 1 level)

Data transfer controller (DTC)

- Transfer mode: Normal mode, repeat mode, block mode
- Activation source: Start by interrupt sources
- Chain transfer function

Event link controller (ELC)

- Event signals of 22 types can be linked to the specified peripheral function.

On-chip 32-bit multiplier and multiply-accumulator

- 32 bits × 32 bits = 64 bits (Unsigned or signed)
- 32 bits × 32 bits + 64 bits = 64 bits (Unsigned or signed)

Serial interface

- Simplified SPI (CSI): 2 to 3 channels
- UART/UART (LIN-bus supported): 2 to 3 channels
- UART/IrDA: 1 channel
- Simplified I^2C communication: 2 to 3 channels
- I^2C communication: 1 channel

Timer

- 16-bit timer: 8 channels
- 12-bit interval timer: 1 channel
- 8-bit interval timer: 4 channels
- Independent power supply RTC: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel
- Oscillation stop detection circuit: 1 channel

LCD controller/driver

- Internal voltage boosting method, capacitor split method, and external resistance division method are switchable
- Segment signal output: 19 (15)[Note 4] to 42 (38)[Note 4]
- Common signal output: 4 (8)[Note 4]

A/D converter

- 24-Bit ΔΣ A/D converter: 3 or 4 channels
- 8/10-bit resolution A/D converter (V_{DD} = 1.9 to 5.5 V): 4 or 6 channels
- Internal reference voltage (1.45 V) and temperature sensor

I/O port

- I/O port: 35 to 68 (N-ch open drain I/O [6 V tolerance]: 3, N-ch open drain I/O [V_{DD} tolerance[Note 5]/EV_{DD} tolerance[Note 6]]: 10 to 16)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5/3 V device
- On-chip clock output/buzzer output controller
- On-chip key interrupt function

AES circuit[Note 7]

- Cipher modes of operation: GCM/ECB/CBC
- Encryption key length: 128/192/256 bits

Others

- On-chip BCD (binary-coded decimal) correction circuit
- On-chip battery backup function

Notes **1.** The minimum operating voltage of this product varies according to the VBATEN setting value.
When VBATEN = 0, the minimum operating voltage is 1.7 V.
When VBATEN = 1, the minimum operating voltage is 1.9 V.
As well, the minimum operating voltage of VRTC is 1.6 V.
2. R5F10NPJ, R5F10NMJ, R5F10NPG only.
3. Either V_{DD} or VBAT is selected by the battery backup function.
4. The values in parentheses are the number of signal outputs when 8 com is used.
5. 64 pin products only
6. 80 pin, 100 pin products only
7. Only available in R5F10N products.

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

O ROM, RAM capacities

Code Flash	Data Flash	RAM	AES Function	RL78/I1C		
				64 pins	80 pins	100 pins
256 KB	2 KB	16 KB[Note 1]	Mounted	-	R5F10NMJ	R5F10NPJ
128 KB	2 KB	8 KB[Note 2]	Mounted	R5F10NLG	R5F10NMG	R5F10NPG
			Not mounted	R5F11TLG	-	-
64 KB	2 KB	6 KB	Mounted	R5F10NLE	R5F10NME	-
			Not mounted	R5F11TLE	-	-

Notes 1. This is about 15 KB when the self-programming function is used. (For details, refer to **CHAPTER 3 in the RL78/I1C User's Manual**.)

2. This is about 7 KB when the self-programming function is used (excluding in the case of the R5F10NPG). (For details, refer to **CHAPTER 3 in the RL78/I1C User's Manual**.)

1.2 List of Part Numbers

<R> **Figure 1-1. Part Number, Memory Size, and Package of RL78/I1C**

Part No. R 5 F 1 0 N P J D x x x F B #30

- **#30** — Packaging specification
  - #10, #30, #70 : Tray (LFQFP) Ver.1.0
  - #15, #35, #75 : Tray (LFQFP) Ver.1.1
  - #50 : Embossed Tape (LFQFP) Ver.1.0
  - #55 : Embossed Tape (LFQFP) Ver.1.1
- **F B** — Package type:
  - FB : LFQFP, 0.50 mm pitch
- **x x x** — ROM number (Omitted with blank products)
- **D** — Fields of application:
  - D : Industrial applications, T_A = -40°C to +85°C
- **J** — ROM capacity:
  - E : 64 KB
  - G : 128 KB
  - J : 256 KB
- **P** — Pin count:
  - L : 64-pin
  - M : 80-pin
  - P : 100-pin
- **1 0 N** — RL78/I1C group
  - 10N : On-chip AES circuit
  - 11T : No on-chip AES circuit
- **F** — Memory type:
  - F : Flash memory
- **5** — Renesas MCU
- **R** — Renesas semiconductor product

Table 1-1. List of Ordering Part Numbers

Pin Count	Package	Data Flash	AES Function	Fields of Application[Note]	Ordering Part Number
64 pins	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	Mounted	Mounted	D	R5F10NLEDFB#10, R5F10NLGDFB#10, R5F10NLEDFB#15, R5F10NLGDFB#15, R5F10NLEDFB#30, R5F10NLGDFB#30, R5F10NLEDFB#50, R5F10NLGDFB#50, <R> R5F10NLEDFB#70, R5F10NLGDFB#70, R5F10NLEDFB#35, R5F10NLGDFB#35, R5F10NLEDFB#55, R5F10NLGDFB#55, <R> R5F10NLEDFB#75, R5F10NLGDFB#75
			Not mounted	D	R5F11TLEDFB#10, R5F11TLGDFB#10, R5F11TLEDFB#15, R5F11TLGDFB#15, R5F11TLEDFB#30, R5F11TLGDFB#30, R5F11TLEDFB#50, R5F11TLGDFB#50, <R> R5F11TLEDFB#70, R5F11TLGDFB#70, R5F11TLEDFB#35, R5F11TLGDFB#35, R5F11TLEDFB#55, R5F11TLGDFB#55, <R> R5F11TLEDFB#75, R5F11TLGDFB#75
80 pins	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	Mounted	Mounted	D	R5F10NMEDFB#10, R5F10NMGDFB#10, R5F10NMJDFB#10, R5F10NMEDFB#15, R5F10NMGDFB#15, R5F10NMJDFB#15, R5F10NMEDFB#30, R5F10NMGDFB#30, R5F10NMJDFB#30, R5F10NMEDFB#35, R5F10NMGDFB#35, R5F10NMJDFB#35, R5F10NMEDFB#50, R5F10NMGDFB#50, R5F10NMJDFB#50, R5F10NMEDFB#55, R5F10NMGDFB#55, R5F10NMJDFB#55, <R> R5F10NMEDFB#70, R5F10NMGDFB#70, <R> R5F10NMJDFB#70, R5F10NMEDFB#75 <R> R5F10NMGDFB#75, R5F10NMJDFB#75
100 pins	100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)	Mounted	Mounted	D	R5F10NPJDFB#10, R5F10NPGDFB#10, R5F10NPJDFB#15, R5F10NPGDFB#15, R5F10NPJDFB#30, R5F10NPGDFB#30, R5F10NPJDFB#35, R5F10NPGDFB#35, R5F10NPJDFB#50, R5F10NPGDFB#50, R5F10NPJDFB#55, R5F10NPGDFB#55, <R> R5F10NPJDFB#70, R5F10NPGDFB#70, <R> R5F10NPJDFB#75, R5F10NPGDFB#75

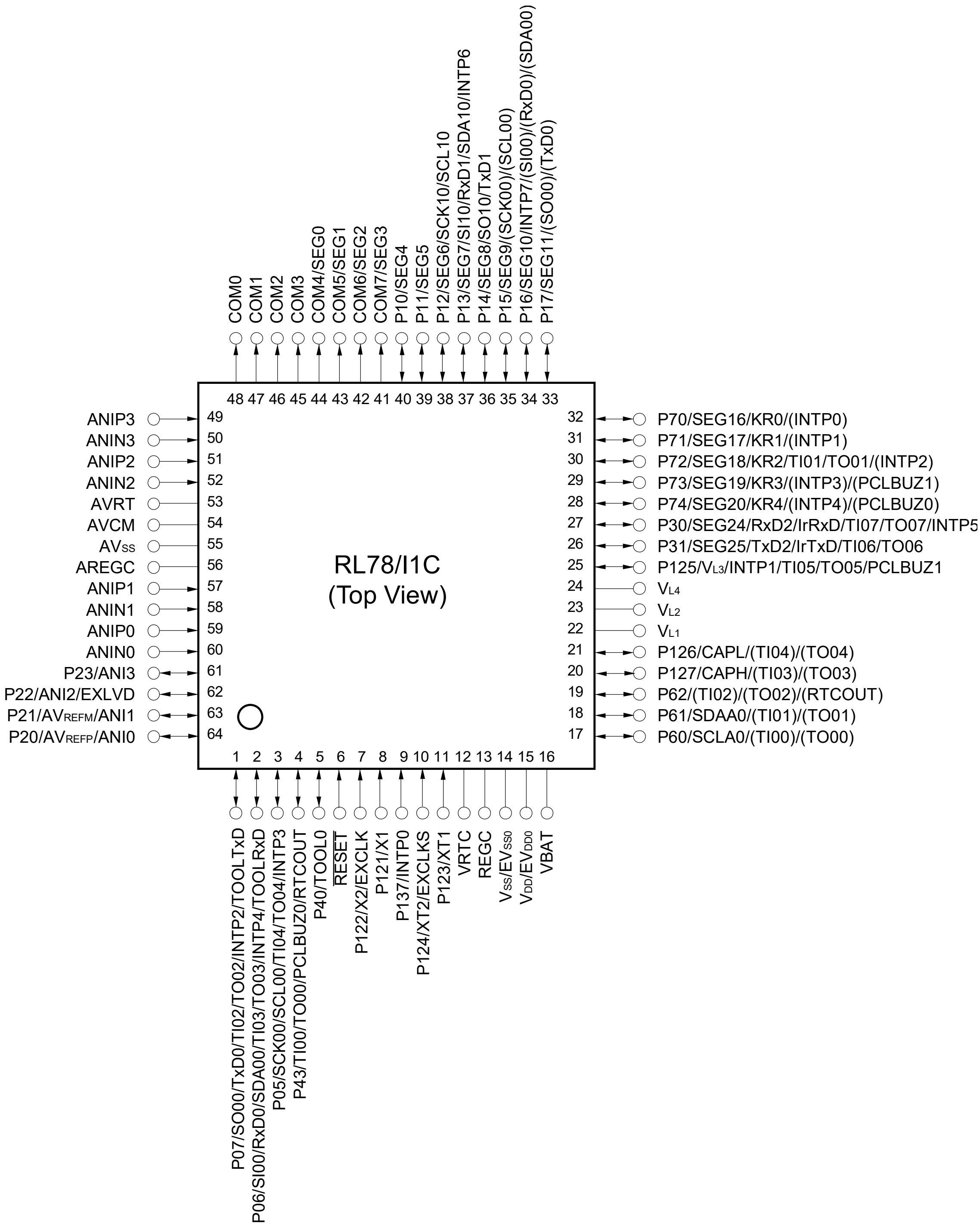
Note For the fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/I1C**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 64-pin products

- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



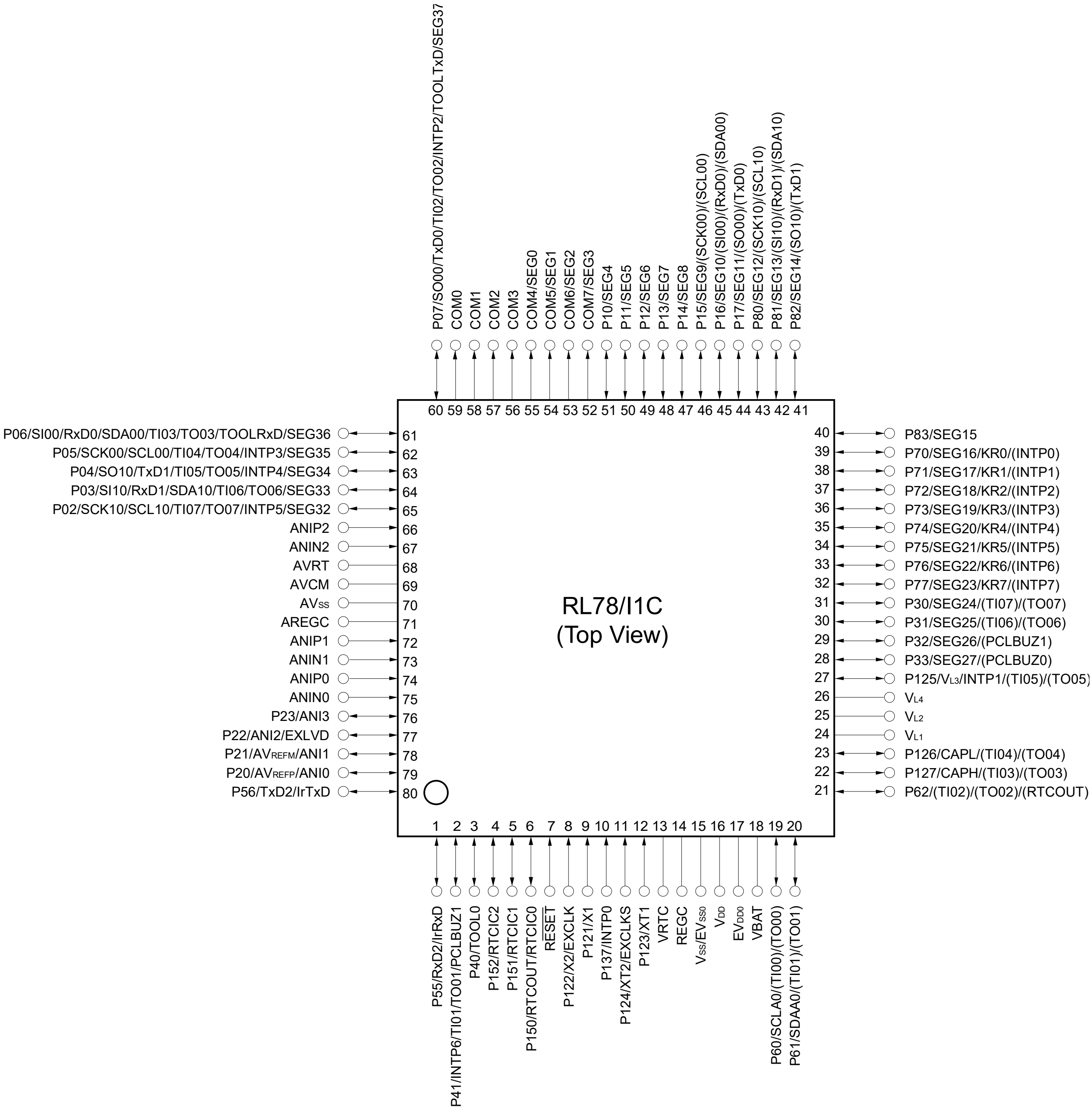
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR0). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR0) in the RL78/I1C User's Manual**.

1.3.2 80-pin products

- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



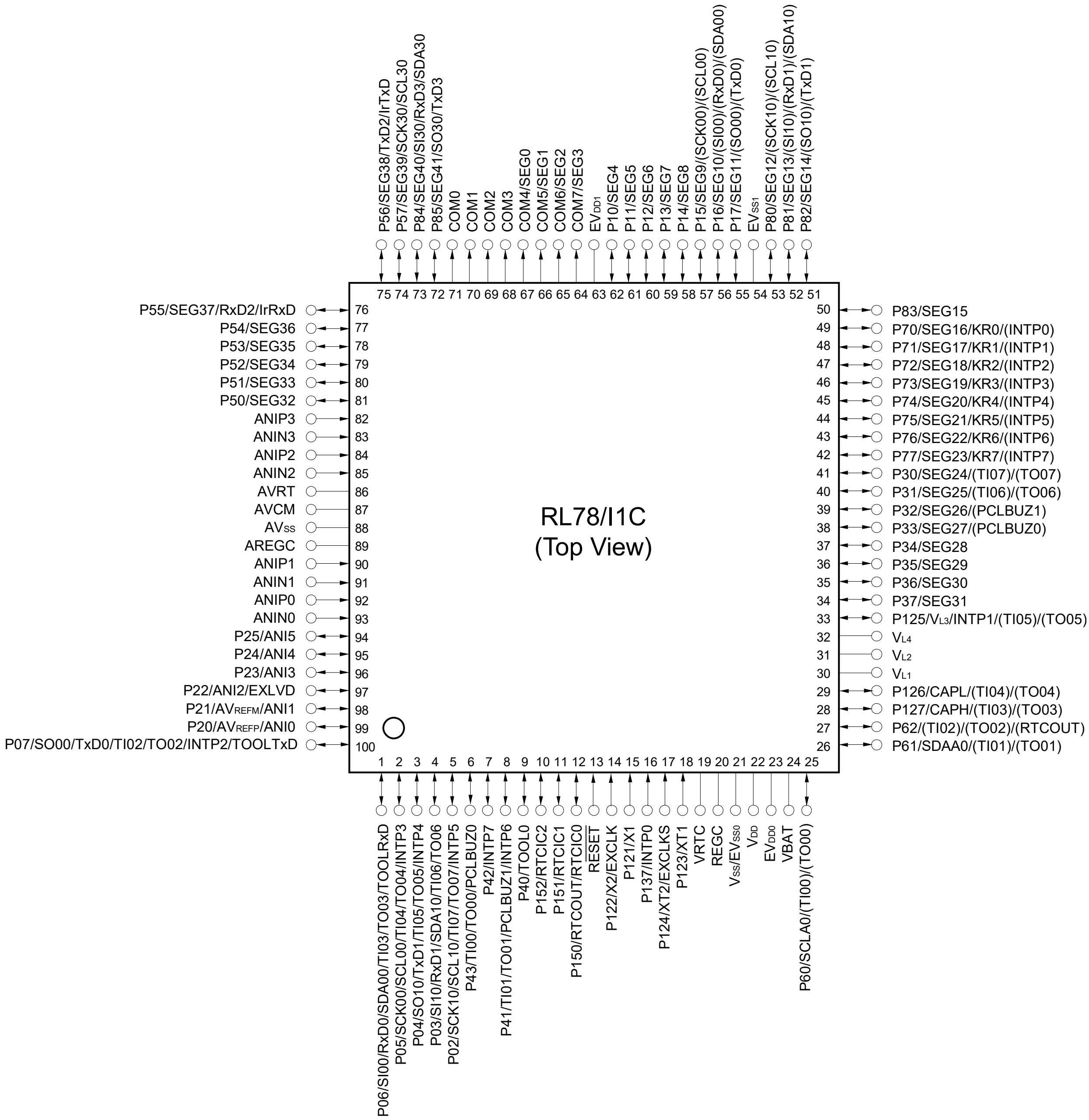
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR0). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR0) in the RL78/I1C User's Manual**.

1.3.3 100-pin products

- 100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)



Cautions 1. Make EV_{SS1} the same potential as V_{SS}/EV_{SS0}.

2. Make EV_{DD1} the same potential as EV_{DD0}.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD1} pins and connect the V_{SS} and EV_{SS1} pins to separate ground lines.

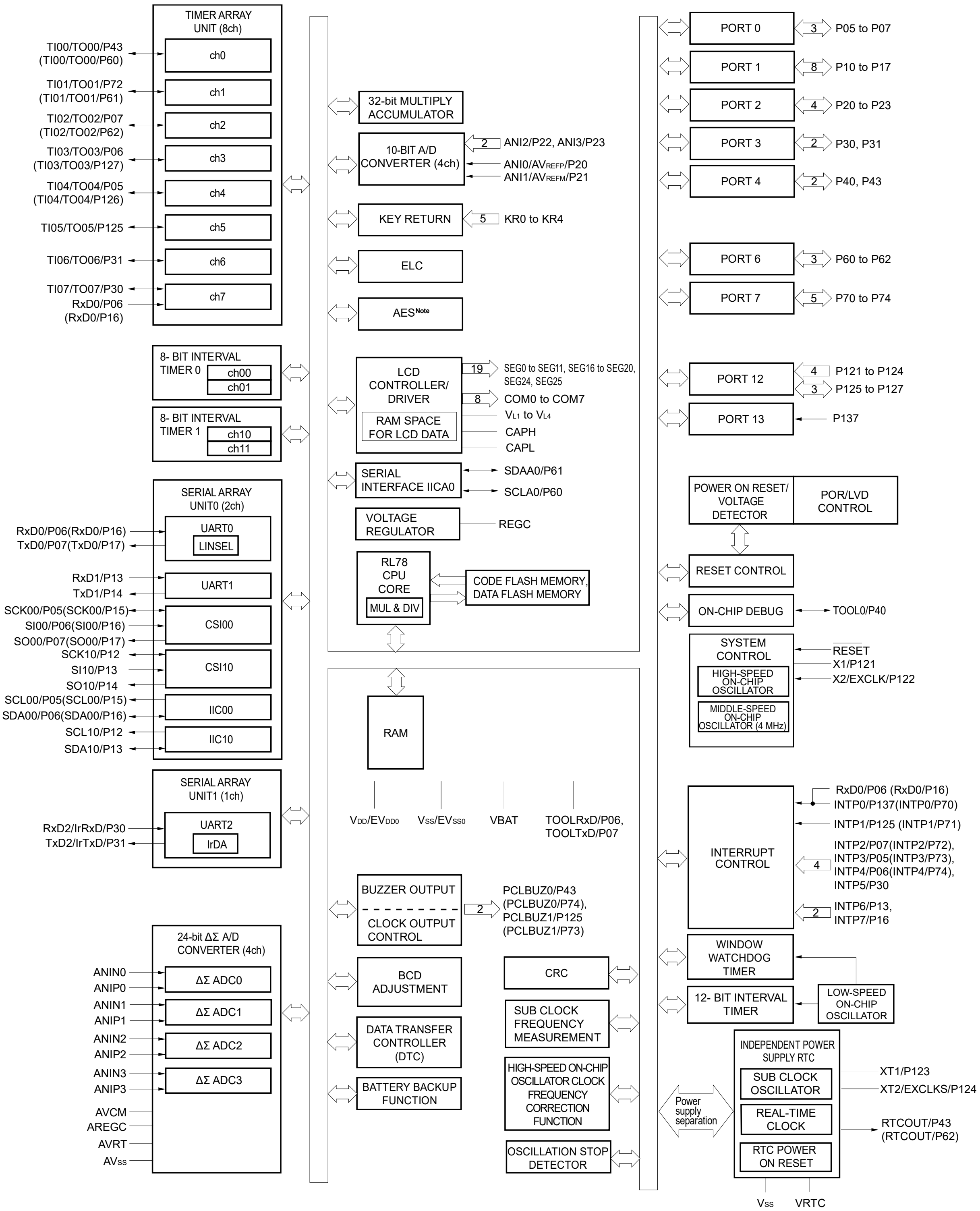
3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR0). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR0) in the RL78/I1C User's Manual**.

1.4 Pin Identification

ANI0 to ANI5:	Analog Input
ANIN0 to ANIN3, ANIP0 to ANIP3:	Analog Input for ΔΣ ADC
AREGC:	Regulator Capacitance for ΔΣ ADC
AVCM:	Control for ΔΣ ADC
AV_{REFM}:	A/D Converter Reference Potential (– side) Input
AV_{REFP}:	A/D Converter Reference Potential (+ side) Input
AVRT:	Reference Potential for ΔΣ ADC
AV_{SS}:	Ground for ΔΣ ADC
CAPH, CAPL:	Capacitor Connection for LCD Controller/Driver
COM0 to COM7:	Common Signal Output for LCD Controller/Driver
EV_{DD0}, EV_{DD1}:	Power Supply for Port
EV_{SS0}, EV_{SS1}:	Ground for Port
EXCLK:	External Clock Input (Main System Clock)
EXCLKS:	External Clock Input (Subsystem clock)
EXLVD:	External Input for Low Voltage Detector
INTP0 to INTP7:	Interrupt Request From Peripheral
IrRxD:	Receive Data for IrDA
IrTxD:	Transmit Data for IrDA
KR0 to KR7:	Key Return
P02 to P07:	Port 0
P10 to P17:	Port 1
P20 to P25:	Port 2
P30 to P37:	Port 3
P40 to P43:	Port 4
P50 to P57:	Port 5
P60 to P62:	Port 6
P70 to P77:	Port 7
P80 to P85:	Port 8
P121 to P127:	Port 12
P137:	Port 13
P150 to P152:	Port 15
PCLBUZ0, PCLBUZ1:	Programmable Clock Output/Buzzer Output
REGC:	Regulator Capacitance
$\overline{RESET}$:	Reset
RTCOUT:	Real-time Clock Correction Clock (1 Hz/64 Hz) Output
RTCIC0 to RTCIC2:	RTC Time Capture Event Input
RxD0 to RxD3:	Receive Data for UART
SCL00, SCL10, SCL30:	Serial Clock Output for Simplified IIC
SDA00, SDA10, SDA30:	Serial Data Input/Output for Simplified IIC
SCLA0 :	Serial Clock Input/Output for IICA0
SDAA0:	Serial Data Input/Output for IICA0
SCK00, SCK10, SCK30:	Serial Clock Input/Output for CSI
SEG0 to SEG41:	Segment Signal Output for LCD Controller/Driver
SI00, SI10, SI30:	Serial Data Input for CSI
SO00, SO10, SO30:	Serial Data Output for CSI
TI00 to TI07:	Timer Input
TO00 to TO07:	Timer Output
TOOL0:	Data Input/Output for Tool
TOOLRxD, TOOLTxD:	Data Input/Output for External Device
TxD0 to TxD3:	Transmit Data for UART
VBAT:	Battery Backup Power Supply
V_{DD}:	Power Supply
V_{L1} to V_{L4}:	Voltage for Driving LCD
VRTC:	RTC Power Supply
V_{SS}:	Ground
X1, X2:	Crystal Oscillator (Main System Clock)
XT1, XT2:	Crystal Oscillator (Subsystem Clock)

1.5 Block Diagram

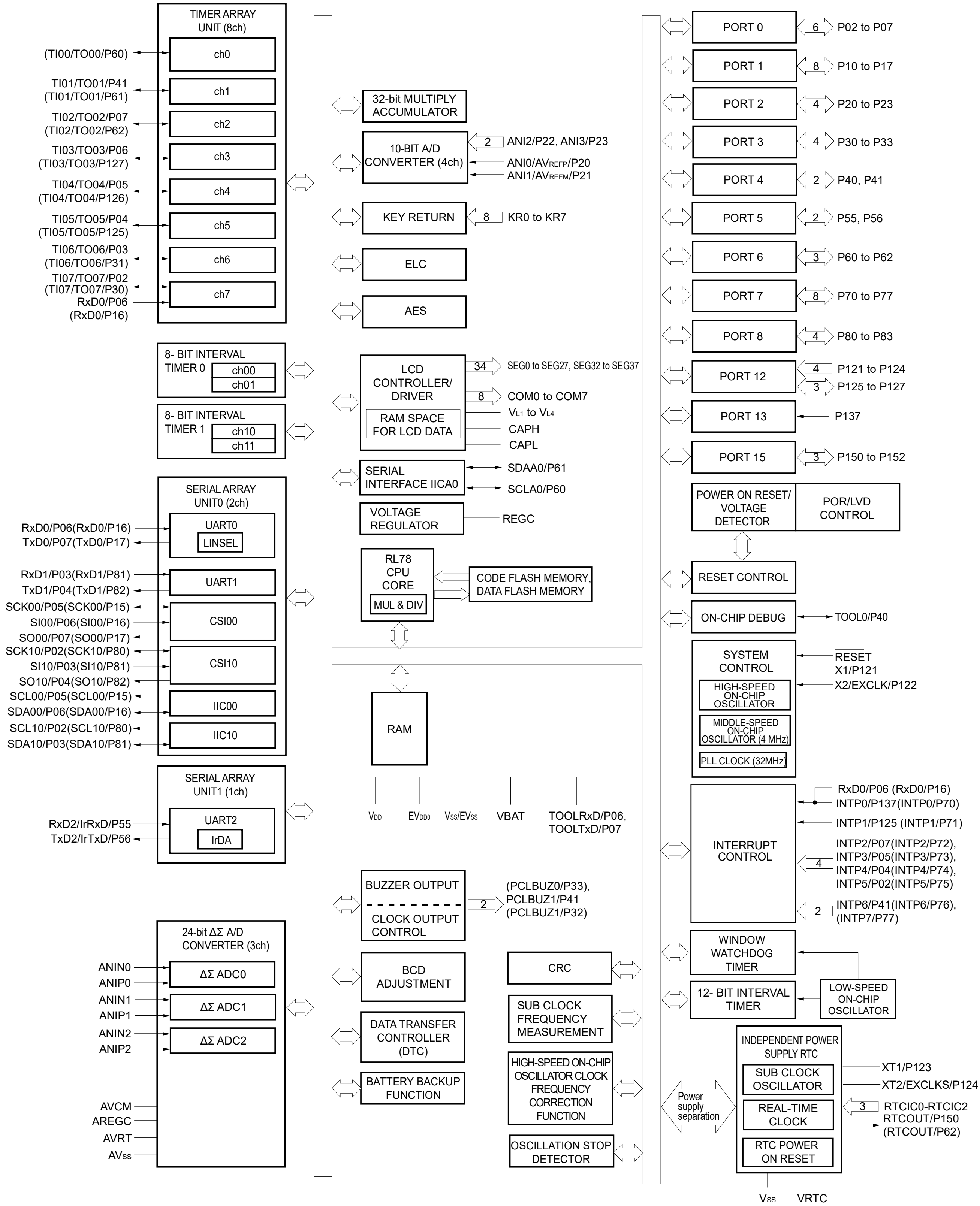
1.5.1 64-pin products



Note Only available in R5F10N products.

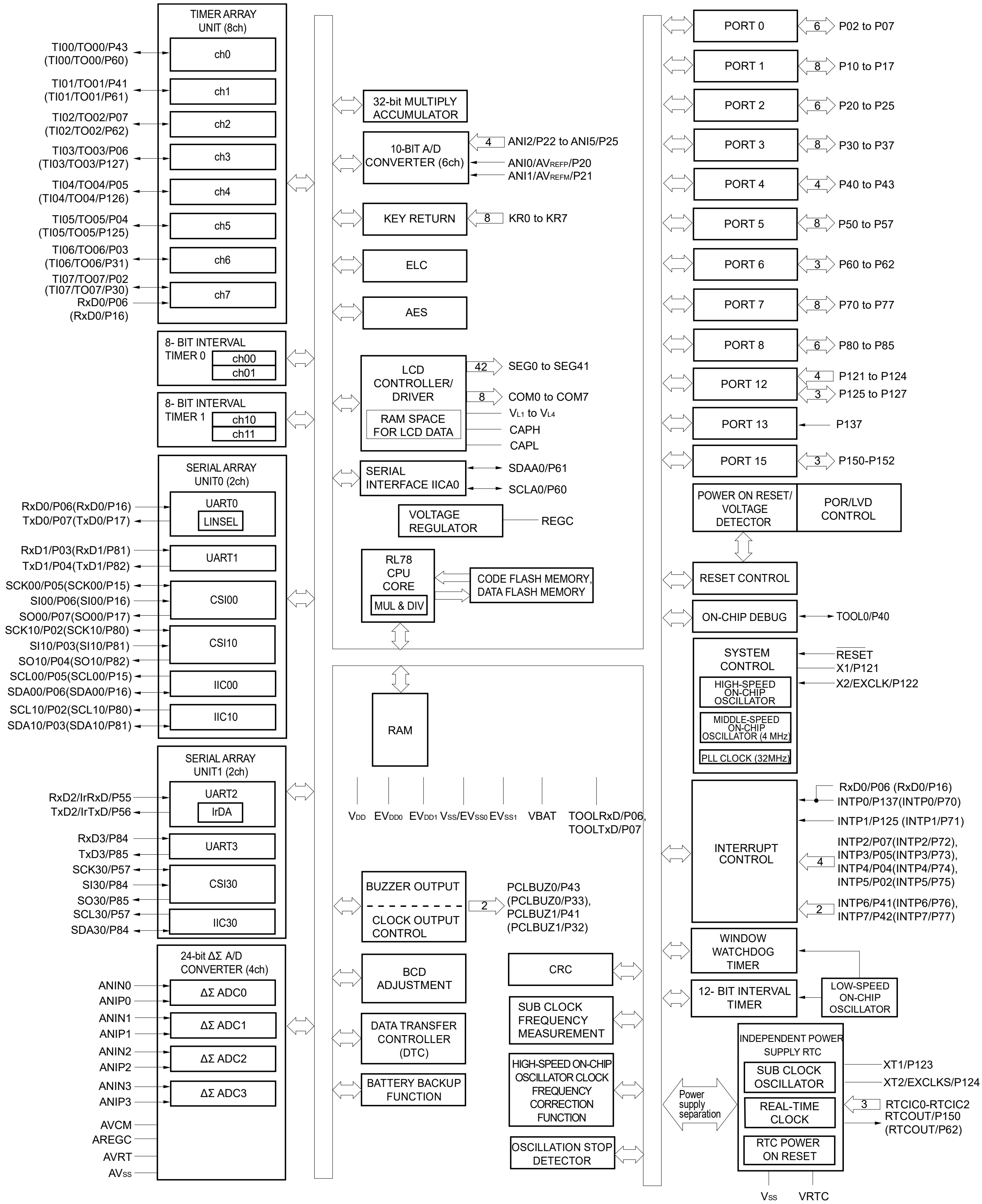
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR0). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR0) in the RL78/I1C User's Manual**.

1.5.2 80-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR0). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR0) in the RL78/I1C User's Manual**.

1.5.3 100-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR0). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR0) in the RL78/I1C User's Manual**.

1.6 Outline of Functions

(1/3)

Item		64-pin		80-pin			100-pin	
		R5F10NLEDFB/ R5F11TLEDFB	R5F10NLGDFB/ R5F11TLGDFB	R5F10NMEDFB	R5F10NMGDFB	R5F10NMJDFB	R5F10NPGDFB	R5F10NPJDFB
Code flash memory (KB)		64 KB	128 KB	64 KB	128 KB	256 KB	128 KB	256 KB
Data flash memory (KB)		2 KB						
RAM (KB)		6 KB	8 KB Note 1	6 KB	8 KB Note 1	16 KB Note 2	8 KB	16 KB Note 2
Address space		1 MB						
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.5 to 5.5 V), HS (High-speed main) mode: 1 to 12 MHz (V_{DD} = 2.4 to 5.5 V), HS (High-speed main) mode: 1 to 6 MHz (V_{DD} = 2.1 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.9 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.7 to 5.5 V), LP (Low-power main) mode: 1 MHz (V_{DD} = 1.9 to 5.5 V)						
	High -speed on-chip oscillator clock (f_{IH}) MAX.: 24 MHz	HS (High-speed main) mode: 1 to 24 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.5 to 5.5 V), HS (High-speed main) mode: 1 to 12 MHz (V_{DD} = 2.4 to 5.5 V), HS (High-speed main) mode: 1 to 6 MHz (V_{DD} = 2.1 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.9 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.7 to 5.5 V), LP (Low-power main) mode: 1 MHz (V_{DD} = 1.9 to 5.5 V)						
	Middle -speed on-chip oscillator clock (f_{IM}) MAX.: 4 MHz							
	PLL clock (f_{PLL})	-				HS (High-speed main) mode: 32 MHz (V_{DD} = 2.8 to 5.5 V)		
Subsystem clock	Subsystem clock oscillator clock (f_{SX})	XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.): V_{DD} = 1.7 to 5.5 V						
	Low-speed on-chip oscillator clock (f_{IL})	15 kHz (TYP.): V_{DD} = 1.7 to 5.5V						
High-speed on-chip oscillator clock frequency correction function		Correct the frequency of the high-speed on-chip oscillator clock by the subsystem clock.						
General-purpose register		8 bits × 8 registers × 4 banks						
Minimum instruction execution time		0.03125 μs (PLL clock: f_{PLL} = 32 MHz selection)						
		0.04167 μs (High-speed on-chip oscillator: f_{IH} = 24 MHz operation)						
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)						
		66.6 μs (Low-speed on-chip oscillator: f_{IL} = 15 kHz operation)						
Instruction set		● Data transfer (8/16 bits) ● Adder and subtractor/logical operation (8/16 bits) ● Multiplication (16 bits × 16 bits), division (32 bits ÷ 32 bits) ● Multiplication and accumulation (16 bits × 16 bits + 32 bits) ● Rotate, barrel shift, and bit manipulation (set, reset, test, and boolean operation), etc.						
I/O port	Total	35		52			68	
	CMOS I/O	27		44			60	
	CMOS input	5		5			5	
	CMOS output	-		-			-	
	N-ch O.D I/O (6 V tolerance)	3		3			3	

Notes 1. In the case of the 8 KB, this is about 7 KB when the self-programming function is used.

2. In the case of the 16 KB, this is about 15 KB when the self-programming function is used.

(2/3)

Item		64-pin		80-pin			100-pin	
		R5F10NLEDFB/ R5F11TLEDFB	R5F10NLGDFB/ R5F11TLGDFB	R5F10NMEDFB	R5F10NMGDFB	R5F10NMJDFB	R5F10NPGDFB	R5F10NPJDFB
Timer	16-bit timer TAU	8 channels						
	Watchdog timer	1 channel						
	12-bit interval timer	1 channel						
	8/16-bit interval timer	4 channels (8-bit)/2 channels (16-bit)						
	Independent power supply real-time clock (RTC)	1 channel						
	Oscillation stop detection circuit	1 channel						
	Timer output	Timer outputs: 8 channels PWM outputs: 7 Note 1						
	RTC output	1 channel ● 1 Hz/64 Hz (sub clock: f_{SX} = 32.768 kHz)						
	RTC time capture input	-		3 channels				
Clock output/buzzer output		2						
		● 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) ● 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Sub clock: f_{SX} = 32.768 kHz operation)						
10-bit resolution A/D converter		4 channels		4 channels			6 channels	
24-Bit ΔΣ A/D Converter		4 channels		3 channels			4 channels	
	SNDR	Typ. 80 dB (gain ×1) Min. 69 dB (gain ×16) Min. 65 dB (gain ×32)						
	Sampling frequency	3.906 kHz/1.953 kHz						
	PGA	×1, ×2, ×4, ×8, ×16, ×32						
Serial interface	Simplified SPI (CSI)/ UART/simplified I^2C:	2 channels		2 channels			3 channels	
	UART/IrDA	1 channel						
	I^2C bus	1 channel						
32-bit multiplier and multiply-accumulator		32 bits × 32 bits = 64 bits (Unsigned or signed) (5 clock) 32 bits × 32 bits + 64 bits = 64 bits (Unsigned or signed) (5 clock)						
Data transfer controller (DTC)		36 sources					38 sources	
Event link controller (ELC)	Event input	9						
	Event trigger input	13						
LCD controller/driver		Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.						
	Segment signal output	19 (15) Note 2		34 (30) Note 2			42 (38) Note 2	
	Common signal output	4 (8) Note 2						
Vectored interrupt sources	Internal	41		41			44	
	External	9		12			12	

Notes 1. The number of outputs varies, depending on the setting of channels in use and the number of the master (see **8.9.3 Operation as multiple PWM output function in the RL78/I1C User's Manual**).

2. The values in parentheses are the number of signal outputs when 8 com is used.

(3/3)

Item		64-pin		80-pin			100-pin	
		R5F10NLEDFB/ R5F11TLEDFB	R5F10NLGDFB/ R5F11TLGDFB	R5F10NMEDFB	R5F10NMGDFB	R5F10NMJDFB	R5F10NPGDFB	R5F10NPJDFB
Key interrupt input		5		8				
AES circuit[Note 3]		Cipher modes of operation: GCM/ECB/CBC Encryption key length: 128/192/256-bit						
Reset	MCU	• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset of internal V_{DD}[Note 1] power supply • Internal reset by voltage detector of internal V_{DD}[Note 1] power supply • Internal reset by illegal instruction execution[Note 2] • Internal reset by RAM parity error • Internal reset by illegal-memory access						
	RTC	• RTC circuit reset by RTC Power-on-reset						
Power-on-reset circuit	Internal V_{DD} Note 1	• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)						
	VRTC	• RTC Power-on-reset: 1.52 V (TYP.) • RTC Power-down-reset: 1.50 V (TYP.)						
Voltage detector	Internal V_{DD} Note 1	• Rising edge: 1.77 V to 4.06 V (13 stages) • Falling edge: 1.73 V to 3.98 V (13 stages)						
	V_{DD}	• Rising edge: 2.53 V to 3.77 V (6 stages) • Falling edge: 2.46 V to 3.70 V (6 stages)						
	VBAT	• Rising edge: 2.11 V to 2.73 V (7 stages) • Falling edge: 2.05 V to 2.67 V (7 stages)						
	VRTC	• Rising edge: 2.22 V to 2.84 V (4 stages) • Falling edge: 2.16 V to 2.78 V (4 stages)						
	EXLVD	• Rising edge: 1.33 V • Falling edge: 1.28 V						
Battery backup function	CPU	V_{DD}/VBAT						
	ΔΣ A/D Converter	V_{DD}/VBAT						
	RTC	VRTC (independent power supply)						
On-chip debug function		Provided						
Power supply voltage		V_{DD} = 1.7 to 5.5 V						
Operating ambient temperature		T_A = –40 to +85°C						

Notes 1. Either V_{DD} or VBAT is selected by the battery backup function.

2. This reset occurs when instruction code FFH is executed.
This reset does not occur during emulation using an in-circuit emulator or an on-chip debugging emulator.

3. Only available in R5F10N products.

2. ELECTRICAL SPECIFICATIONS

Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. See 2.1 Port Function to 2.2.1 With functions for each product in the RL78/I1C User's Manual.

Remarks 1. In the descriptions in this chapter, read EV_{DD} as EV_{DD0} and EV_{DD1}, and EV_{SS} as EV_{SS0} and EV_{SS1}.

2. For 64-pin products, read EV_{DD} as V_{DD} and EV_{SS} as V_{SS}.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (1/3)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +6.5	V
	EV_{DD}		–0.5 to +6.5	V
	V_{BAT}		–0.5 to +6.5	V
	V_{RTC}		–0.5 to +6.5	V
REGC pin input voltage	V_{IREGC}	REGC	–0.3 to +2.8 and –0.3 to V_{DD} Note 4 +0.3 Note 1	V
Input voltage	V_{I1}	P02 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P57, P70 to P77, P80 to P85, P125 to P127	–0.3 to EV_{DD} +0.3 and –0.3 to V_{DD} Note 4 +0.3 Note 2	V
	V_{I2}	P60 to P62 (N-ch open-drain)	–0.3 to +6.5	V
	V_{I3}	P20 to P25, P121 to P122, P137, P150 to 152, EXCLK	–0.3 to V_{DD} Note 4 +0.3 Note 2	V
	V_{I4}	$\overline{\text{RESET}}$	–0.3 to +6.5	V
	V_{I5}	P123, P124, EXCLKS	–0.3 to V_{RTC} +0.3 Note 2	V
Output voltage	V_{O1}	P02 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P57, P60 to P62, P70 to P77, P80 to P85, P125 to P127	–0.3 to EV_{DD} +0.3 and –0.3 to V_{DD} Note 4 +0.3 Note 2	V
	V_{O2}	P20 to P25, P150 to P152	–0.3 to V_{DD} Note 4 +0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI0 to ANI5	–0.3 to V_{DD} Note 4 +0.3 and –0.3 to $AV_{REF(+)}$ +0.3 Notes 2, 3	V
	V_{AI2}	ANIP0 to ANIP3, ANIN0 to ANIN3	–0.6 to +2.8 and –0.6 to AREGC +0.3 Note 5	V
Reference supply voltage	V_{IDSAD}	AREGC, AVCM, AVRT	–0.3 to +2.8 and –0.3 to V_{DD} Note 4 +0.3 Note 6	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

4. Either V_{DD} or VBAT is selected by the battery backup function.

5. The ΔΣ A/D conversion target pin must not exceed AREGC +0.3 V.

6. Connect AREGC, AVCM, and AVRT terminals to V_{SS} via capacitor (0.47 μF). This value defines the absolute maximum rating of AREGC, AVCM, and AVRT terminal. Do not use with voltage applied.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. V_{SS}: Reference voltage

Absolute Maximum Ratings (2/3)

Parameter	Symbols	Conditions		Ratings	Unit
LCD voltage	V_{LI1}	V_{L1} voltage[Note 1]		–0.3 to 2.8 and –0.3 to V_{L4} +0.3	V
	V_{LI2}	V_{L2} voltage[Note 1]		–0.3 to V_{L4} +0.3[Note 2]	V
	V_{LI3}	V_{L3} voltage[Note 1]		–0.3 to V_{L4} +0.3[Note 2]	V
	V_{LI4}	V_{L4} voltage[Note 1]		–0.3 to +6.5	V
	V_{LCAP}	CAPL, CAPH voltage[Note 1]		–0.3 to V_{L4} +0.3[Note 2]	V
	V_{OUT}	COM0 to COM7, SEG0 to SEG41, output voltage	External resistance division method	–0.3 to V_{DD}[Note 3] +0.3[Note 2]	V
			Capacitor split method	–0.3 to V_{DD}[Note 3] +0.3[Note 2]	V
			Internal voltage boosting method	–0.3 to V_{L4} +0.3[Note 2]	V

Notes 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 μF ± 30%) and connect a capacitor (0.47 μF ± 30%) between the CAPL and CAPH pins.

2. Must be 6.5 V or lower.

3. Either V_{DD} or VBAT is selected by the battery backup function.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark V_{SS}: Reference voltage

Absolute Maximum Ratings (3/3)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P02 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P57, P70 to P77, P80 to P85, P125 to P127	–40	mA
		Total of all pins –170 mA	P02 to P07, P40 to P43	–70	mA
			P10 to P17, P30 to P37, P50 to P57, P70 to P77, P80 to P85, P125 to P127	–100	mA
	I_{OH2}	Per pin	P20 to P25, P150 to P152	–0.5	mA
		Total of all pins		–2	mA
Output current, low	I_{OL1}	Per pin	P02 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P57, P70 to P77, P80 to P85, P125 to P127	40	mA
		Total of all pins 170 mA	P02 to P07, P40 to P43	70	mA
			P10 to P17, P30 to P37, P50 to P57, P60 to P62, P70 to P77, P80 to P85, P125 to P127	100	mA
	I_{OL2}	Per pin	P20 to P25, P150 to P152	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(T_A = –40 to +85°C, 1.7 V ≤ V_{DD} Note 2 ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Notes 1, 2	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.5 V ≤ V_{DD} < 2.7 V	1.0		16.0	MHz
		2.4 V ≤ V_{DD} < 2.5 V	1.0		12.0	MHz
		1.9 V ≤ V_{DD} < 2.4 V	1.0		8.0	MHz
		1.7 V ≤ V_{DD} < 1.9 V	1.0		4.0	MHz
XT1 clock oscillation frequency (f_{XT}) Notes 1, 2	Crystal resonator		32	32.768	35	kHz

Notes 1. Indicates only permissible oscillator frequency ranges. See **2.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

2. Either V_{DD} or VBAT is selected by the battery backup function.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, see **6.4 System Clock Oscillator in the RL78/I1C User's Manual**.

2.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 1.7 V ≤ V_{DD} Note 3 ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}			1.5		24	MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to +85°C	1.9 V ≤ V_{DD} Note 3 ≤ 5.5 V	–1.0		+1.0	%
			1.7 V ≤ V_{DD} Note 3 ≤ 1.9 V	–5.0		+5.0	%
		–40 to –20°C	1.9 V ≤ V_{DD} Note 3 ≤ 5.5 V	–1.5		+1.5	%
			1.7 V ≤ V_{DD} Note 3 ≤ 1.9 V	–5.5		+5.5	%
Middle-speed on-chip oscillator clock frequency Note 2	f_{IM}			1		4	MHz
Middle-speed on-chip oscillator clock frequency accuracy		1.9 V ≤ V_{DD} Note 3 ≤ 5.5 V		–12		+12	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				–15		+15	%

Notes 1. The high-speed on-chip oscillator frequency is selected by using bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

2. This indicates the oscillator characteristics only. See **2.4 AC Characteristics** for the instruction execution time.

3. Either V_{DD} or VBAT is selected by the battery backup function.

2.2.3 PLL oscillator characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} Note 2 ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
PLL input frequency Note 1	f_{PLLIN}	f_{IH}		4		MHz
PLL output frequency Note 1	f_{PLL}			32		MHz
Lockup wait time		Wait time from PLL output enable to frequency stabilization	40			μs
Interval wait time		Wait time from PLL stop to PLL restart setting	4			μs
Setting wait time		Wait time from PLL input clock stabilization and PLL setting fixedness to start-up setting	1			μs

Notes 1. Indicates only permissible oscillator frequency ranges.

2. Either V_{DD} or VBAT is selected by the battery backup function.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 4 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P02 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P57, P70 to P77, P80 to P85, P125 to P127	1.9 V ≤ EV_{DD} ≤ 5.5 V			–10.0 Note 2	mA
		Total of P02 to P07, P40 to P43 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			–55.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–10.0	mA
			1.9 V ≤ EV_{DD} < 2.7 V			–5.0	mA
			1.7 V ≤ EV_{DD} < 1.9 V			–2.5	mA
		Total of P10 to P17, P30 to P37, P50 to P57, P70 to P77, P80 to P85, P125 to P127 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			–80.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–19.0	mA
			1.9 V ≤ EV_{DD} < 2.7 V			–10.0	mA
			1.7 V ≤ EV_{DD} < 1.9 V			–5.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				–100.0	mA
	I_{OH2}	Per pin for P20 to P25, P150 to P152	1.7 V ≤ V_{DD} Note 4 ≤ 5.5 V			–0.1 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.7 V ≤ V_{DD} Note 4 ≤ 5.5 V			–0.9	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD} and V_{DD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

4. Either V_{DD} or VBAT is selected by the battery backup function.

Caution P02 to P07, P12 to P17, P31, P56, P57, P80 to P82, P84, and P85 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note 4] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P02 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P57, P70 to P77, P80 to P85, P125 to P127				20.0[Note 2]	mA
		Per pin for P60 to P62				15.0[Note 2]	mA
		Total of P02 to P07, P40 to P43 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV_{DD} ≤ 5.5 V			70.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			15.0	mA
			1.9 V ≤ EV_{DD} < 2.7 V			9.0	mA
			1.7 V ≤ EV_{DD} < 1.9 V			4.5	mA
		Total of P10 to P17, P30 to P37, P50 to P57, P60 to P62, P70 to P77, P80 to P85, P125 to P127 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV_{DD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			35.0	mA
			1.9 V ≤ EV_{DD} < 2.7 V			20.0	mA
			1.7 V ≤ EV_{DD} < 1.9 V			10.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])				150.0	mA
	I_{OL2}	Per pin for P20 to P25, P150 to P152	1.7 V ≤ V_{DD}[Note 4] ≤ 5.5 V			0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.7 V ≤ V_{DD}[Note 4] ≤ 5.5 V			3.6	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS} and V_{SS} pins.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Either V_{DD} or VBAT is selected by the battery backup function.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P02 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P57, P70 to P77, P80 to P85, P125 to P127	Normal input buffer	$0.8EV_{DD}$		EV_{DD}	V
	V_{IH2}	P02, P03, P05, P06, P12, P13, P15, P16, P30, P55, P57, P80, P81, P84	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	2.2		EV_{DD}	V
			TTL input buffer 3.3 V ≤ EV_{DD} < 4.0 V	2.0		EV_{DD}	V
			TTL input buffer 1.7 V ≤ EV_{DD} < 3.3 V	1.5		EV_{DD}	V
	V_{IH3}	P20 to P25		$0.7V_{DD}$ Note		V_{DD} Note	V
	V_{IH4}	P60 to P62		$0.7EV_{DD}$		6.0	V
	V_{IH5}	P121 to P122, P137, P150 to P152, EXCLK		$0.8V_{DD}$ Note		V_{DD} Note	V
	V_{IH6}	$\overline{\text{RESET}}$		$0.8V_{DD}$ Note		6.0	V
	V_{IH7}	P123, P124, EXCLKS		$0.8V_{RTC}$		V_{RTC}	V
Input voltage, low	V_{IL1}	P02 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P57, P70 to P77, P80 to P85, P125 to P127	Normal input buffer	0		$0.2EV_{DD}$	V
	V_{IL2}	P02, P03, P05, P06, P12, P13, P15, P16, P30, P55, P57, P80, P81, P84	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.7 V ≤ EV_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P25		0		$0.3V_{DD}$ Note	V
	V_{IL4}	P60 to P62		0		$0.3EV_{DD}$	V
	V_{IL5}	P121, P122, P137, P150 to P152, EXCLK, $\overline{\text{RESET}}$		0		$0.2V_{DD}$ Note	V
	V_{IL6}	P123, P124, EXCLKS		0		$0.2V_{RTC}$	V

Note Either V_{DD} or VBAT is selected by the battery backup function.

Caution The maximum value of V_{IH} of pins P02 to P07, P12 to P17, P31, P56, P57, P80 to P82, P84, and P85 is EV_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P02 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P57, P70 to P77, P80 to P85, P125 to P127	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –10.0 mA	EV_{DD} – 1.5			V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	EV_{DD} – 0.7			V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –2.0 mA	EV_{DD} – 0.6			V
			1.9 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –1.5 mA	EV_{DD} – 0.5			V
			1.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –1.0 mA	EV_{DD} – 0.5			V
	V_{OH2}	P20 to P25, P150 to P152	1.7 V ≤ V_{DD} Note ≤ 5.5 V, I_{OH2} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P02 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P57, P70 to P77, P80 to P85, P125 to P127	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 20 mA			1.3	V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			1.9 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
			1.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20 to P25, P150 to P152	1.7 V ≤ V_{DD} Note ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P62	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 15.0 mA			2.0	V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 5.0 mA			0.4	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 3.0 mA			0.4	V
			1.9 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 2.0 mA			0.4	V
			1.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 1.0 mA			0.4	V

Note Either V_{DD} or VBAT is selected by the battery backup function.

Caution P02 to P07, P12 to P17, P31, P56, P57, P80 to P82, P84, and P85 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}^Note^ ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P02 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P57, P60 to P62, P70 to P77, P80 to P85, P125 to P127	V_I = EV_{DD}				1	μA
	I_{LIH2}	P20 to P25, P137, P150 to P152, $\overline{\text{RESET}}$	V_I = V_{DD} Note				1	μA
	I_{LIH3}	P121, P122 (X1, X2, EXCLK)	V_I = V_{DD} Note	In input port or external clock input			1	μA
				In resonator connection			10	μA
	I_{LIH4}	P123, P124 (EXCLKS)	V_I = V_{RTC}	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P02 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P57, P70 to P77, P80 to P85, P125 to P127	V_I = EV_{SS}				–1	μA
	I_{LIL2}	P20 to P25, P137, P150 to P152, $\overline{\text{RESET}}$	V_I = V_{SS}				–1	μA
	I_{LIL3}	P121, P122 (X1, X2, EXCLK)	V_I = V_{SS}	In input port or external clock input			–1	μA
				In resonator connection			–10	μA
	I_{LIL4}	P123, P124 (EXCLKS)	V_I = V_{SS}	In input port or external clock input			–1	μA
				In resonator connection			–10	μA
On-chip pull-up resistance	R_{U1}	P10 to P17, P30 to P37, P50 to P57, P70 to P77, P80 to P85, P125 to P127	V_I = EV_{SS}	2.4 V ≤ EV_{DD} ≤ 5.5 V	10	20	100	kΩ
				1.7 V ≤ EV_{DD} ≤ 5.5 V	10	30	100	kΩ
	R_{U2}	P02 to P07, P40 to P43, P150 to P152	V_I = EV_{SS}		10	20	100	kΩ

Note Either V_{DD} or VBAT is selected by the battery backup function.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 8 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/6)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{CLK} = 32 MHz Note 3 PLL operation	Normal operation	V_{DD} = 5.0 V		5.2	8.5	mA
						V_{DD} = 3.0 V		5.2	8.5	mA
				f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V		1.7		mA
						V_{DD} = 3.0 V		1.7		mA
					Normal operation	V_{DD} = 5.0 V		3.9	6.6	mA
						V_{DD} = 3.0 V		3.9	6.6	mA
				f_{IH} = 12 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.4	3.8	mA
						V_{DD} = 3.0 V		2.4	3.8	mA
				f_{IH} = 6 MHz Note 3	Normal operation	V_{DD} = 5.0 V		1.7	2.6	mA
						V_{DD} = 3.0 V		1.7	2.6	mA
				f_{IH} = 3 MHz Note 3	Normal operation	V_{DD} = 5.0 V		1.3	2.0	mA
						V_{DD} = 3.0 V		1.3	2.0	mA
			LS (low-speed main) mode Note 5	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	2.2	mA
						V_{DD} = 2.0 V		1.3	2.2	mA
				f_{IH} = 6 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.1	2.1	mA
						V_{DD} = 2.0 V		1.1	2.1	mA
				f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		0.84	1.40	mA
						V_{DD} = 2.0 V		0.84	1.40	mA
				f_{IM} = 4 MHz Note 6	Normal operation	V_{DD} = 3.0 V		0.70	1.20	mA
						V_{DD} = 2.0 V		0.70	1.20	mA
				f_{IH} = 3 MHz Note 3	Normal operation	V_{DD} = 3.0 V		0.7	1.4	mA
						V_{DD} = 2.0 V		0.7	1.4	mA
			LV (low-voltage main) mode Note 5	f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	1.9	mA
						V_{DD} = 2.0 V		1.3	1.9	mA
			LP (low-power main) mode Note 5	f_{IH} = 1 MHz Note 3	Normal operation	V_{DD} = 3.0 V		315	530	μA
						V_{DD} = 2.0 V		315	530	μA
				f_{IM} = 1 MHz Note 6	Normal operation	V_{DD} = 3.0 V		160	300	μA
						V_{DD} = 2.0 V		160	300	μA

(**Notes** and **Remarks** are listed on the page after the next page.)

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 8 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/6)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.3	5.5	mA
						Resonator connection		3.5	5.7	mA
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.3	5.5	mA
						Resonator connection		3.5	5.7	mA
				f_{MX} = 16 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.8	4.4	mA
						Resonator connection		2.9	4.6	mA
				f_{MX} = 16 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.8	4.4	mA
						Resonator connection		2.9	4.6	mA
				f_{MX} = 12 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.3	3.6	mA
						Resonator connection		2.4	3.7	mA
				f_{MX} = 12 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.3	3.6	mA
						Resonator connection		2.4	3.7	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.0	3.2	mA
						Resonator connection		2.1	3.3	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.0	3.2	mA
						Resonator connection		2.1	3.3	mA
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.1	2.0	mA
						Resonator connection		1.2	2.1	mA
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.1	2.0	mA
						Resonator connection		1.2	2.1	mA
				f_{MX} = 4 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		0.7	1.2	mA
						Resonator connection		0.7	1.3	mA
				f_{MX} = 4 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		0.7	1.2	mA
						Resonator connection		0.7	1.3	mA
			LP (low-power main) mode Note 5	f_{IH} = 1 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		140	240	μA
						Resonator connection		190	300	μA
				f_{IH} = 1 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		140	240	μA
						Resonator connection		190	300	μA
			Subclock operation	f_{SUB} = 32.768 kHz Note 4, T_A = –40°C	Normal operation	Square wave input		5.1	6.6	μA
						Resonator connection		5.2	6.7	μA
				f_{SUB} = 32.768 kHz Note 4, T_A = +25°C	Normal operation	Square wave input		5.4	7.1	μA
						Resonator connection		5.5	7.2	μA
				f_{SUB} = 32.768 kHz Note 4, T_A = +50°C	Normal operation	Square wave input		5.6	8.0	μA
						Resonator connection		5.7	8.1	μA
				f_{SUB} = 32.768 kHz Note 4, T_A = +70°C	Normal operation	Square wave input		6.1	9.7	μA
						Resonator connection		6.2	9.8	μA
				f_{SUB} = 32.768 kHz Note 4, T_A = +85°C	Normal operation	Square wave input		6.8	13.7	μA
						Resonator connection		6.9	13.8	μA
				f_{IL} = 15 kHz, T_A = +85°C Note 7	Normal operation			2.5	7.0	μA
				f_{IL} = 15 kHz, T_A = –40°C Note 7	Normal operation			2.8	7.0	μA
				f_{IL} = 15 kHz, T_A =+ 25°C Note 7	Normal operation			4.1	11.0	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD}, EV_{DD}, and V_{RTC} including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. When the VBAT pin (pin for battery backup) is selected, current flowing into VBAT. The following points apply in the HS (high-speed main), LS (low-speed main), LV (low-voltage main), and LP (low-power main) modes.

•The currents in the "TYP." column do not include the operating currents of the peripheral modules.

• The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the LCD controller/driver, A/D converter, ΔΣA/D converter, LVD circuit, battery backup circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the independent power supply RTC.

2. When high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

3. When high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

4. When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1).

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.8\ V \le V_{DD} \le 5.5\ V$@1 MHz to 32 MHz
$2.7\ V \le V_{DD} \le 5.5\ V$@1 MHz to 24 MHz
$2.5\ V \le V_{DD} \le 5.5\ V$@1 MHz to 16 MHz
$2.4\ V \le V_{DD} \le 5.5\ V$@1 MHz to 12 MHz
$2.1\ V \le V_{DD} \le 5.5\ V$@1 MHz to 6 MHz

LS (low-speed main) mode: $1.9\ V \le V_{DD} \le 5.5\ V$@1 MHz to 8 MHz

LP (low-power main) mode: $1.9\ V \le V_{DD} \le 5.5\ V$@1 MHz

LV (low-voltage main) mode: $1.7\ V \le V_{DD} \le 5.5\ V$@1 MHz to 4 MHz

6. When high-speed on-chip oscillator, low-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

7. When high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

8. Either V_{DD} or VBAT is selected by the battery backup function.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{IM}: Middle-speed on-chip oscillator clock frequency

4. f_{IL}: Low-speed on-chip oscillator clock frequency

5. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

6. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25°C$

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 10 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/6)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{CLK} = 32 MHz Note 4, PLL operation	V_{DD} = 5.0 V		0.80	2.0	mA
					V_{DD} = 3.0 V		0.80	2.0	mA
				f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.48	1.45	mA
					V_{DD} = 3.0 V		0.48	1.45	mA
				f_{IH} = 12 MHz Note 4	V_{DD} = 5.0 V		0.37	0.91	mA
					V_{DD} = 3.0 V		0.37	0.91	mA
				f_{IH} = 6 MHz Note 4	V_{DD} = 5.0 V		0.32	0.63	mA
					V_{DD} = 3.0 V		0.32	0.63	mA
				f_{IH} = 3 MHz Note 4	V_{DD} = 5.0 V		0.29	0.49	mA
					V_{DD} = 3.0 V		0.29	0.49	mA
			LS (low-speed main) mode Note 7	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		280	740	μA
					V_{DD} = 2.0 V		280	740	μA
				f_{IH} = 6 MHz Note 4	V_{DD} = 3.0 V		230	620	μA
					V_{DD} = 2.0 V		230	620	μA
				f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V		220	440	μA
					V_{DD} = 2.0 V		220	440	μA
				f_{IM} = 4 MHz Note 5	V_{DD} = 3.0 V		55	300	μA
					V_{DD} = 2.0 V		55	300	μA
				f_{IH} = 3 MHz Note 4	V_{DD} = 3.0 V		200	534	μA
					V_{DD} = 2.0 V		200	534	μA
			LV (low-voltage main) mode Note 7	f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V		450	825	μA
					V_{DD} = 2.0 V		450	825	μA
			LP (low-power main) mode Note 7	f_{IH} = 1 MHz Note 4	V_{DD} = 3.0 V		195	400	μA
					V_{DD} = 2.0 V		195	400	μA
				f_{IM} = 1 MHz Note 5	V_{DD} = 3.0 V		33	100	μA
					V_{DD} = 2.0 V		33	100	μA
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.31	1.08	mA
					Resonator connection		0.48	1.28	mA
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.31	1.08	mA
					Resonator connection		0.48	1.28	mA
				f_{MX} = 16 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.28	0.86	mA
					Resonator connection		0.42	1.00	mA
				f_{MX} = 16 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.28	0.86	mA
					Resonator connection		0.42	1.00	mA
				f_{MX} = 12 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.23	0.70	mA
					Resonator connection		0.37	0.79	mA
				f_{MX} = 12 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.23	0.70	mA
					Resonator connection		0.36	0.79	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.21	0.63	mA
					Resonator connection		0.29	0.71	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.21	0.63	mA
					Resonator connection		0.28	0.71	mA

(**Notes** and **Remarks** are listed on the page after the next page.)

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 10 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (4/6)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	LS (low-speed main) mode Note 7	f_{MX} = 8 MHz Note 3, V_{DD} = 3.0 V	Square wave input		110	360	μA
					Resonator connection		160	420	μA
				f_{MX} = 8 MHz Note 3, V_{DD} = 2.0 V	Square wave input		110	360	μA
					Resonator connection		160	420	μA
				f_{MX} = 4 MHz Note 3, V_{DD} = 3.0 V	Square wave input		39	200	μA
					Resonator connection		81	250	μA
				f_{MX} = 4 MHz Note 3, V_{DD} = 2.0 V	Square wave input		39	200	μA
					Resonator connection		81	250	μA
			LP (low-power main) mode Note 7	f_{MX} = 1 MHz Note 3, V_{DD} = 3.0 V	Square wave input		14	100	μA
					Resonator connection		70	200	μA
				f_{MX} = 1 MHz Note 3, V_{DD} = 2.0 V	Square wave input		14	100	μA
					Resonator connection		70	200	μA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 6, T_A = –40°C	Square wave input		0.80	1.60	μA
					Resonator connection		1.00	1.80	μA
				f_{SUB} = 32.768 kHz Note 6, T_A = +25°C	Square wave input		0.93	1.70	μA
					Resonator connection		1.13	1.90	μA
				f_{SUB} = 32.768 kHz Note 6, T_A = +50°C	Square wave input		1.10	3.00	μA
					Resonator connection		1.30	3.20	μA
				f_{SUB} = 32.768 kHz Note 6, T_A = +70°C	Square wave input		1.50	5.00	μA
					Resonator connection		1.70	5.20	μA
				f_{SUB} = 32.768 kHz Note 6, T_A = +85°C	Square wave input		2.80	9.00	μA
					Resonator connection		3.00	9.20	μA
				f_{IL} = 15 kHz Note 9, T_A = –40°C			0.78	1.60	μA
									μA
				f_{IL} = 15 kHz Note 9, T_A = +25°C			1.01	1.76	μA
									μA
				f_{IL} = 15 kHz Note 9, T_A = +85°C			2.25	8.45	μA
									μA
	I_{DD3}	STOP mode Note 8	T_A = –40°C				0.47	0.90	μA
			T_A = +25°C				0.65	1.20	μA
			T_A = +50°C				0.84	2.80	μA
			T_A = +70°C				1.21	4.70	μA
			T_A = +85°C				1.82	9.00	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD}, EV_{DD}, and V_{RTC} including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. When the VBAT pin (pin for battery backup) is selected, current flowing into VBAT. The following points apply in the HS (high-speed main), LS (low-speed main), LV (low-voltage main), and LP (low-power main) modes.

•The currents in the “TYP.” column do not include the operating currents of the peripheral modules.

• The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into LCD controller/driver, the A/D converter, ΔΣA/D converter, LVD circuit, battery backup circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the independent power supply RTC.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

4. When high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

5. When high-speed on-chip oscillator, low-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

6. When operating independent power supply RTC and setting ultra-low current consumption (AMPHS1 = 1). When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	2.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
	2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
	2.5 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
	2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 12 MHz
	2.1 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 6 MHz
LS (low-speed main) mode:	1.9 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
LP (low-power main) mode:	1.9 V ≤ V_{DD} ≤ 5.5 V@1 MHz
LV (low-voltage main) mode:	1.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

8. If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.

9. When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.

10. Either V_{DD} or VBAT is selected by the battery backup function.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{IM}: Middle-speed on-chip oscillator clock frequency

4. f_{IL}: Low-speed on-chip oscillator clock frequency

5. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

6. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 15 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (5/6)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Independent power supply RTC operating current	I_{RTC} Notes 3	f_{SUB} = 32.768 kHz			0.70		μA
12-bit interval timer operating current	I_{TMKA} Notes 1, 2, 4	f_{SUB} = 32.768 kHz, f_{MAIN} is stopped			0.04		μA
8-bit interval timer operating current	I_{TMT} Notes 1, 2, 5	f_{SUB} = 32.768 kHz, f_{MAIN} is stopped, per unit	8-bit counter mode × 2 ch operation		0.12		μA
			16-bit counter mode operation		0.10		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 6	f_{IL} = 15 kHz, f_{MAIN} is stopped			0.22		μA
LVD operating current	I_{LVD} Notes 1, 7				0.10		μA
LVDVDD operating current	I_{LVDVDD}	Current flowing to V_{DD}			0.05		μA
		Current flowing to V_{DD} or VBAT Note 1			0.04		μA
LVDVBAT operating current	$I_{LVDVBAT}$	Current flowing to VBAT			0.04		μA
		Current flowing to V_{DD} or VBAT Note 1			0.04		μA
LVDVRTC operating current	$I_{LVDVRTC}$	Current flowing to VRTC			0.04		μA
		Current flowing to V_{DD} or VBAT Note 1			0.04		μA
LVDEXLVD operating current	$I_{LVDEXLVD}$	Current flowing to EXLVD			0.16		μA
		Current flowing to V_{DD} or VBAT Note 1			0.04		μA
Oscillation stop detection circuit operating current	I_{OSDC} Note 1				0.02		μA
Battery backup circuit operating current	I_{BUP} Note 1				0.05		μA
A/D converter operating current	I_{ADC} Notes 1, 8	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	2.4	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	1.0	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				105		μA
BGO operating current	I_{BGO} Notes 1, 9				2.00	12.20	mA
Self-programming operating current	I_{FSP} Notes 1, 10				2.00	12.20	mA

(**Notes** and **Remarks** are listed on the next page.)

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note 15] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (6/6)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
24-Bit ΔΣ A/D Converter operating current	I_{DSAD}[Notes 1, 11]	In 4 ch ΔΣ A/D converter operation				1.45	2.30	mA
		In 3 ch ΔΣ A/D converter operation				1.14	1.85	mA
		In 1 ch ΔΣA/D converter operation				0.52	0.94	mA
SNOOZE operating current	I_{SNOZ}[Notes 1, 12]	ADC operation	The mode is performed			0.50	0.80	mA
			The A/D conversion operations are performed, low voltage mode, AV_{REFP} = V_{DD} = 3.0 V			1.20	1.80	mA
		Simplified SPI (CSI)/UART operation				0.70	1.05	mA
		DTC operation				2.20		mA
LCD operating current	I_{LCD1}[Notes 1, 13, 14]	External resistance division method	f_{LCD} = f_{SUB} LCD clock = 128 Hz 1/3 bias, four-time-slices	V_{DD} = 5.0 V, V_{L4} = 5.0 V		0.06		μA
	I_{LCD2}[Notes 1, 13]	Internal voltage boosting method	f_{LCD} = f_{SUB} LCD clock = 128 Hz 1/3 bias, four-time-slices	V_{DD} = 3.0 V, V_{L4} = 3.0 V (VLCD = 04H)		0.85		μA
				V_{DD} = 5.0 V, V_{L4} = 5.1 V (VLCD = 12H)		1.55		μA
	I_{LCD3}[Notes 1, 13]	Capacitor split method	f_{LCD} = f_{SUB} LCD clock = 128 Hz 1/3 bias, four-time-slices	V_{DD} = 3.0 V, V_{L4} = 3.0 V		0.20		μA

Notes 1. Current flowing to V_{DD}. When the VBAT pin (battery backup power supply pin) is selected, current flowing to the VBAT.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing to VRTC pin, including RTC power supply, subsystem clock oscillator circuit, and RTC.

4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and XT1 oscillator). The value of the current value of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{TMKA}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

5. Current flowing only to the 8-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and XT1 oscillator). The value of the current value of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{TMT}, when the 8-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

6. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

7 Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit operates.

8. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

9. Current flowing only during rewrite of 1 KB data flash memory.

10. Current flowing only during self programming.

11. Current flowing only to the 24-bit ΔΣ A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2}, and I_{DSAD} when the 24-bit ΔΣ A/D converter operates.

12. For shift time to the SNOOZE mode, see **26.3.3 SNOOZE mode in the RL78/I1C User's Manual**.

Notes 13. Current flowing only to the LCD controller/driver. The current value of the RL78 microcontrollers is the sum of the LCD operating current (I_{LCD1}, I_{LCD2} or I_{LCD3}) to the supply current (I_{DD1}, or I_{DD2}) when the LCD controller/driver operates in an operation mode or HALT mode. Not including the current that flows through the LCD panel. Conditions of the TYP. value and MAX. value are as follows.

- Setting 20 pins as the segment function and blinking all
- Selecting f_{SUB} for system clock when LCD clock = 128 Hz (LCDC0 = 07H)
- Setting four time slices and 1/3 bias

14. Not including the current flowing into the external division resistor when using the external resistance division method.

15. Either V_{DD} or VBAT is selected by the battery backup function.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

2.4 AC Characteristics

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note 1] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.8 V ≤ V_{DD}[Note 1] ≤ 5.5 V	0.03125		1	μs
				2.7 V ≤ V_{DD}[Note 1] < 2.8 V	0.04167		1	μs
				2.5 V ≤ V_{DD}[Note 1] < 2.7 V	0.0625		1	μs
				2.4 V ≤ V_{DD}[Note 1] < 2.5 V	0.08333		1	μs
				2.1 V ≤ V_{DD}[Note 1] < 2.4 V	0.16667		1	μs
			LS (low-speed main) mode	1.9 V ≤ V_{DD}[Note 1] ≤ 5.5 V	0.125		1	μs
			LS (low-speed main) mode @4 MHz	1.9 V ≤ V_{DD}[Note 1] ≤ 5.5 V	0.25		1	μs
			LP (low-power main) mode	1.9 V ≤ V_{DD}[Note 1] ≤ 5.5 V	1		2	μs
			LV (low-voltage main) mode	1.7 V ≤ V_{DD}[Note 1] ≤ 5.5 V	0.25		1	μs
		Subsystem clock (f_{SUB}) operation		1.9 V ≤ V_{DD}[Note 1] ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.8 V ≤ V_{DD}[Note 1] ≤ 5.5 V	0.03125		1	μs
				2.7 V ≤ V_{DD}[Note 1] < 2.8 V	0.04167		1	μs
				2.5 V ≤ V_{DD}[Note 1] < 2.7 V	0.0625		1	μs
				2.4 V ≤ V_{DD}[Note 1] < 2.5 V	0.08333		1	μs
				2.1 V ≤ V_{DD}[Note 1] < 2.4 V	0.16667		1	μs
			LS (low-speed main) mode	1.9 V ≤ V_{DD}[Note 1] ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.7 V ≤ V_{DD}[Note 1] ≤ 5.5 V	0.25		1	μs
External system clock frequency	f_{EX}	2.7 V ≤ V_{DD}[Note 1] ≤ 5.5 V			1		20	MHz
		2.5 V ≤ V_{DD}[Note 1] < 2.7 V			1		16	MHz
		2.4 V ≤ V_{DD}[Note 1] < 2.5 V			1		12	MHz
		1.9 V ≤ V_{DD}[Note 1] < 2.4 V			1		8	MHz
		1.7 V ≤ V_{DD}[Note 1] < 1.9 V			1		4	MHz
	f_{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD}[Note 1] ≤ 5.5 V			24			ns
		2.5 V ≤ V_{DD}[Note 1] < 2.7 V			30			ns
		2.4 V ≤ V_{DD}[Note 1] < 2.5 V			40			ns
		1.9 V ≤ V_{DD}[Note 1] < 2.4 V			60			ns
		1.7 V ≤ V_{DD}[Note 1] < 1.9 V			120			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				$1/f_{MCK}+10$			ns[Note 2]

(**Notes** and **Remark** are listed on the next page.)

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 1 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

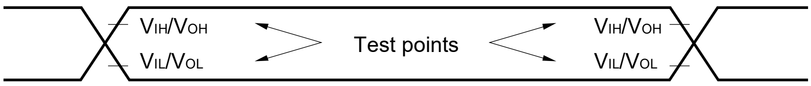
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
TO00 to TO07 output frequency	f_{TO}	HS (high-speed main) mode	4.0 V ≤ EV_{DD} ≤ 5.5 V			16	MHz
			2.7 V ≤ EV_{DD} < 4.0 V			8	MHz
			2.4 V ≤ EV_{DD} < 2.7 V			4	MHz
			2.1 V ≤ EV_{DD} < 2.4 V			4	MHz
		LS (low-speed main) mode	1.9 V ≤ EV_{DD} ≤ 5.5 V			4	MHz
		LP (low-power main) mode	1.9 V ≤ EV_{DD} ≤ 5.5 V			0.5	MHz
		LV (low-voltage main) mode	1.7 V ≤ EV_{DD} ≤ 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode	4.0 V ≤ EV_{DD} ≤ 5.5 V			16	MHz
			2.7 V ≤ EV_{DD} < 4.0 V			8	MHz
			2.4 V ≤ EV_{DD} < 2.7 V			4	MHz
			2.1 V ≤ EV_{DD} < 2.4 V			4	MHz
		LS (low-speed main) mode	1.9 V ≤ EV_{DD} ≤ 5.5 V			4	MHz
		LP (low-power main) mode	1.9 V ≤ EV_{DD} ≤ 5.5 V			1	MHz
		LV (low-voltage main) mode	1.9 V ≤ EV_{DD} ≤ 5.5 V			4	MHz
			1.7 V ≤ EV_{DD} < 1.9 V			2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0	1.7 V ≤ V_{DD} Note 1 ≤ 5.5 V	1			μs
		INTP1 to INTP7	1.7 V ≤ EV_{DD} ≤ 5.5 V	1			μs
Key interrupt input low-level width	t_{KR}	KR0 to KR7	1.9 V ≤ EV_{DD} ≤ 5.5 V	250			ns
			1.7 V ≤ EV_{DD} < 1.9 V	1			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Notes **1.** Either V_{DD} or VBAT is selected by the battery backup function.

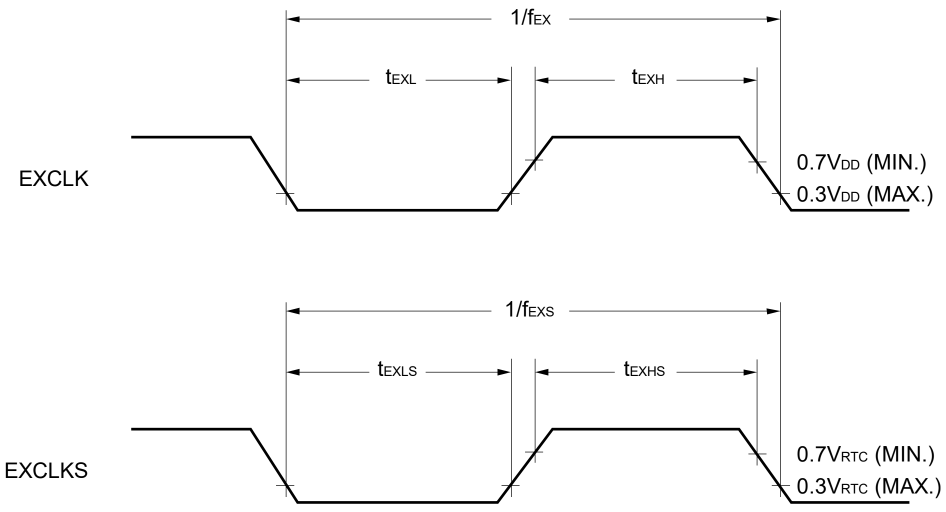
2. The following conditions are required for low voltage interface:
1.9 V ≤ V_{DD} < 2.7 V: MIN. 125 ns

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn)
m: Unit number (m = 0), n: Channel number (n = 0 to 7))

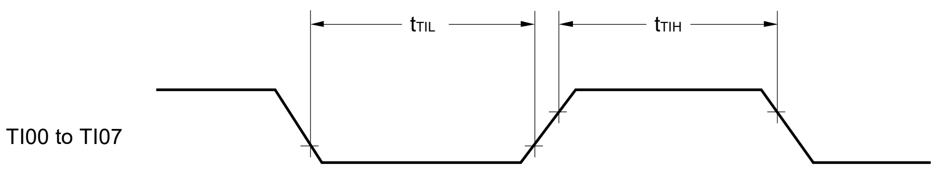
AC Timing Test Points

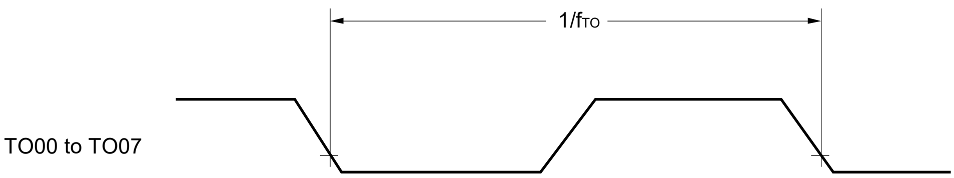


External System Clock Timing

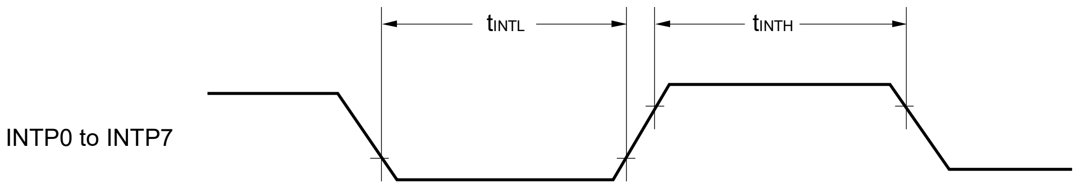


TI/TO Timing

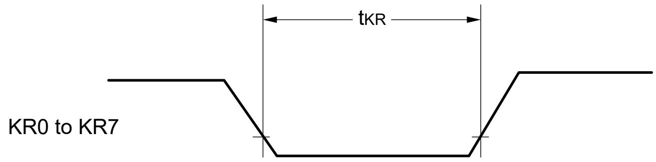




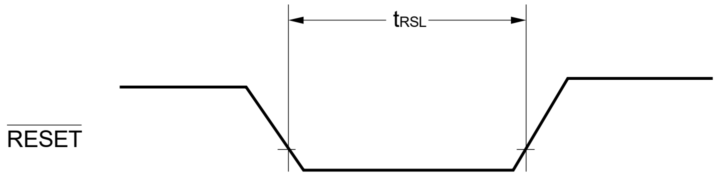
Interrupt Request Input Timing



Key interrupt Input Timing

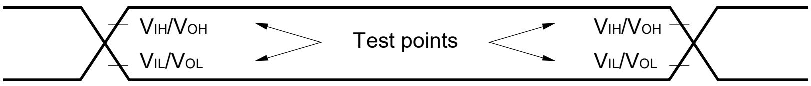


$\overline{\text{RESET}}$ Input Timing



2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)
(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} [Note 4] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate [Note 1]		2.4 V ≤ V_{DD} ≤ 5.5 V		$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$ [Note 2]	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 3]		4.0		1.3		0.1		0.6	Mbps
		1.9 V ≤ V_{DD} ≤ 5.5 V		$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$ [Note 2]	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 3]		1.0		1.3		0.1		0.6	Mbps
		1.8 V ≤ V_{DD} ≤ 5.5 V		$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$ [Note 2]	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 3]		1.0		1.3		0.1		0.6	Mbps
		1.7 V ≤ V_{DD} ≤ 5.5 V								$f_{MCK}/6$ [Note 2]	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 3]								0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

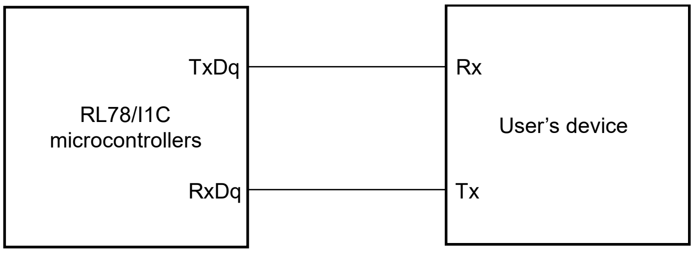
2. The following conditions are required for low voltage interface.
2.4 V ≤ EV_{DD} < 2.7 V: MAX. 2.6 Mbps
1.9 V ≤ EV_{DD} < 2.4 V: MAX. 1.3 Mbps

3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 32 MHz (2.8 V ≤ EV_{DD} ≤ 5.5 V), 24 MHz (2.7 V ≤ EV_{DD} ≤ 5.5 V), 16 MHz (2.5 V ≤ EV_{DD} ≤ 5.5 V), 12 MHz (2.4 V ≤ EV_{DD} ≤ 5.5 V), 6 MHz (2.1 V ≤ EV_{DD} ≤ 5.5 V),
LS (low-speed main) mode: 8 MHz (1.9 V ≤ EV_{DD} ≤ 5.5 V), 4 MHz (1.9 V ≤ EV_{DD} ≤ 5.5 V)
LP (low-power main) mode: 1 MHz (1.9 V ≤ EV_{DD} ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.7 V ≤ EV_{DD} ≤ 5.5 V)

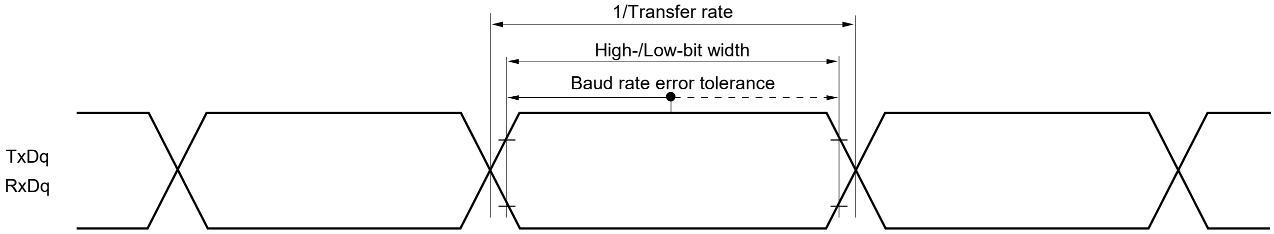
4. Either V_{DD} or VBAT is selected by the battery backup function.

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 8)

2. f_{MCK}: Serial array unit operation clock frequency
(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)
(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 4 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD} ≤ 5.5 V	125		500		4000		1000		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V	250		500		4000		1000		ns
		1.9 V ≤ EV_{DD} ≤ 5.5 V	500		500		4000		1000		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V	1000		1000		4000		1000		ns
		1.7 V ≤ EV_{DD} ≤ 5.5 V			1000		4000		1000		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V	t_{KCY1}/2 – 12		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V	t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V	t_{KCY1}/2 – 38		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.9 V ≤ EV_{DD} ≤ 5.5 V	t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V			t_{KCY1}/2 – 100		t_{KCY1}/2 – 100		t_{KCY1}/2 – 100		ns
		1.7 V ≤ EV_{DD} ≤ 5.5 V			t_{KCY1}/2 – 100		t_{KCY1}/2 – 100		t_{KCY1}/2 – 100		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V	44		110		110		110		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V	44		110		110		110		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V	75		110		110		110		ns
		1.9 V ≤ EV_{DD} ≤ 5.5 V	110		110		110		110		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V	220		220		220		220		ns
		1.7 V ≤ EV_{DD} ≤ 5.5 V			220		220		220		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	1.8 V ≤ EV_{DD} ≤ 5.5 V	19		19		19		19		ns
		1.7 V ≤ EV_{DD} ≤ 5.5 V			19		19		19		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 3, 1.8 V ≤ EV_{DD} ≤ 5.5 V		25		25		25		25	ns
		C = 30 pF Note 3, 1.7 V ≤ EV_{DD} ≤ 5.5 V				25		25		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

4. Either V_{DD} or VBAT is selected by the battery backup function.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 10, 30), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 0, 1, 8)

2. f_{MCK}: Serial array unit operation clock frequency
(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 10, 30))

(3) During communication at same potential (Simplified SPI (CSI) mode) (slave mode, SCKp... external clock input)
(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 5 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 4	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}		–		–		–		ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V	16 MHz < f_{MCK}	8/f_{MCK}		–		–		–		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		6/f_{MCK} and 500		6/f_{MCK} and 500		6/f_{MCK} and 500		6/f_{MCK} and 500		ns
		1.9 V ≤ EV_{DD} ≤ 5.5 V		6/f_{MCK} and 750		6/f_{MCK} and 750		6/f_{MCK} and 750		6/f_{MCK} and 750		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V		6/f_{MCK} and 1500		6/f_{MCK} and 1500		6/f_{MCK} and 1500		6/f_{MCK} and 1500		ns
		1.7 V ≤ EV_{DD} ≤ 5.5 V				6/f_{MCK} and 1500		6/f_{MCK} and 1500		6/f_{MCK} and 1500		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY2}/2 – 7		t_{KCY2}/2 – 7		t_{KCY2}/2 – 7		t_{KCY2}/2 – 7		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY2}/2 – 8		t_{KCY2}/2 – 8		t_{KCY2}/2 – 8		t_{KCY2}/2 – 8		ns
		1.9 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY2}/2 – 18		t_{KCY2}/2 – 18		t_{KCY2}/2 – 18		t_{KCY2}/2 – 18		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY2}/2 – 66		t_{KCY2}/2 – 66		t_{KCY2}/2 – 66		t_{KCY2}/2 – 66		ns
		1.7 V ≤ EV_{DD} ≤ 5.5 V				t_{KCY2}/2 – 66		t_{KCY2}/2 – 66		t_{KCY2}/2 – 66		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK}+20		1/f_{MCK}+30		1/f_{MCK}+30		1/f_{MCK}+30		ns
		1.9 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK}+30		1/f_{MCK}+30		1/f_{MCK}+30		1/f_{MCK}+30		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK}+40		1/f_{MCK}+40		1/f_{MCK}+40		1/f_{MCK}+40		ns
		1.7 V ≤ EV_{DD} ≤ 5.5 V				1/f_{MCK}+40		1/f_{MCK}+40		1/f_{MCK}+40		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI2}	2.1 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK}+31		1/f_{MCK}+31		1/f_{MCK}+31		1/f_{MCK}+31		ns
		1.9 V ≤ EV_{DD} ≤ 5.5 V				1/f_{MCK}+31		1/f_{MCK}+31		1/f_{MCK}+31		ns
		1.7 V ≤ EV_{DD} ≤ 5.5 V								1/f_{MCK}+250		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO2}	C = 30 pF Note 3	2.7 V ≤ EV_{DD} ≤ 5.5 V		2/f_{MCK}+44		2/f_{MCK}+110		2/f_{MCK}+110		2/f_{MCK}+110	ns
			2.4 V ≤ EV_{DD} ≤ 5.5 V		2/f_{MCK}+75		2/f_{MCK}+110		2/f_{MCK}+110		2/f_{MCK}+110	ns
			1.9 V ≤ EV_{DD} ≤ 5.5 V		2/f_{MCK}+100		2/f_{MCK}+110		2/f_{MCK}+110		2/f_{MCK}+110	ns
			1.8 V ≤ EV_{DD} ≤ 5.5 V		2/f_{MCK}+220		2/f_{MCK}+220		2/f_{MCK}+220		2/f_{MCK}+220	ns
			1.7 V ≤ EV_{DD} ≤ 5.5 V				2/f_{MCK}+220		2/f_{MCK}+220		2/f_{MCK}+220	ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SOp output lines.

4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

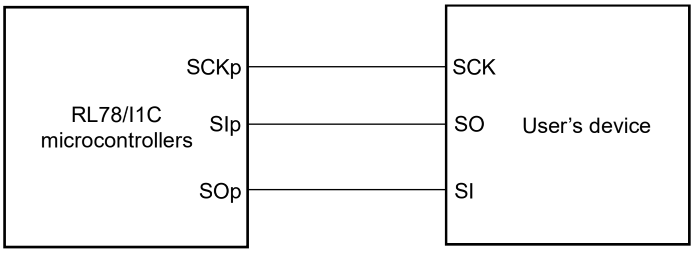
5. Either V_{DD} or VBAT is selected by the battery backup function.

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

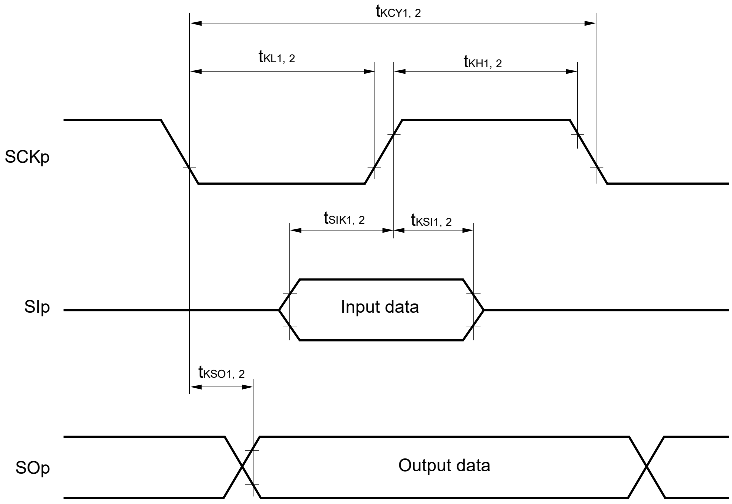
Remarks 1. p: CSI number (p = 00, 10, 30), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 0, 1, 8)

2. f_{MCK}: Serial array unit operation clock frequency
(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 10, 30))

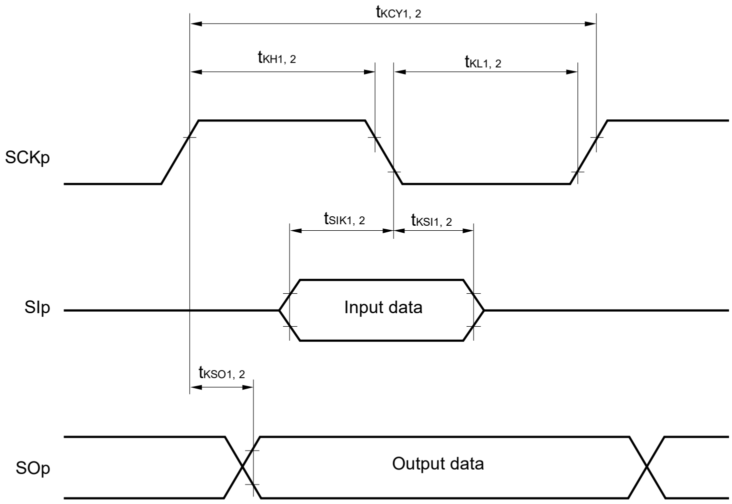
Simplified SPI (CSI) mode connection diagram (during communication at same potential)



Simplified SPI (CSI) mode serial transfer timing (during communication at same potential)
(when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



Simplified SPI (CSI) mode serial transfer timing (during communication at same potential)
(when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



Remarks 1. p: CSI number (p = 00, 10, 30)

2. m: Unit number, n: Channel number (mn = 00, 10, 30)

(4) During communication at same potential (simplified I^2C mode)

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note 3] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) **(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000[Note 1]		400[Note 1]		400[Note 1]		400[Note 1]	kHz
		1.9 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400[Note 1]		400[Note 1]		400[Note 1]		400[Note 1]	kHz
		1.9 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300[Note 1]		300[Note 1]		300[Note 1]		300[Note 1]	kHz
		1.8 V ≤ EV_{DD} < 1.9 V, C_b = 100 pF, R_b = 5 kΩ		250[Note 1]		250[Note 1]		250[Note 1]		250[Note 1]	kHz
		1.7 V ≤ EV_{DD} < 1.9 V, C_b = 100 pF, R_b = 5 kΩ				250[Note 1]		250[Note 1]		250[Note 1]	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		1150		ns
		1.9 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		1150		ns
		1.9 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		1550		ns
		1.8 V ≤ EV_{DD} < 1.9 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		1850		ns
		1.7 V ≤ EV_{DD} < 1.9 V, C_b = 100 pF, R_b = 5 kΩ			1850		1850		1850		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		1150		ns
		1.9 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		1150		ns
		1.9 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		1550		ns
		1.8 V ≤ EV_{DD} < 1.9 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		1850		ns
		1.7 V ≤ EV_{DD} < 1.9 V, C_b = 100 pF, R_b = 5 kΩ			1850		1850		1850		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 85[Notes 1, 2]		$1/f_{MCK}$ + 145[Notes 1, 2]		$1/f_{MCK}$ + 145[Notes 1, 2]		$1/f_{MCK}$ + 145[Notes 1, 2]		ns
		1.9 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 145[Notes 1, 2]		$1/f_{MCK}$ + 145[Notes 1, 2]		$1/f_{MCK}$ + 145[Notes 1, 2]		$1/f_{MCK}$ + 145[Notes 1, 2]		ns
		1.9 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	$1/f_{MCK}$ + 230[Notes 1, 2]		$1/f_{MCK}$ + 230[Notes 1, 2]		$1/f_{MCK}$ + 230[Notes 1, 2]		$1/f_{MCK}$ + 230[Notes 1, 2]		ns
		1.8 V ≤ EV_{DD} < 1.9 V, C_b = 100 pF, R_b = 5 kΩ	$1/f_{MCK}$ + 290[Notes 1, 2]		$1/f_{MCK}$ + 290[Notes 1, 2]		$1/f_{MCK}$ + 290[Notes 1, 2]		$1/f_{MCK}$ + 290[Notes 1, 2]		ns
		1.7 V ≤ EV_{DD} < 1.9 V, C_b = 100 pF, R_b = 5 kΩ			$1/f_{MCK}$ + 290[Notes 1, 2]		$1/f_{MCK}$ + 290[Notes 1, 2]		$1/f_{MCK}$ + 290[Notes 1, 2]		ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 3 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

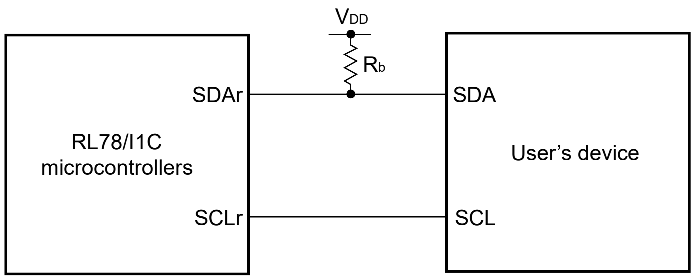
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		1.9 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	0	355	0	355	0	355	ns
		1.9 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	0	405	ns
		1.8 V ≤ EV_{DD} < 1.9 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	0	405	ns
		1.7 V ≤ EV_{DD} < 1.9 V, C_b = 100 pF, R_b = 5 kΩ			0	405	0	405	0	405	ns

Notes 1. The value must also be equal to or less than $f_{MCK}/4$.

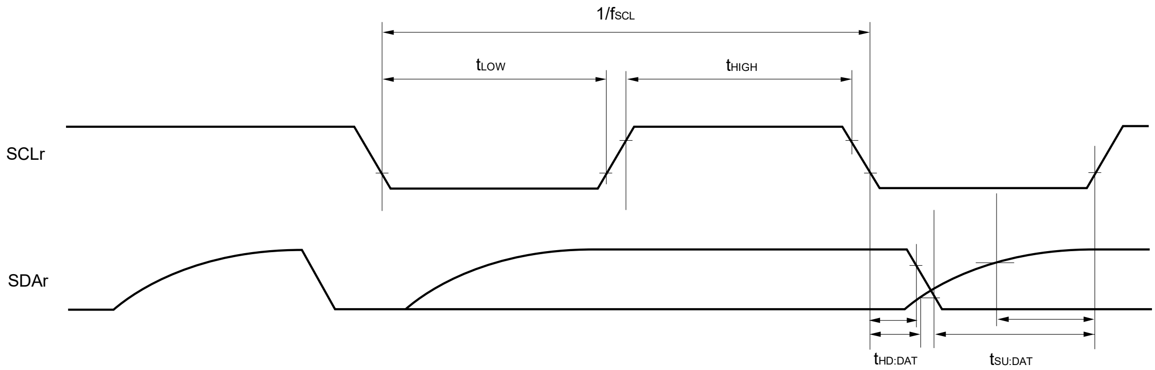
2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

3. Either V_{DD} or VBAT is selected by the battery backup function.

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 10, 30), g: PIM and POM number (g = 0, 1, 8)

3. f_{MCK}: Serial array unit operation clock frequency
(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 12))

(5) Communication at different potential (1.9 V, 2.5 V, 3 V) (UART mode) (1/2)
(T_A = –40 to +85°C, 1.9 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 1 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 4		5.3		1.3		0.1		0.6	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 4		5.3		1.3		0.1		0.6	Mbps
			1.9 V ≤ EV_{DD} < 3.3 V, 1.8 V ≤ V_b ≤ 2.0 V		$f_{MCK}/6$ Notes 1 to 3		$f_{MCK}/6$ Notes 1, 2		$f_{MCK}/6$ Notes 1, 2		$f_{MCK}/6$ Notes 1, 2	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 4		5.3		1.3		0.1		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.
2. Use it with EV_{DD} ≥ V_b.
3. The following conditions are required for low voltage interface.
2.4 V ≤ EV_{DD} < 2.7 V: MAX. 2.6 Mbps
1.9 V ≤ EV_{DD} < 2.4 V: MAX. 1.3 Mbps
4. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 32 MHz (2.8 V ≤ EV_{DD} ≤ 5.5 V), 24 MHz (2.7 V ≤ EV_{DD} ≤ 5.5 V), 16 MHz (2.5 V ≤ EV_{DD} ≤ 5.5 V), 12 MHz (2.4 V ≤ EV_{DD} ≤ 5.5 V), 6 MHz (2.1 V ≤ EV_{DD} ≤ 5.5 V),
LS (low-speed main) mode: 8 MHz (1.9 V ≤ EV_{DD} ≤ 5.5 V), 4 MHz (1.9 V ≤ EV_{DD} ≤ 5.5 V)
LP (low-power main) mode: 1 MHz (1.9 V ≤ EV_{DD} ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.7 V ≤ EV_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage
2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 8)
3. f_{MCK}: Serial array unit operation clock frequency
(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = –40 to +85°C, 1.9 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 10 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode MIN.	HS MAX.	LS (low-speed main) Mode MIN.	LS MAX.	LP (low-power main) Mode MIN.	LP MAX.	LV (low-voltage main) Mode MIN.	LV MAX.	Unit
Transfer rate		Transmission	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			**Notes 1, 2**		**Notes 1, 2**		**Notes 1, 2**		**Notes 1, 2**	bps
				Theoretical value of the maximum transfer rate Note 9 C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 Note 3		2.8 Note 3		2.8 Note 3		2.8 Note 3	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			**Notes 2, 4**		**Notes 2, 4**		**Notes 2, 4**		**Notes 2, 4**	bps
				Theoretical value of the maximum transfer rate Note 9 C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 5		1.2 Note 5		1.2 Note 5		1.2 Note 5	Mbps
			1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			**Notes 2, 6, 7**		**Notes 2, 6, 7**		**Notes 2, 6, 7**		**Notes 2, 6, 7**	bps
				Theoretical value of the maximum transfer rate Note 9 C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 8		0.43 Note 8		0.43 Note 8		0.43 Note 8	Mbps

Notes 1. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. Transfer rate in the SNOOZE mode is 4800 bps only.

3. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

4. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Notes 5. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 4** above to calculate the maximum transfer rate under conditions of the customer.

6. Use it with $EV_{DD} \geq V_b$.

7. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.9\ V \leq EV_{DD} < 2.7\ V$ and $1.6\ V \leq V_b \leq 2.0\ V$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

8. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 7** above to calculate the maximum transfer rate under conditions of the customer.

9. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode: 32 MHz ($2.8\ V \leq EV_{DD} \leq 5.5\ V$), 24 MHz ($2.7\ V \leq EV_{DD} \leq 5.5\ V$), 16 MHz ($2.5\ V \leq EV_{DD} \leq 5.5\ V$), 12 MHz ($2.4\ V \leq EV_{DD} \leq 5.5\ V$), 6 MHz ($2.1\ V \leq EV_{DD} \leq 5.5\ V$),

LS (low-speed main) mode: 8 MHz ($1.9\ V \leq EV_{DD} \leq 5.5\ V$), 4 MHz ($1.9\ V \leq EV_{DD} \leq 5.5\ V$)

LP (low-power main) mode: 1 MHz ($1.9\ V \leq EV_{DD} \leq 5.5\ V$)

LV (low-voltage main) mode: 4 MHz ($1.7\ V \leq EV_{DD} \leq 5.5\ V$)

10. Either V_{DD} or VBAT is selected by the battery backup function.

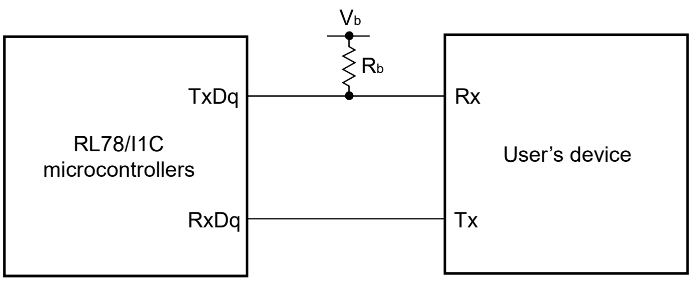
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. $R_b[\Omega]$:Communication line (TxDq) pull-up resistance, $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage

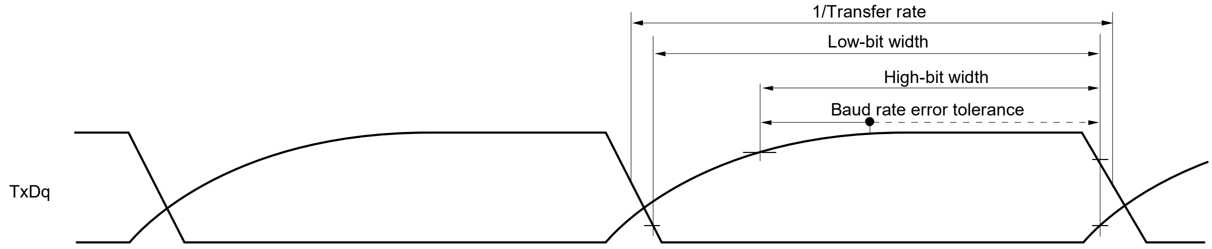
2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 8)

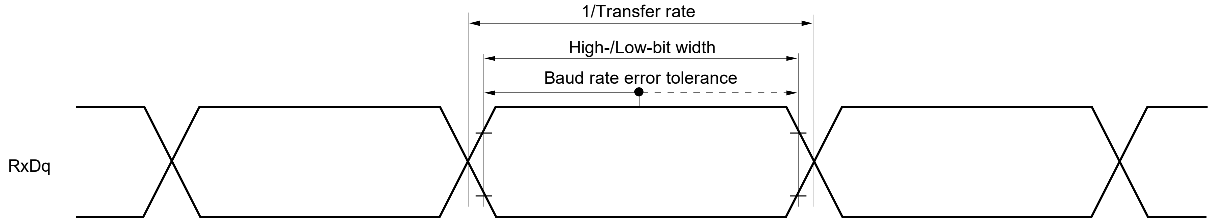
3. f_{MCK}: Serial array unit operation clock frequency (Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)





Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance, V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 8)

(6) Communication at different potential (2.5 V, 3 V) (f_{MCK}/2) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (1/2)
(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 3 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 2/f_{CLK}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	200		1150		1150		1150		ns
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	300		1150		1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 7		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 10		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		58		479		479		479		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121		479		479		479		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10		10		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ			60		60		60		60	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130		130		130		130	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		23		110		110		110		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		33		110		110		110		ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

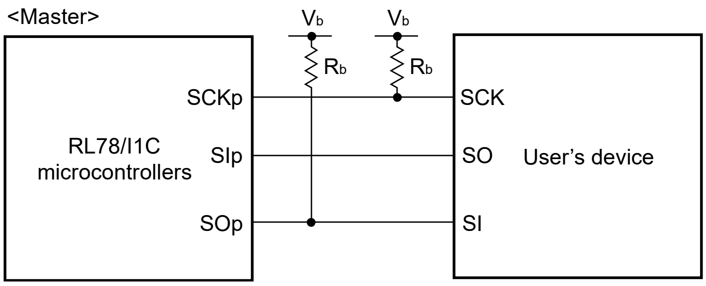
(6) Communication at different potential (2.5 V, 3 V) (f_{MCK}/2) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (2/2)
(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 3 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	10		10		10		10		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	10		10		10		10		ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10		10	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		10	ns

Notes
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. Either V_{DD} or VBAT is selected by the battery backup function.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Simplified SPI (CSI) mode connection diagram (during communication at different potential)



Remarks
1. R_b[Ω]:Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage
2. p: CSI number (p = 00, 10, 30), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1, 8)
3. f_{MCK}: Serial array unit operation clock frequency
(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 12))
4. This specification is valid only when CSI00’s peripheral I/O redirect function is not used.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (f_{MCK}/4) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output) (1/2)

(T_A = –40 to +85°C, 1.9 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 4 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode MIN.	HS MAX.	LS (low-speed main) Mode MIN.	LS MAX.	LP (low-power main) Mode MIN.	LP MAX.	LV (low-voltage main) Mode MIN.	LV MAX.	Unit
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		1150		1150		ns
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		1150		1150		ns
			1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 75		t_{KCY1}/2 – 75		t_{KCY1}/2 – 75		t_{KCY1}/2 – 75		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 170		t_{KCY1}/2 – 170		t_{KCY1}/2 – 170		t_{KCY1}/2 – 170		ns
		1.9 V Note 4 ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 12		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.9 V Note 4 ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		81		479		479		479		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		177		479		479		479		ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		479		479		479		479		ns

(**Notes**, **Caution** and **Remarks** are listed on the page after the next page.)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (f_{MCK}/4) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output) (2/2)
(T_A = –40 to +85°C, 1.9 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 4 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		19		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		19		ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		19		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		100		100		100		100	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195		195		195		195	ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		483		483		483		483	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		110		110		110		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		110		ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		110		ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		19		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		19		ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		19		ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25		25	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25		25	ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		25		25		25		25	ns

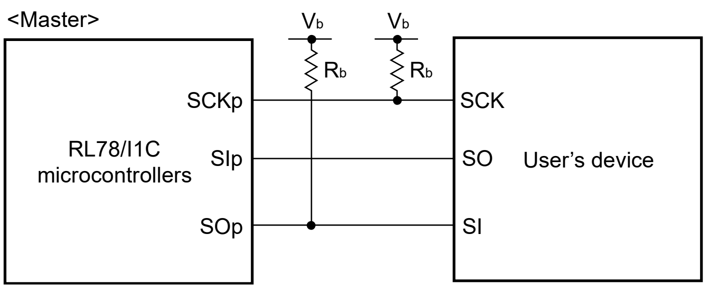
(**Notes**, **Caution** and **Remarks** are listed on the next page.)

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. Use it with $EV_{DD} \geq V_b$.
4. Either V_{DD} or VBAT is selected by the battery backup function.

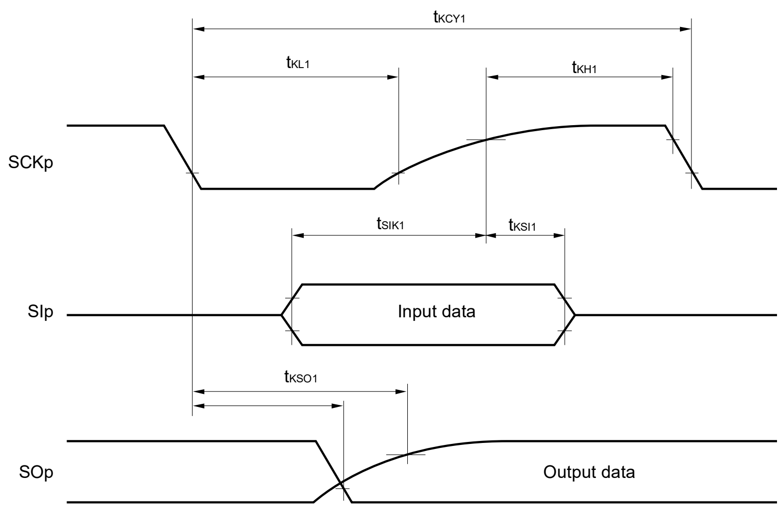
Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]:Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage
2. p: CSI number (p = 00, 10, 30), m: Unit number , n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1, 8)
3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 12))

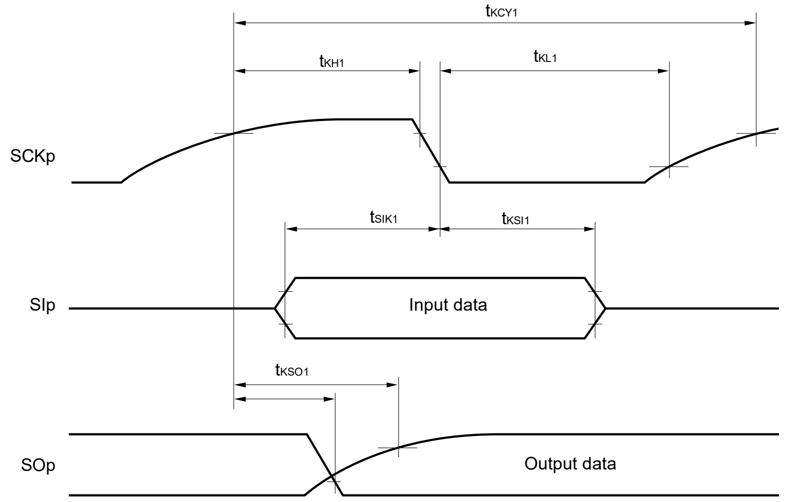
Simplified SPI (CSI) mode connection diagram (during communication at different potential)



Simplified SPI (CSI) mode serial transfer timing (master mode) (during communication at different potential) (when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



Simplified SPI (CSI) mode serial transfer timing (master mode) (during communication at different potential) (when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remark p: CSI number (p = 00, 10, 30), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1, 8)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (Simplified SPI (CSI) mode) (slave mode, SCKp ... external clock input)
(T_A = –40 to +85°C, 1.9 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 5 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	24 MHz < f_{MCK}	14/f_{MCK}		–		–		–		ns
			20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}		–		–		–		ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		–		–		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		–		–		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	20/f_{MCK}		–		–		–		ns
			20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		–		–		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		–		–		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		–		–		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		–		–		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	24 MHz < f_{MCK}	48/f_{MCK}		–		–		–		ns
			20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		–		–		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		–		–		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		–		–		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		–		–		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 – 12		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 – 18		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	2.7 V ≤ EV_{DD} ≤ 5.5 V, 2.3 V ≤ V_b ≤ 4.0 V Note 2		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 3	t_{KSI2}	2.7 V ≤ EV_{DD} ≤ 5.5 V, 2.3 V ≤ V_b ≤ 4.0 V Note 2		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

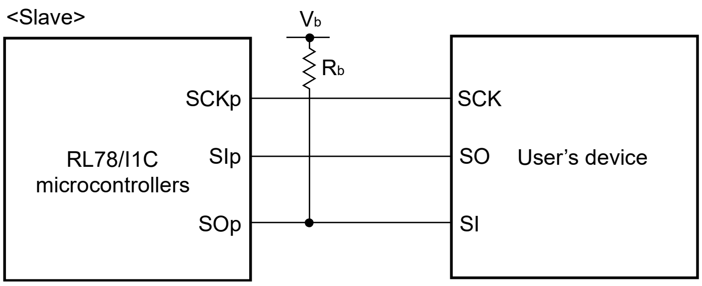
(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (Simplified SPI (CSI) mode) (slave mode, SCKp ... external clock input)
(T_A = –40 to +85°C, 1.9 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 5 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Delay time from SCKp↓ to SOp output Note 4	t_{KSO2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		2/f_{MCK} + 120		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		2/f_{MCK} + 214		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns

Notes 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps
2. Use it with EV_{DD} ≥ V_b.
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
5. Either V_{DD} or VBAT is selected by the battery backup function.

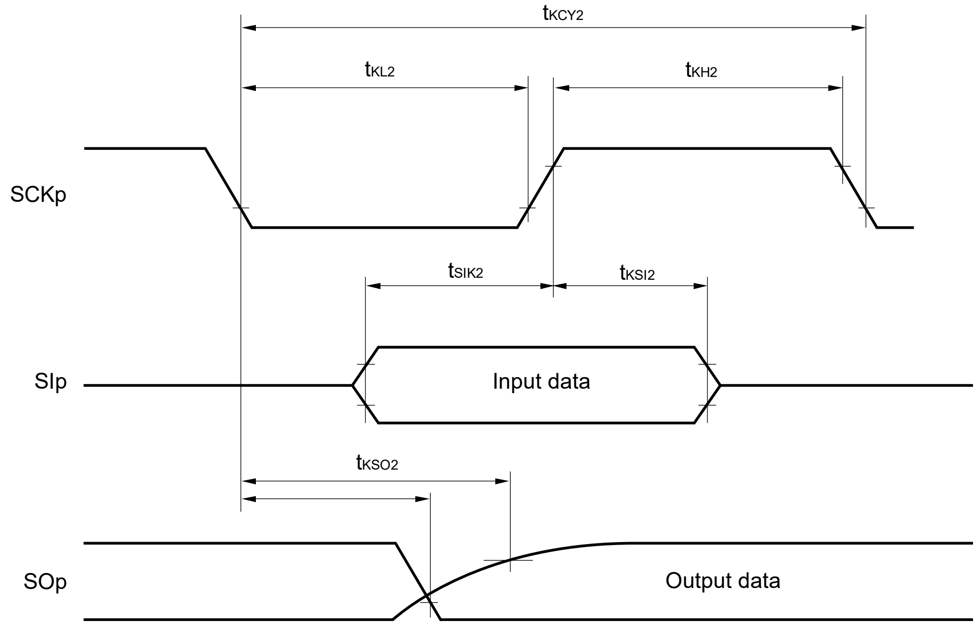
Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Simplified SPI (CSI) mode connection diagram (during communication at different potential)

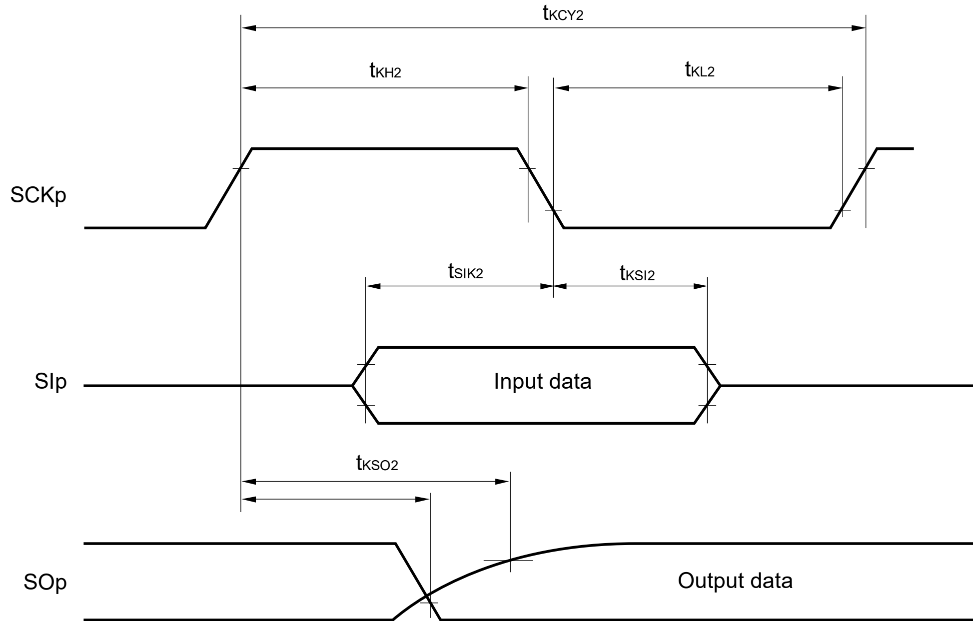


Remarks 1. R_b[Ω]:Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage
2. p: CSI number (p = 00, 10, 30), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1, 8)
3. f_{MCK}: Serial array unit operation clock frequency
(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 12))

Simplified SPI (CSI) mode serial transfer timing (slave mode) (during communication at different potential) (when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



Simplified SPI (CSI) mode serial transfer timing (slave mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution **Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remark p: CSI number (p = 00, 10, 30), m: Unit number, n: Channel number (mn = 00, 02, 12),
g: PIM and POM number (g = 0, 1, 8)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (1/2)

(T_A = –40 to +85°C, 1.9 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note 4] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ		1000[Note 1]		300[Note 1]		300[Note 1]		300[Note 1]	kHz
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		1000[Note 1]		300[Note 1]		300[Note 1]		300[Note 1]	kHz
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		400[Note 1]		300[Note 1]		300[Note 1]		300[Note 1]	kHz
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		400[Note 1]		300[Note 1]		300[Note 1]		300[Note 1]	kHz
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 2], C_b = 100 pF, R_b = 5.5 kΩ		300[Note 1]		300[Note 1]		300[Note 1]		300[Note 1]	kHz
Hold time when SCLr = “L”	t_{LOW}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1550		1550		1550		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1550		1550		1550		ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1150		1150		1150		1150		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1150		1150		1150		1150		ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 2], C_b = 100 pF, R_b = 5.5 kΩ	1150		1150		1150		1150		ns
Hold time when SCLr = “H”	t_{HIGH}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	245		610		610		610		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	200		610		610		610		ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	675		610		610		610		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	600		610		610		610		ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 2], C_b = 100 pF, R_b = 5.5 kΩ	610		610		610		610		ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)
(T_A = –40 to +85°C, 1.9 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 4 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

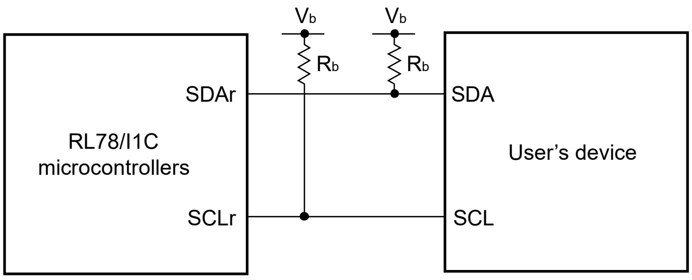
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 135 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 135 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	355	0	355	0	355	0	355	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	0	355	0	355	0	355	ns
		1.9 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	0	405	0	405	0	405	0	405	ns

Notes 1. The value must also be equal to or less than $f_{MCK}/4$.
2. Use it with EV_{DD} ≥ V_b.
3. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.
4. Either V_{DD} or VBAT is selected by the battery backup function.

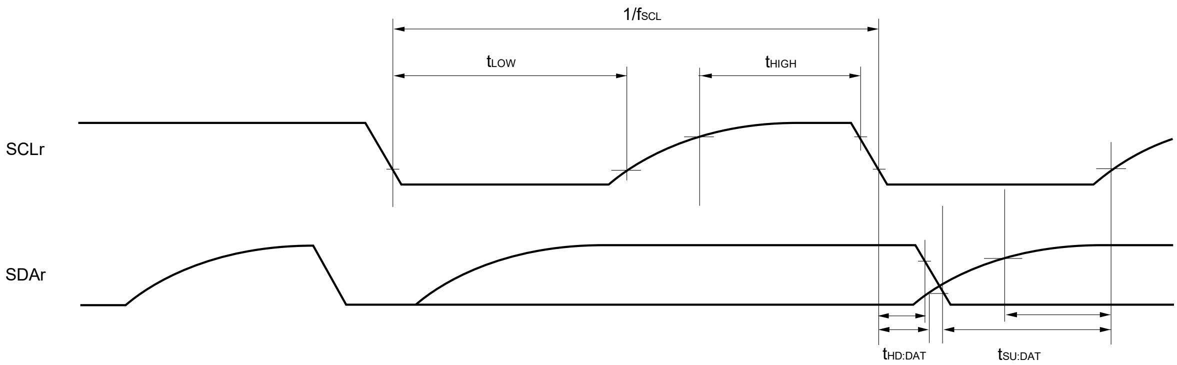
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 10, 30), g: PIM, POM number (g = 0, 1, 8)

3. f_{MCK}: Serial array unit operation clock frequency
(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 12))

2.5.2 Serial interface IICA

(1) I²C standard mode (1/2)

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 3 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	0	100	0	100	kHz
			1.9 V ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	0	100	0	100	kHz
			1.8 V ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	0	100	0	100	kHz
			1.7 V ≤ EV_{DD} ≤ 5.5 V	–	–	0	100	0	100	0	100	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		–	–	4.7		4.7		4.7		μs
Hold time Note 1	$t_{HD:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		–	–	4.0		4.0		4.0		μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		–	–	4.7		4.7		4.7		μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		–	–	4.0		4.0		4.0		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		250		250		250		250		μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V		250		250		250		250		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		250		250		250		250		μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		–	–	250		250		250		μs
Data hold time (transmission) Note 2	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0	3.45	0	3.45	0	3.45	0	3.45	μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V		0	3.45	0	3.45	0	3.45	0	3.45	μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		0	3.45	0	3.45	0	3.45	0	3.45	μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		–	–	0	3.45	0	3.45	0	3.45	μs

(**Notes** and **Remark** are listed on the next page.)

(1) I²C standard mode (2/2)

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 3 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V	4.0		4.0		4.0		4.0		μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V	4.0		4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V	4.0		4.0		4.0		4.0		μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V	–	–	4.0		4.0		4.0		μs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V	4.7		4.7		4.7		4.7		μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V	4.7		4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V	4.7		4.7		4.7		4.7		μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V	–	–	4.7		4.7		4.7		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

3. Either V_{DD} or VBAT is selected by the battery backup function.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I²C fast mode

(T_A = –40 to +85°C, 1.9 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 3 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	400	0	400	–	–	0	400	kHz
			1.9 V ≤ EV_{DD} ≤ 5.5 V	0	400	0	400	–	–	0	400	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
Hold time Note 1	$t_{HD:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		–	–	1.3		μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		–	–	1.3		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		100		100		–	–	100		ns
		1.9 V ≤ EV_{DD} ≤ 5.5 V		100		100		–	–	100		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0	0.9	0	0.9	–	–	0	0.9	μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V		0	0.9	0	0.9	–	–	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		–	–	1.3		μs
		1.9 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		–	–	1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

3. Either V_{DD} or VBAT is selected by the battery backup function.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(3) I²C fast mode plus

(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 3 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	1000	–	–	–	–	–	–	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.26		–	–	–	–	–	–	μs
Hold time Note 1	$t_{HD:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.26		–	–	–	–	–	–	μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.5		–	–	–	–	–	–	μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.26		–	–	–	–	–	–	μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		50		–	–	–	–	–	–	ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0	0.5	–	–	–	–	–	–	μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.26		–	–	–	–	–	–	μs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.5		–	–	–	–	–	–	μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

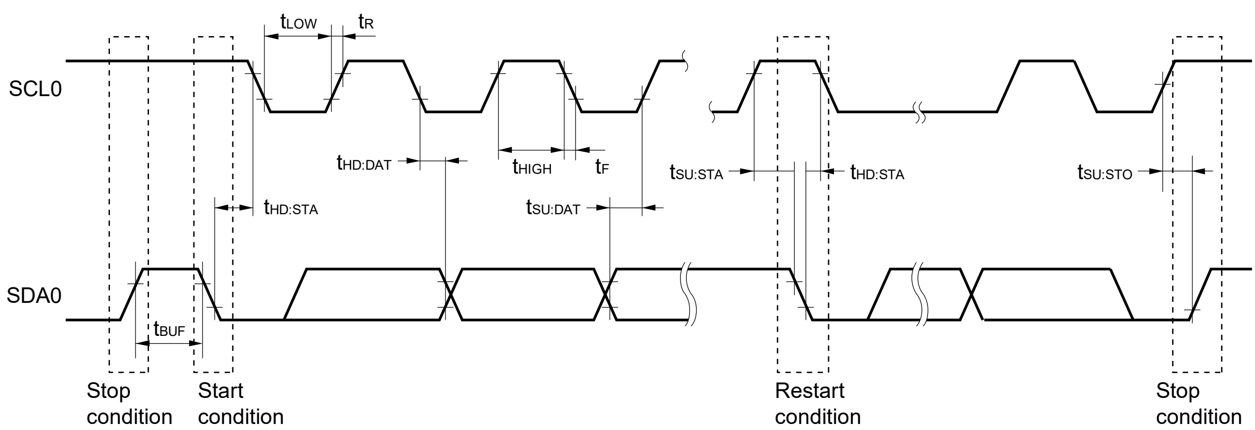
2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

3. Either V_{DD} or VBAT is selected by the battery backup function.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pins: ANI2 to ANI5 and internal reference voltage

(T_A = –40 to +85°C, 1.9 V ≤ V_{DD}[Note 3] ≤ 5.5 V, V_{SS} = 0 V, reference voltage (+) = AV_{REFP}, reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD}	1.9 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.9 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD}	1.9 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution AV_{REFP} = V_{DD}	1.9 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD}	1.9 V ≤ AV_{REFP} ≤ 5.5 V			±3.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD}	1.9 V ≤ AV_{REFP} ≤ 5.5 V			±2.0	LSB
Reference voltage (+)	AV_{REFP}			1.9		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP}	V
	V_{BGR}	Select internal reference voltage output 2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode		1.38	1.45	1.5	V

Notes **1.** Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Either V_{DD} or VBAT is selected by the battery backup function.

(2) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pins: ANI0 to ANI5 and internal reference voltage

(T_A = –40 to +85°C, 1.9 V ≤ V_{DD}[Note 3] ≤ 5.5 V, V_{SS} = 0 V, reference voltage (+) = V_{DD}[Note 3], reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution	1.9 V ≤ V_{DD} ≤ 5.5 V		1.2	±10.5	LSB
Conversion time	t_{CONV}	10-bit resolution	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.9 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution	1.9 V ≤ V_{DD} ≤ 5.5 V			±0.85	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution	1.9 V ≤ V_{DD} ≤ 5.5 V			±0.85	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution	1.9 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	1.9 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}			0		V_{DD}	V
	V_{BGR}	Select internal reference voltage output, 2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode		1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).
2. This value is indicated as a ratio (%FSR) to the full-scale value.
3. Either V_{DD} or VBAT is selected by the battery backup function.

Caution When using reference voltage (+) = V_{DD}, taking into account the voltage drop due to the effect of the power switching circuit of the battery backup function and use the A/D conversion result. In addition, enter HALT mode during A/D conversion and set V_{DD} port to input.

(3) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pins: ANI0, ANI2 to ANI5

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD}[Note 3] ≤ 5.5 V, V_{SS} = 0 V, reference voltage (+) = V_{BGR}, reference voltage (–) = AV_{REFM} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error[Note 1]	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Reference voltage (+)	V_{BGR}			1.38	1.45	1.5	V
Analog input voltage	V_{AIN}			0		V_{BGR}	V

Notes 1. Excludes quantization error (±1/2 LSB).
2. This value is indicated as a ratio (%FSR) to the full-scale value.
3. Either V_{DD} or VBAT is selected by the battery backup function.

2.6.2 24-bit ΔΣ A/D converter characteristics

(1) Reference voltage

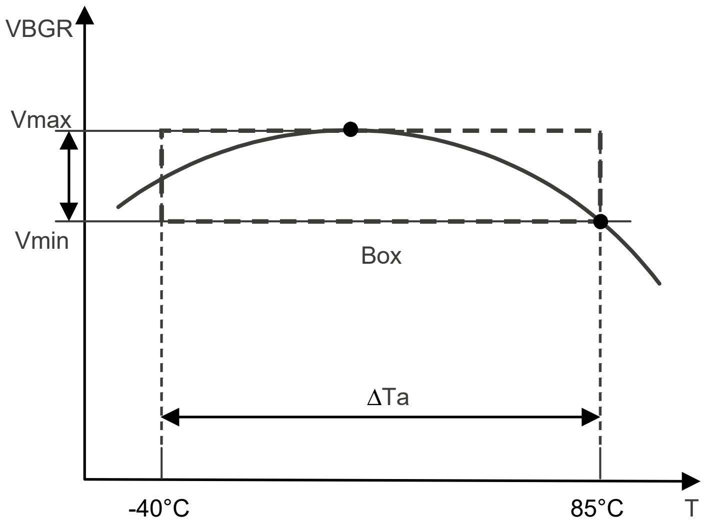
(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} Note 1 ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal reference voltage	V_{AVRTO}			0.8		V
Temperature coefficient for internal reference voltage Note 2	TC_{BOX}	0.47 μF capacitor connected to AREGC, AVRT, and AVCM pins		10		ppm/°C

Notes 1. Either V_{DD} or VBAT is selected by the battery backup function.

2. This is as stipulated by the BOX method.

$$TC_{BOX} = \frac{1}{V_{min}} \cdot \frac{Vmax - Vmin}{\Delta T_a}$$



(2) Analog input

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} Note ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage range (differential voltage)	V_{AIN}	x1 gain	–500		500	mV
		x2 gain	–250		250	
		x4 gain	–125		125	
		x8 gain	–62.5		62.5	
		x16 gain	–31.25		31.25	
		x32 gain	–15.625		15.625	
Input gain	ainGAIN	x1 gain		1		Times
		x2 gain		2		
		x4 gain		4		
		x8 gain		8		
		x16 gain		16		
		x32 gain		32		
Input impedance	ainRIN	Differential voltage	150	360		kΩ
		Single-ended voltage	100	240		

Note Either V_{DD} or VBAT is selected by the battery backup function.

(3) 4 kHz sampling mode

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD}Note ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation clock	f_{DSAD}	f_X oscillation clock, input external clock or high-speed on-chip oscillator clock is used		12		MHz
Sampling frequency	f_S			3906.25		Hz
Oversampling frequency	f_{OS}			1.5		MHz
Output data rate	T_{DATA}			256		μs
Data width	RES			24		bit
SNDR	SNDR	x1 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)		80		dB
		x16 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)	69	74		
		x32 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)	65	69		
Passband (low pass band)	f_{Chpf}	At –3 dB (phase in high pass filter not adjusted) Bits 7 and 6 of DSADHPFCR register (DSADCOF1, DSADCOF0) = 00		0.607		Hz
		At –3 dB (phase in high pass filter not adjusted) Bits 7 and 6 of DSADHPFCR register (DSADCOF1, DSADCOF0) = 01		1.214		Hz
		At –3 dB (phase in high pass filter not adjusted) Bits 7 and 6 of DSADHPFCR register (DSADCOF1, DSADCOF0) = 10		2.429		Hz
		At –3 dB (phase in high pass filter not adjusted) Bits 7 and 6 of DSADHPFCR register (DSADCOF1, DSADCOF0) = 11		4.857		Hz
In-band ripple 1	rp1	45 Hz to 55 Hz @50 Hz 54 Hz to 66 Hz @60 Hz	–0.01		0.01	dB
In-band ripple 2	rp2	45 Hz to 275 Hz @50 Hz 54 Hz to 330 Hz @60 Hz	–0.1		0.1	
In-band ripple 3	rp3	45 Hz to 1100 Hz @50 Hz 54 Hz to 1320 Hz @60 Hz	–0.1		0.1	
Passband (high pass band)	f_{Clpf}	–3 dB		1672		Hz
Stopband (high pass band)	fatt	–80 dB		2545		Hz
Out-band attenuation	ATT1	f_S	–80			dB
	ATT2	2 f_S	–80			dB

Note Either V_{DD} or VBAT is selected by the battery backup function.

(4) 2 kHz sampling mode

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD}^Note ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation clock	f_{DSAD}	f_X oscillation clock, input external clock or high-speed on-chip oscillator clock is used		12		MHz
Sampling frequency	f_S			1953.125		Hz
Oversampling frequency	f_{OS}			0.75		MHz
Output data rate	T_{DATA}			512		μs
Data width	RES			24		bit
SNDR	SNDR	x1 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)		80		dB
		x16 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)	69	74		
		x32 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)	65	69		
Passband (low pass band)	f_{Chpf}	At –3 dB (phase in high pass filter not adjusted)		0.303		Hz
In-band ripple 1	rp1	45 Hz to 55 Hz @50 Hz 54 Hz to 66 Hz @60 Hz	–0.01		0.01	dB
In-band ripple 2	rp2	45 Hz to 275 Hz @50 Hz 54 Hz to 330 Hz @60 Hz	–0.1		0.1	
In-band ripple 3	rp3	45 Hz to 660 Hz @50 Hz 54 Hz to 550 Hz @60 Hz	–0.1		0.1	
Passband (high pass band)	f_{Clpf}	–3 dB		836		Hz
Stopband (high pass band)	fatt	–80 dB		1273		Hz
Out-band attenuation	ATT1	f_S	–80			dB
	ATT2	2 f_S	–80			dB

Note Either V_{DD} or VBAT is selected by the battery backup function.

2.6.3 Temperature sensor 2 characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD}^Note 2 ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor 2 output voltage	V_{OUT}			0.67		V
Temperature coefficient	F_{VTMPS2}	Temperature sensor that depends on the temperature	–11.7	–10.7	–9.7	mV/°C
Operation stabilization wait time^Note 1	t_{TMPON}	Operable		15	50	μs
	t_{TMPCHG}	Switching mode		5	15	μs

Notes 1. Time to drop to output stable value ±5LSB (±7 mV) or less.

2. Either V_{DD} or VBAT is selected by the battery backup function.

2.6.4 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	When power supply rises[Note 1]	1.47	1.51	1.55	V
	V_{PDR}	When power supply falls[Note 2]	1.46	1.50	1.54	V

Notes 1. Be sure to maintain the reset state until the power supply voltage rises over the minimum V_{DD} value in the operating voltage range specified in **2.4 AC Characteristics**, by using the voltage detector or external reset pin.

2. If the power supply voltage falls while the voltage detector is off, be sure to either shift to STOP mode or execute a reset by using the voltage detector or external reset pin before the power supply voltage falls below the minimum operating voltage specified in **2.4 AC Characteristics**.

2.6.5 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = –40 to +85°C, $V_{PDR} \le V_{DD}$[Note] $\le$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVD0}	When power supply rises	3.98	4.06	4.24	V
		When power supply falls	3.90	3.98	4.16	V
	V_{LVD1}	When power supply rises	3.68	3.75	3.92	V
		When power supply falls	3.60	3.67	3.84	V
	V_{LVD2}	When power supply rises	3.07	3.13	3.29	V
		When power supply falls	3.00	3.06	3.22	V
	V_{LVD3}	When power supply rises	2.96	3.02	3.18	V
		When power supply falls	2.90	2.96	3.12	V
	V_{LVD4}	When power supply rises	2.86	2.92	3.07	V
		When power supply falls	2.80	2.86	3.01	V
	V_{LVD5}	When power supply rises	2.76	2.81	2.97	V
		When power supply falls	2.70	2.75	2.91	V
	V_{LVD6}	When power supply rises	2.66	2.71	2.86	V
		When power supply falls	2.60	2.65	2.80	V
	V_{LVD7}	When power supply rises	2.56	2.61	2.76	V
		When power supply falls	2.50	2.55	2.70	V
	V_{LVD8}	When power supply rises	2.45	2.50	2.65	V
		When power supply falls	2.40	2.45	2.60	V
	V_{LVD9}	When power supply rises	2.05	2.09	2.23	V
		When power supply falls	2.00	2.04	2.18	V
	V_{LVD10}	When power supply rises	1.94	1.98	2.12	V
		When power supply falls	1.90	1.94	2.08	V
	V_{LVD11}	When power supply rises	1.84	1.88	2.01	V
		When power supply falls	1.80	1.84	1.97	V
	V_{LVD12}	When power supply rises	1.74	1.77	1.81	V
		When power supply falls	1.70	1.73	1.77	V
Minimum pulse width	t_{LW}		300			μs
Detection delay time					300	μs

Note Either V_{DD} or VBAT is selected by the battery backup function.

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD}$ Note ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVD8}	VPOC2, VPOC1, VPOC0 = 0, 0, 1, falling reset voltage: 1.8 V			1.80	1.84	1.97	V
	V_{LVD7}		LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	1.94	1.98	2.12	V
				Falling interrupt voltage	1.90	1.94	2.08	V
	V_{LVD6}		LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	2.05	2.09	2.23	V
				Falling interrupt voltage	2.00	2.04	2.18	V
	V_{LVD1}		LVIS1, LVIS0 = 0, 0 (+1.2 V)	Rising release reset voltage	3.07	3.13	3.29	V
				Falling interrupt voltage	3.00	3.06	3.22	V
	V_{LVD8}	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage			2.40	2.45	2.60	V
	V_{LVD7}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.76	V
				Falling interrupt voltage	2.50	2.55	2.70	V
	V_{LVD6}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.86	V
				Falling interrupt voltage	2.60	2.65	2.80	V
	V_{LVD1}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.92	V
				Falling interrupt voltage	3.60	3.67	3.84	V
	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage			2.70	2.75	2.91	V
	V_{LVD4}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	3.07	V
				Falling interrupt voltage	2.80	2.86	3.01	V
	V_{LVD3}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.18	V
				Falling interrupt voltage	2.90	2.96	3.12	V
	V_{LVD0}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.24	V
				Falling interrupt voltage	3.90	3.98	4.16	V

Note Either V_{DD} or VBAT is selected by the battery backup function.

2.6.6 Power supply voltage rising slope characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SV_{DDR} SV_{RTCR}				54	V/ms

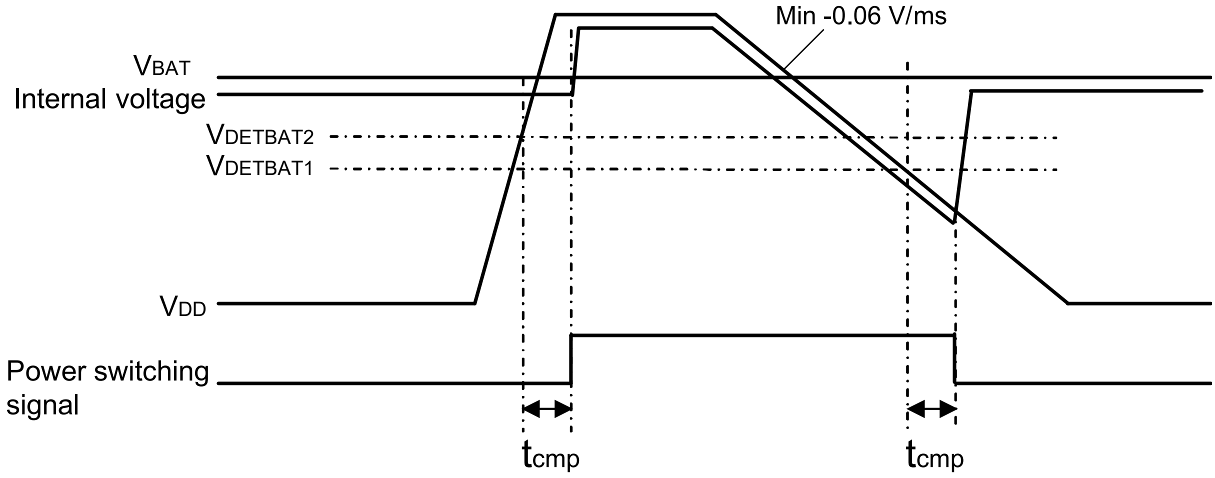
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

2.7 Battery Backup Function

2.7.1 Power supply switching characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power switching detection voltage	$V_{DETBAT1}$	$V_{DD} \rightarrow$ VBAT $V_{BAT} \leq 3.6$ V	2.09	2.18	2.26	V
	$V_{DETBAT2}$	VBAT $\rightarrow V_{DD}$ $V_{BAT} \leq 3.6$ V	2.19	2.28	2.36	V
V_{DD} fall slope	SV_{DDF}		-0.06			V/ms
Response time of power switch detector	t_{cmp}	$V_{BAT} \leq 3.6$ V			500	μs

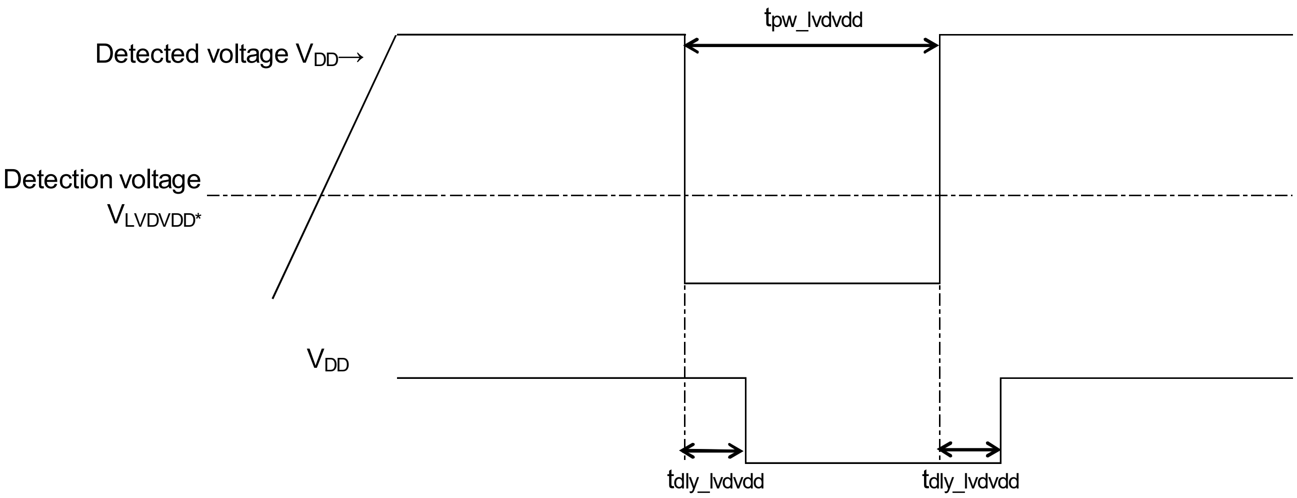


2.7.2 V_{DD} pin voltage detection characteristics

(T_A = –40 to +85°C, 1.9 V ≤ V_{DD}[Note] ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	LVDVDD[2:0]	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	$V_{LVDVDD0}$	000	Rising	2.40	2.53	2.65	V
			Falling	2.33	2.46	2.58	V
	$V_{LVDVDD1}$	001	Rising	2.60	2.74	2.86	V
			Falling	2.53	2.67	2.79	V
	$V_{LVDVDD2}$	010	Rising	2.79	2.94	3.07	V
			Falling	2.73	2.87	2.99	V
	$V_{LVDVDD3}$	011	Rising	3.00	3.15	3.28	V
			Falling	2.93	3.08	3.21	V
	$V_{LVDVDD4}$	100	Rising	3.30	3.46	3.60	V
			Falling	3.23	3.39	3.52	V
	$V_{LVDVDD5}$	101	Rising	3.59	3.77	3.91	V
			Falling	3.53	3.70	3.84	V
Minimum pulse width	t_{pw_lvdvdd}	–	–	300			μs
Detection delay time	t_{dly_lvdvdd}	–	–			300	μs

Note Either V_{DD} or VBAT is selected by the battery backup function.

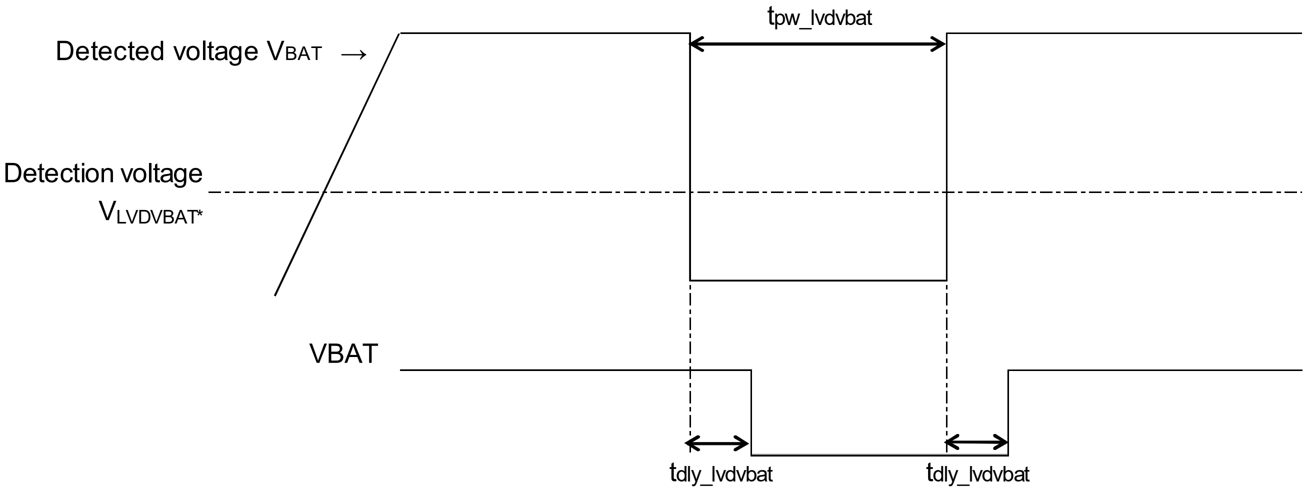


2.7.3 VBAT pin voltage detection characteristics

(T_A = –40 to +85°C, 1.9 V ≤ V_{DD}[Note] ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	LVDVBAT[2:0]	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	$V_{LVDVBAT0}$	000	Rising	1.99	2.11	2.22	V
			Falling	1.94	2.05	2.16	V
	$V_{LVDVBAT1}$	001	Rising	2.09	2.21	2.32	V
			Falling	2.03	2.15	2.26	V
	$V_{LVDVBAT2}$	010	Rising	2.20	2.32	2.43	V
			Falling	2.14	2.26	2.37	V
	$V_{LVDVBAT3}$	011	Rising	2.29	2.42	2.53	V
			Falling	2.23	2.36	2.47	V
	$V_{LVDVBAT4}$	100	Rising	2.38	2.52	2.64	V
			Falling	2.33	2.46	2.58	V
	$V_{LVDVBAT5}$	101	Rising	2.48	2.62	2.74	V
			Falling	2.42	2.56	2.68	V
	$V_{LVDVBAT6}$	110	Rising	2.59	2.73	2.86	V
			Falling	2.53	2.67	2.79	V
Minimum pulse width	$t_{pw\_lvdvbat}$	–	–	300			μs
Detection delay time	$t_{dly\_lvdvbat}$	–	–			300	μs

Note Either V_{DD} or VBAT is selected by the battery backup function.

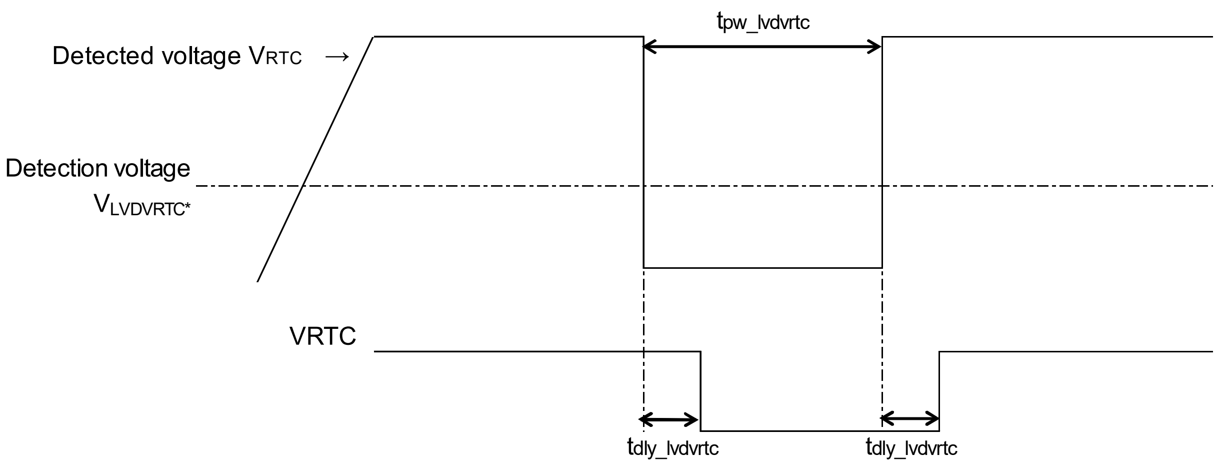


2.7.4 VRTC pin voltage detection characteristics

(T_A = –40 to +85°C, 1.9 V ≤ V_{DD}[Note] ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	LVDVRTC[1:0]	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	$V_{LVDVRTC0}$	00	Rising	2.16	2.22	2.28	V
			Falling	2.10	2.16	2.22	V
	$V_{LVDVRTC1}$	01	Rising	2.36	2.43	2.50	V
			Falling	2.30	2.37	2.44	V
	$V_{LVDVRTC2}$	10	Rising	2.56	2.63	2.70	V
			Falling	2.50	2.57	2.64	V
	$V_{LVDVRTC3}$	11	Rising	2.76	2.84	2.92	V
			Falling	2.70	2.78	2.86	V
Minimum pulse width	$t_{pw\_lvdvrtc}$	–	–	300			μs
Detection delay time	$t_{dly\_lvdvrtc}$	–	–			300	μs

Note Either V_{DD} or VBAT is selected by the battery backup function.

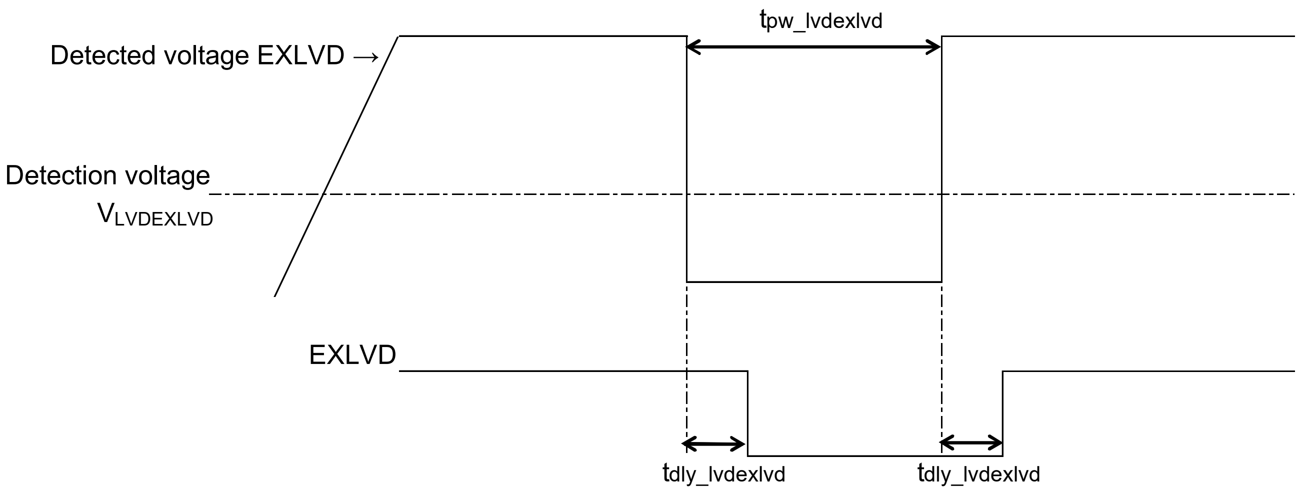


2.7.5 EXLVD pin voltage detection

(T_A = –40 to +85°C, 1.9 V ≤ V_{DD}Note ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	$V_{LVDEXLVD}$	Rising	1.25	1.33	1.41	V
		Falling	1.20	1.28	1.36	V
Minimum pulse width	$t_{pw\_lvdexlvd}$	–	300			μs
Detection delay time	$t_{dly\_lvdexlvd}$	–			300	μs
Pin resistor	r_{in_exlvd}	LVDEXLVDEN = 1		34		MΩ

Note Either V_{DD} or VBAT is selected by the battery backup function.



2.8 LCD Characteristics

2.8.1 Resistance division method

(1) Static display mode

(T_A = –40 to +85°C, V_{L4} (MIN.) ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}Note ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}Note	V

Note Either V_{DD} or VBAT is selected by the battery backup function.

(2) 1/2 bias method, 1/4 bias method

(T_A = –40 to +85°C, V_{L4} (MIN.) ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}Note ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}Note	V

Note Either V_{DD} or VBAT is selected by the battery backup function.

(3) 1/3 bias method

(T_A = –40 to +85°C, V_{L4} (MIN.) ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}Note ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}Note	V

Note Either V_{DD} or VBAT is selected by the battery backup function.

2.8.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 4 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C4 Note 1 = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C4 Note 1 = 0.47 μF		2 V_{L1}–0.10	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L4}	C1 to C4 Note 1 = 0.47 μF		3 V_{L1}–0.15	3 V_{L1}	3 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C4 Note 1 = 0.47 μF		500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 μF±30%

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

4. Either V_{DD} or VBAT is selected by the battery backup function.

(2) 1/4 bias method

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 4 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C5 Note 1 = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	V_{L2}	C1 to C5 Note 1 = 0.47 μF		2 V_{L1}–0.08	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L3}	C1 to C5 Note 1 = 0.47 μF		3 V_{L1}–0.12	3 V_{L1}	3 V_{L1}	V
Quadruply output voltage	V_{L4}	C1 to C5 Note 1 = 0.47 μF		4 V_{L1}–0.16	4 V_{L1}	4 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C5 Note 1 = 0.47 μF		500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L3} and GND
C5: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = C5 = 0.47 μF±30%

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

4. Either V_{DD} or VBAT is selected by the battery backup function.

2.8.3 Capacitor split method

(1) 1/3 bias method

(T_A = –40 to +85°C, 2.2 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 3 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C4 = 0.47 μF Note 2		V_{DD} Note 3		V
V_{L2} voltage	V_{L2}	C1 to C4 = 0.47 μF Note 2	2/3 V_{L4}– 0.1	2/3 V_{L4}	2/3 V_{L4} + 0.1	V
V_{L1} voltage	V_{L1}	C1 to C4 = 0.47 μF Note 2	1/3 V_{L4}– 0.1	1/3 V_{L4}	1/3 V_{L4} + 0.1	V
Capacitor split wait time Note 1	t_{VWAIT}		100			ms

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GND

C3: A capacitor connected between V_{L2} and GND

C4: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = 0.47 μF±30%

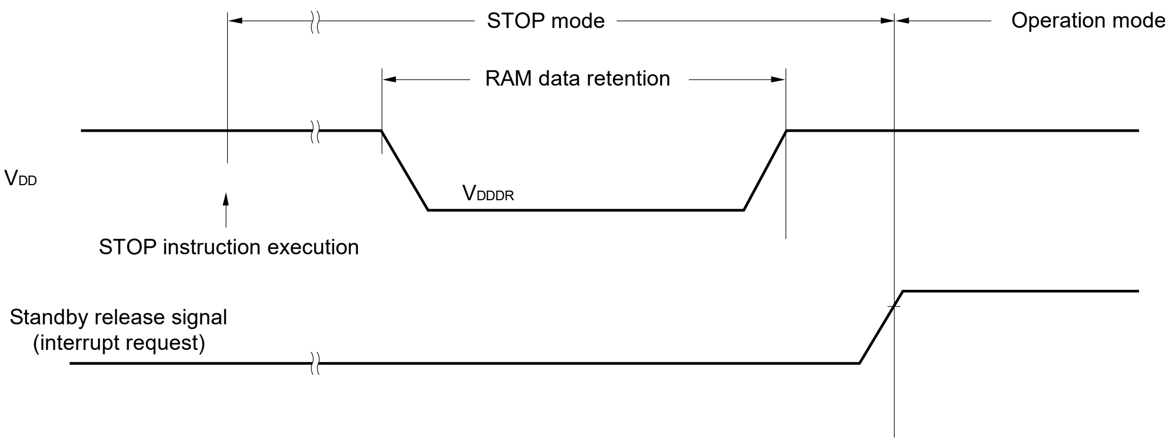
3. Either V_{DD} or VBAT is selected by the battery backup function.

2.9 RAM Data Retention Characteristics

(T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46[Note]		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data in RAM are retained until a POR is applied, but are not retained following a POR.



2.10 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.9 V ≤ V_{DD}[Note 4] ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	1.9 V ≤ V_{DD}[Note 4] ≤ 5.5 V	1		24	MHz
Number of code flash rewrites[Notes 1, 2, 3]	C_{erwr}	Retained for 20 years T_A = 85°C	1,000			Times
Number of data flash rewrites[Notes 1, 2, 3]		Retained for 1 year T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C	100,000			
		Retained for 20 years T_A = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

4. Either V_{DD} or VBAT is selected by the battery backup function.

2.11 Dedicated Flash Memory Programmer Communication (UART)

(T_A = –40 to +85°C, 1.9 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

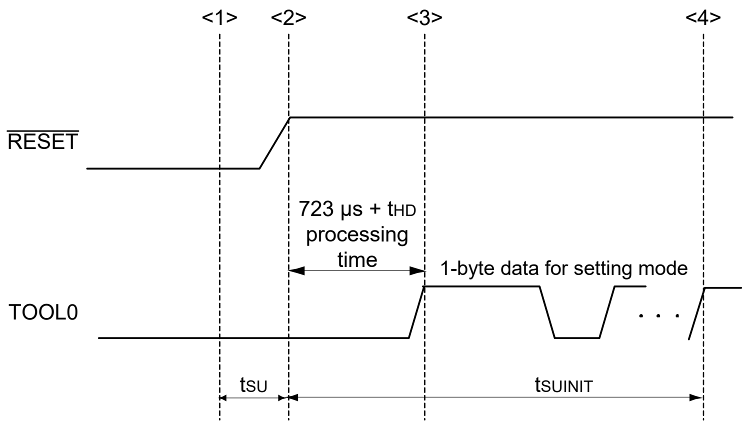
Note Either V_{DD} or VBAT is selected by the battery backup function.

2.12 Timing Specs for Switching Flash Memory Programming Modes

(T_A = –40 to +85°C, 1.9 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms

Note Either V_{DD} or VBAT is selected by the battery backup function.



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level.

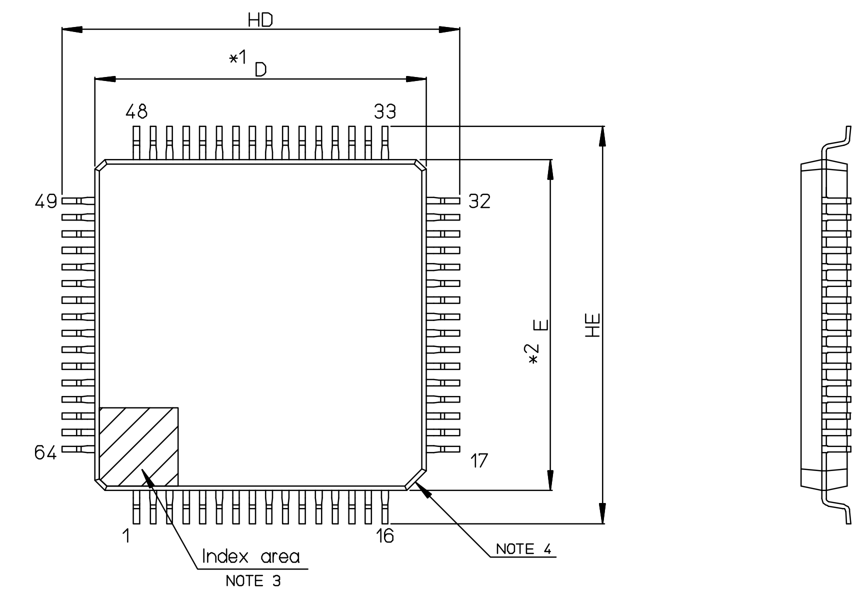
t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

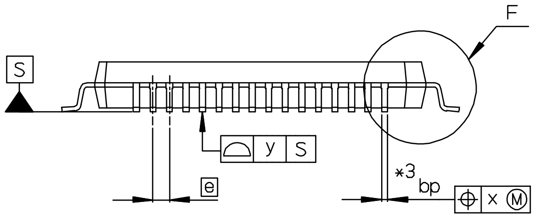
3. PACKAGE DRAWINGS

3.1 64-pin Products

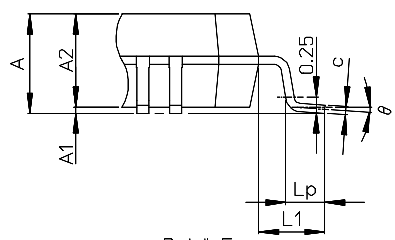
R5F10NLEDFB, R5F10NLGDFB, R5F11TLEDFB, R5F11TLGDFB

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	——	0.3g





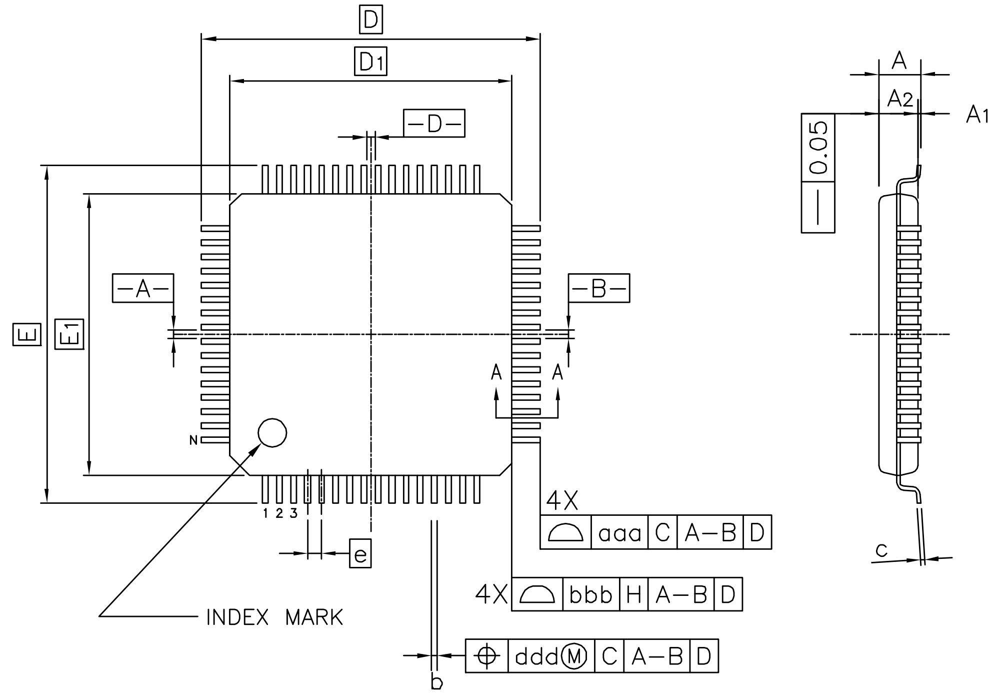
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

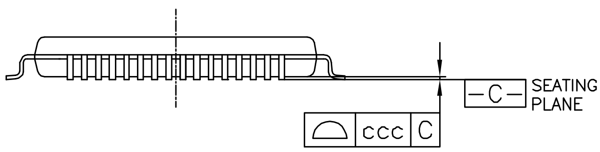


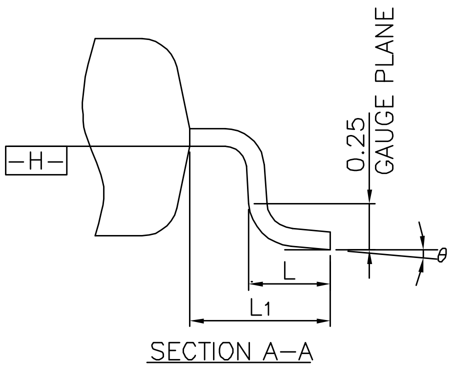
Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A2	——	1.4	——
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFQFP064-10x10-0.50	PLQP0064KL-A	0.36







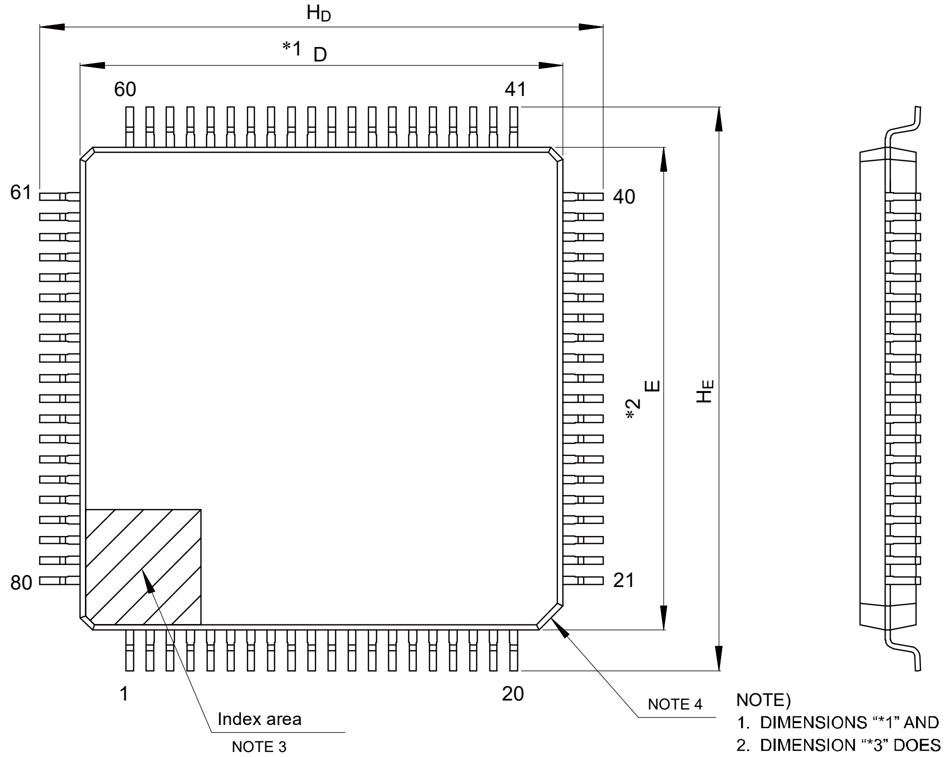
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	−	−	1.60
A_1	0.05	−	0.15
A_2	1.35	1.40	1.45
D	−	12.00	−
D_1	−	10.00	−
E	−	12.00	−
E_1	−	10.00	−
N	−	64	−
e	−	0.50	−
b	0.17	0.22	0.27
c	0.09	−	0.20
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L_1	−	1.00	−
aaa	−	−	0.20
bbb	−	−	0.20
ccc	−	−	0.08
ddd	−	−	0.08

3.2 80-pin Products

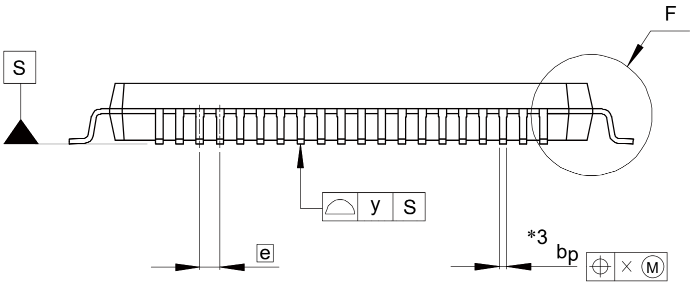
R5F10NMEDFB, R5F10NMGDFB, R5F10NMJDFB

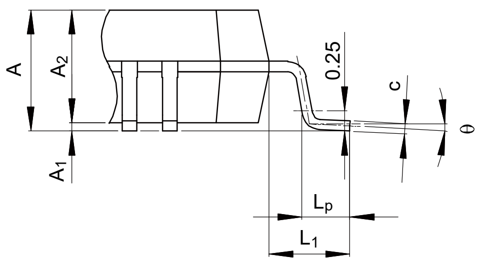
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	—	0.5

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

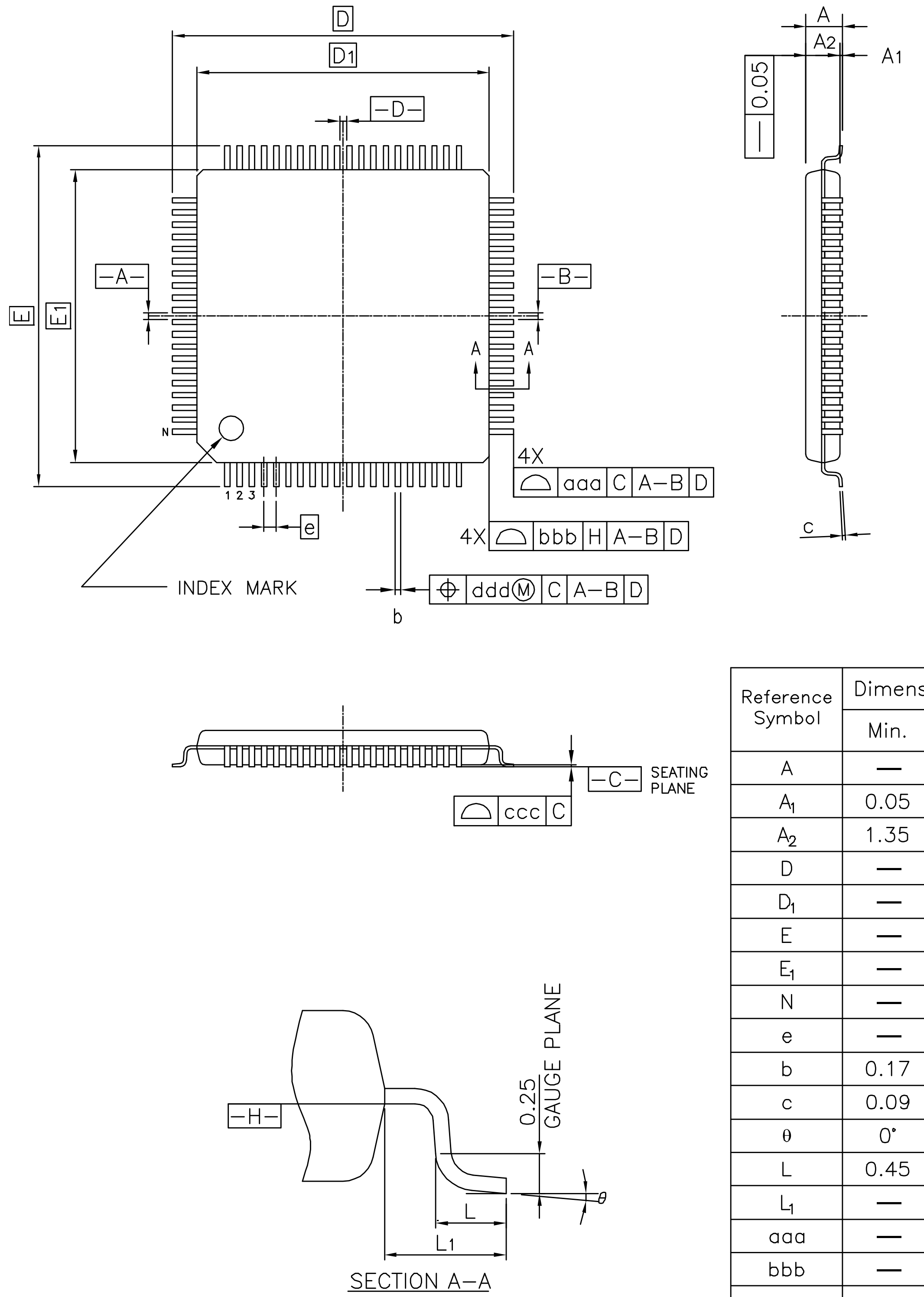




Detail F

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

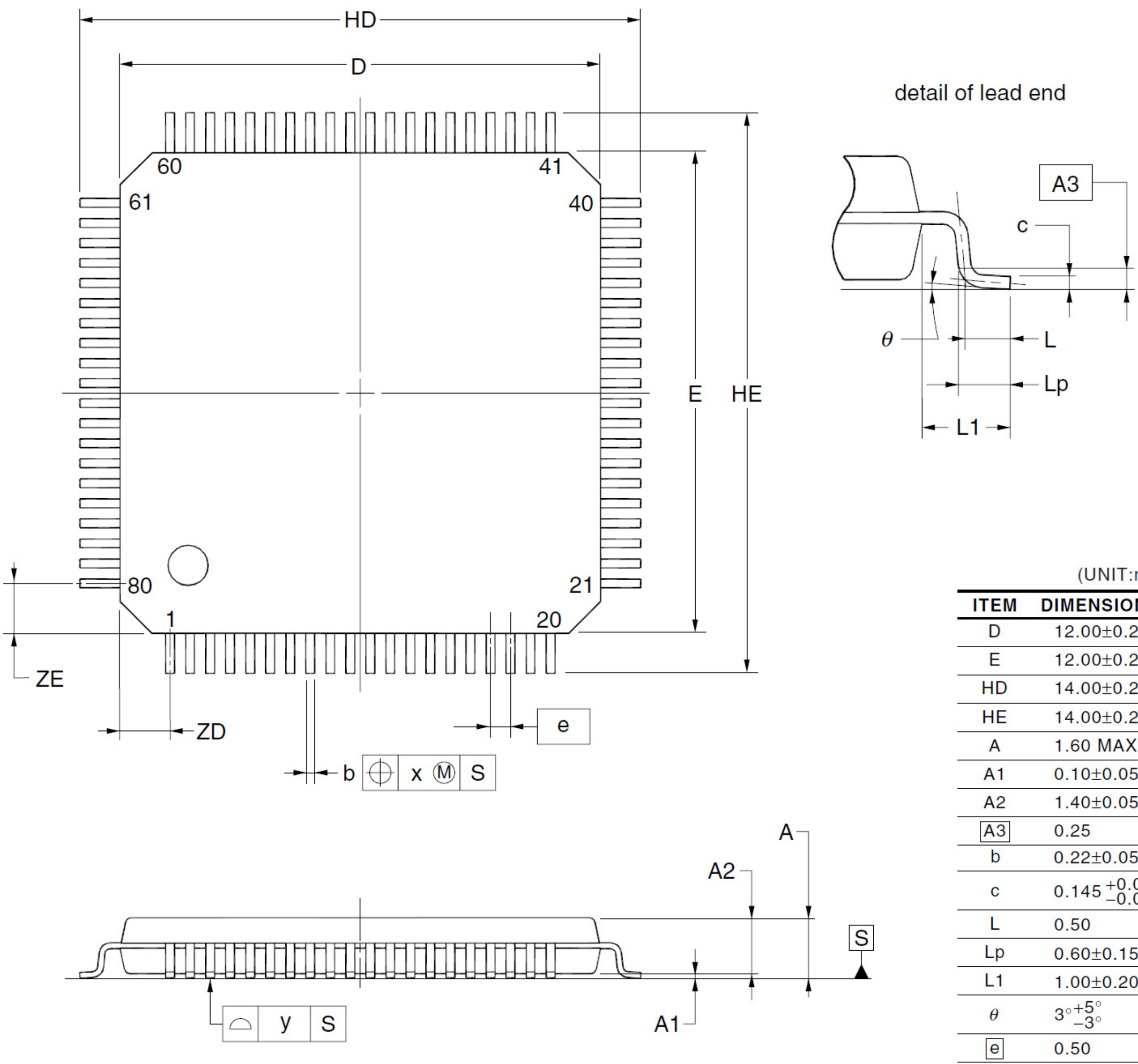
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFQFP80-12x12-0.50	PLQP0080KJ-A	0.49



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	1.60
A_1	0.05	—	0.15
A_2	1.35	1.40	1.45
D	—	14.00	—
D_1	—	12.00	—
E	—	14.00	—
E_1	—	12.00	—
N	—	80	—
e	—	0.50	—
b	0.17	0.22	0.27
c	0.09	—	0.20
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L_1	—	1.00	—
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU	0.53



(UNIT:mm)

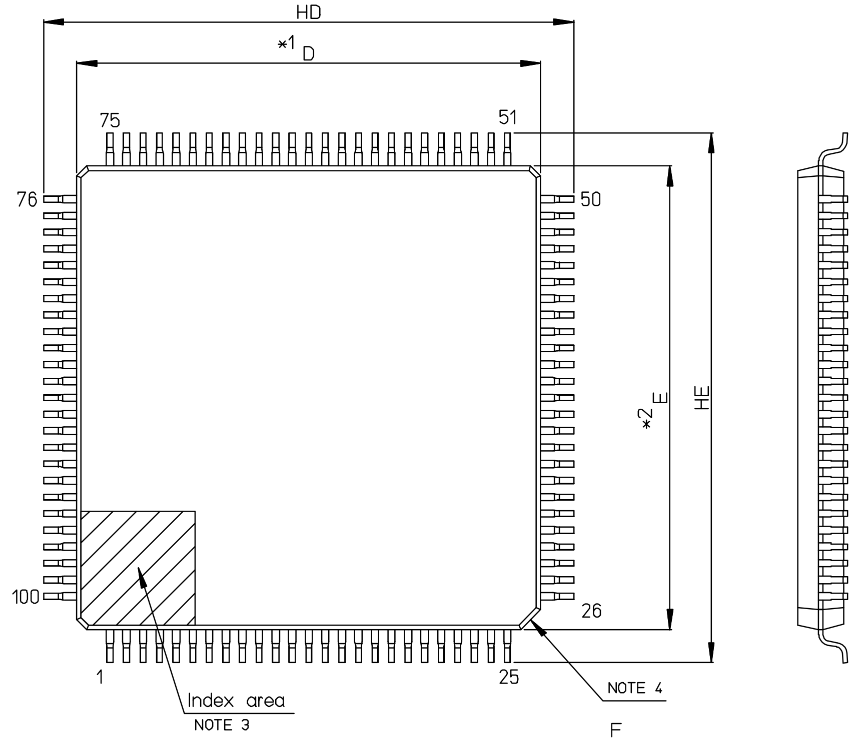
ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

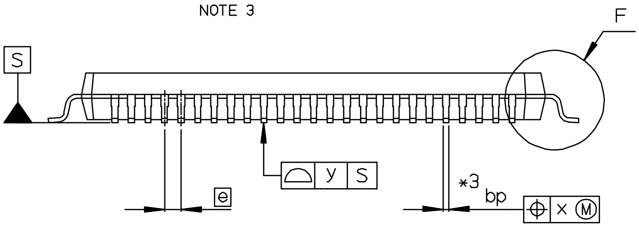
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

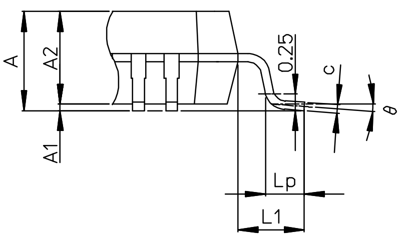
3.3 100-pin Products

R5F10NPJDFB, R5F10NPGDFB

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6g





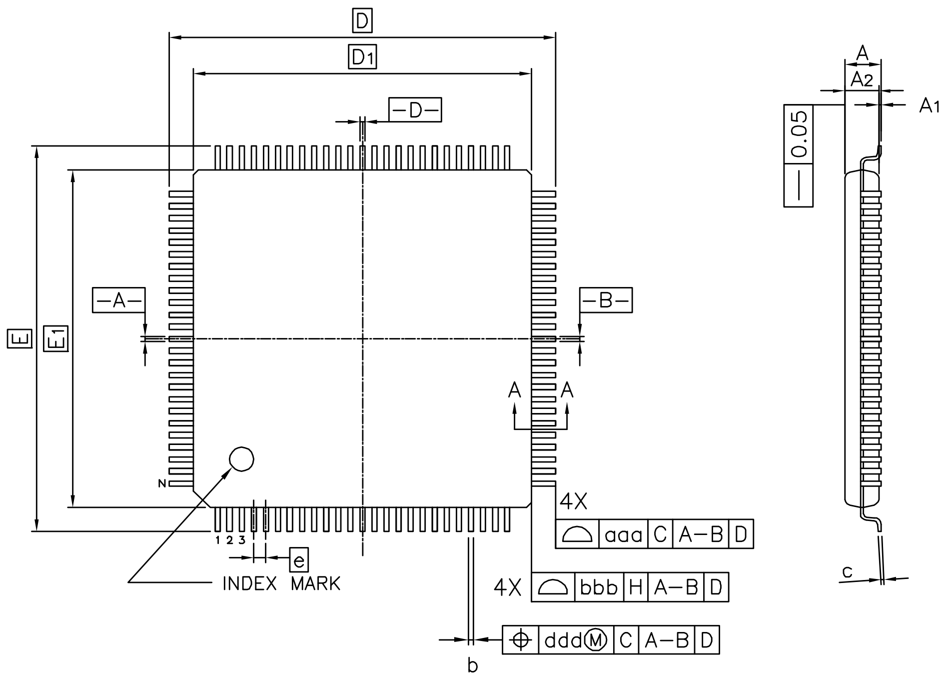


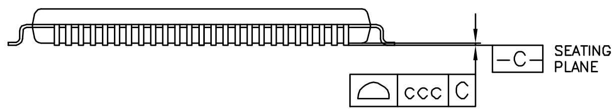
Detail F

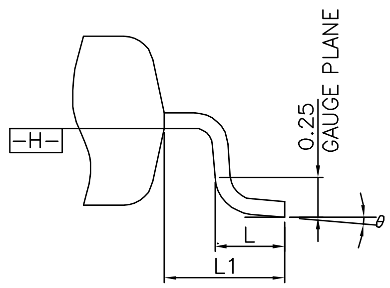
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A2	—	1.4	—
HD	15.8	16.0	16.2
HE	15.8	16.0	16.2
A	—	—	1.7
A1	0.05	—	0.15
bp	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
$\boxed{e}$	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Lp	0.45	0.6	0.75
L1	—	1.0	—

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFQFP100-14x14-0.50	PLQP0100KP-A	0.67







SECTION A-A

Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.60
A_1	0.05	–	0.15
A_2	1.35	1.40	1.45
D	–	16.00	–
D_1	–	14.00	–
E	–	16.00	–
E_1	–	14.00	–
N	–	100	–
e	–	0.50	–
b	0.17	0.22	0.27
c	0.09	–	0.20
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L_1	–	1.00	–
aaa	–	–	0.20
bbb	–	–	0.20
ccc	–	–	0.08
ddd	–	–	0.08

Rev.	Date	Description: Page	Description: Summary
1.00	May 31, 2016	–	First Edition issued
2.00	Aug 31, 2018	p.12	Modification of table in 1.6 Outline of Functions
		p.21, 22	Modification of description in 2.3.1 Pin characteristics
		p.67	Modification of table in 2.6.1 (1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pins: ANI2 to ANI5 and internal reference voltage
		p.68	Modification of table in 2.6.1 (2) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pins: ANI0 to ANI5 and internal reference voltage
		p.69	Modification of parameter and symbol, and addition of note 2 in 2.6.2 (1) Reference voltage
		p.70	Modification of condition and unit in 2.6.2 (2) Analog input
		p.72	Modification of typical value in 2.6.2 (4) 2 kHz sampling mode
2.10	Aug 23, 2019	Throughout	Addition of products in which AES function is not available (R5F11TLG and R5F11TLE)
		p.1	Addition of description in 1.1 Features
		p.3	Modification of note 2 in 1.1 Features
		p.4	Modification of Figure 1-1 Part Number, Memory Size, and Package of RL78/I1C
		p.4	Modification of Table 1-1 List of Ordering Part Numbers
		p.12	Deletion of note 1 in the “100-pin” column in 1.6 Outline of Functions
		p.13, 14	Modification of 1.6 Outline of Functions
		p.78	Modification of 2.7.3 VBAT pin voltage detection characteristics
		p.79	Modification of 2.7.4 VRTC pin voltage detection characteristics
		p.82	Deletion of note 2 for V_{L1} in 2.8.2 Internal voltage boosting method, (1) 1/3 bias method
		p.83	Deletion of note 2 for V_{L1} in 2.8.2 Internal voltage boosting method, (2) 1/4 bias method
2.11	Nov 30, 2022	Throughout	The module name for CSI was changed to simplified SPI.
			“Wait” was modified to “clock stretch”
		p.4	Modification of Figure 1-1. Part Number, Memory Size, and Package of RL78/I1C
		p.5	Modification of Table 1-1. List of Ordering Part Numbers
		p.88	Modification of package drawing in 3.1 64-pin Products (PLQP0064KB-C)
		p.89	Addition of package drawing in 3.1 64-pin Products (PLQP0064KL-A)
		p.90	Modification of package drawing in 3.2 80-pin Products (PLQP0080KB-B)
		p.91	Addition of package drawing in 3.2 80-pin Products (PLQP0080KJ-A)
		p.92	Modification of package drawing in 3.3 100-pin Products (PLQP0100KB-B)
		p.93	Addition of package drawing in 3.3 100-pin Products (PLQP0100KP-A)
2.20	Jul 20, 2023	p.30	Modification of Note 1 and 4 in 2.3.2 Supply current characteristics
		p.31	Modification of Note 9 to Note 5 in 2.3.2 Supply current characteristics
		p.32	Modification of Note 5 to Note 6 in 2.3.2 Supply current characteristics
			Deletion of Note 6 in 2.3.2 Supply current characteristics
		p.33	Modification of Note 1, 5 and 6 in 2.3.2 Supply current characteristics
2.30	Mar 29, 2024	p.4	Modification of Figure 1-1. Part Number, Memory Size, and Package of RL78/I1C
		p.5	Modification of Table 1-1. List of Ordering Part Numbers
		p.92	Addition of package drawing in 3.2 80-pin Products (PLQP0080KE-A)

The mark “<R>” shows major revised points. The revised points can be easily searched by copying an “<R>” in the PDF file and specifying it in the “Find what:” field.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Renesas Electronics:

R5F11TLGDFB#35 R5F11TLGDFB#55 R5F10NPJDFB#35 R5F10NPJDFB#55 R5F11TLEDFB#35
R5F11TLEDFB#55 R5F10NMGDFB#35 R5F10NMGDFB#55 R5F10NMJDFB#35 R5F10NMJDFB#55
R5F10NPGDFB#35 R5F10NPGDFB#55 R5F10NLEDFB#35 R5F10NLEDFB#55 R5F10NLGDFB#35
R5F10NLGDFB#55 R5F10NMEDFB#35 R5F10NMEDFB#55 R5F11TLEDFB#10 R5F11TLGDFB#10
R5F10NLEDFB#10 R5F10NLGDFB#10 R5F10NMEDFB#10 R5F10NMGDFB#10 R5F10NMJDFB#10
R5F10NPGDFB#10 R5F10NPJDFB#10 R5F10NLEDFB#15 R5F10NLGDFB#15 R5F10NMEDFB#15
R5F11TLEDFB#15 R5F10NMGDFB#15 R5F10NMJDFB#15 R5F10NPGDFB#15 R5F10NPJDFB#15
R5F11TLGDFB#15 R5F10NMLDFB#10 R5F10NMLDFB#30 R5F10NMLDFB#50 R5F10NPLDFB#10
R5F10NPLDFB#30 R5F10NPLDFB#50 R5F11TLEDFB#75 R5F11TLGDFB#75