ISL59830

True Single Supply Video Driver

NOT RECOMMENDED FOR NEW DESIGNS
PLEASE REFER TO ISL59833
FOR A PIN COMPATIBLE UPGRADE

FN7489
Rev.1.00
May 4, 2006

The ISL59830 is a revolutionary device that allows true single-supply operation of video amplifiers. The device runs off a single 3.3V supply and generates the required negative voltage internally. This allows for DC-accurate coupling of video onto a 75Ω double-terminated line. Since the buffers have an integrated 6dB gain, no external gain setting resistors are required. An input reference voltage can be supplied to shift the analog video level down by an amount equal to the reference (typically 0.6V).

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
ISL59830IA	59830IA	-	16 Ld QSOP	M16.15A
ISL59830IA-T7	59830IA	7”	16 Ld QSOP	M16.15A
ISL59830IA-T13	59830IA	13”	16 Ld QSOP	M16.15A
ISL59830IAZ (See Note)	59830IAZ	-	16 Ld QSOP (Pb-Free)	M16.15A
ISL59830IAZ-T7 (See Note)	59830IAZ	7”	16 Ld QSOP (Pb-Free)	M16.15A
ISL59830IAZ-T13 (See Note)	59830IAZ	13”	16 Ld QSOP (Pb-Free)	M16.15A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

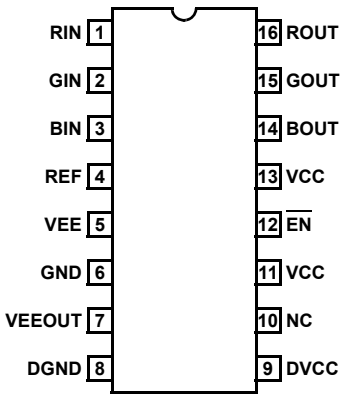
- Triple single-supply buffer
- Operates from single +3.3V supply
- No output DC blocking capacitor needed
- Fixed gain of 2 output buffer
- Output three-statable
- Enable/disable function
- 50MHz 0.1dB bandwidth
- 200MHz -3dB bandwidth
- Pb-free plus anneal available (RoHS compliant)

Applications

- Driving video

Pinout

ISL59830
(16 LD QSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

V_{CC}, Supply Voltage between V_S and GND 5V
V_{IN}, V_{REF} . . . . . .VCC+0.3V, VEE-0.3V
Voltage between V_{IN} and V_{REF} . . . . . .±2V
Maximum Continuous Output Current 30mA

Operating Temperature . . . . . .-40°C to +85°C
Maximum Die Temperature . . . . . .+150°C
Storage Temperature . . . . . .-65°C to +150°C
Lead Temperature . . . . . .260°C
Power Dissipation . . . . . See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

AC Electrical Specifications

V_{CC} = DV_{CC} = +3.3V, REF = GND, T_A = 25°C, R_L = 150Ω, unless otherwise specified.

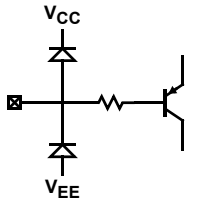
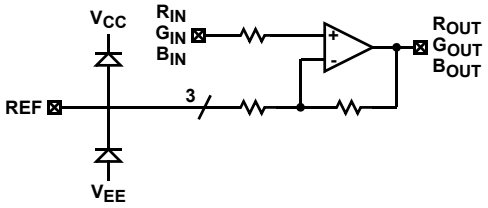
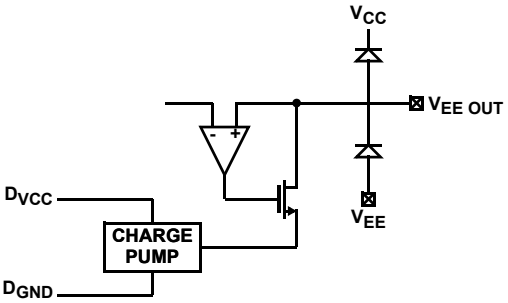
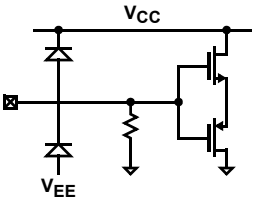
PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
BW -3dB	3dB Bandwidth	V_{OUT} = 200mV_{PP}		200		MHz
		V_{OUT} = 2V_{PP}		100		MHz
BW 0.1dB	0.1dB Bandwidth	V_{OUT} = 2V_{PP}		50		MHz
S_R	Slew Rate	V_{OUT} = 2V_{PP}	500			V/µs
d_G	Differential Gain			0.07		%
d_P	Differential Phase			0.06		°
X_T	Hostile Crosstalk	6MHz		-90		dB
I	Input to Output Isolation	6MHz		-70		dB
V_N	Input Noise Voltage			20		nV/√Hz
Fcp	Charge Pump Switch Frequency			168		MHz
Load Reg		I_{EE} = 0mA to 10mA		12	60	mV
V_{RIPPLE}	Output Amp Ripple Voltage			30		mV
		With Bead Core to DV_{CC}		10		mV

DC Electrical Specifications

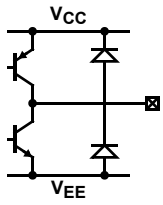
V_{CC} = D_{VCC} = +3.3V, REF = GND, T_A = 25°C, R_L = 150Ω, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V+	Supply Range		3.0		3.6	V
V_G%	Gain Error	R_L = 150Ω, V_{IN} = +2.5V to -1V			1.5	%
ΔG	Gain Matching	R_L = 150Ω		0.5		%
R_{IN}	Input Resistance	V_{IN} = 0V to 1.5V	1.0	1.7	15	MΩ
V_{OS}	Output Offset Voltage	V_{REF} = 0	-25	7	+25	mV
I_{OUT+}	Output Current	R_L = 10Ω, V_{IN} = 1.2V	50			mA
I_{OUT-}	Output Current	R_L = 10Ω, V_{IN} = -0.3V			-18	mA
Z_{OUT}	Output Impedance	Enabled		1		Ω
		Three-stated		10		MΩ
PSRR	Power Supply Rejection Ratio		60	90		dB
I_S	Supply Current	Amp Enabled		120	150	mA
		Amp Disabled		80		mA
R_{REF}	Input Reference Resistor		4	5	6	kΩ

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION	EQUIVALENT CIRCUIT
1	RIN	Analog input	 CIRCUIT 1
2	GIN	Analog input	Reference Circuit 1
3	BIN	Analog input	Reference Circuit 1
4	REF	Reference input	 CIRCUIT 2
5	VEE	Chip substrate	 CIRCUIT 3
6	GND	Analog ground	
7	VEE OUT	Charge pump output	Reference Circuit 3
8	DGND	Charge pump ground	Reference Circuit 3
9	DVCC	Charge pump supply voltage	Reference Circuit 3
10	NC	Not connected	
11, 13	VCC	Positive power supply	
12	$\overline{EN}$	Chip enable	 CIRCUIT 4

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	EQUIVALENT CIRCUIT
14	BOUT	Analog output	 CIRCUIT 5
15	GOUT	Analog output	Reference Circuit 5
16	ROUT	Analog output	Reference Circuit 5

Typical Performance Curves

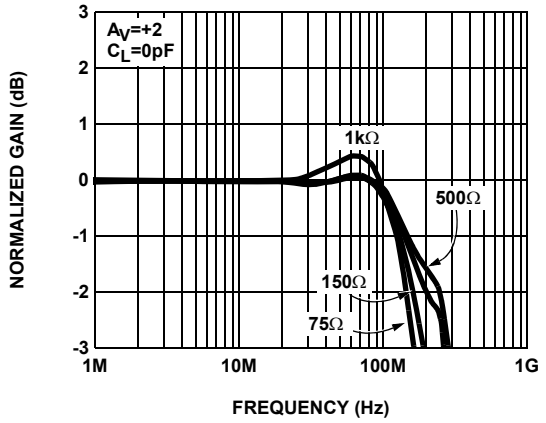


FIGURE 1. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD}

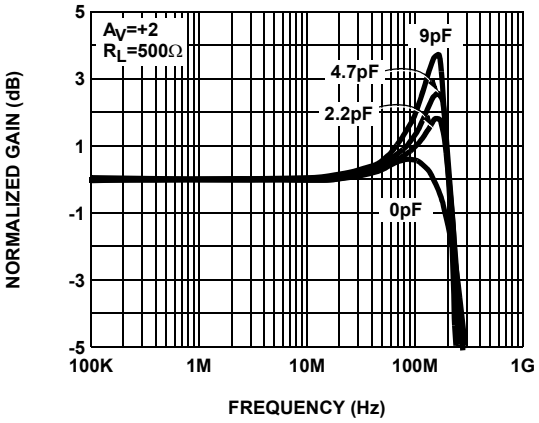


FIGURE 2. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD}

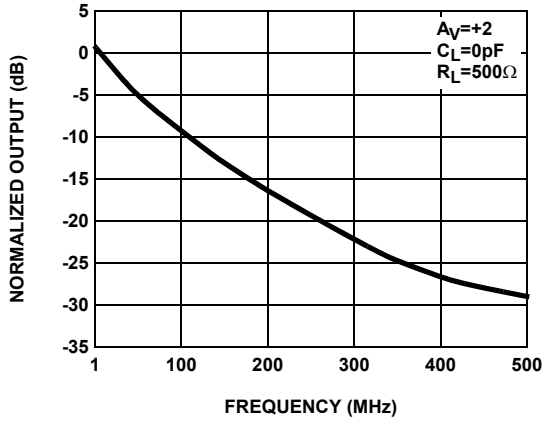


FIGURE 3. V_{REF} PIN OUTPUT FREQUENCY RESPONSE

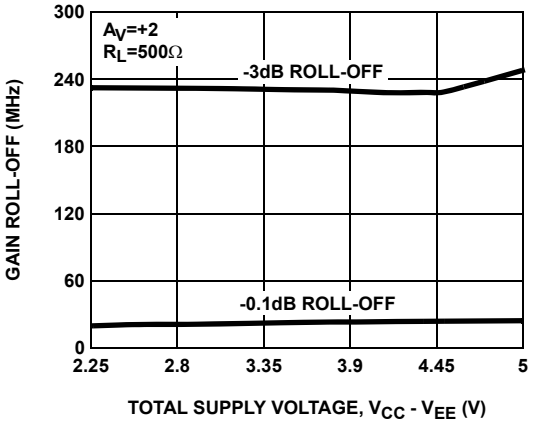


FIGURE 4. GAIN ROLL-OFF

Typical Performance Curves (Continued)

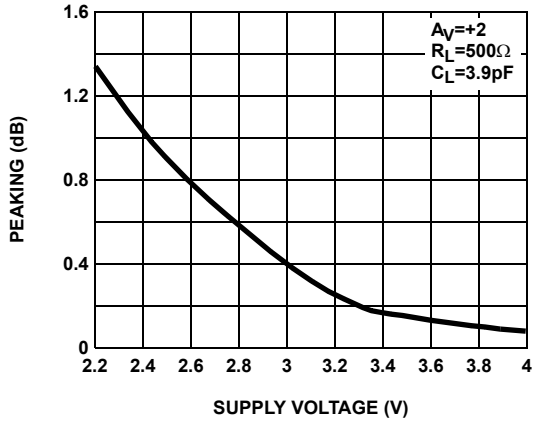


FIGURE 5. PEAKING vs SUPPLY VOLTAGE

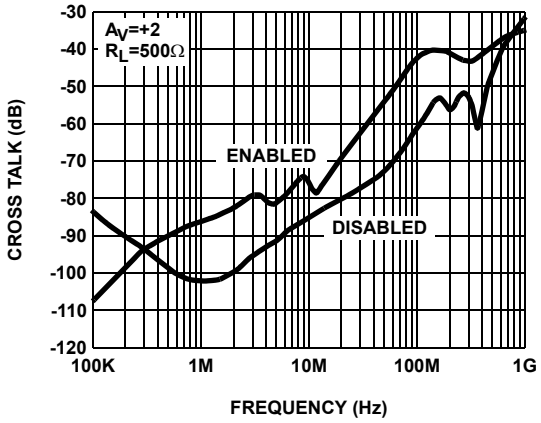


FIGURE 6. CROSS TALK CHANNEL TO CHANNEL (TYPICAL)

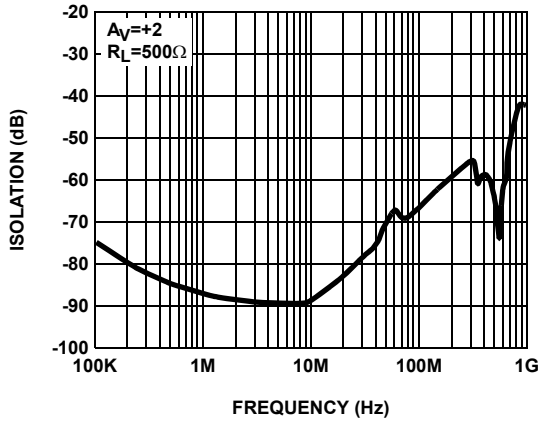


FIGURE 7. INPUT TO OUTPUT ISOLATION vs FREQUENCY

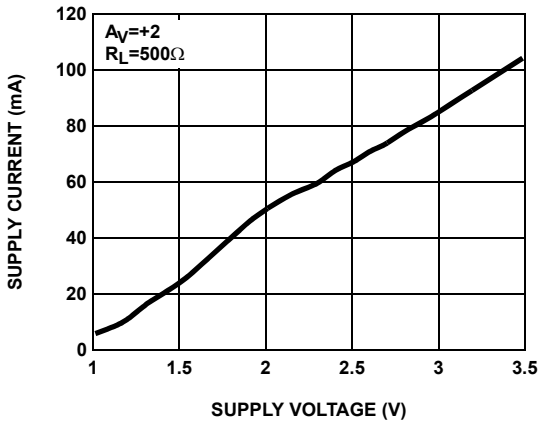


FIGURE 8. SUPPLY CURRENT vs SUPPLY VOLTAGE

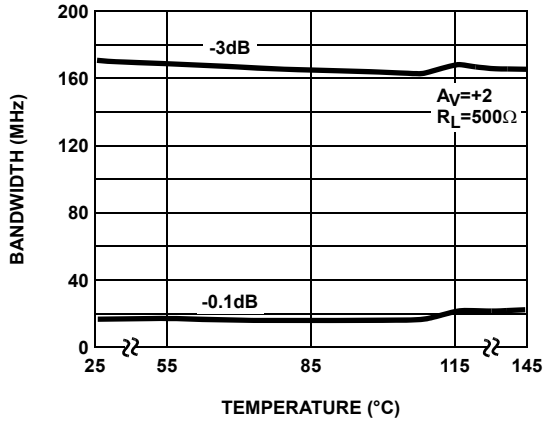


FIGURE 9. BANDWIDTH vs TEMPERATURE

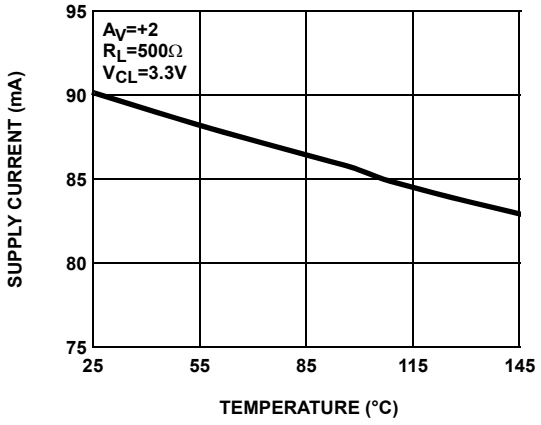


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

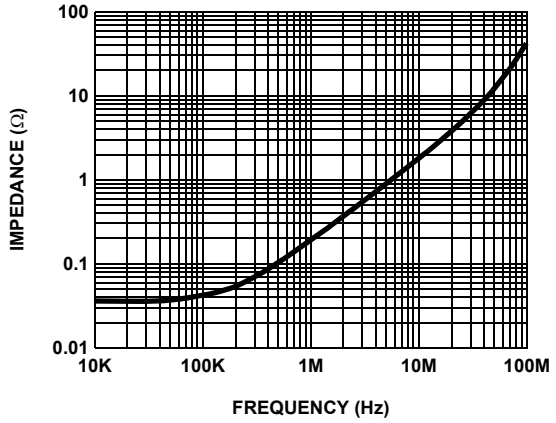


FIGURE 11. OUTPUT IMPEDANCE vs FREQUENCY

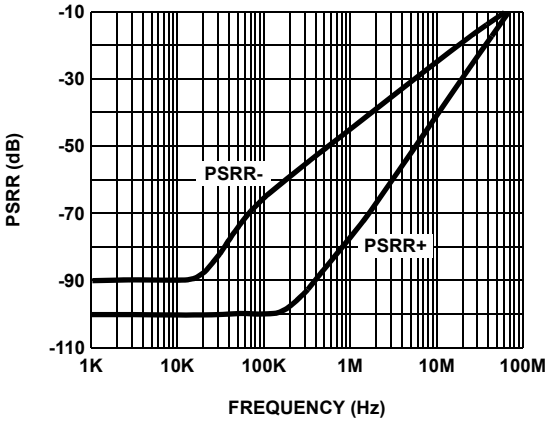


FIGURE 12. POWER SUPPLY REJECTION RATIO vs FREQUENCY

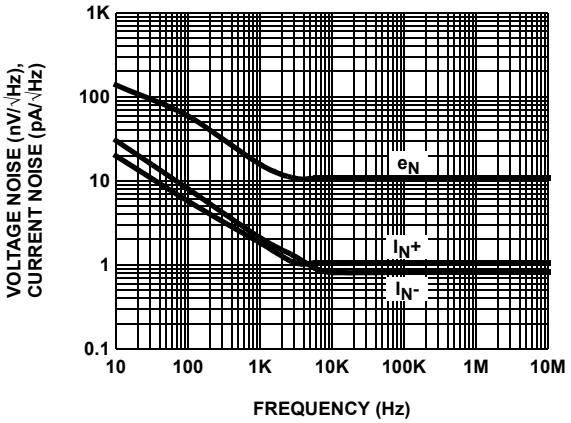


FIGURE 13. VOLTAGE AND CURRENT NOISE vs FREQUENCY

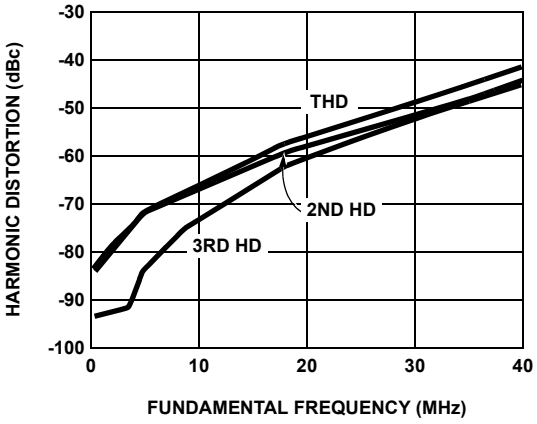


FIGURE 14. HARMONIC DISTORTION vs FREQUENCY

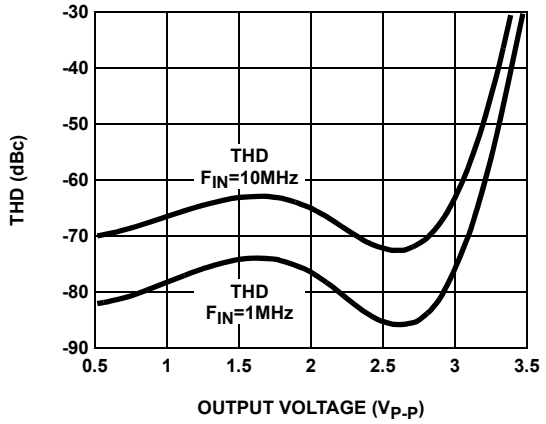


FIGURE 15.

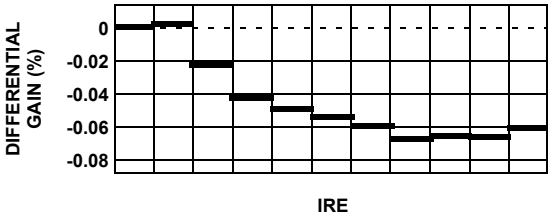


FIGURE 16. DIFFERENTIAL GAIN

Typical Performance Curves (Continued)

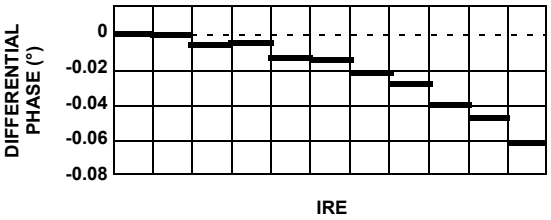


FIGURE 17. DIFFERENTIAL PHASE

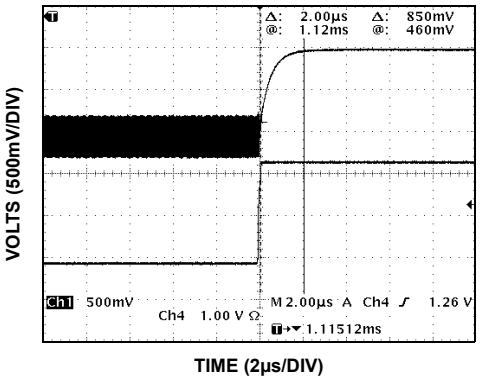


FIGURE 18. DISABLE TIME

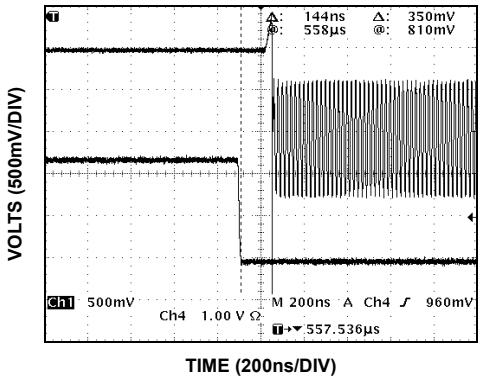


FIGURE 19. ENABLE TIME

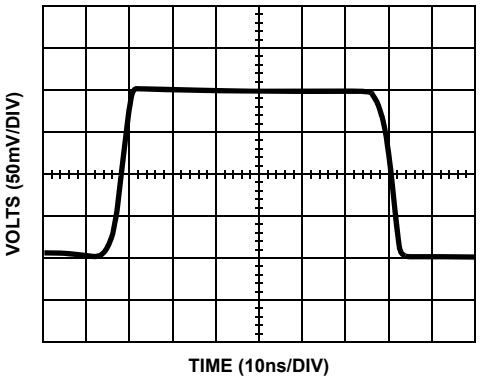


FIGURE 20. SMALL SIGNAL RISE & FALL TIMES

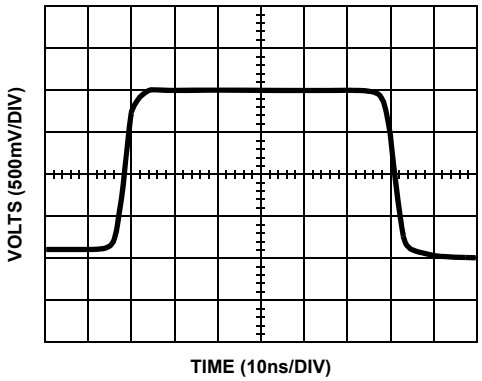


FIGURE 21. LARGE SIGNAL RISE & FALL TIMES

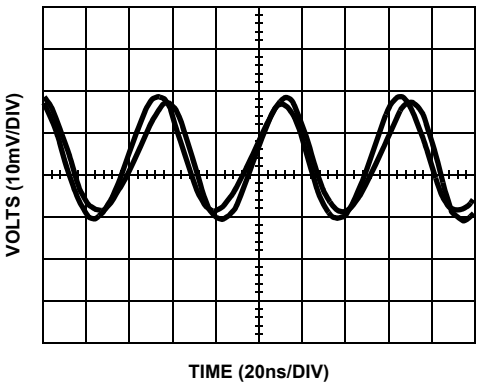


FIGURE 22. AMP OUTPUT NOISE (CHARGE PUMP OSCILLATION)

Typical Performance Curves (Continued)

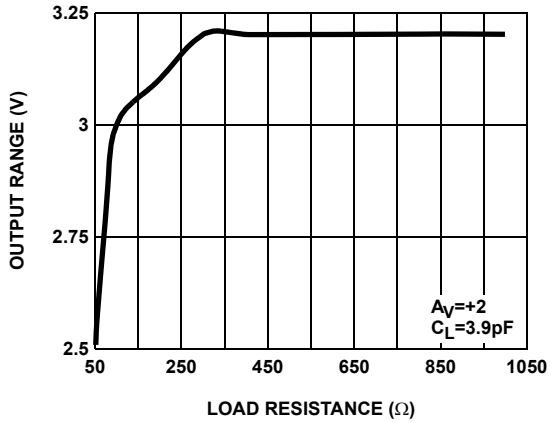


FIGURE 23. MAXIMUM OUTPUT MAGNITUDE vs LOAD RESISTANCE

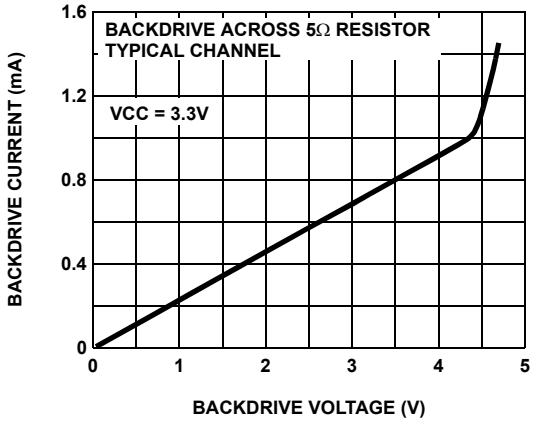


FIGURE 24. BACKDRIVE VOLTAGE vs CURRENT AMP DISABLED OUTPUT LOADING

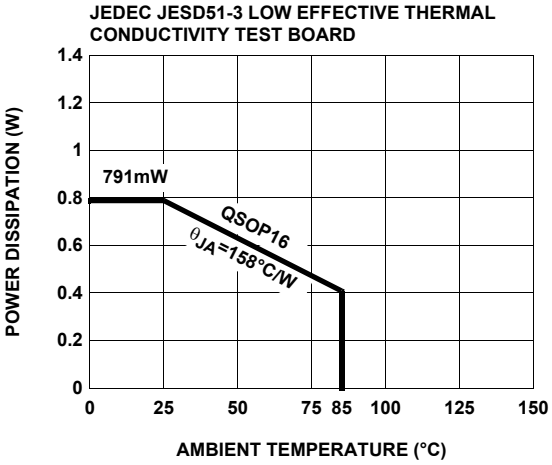


FIGURE 25. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

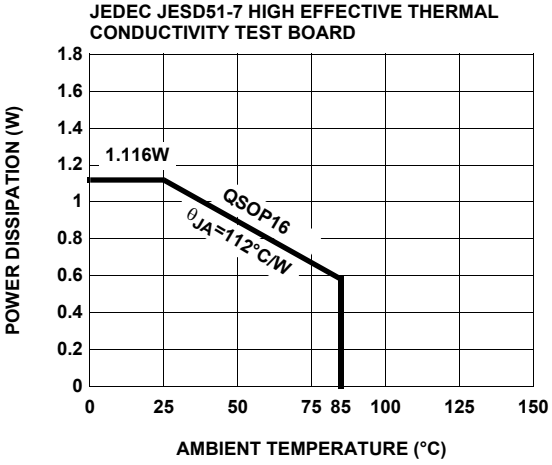
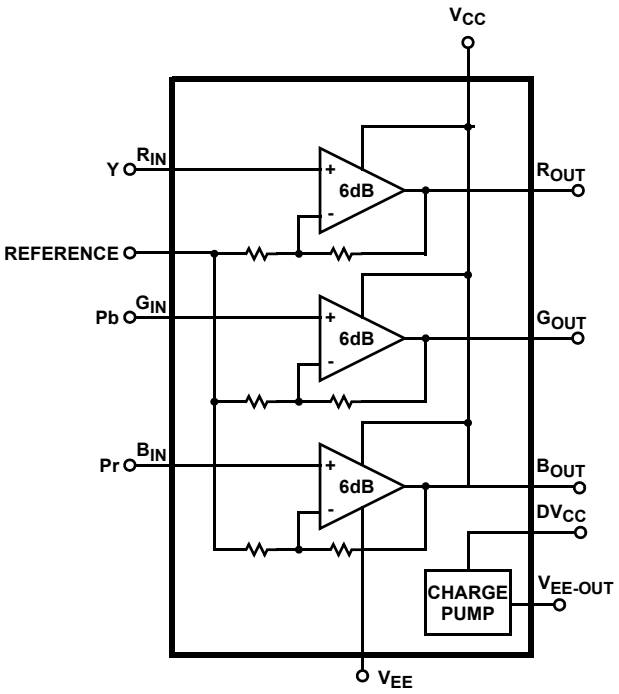


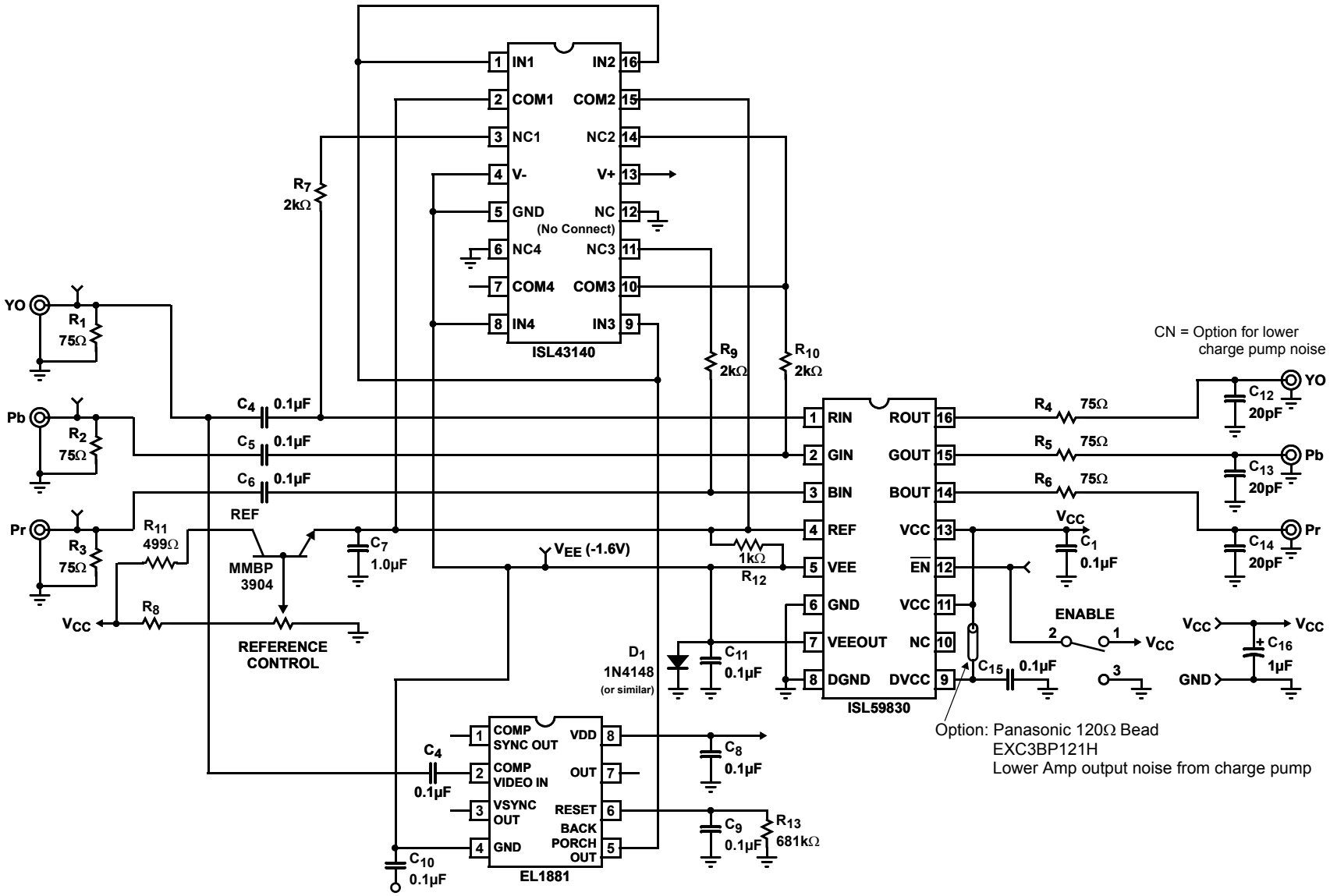
FIGURE 26. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Block Diagram

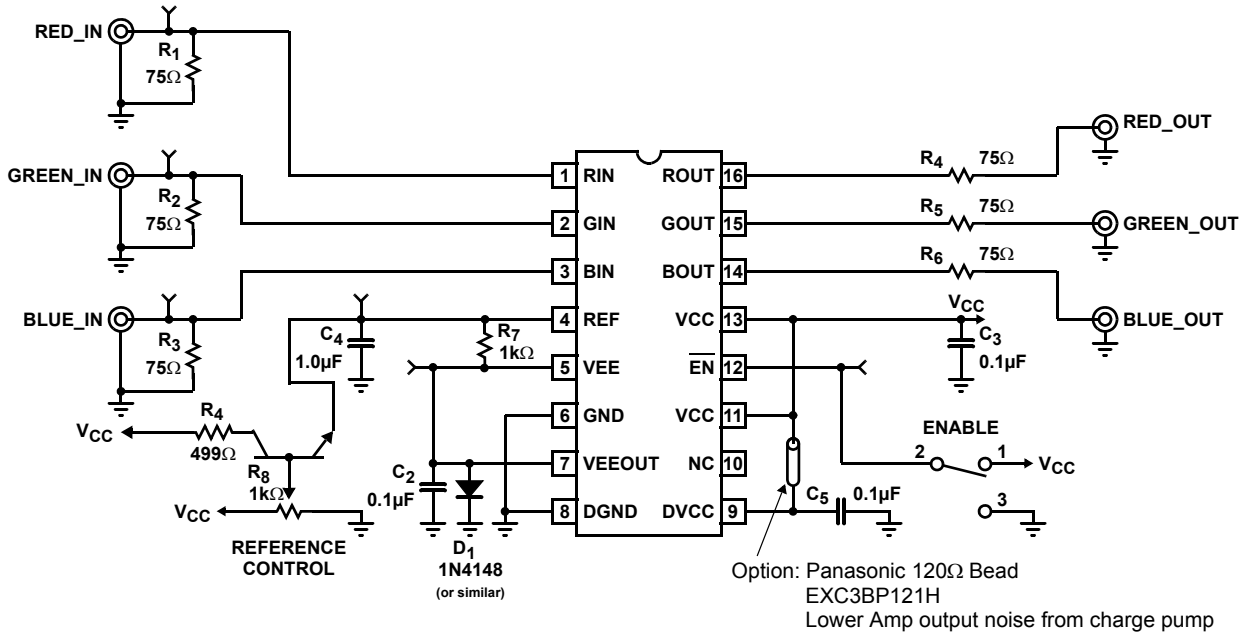


$V_{OUT} = 2V_{IN} - V_{REFERENCE}$

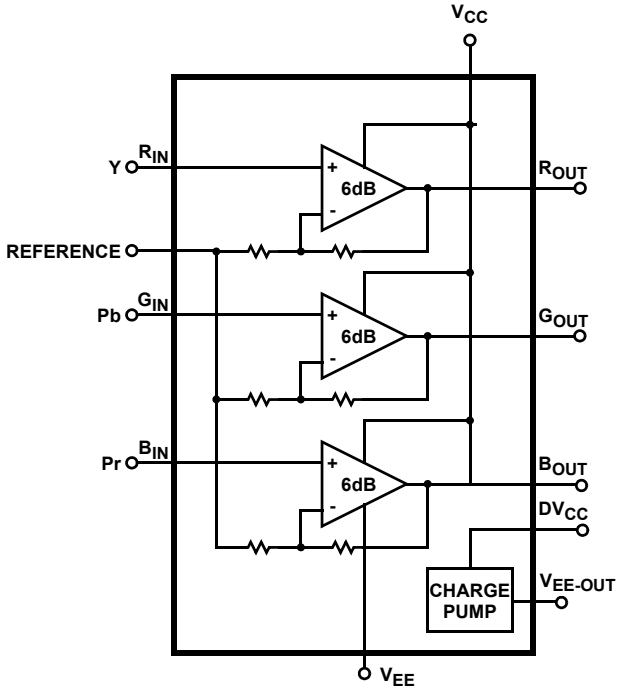
ISL59830 + DC-Restore Solution



Demo Board Schematic



Block Diagram



$V_{OUT} = 2V_{IN} - V_{REFERENCE}$

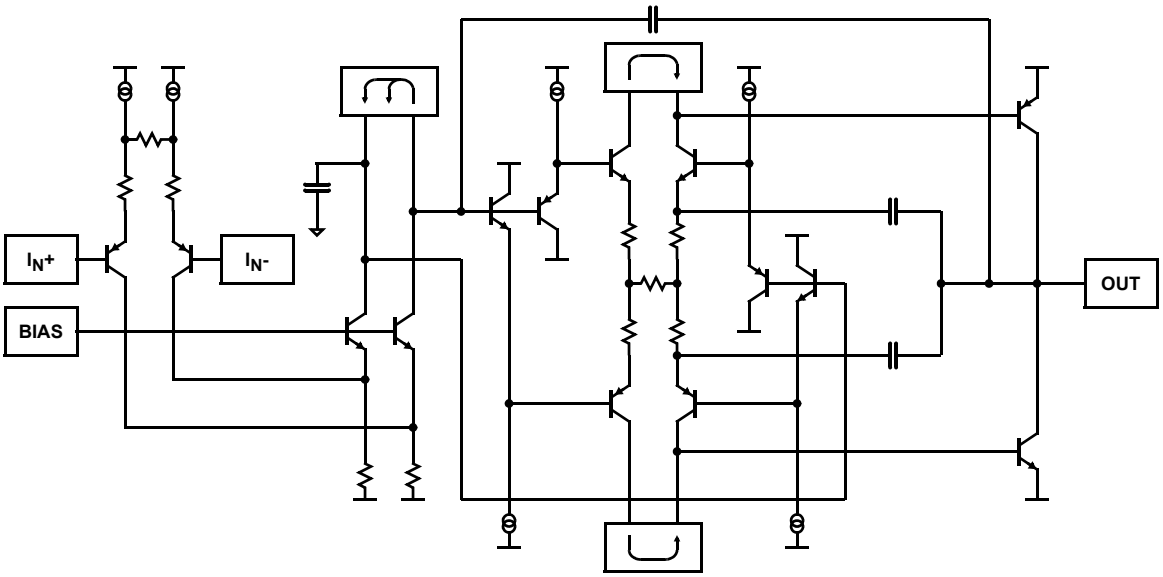


FIGURE 27.

Description of Operation and Application Information

Theory Of Operation

The ISL59830 is a highly practical and robust marriage of three high bandwidth, high speed, low power, rail-to-rail voltage feedback amplifiers with a charge pump, to provide a negative rail without an additional power supply. Designed to operate with a single supply voltage range of from 0V to 3.3V, the ISL59830 eliminates the need for a split supply with the incorporation of a charge pump capable of generating a bottom rail as much as 1.6V below ground; for a 4.9V range on a single 3.3V supply. This performance is ideal for NTSC video with its negative-going sync pulses.

The Amplifier

The ISL59830 fabricated on a dielectrically isolated high speed 5V Bi-CMOS process with 4GHz PNPs and NPN transistor exceeding 20GHz - perfect for low distortion, low power demand and high frequency circuits. While the ISL59830 utilizes somewhat standard voltage mode feedback topologies, there are many non-standard analog features providing its outstanding bandwidth, rail-to-rail operation, and output drive capabilities. The input signal initially passes through a folded cascode, a topology providing enhanced frequency response essentially by fixing the base collector voltage at the junction of the input and gain stage. The collector of each input device looks directly into an emitter that is tied closely to ground through a resistor and biased with a very stable DC source. Since the voltage of this collector is "locked stable" the effective bandwidth limiting of the Miller capacitance is greatly reduced. The signal is then passed through a second fully-realized differential gain stage and finally through a proprietary common emitter output stage for improved rail-to-rail output performance. The result is a highly-stable, low distortion, low power, and high frequency amplifier capable of driving moderately capacitive loads with near rail-to-rail performance.

Input Output Range

The three amplifier channels have an input common mode voltage range from 0.15V below the bottom rail to within 100mV of the positive supply, V_S+ pin (Note: bottom rail is established by the charge pump at negative one half the positive supply). As the input signal moves outside the specified range, the output signal will exhibit increasingly higher levels of harmonic distortion. And of course, as load resistance becomes lower, the current drive capability of the device will be challenged and its ability to drive close to each rail is reduced. For instance, with a load resistance of 1kΩ the output swing is within a 100mV of the rails, while a load resistance of 150Ω limits the output swing to within around 300mV of the rails.

Amplifier Output Impedance

To achieve near rail-to-rail performance, the output stage of the ISL59830 uses transistors in the common emitter configuration, typically producing higher output impedance than the standard emitter follower output stage. The exceptionally high open loop gain of the ISL59830 and local feedback reduces output impedance to less than a 2Ω at low frequency. However, since output impedance of the device is exponentially modulated by the magnitude of the open loop gain, output impedance increases with frequency as the open loop gain decreases with frequency. This inductive-like effect of the output impedance is countered in the ISL59830 with proprietary output stage topology, keeping the output impedance low over a wide frequency range and making it possible to easily and effectively drive relatively heavy capacitive loads.(See Figure 11).

The Charge Pump

The ISL59830 charge pump provides a bottom rail up to 1.65V below ground while operating on a 0V to 3.3V power supply. The charge pump is internally regulated to one-half the potential of the positive supply. This internal multi-phase charge pump is driven by a 160MHz differential ring oscillator driving a series of inverters and charge storage circuitry. Each series inverter charges and places parallel adjoining charge circuitry slightly out of phase with the immediately preceding block. The overall effect is sequential discharge and generation of a very low ripple of about 10mV that is applied to the amplifiers providing a negative rail of up to -1.65V.

There are two options to reduce the output supply noise.

- Add a 120Ω bead in series between V_{CC} and DV_{CC} to further reduce ripple.

Add a 20pF capacitor between the back load 75Ω resistor and ground (see the ISL59830A + DC-Restore Solution schematic on page 10).

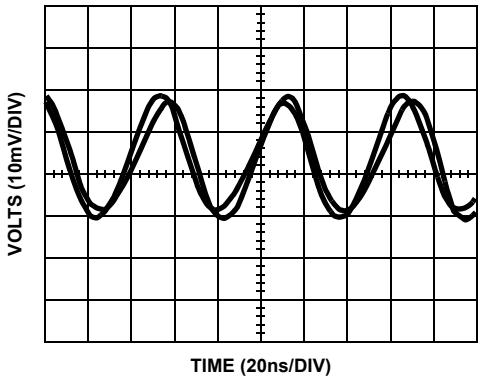


FIGURE 28. CHARGE PUMP OSCILLATION (AMP OUTPUT)

The system operates at sufficiently high frequencies that any related charge pump noise is far beyond standard video bandwidth requirements. Still, appropriate bypassing discipline must be observed, and all pins related to either the power supply or the charge pump must be properly bypassed. See "Power Supply Bypassing and Printed Circuit Board Layout" in this section.

To maximize resistance to latch-up, a diode should be added between the VEEOUT pin (anode) and GND (cathode), as shown in the Demo Board Schematic. This prevents VEE from rising more than 0.7V above ground during startup. (VEE > 1V above GND can cause latchup under some conditions.)

The V_{REF} Pin

Applying a voltage to the V_{REF} pin simply places that voltage on what would usually be the ground side of the gain resistor of the amplifier, resulting in a DC-level shift of the output signal. Applying 100mV to the Vref pin would apply a -100mV DC level shift to the outgoing signal. The charge pump provides sufficient bottom room to accommodate the shifted signal. V_{REF} may be connected to ground for back porch at ground.

Note: The V_{REF} input is the common point of the 3 amps minus input resistors. Any common resistance on V_{REF} input will share the voltage induced on it with all the other amps, so using a resistor source to get offset will cause cross talk and gain change for the offset for all amps and amp +input gain change. Offset on the V_{REF} pin must be low impedance to prevent gain error and cross talk. A transistor emitter follower should work like an NPN MMBT3904 with the emitter connected to the V_{REF} pin and 1k pull down to V- with 1µF cap bypass to ground and the collector to V+ and base to V offset source. If better tempco is needed then a diode may be used in series with the pot to ground. A 499Ω resistor may be added in series with the collector to prevent damage when testing.

See the Block Diagram on page 8.

The V_{EE} Pin

The V_{EE} pin is the output pin for the charge pump. A voltmeter applied to this pin will display the output of the charge pump. This pin does not affect the functionality of the part. One may use this pin as an additional voltage source. Keep in mind that the output of this pin is generated by the internal charge pump and a fully regulated supply that must be properly bypassed. We recommend a 0.1µF ceramic capacitor placed as close to the pin and connected to the ground plane of the board.

Input, Output, and Supply Voltage Range

The ISL59830 is designed to operate with a single supply voltage range of from 0V to 3.3V. The need for a split supply has been eliminated with the incorporation of a charge pump capable of generating a bottom rail as much as 1.6V below ground, for a 4.9V range on a single 3.3V supply. This performance is ideal for NTSC video with its negative-going sync pulses.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency and phase response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω because of the change in output current with changing DC levels. Special circuitry has been incorporated into the ISL59830 for the reduction of output impedance variation with the current output. This results in outstanding differential gain and differential phase specifications of 0.06% and 0.1°, while driving 150Ω at a gain of +2. Driving higher impedance loads would result in similar or better differential gain and differential phase performance.

NTSC

The ISL59830, generating a negative rail internally, is ideally suited for NTSC video with its accompanying negative-going sync signals; easily handled by the ISL59830 without the need of an additional supply as the ISL59830 generates a negative rail with an internal charge pump referenced at negative 1/2 the positive supply.

YPbPr

YPbPr signals originating from a DVD player requiring three channels of very tightly-controlled amplifier gain accuracy present no difficulty for the ISL59830. Specifically, this standard encodes sync on the Y channel and it is a negative-going signal; easily handled by the ISL59830 without the need of an additional supply as the ISL59830 generates a negative rail placed at negative 1/2 the positive supply. Additionally, the Pb and Pr are bipolar analog signals and the video signals are negative-going; and again easily handled by the ISL59830.

Driving Capacitive Loads and Cables

The ISL59830, internally-compensated to drive 75Ω cables, will drive 10pF loads in parallel with 1kΩ with less than 5dB of peaking. If less peaking is required, a small series resistor, usually between 5Ω to 50Ω, can be placed in series with the output. This will reduce peaking at the expense of a slight closed loop gain reduction. When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking. The ISL59830 is a triple amplifier designed to drive three channels; simply deal with each channel separately as described in this section.

DC-Restore

When the ISL59830 is AC-coupled it becomes necessary to restore the DC reference for the signal. This is accomplished with a DC-restore system applied between the capacitive "AC" coupling and the input of the device. Refer to Application Circuit for reference DC-restore solution.

Amplifier Disable

The ISL59830 can be disabled and its output placed in a high impedance state. The turn-off time is around 25ns and the turn-on time is around 200ns. When disabled, the amplifier's supply current is reduced to 80mA typically, reducing power consumption. The amplifier's power-down can be controlled by standard TTL or CMOS signal levels at the $\overline{EN}$ pin. The applied logic signal is relative to GND pin. Letting the $\overline{EN}$ pin float or applying a signal that is less than 0.8V above GND will enable the amplifier. The amplifier will be disabled when the signal at $\overline{EN}$ pin is 2V above GND. The V_{EE} charge pump remains active.

Output Drive Capability

The ISL59830 does not have internal short-circuit protection circuitry. A short-circuit current of 80mA sourcing and 150mA sinking for the output is connected to half way between the rails with a 10Ω resistor. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±40mA, after which the electro-migration limit of the process will be exceeded and the part will be damaged. This limit is set by the design of the internal metal interconnections.

Power Dissipation

With the high output drive capability of the ISL59830, it is possible to exceed the 150°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

Θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

for sourcing:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_S - V_{OUT}i) \times \frac{V_{OUT}i}{R_L i}$$

for sinking:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_{OUT}i - V_S) \times I_{LOAD}i$$

Where:

V_S = Supply voltage

I_{SMAX} = Maximum quiescent supply current

V_{OUT} = Maximum output voltage of the application

R_{LOAD} = Load resistance tied to ground

I_{LOAD} = Load current

i = Number of output channels

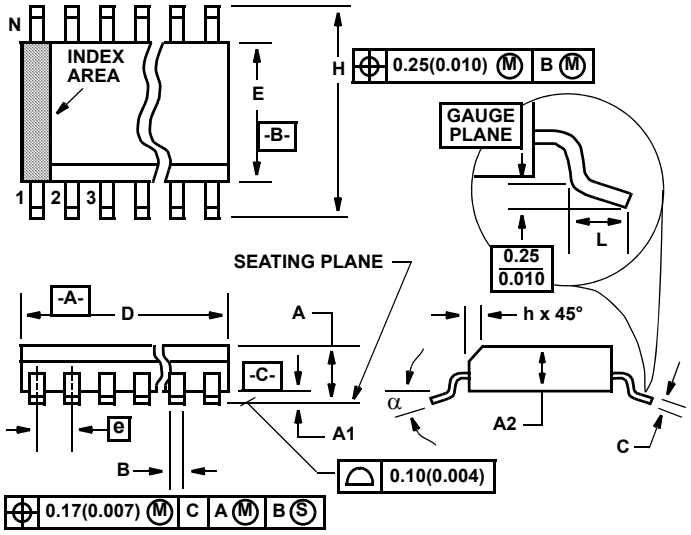
By setting the two P_{DMAX} equations equal to each other, we can solve the output current and R_{LOAD} to avoid the device overheat.

Power Supply Bypassing and Printed Circuit Board Layout

Strip line design techniques are recommended for the input and output signal traces. As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_S+ to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split-internal supplies are to be used. In this case, the V_S- pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to a minimum. Use of wire-wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is also very important.

Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



M16.15A

16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150" WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.061	0.068	1.55	1.73	-
A1	0.004	0.0098	0.102	0.249	-
A2	0.055	0.061	1.40	1.55	-
B	0.008	0.012	0.20	0.31	9
C	0.0075	0.0098	0.191	0.249	-
D	0.189	0.196	4.80	4.98	3
E	0.150	0.157	3.81	3.99	4
e	0.025 BSC		0.635 BSC		-
H	0.230	0.244	5.84	6.20	-
h	0.010	0.016	0.25	0.41	5
L	0.016	0.035	0.41	0.89	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 2 6/04

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

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