Data Sheet | December 6, 2005 | FN3160.8

8-Digit, Microprocessor-Compatible, LED Display Decoder Driver

The Intersil ICM7228 display driver interfaces microprocessors to an 8-digit, 7-segment, numeric LED display. Included on chip are two types of 7-segment decoder, multiplex scan circuitry, LED display segment drivers, LED display digit drivers and an 8-byte static memory as display RAM.

Data can be written to the ICM7228A and ICM7228B's display RAM in sequential 8-digit update or in single-digit update format. Data is written to the ICM7228C display RAM in parallel random access format. The ICM7228A and ICM7228C drive common anode displays. The ICM7228B drives common cathode displays. All versions can display the RAM data as either Hexadecimal or Code B format. The ICM7228A and ICM7228B incorporate a No Decode mode allowing each bit of each digit's RAM word to drive individual display segments resulting in independent control of all display segments. As a result, bargraph and other irregular display segments and formats can be driven directly by this chip.

The Intersil ICM7228 is an alternative to both the Maxim ICM7218 and the Intersil ICM7218 display drivers. Notice that the ICM7228A/B has an additional single digit access mode. This could make the Intersil ICM7218A/B software incompatible with ICM7228A/B operation.

Features

- Pb-Free Plus Anneal Available (RoHS Compliant)
- Improved 2nd Source to Maxim ICM7218
- Fast Write Access Time of 200ns
- Multiple Microprocessor Compatible Versions
- Hexadecimal, Code B and No Decode Modes
- Individual Segment Control with "No Decode" Feature
- Digit and Segment Drivers On-Chip
- Non-Overlapping Digits Drive
- Common Anode and Common Cathode LED Versions
- Low Power CMOS Architecture
- Single 5V Supply

Applications

- Instrumentation
- Test Equipment
- Hand Held Instruments
- Bargraph Displays
- Numeric and Non-Numeric Panel Displays
- High and Low Temperature Environments where LCD Display Integrity is Compromised

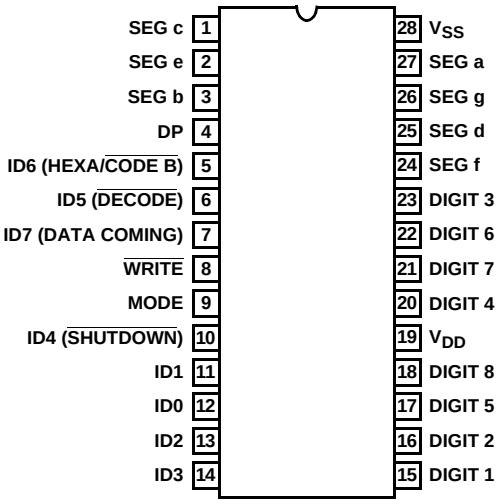
Ordering Information

PART NUMBER	PART MARKING	DATA ENTRY PROTOCOL	DISPLAY TYPE	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
ICM7228AIBI	ICM7228AIBI	Sequential	Common Anode	-40 to 85	28 Ld SOIC	M28.3
ICM7228AIBIZ (Note)	7228AIBIZ	Sequential	Common Anode	-40 to 85	28 Ld SOIC (Pb-free)	M28.3
ICM7228AIPI	ICM7228AIPI	Sequential	Common Anode	-40 to 85	28 Ld PDIP	E28.6
ICM7228AIPIZ (Note)	ICM7228AIPI	Sequential	Common Anode	-40 to 85	28 Ld PDIP* (Pb-free)	E28.6
ICM7228BIBI	ICM7228BIBI	Sequential	Common Cathode	-40 to 85	28 Ld SOIC	M28.3
ICM7228BIBIZ (Note)	ICM7228BIBIZ	Sequential	Common Cathode	-40 to 85	28 Ld SOIC (Pb-free)	M28.3
ICM7228BIPI	ICM7228BIPI	Sequential	Common Cathode	-40 to 85	28 Ld PDIP	E28.6
ICM7228BIPIZ (Note)	ICM7228BIPIZ	Sequential	Common Cathode	-40 to 85	28 Ld PDIP (Pb-free)	E28.6
ICM7228CIBI	ICM7228CIBI	Random	Common Anode	-40 to 85	28 Ld SOIC	M28.3
ICM7228CIBIZ (Note)	ICM7228CIBIZ	Random	Common Anode	-40 to 85	28 Ld SOIC (Pb-free)	M28.3
ICM7228CIPI	ICM7228CIPI	Random	Common Anode	-40 to 85	28 Ld PDIP	E28.6
ICM7228CIPIZ (Note)	ICM7228CIPI	Random	Common Anode	-40 to 85	28 Ld PDIP (Pb-free)	E28.6

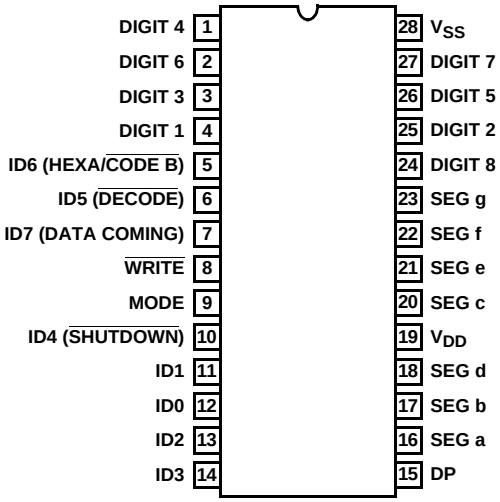
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

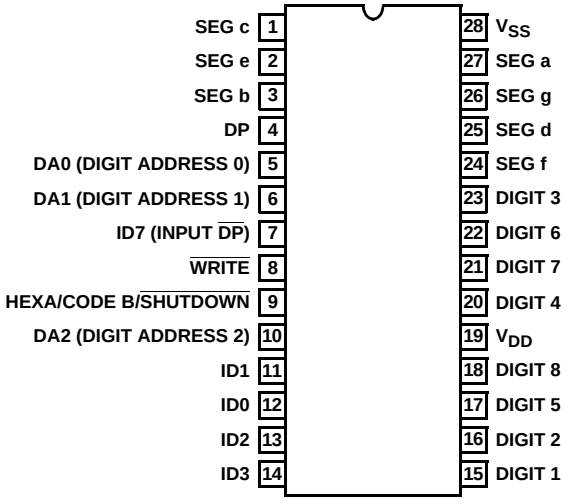
ICM7228A (PDIP, SOIC)
COMMON ANODE
TOP VIEW



ICM7228B (PDIP, SOIC)
COMMON CATHODE
TOP VIEW

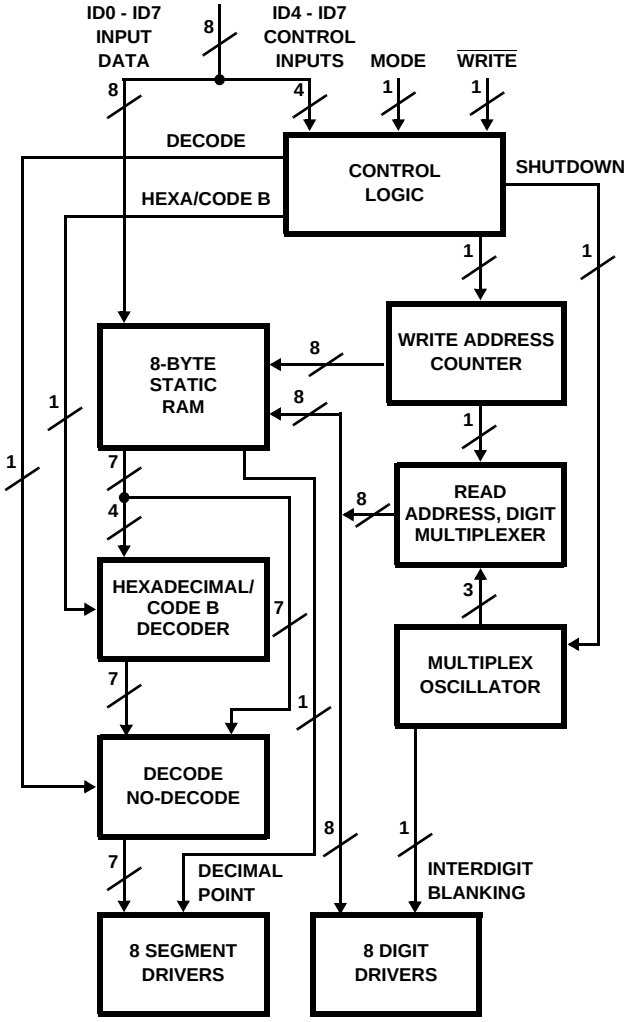


ICM7228C (PDIP, SOIC)
COMMON ANODE
TOP VIEW

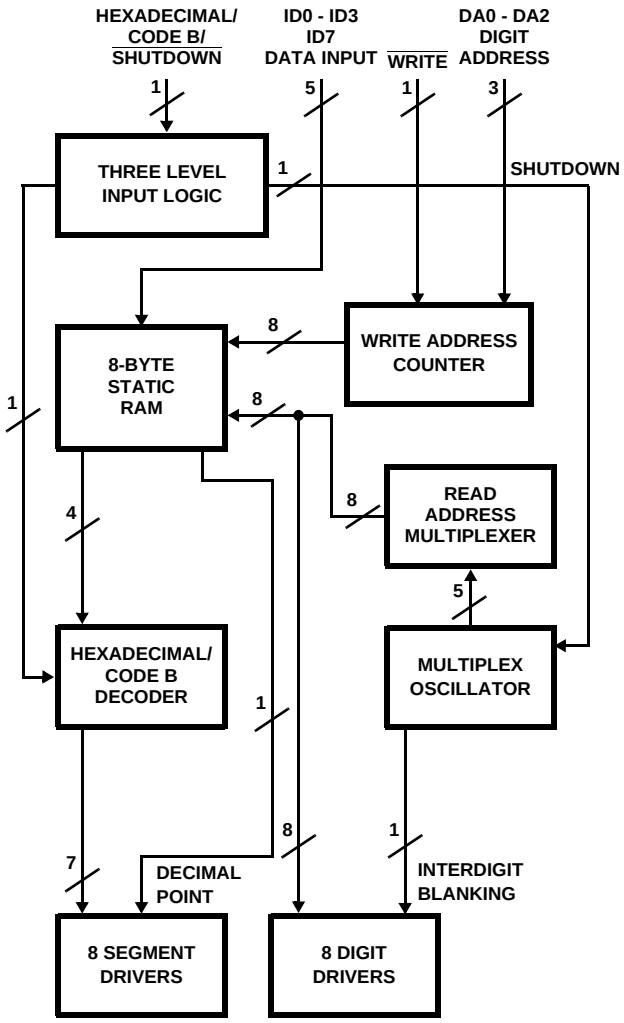


Functional Block Diagram

ICM7228A, ICM7228B



ICM7228C



Absolute Maximum Ratings

Supply Voltage (V_{DD} - V_{SS}) 6V
Digit Output Current 500mA
Segment Output Current 100mA
Input Voltage (Note 1) (Any Terminal) . . (V_{SS}-0.3V)<V_{IN}<(V_{DD}+0.3V)

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package*	55
SOIC Package	75

Maximum Junction Temperature . . . . . .150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .300°C
(SOIC - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less then V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs row sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM7228 should be turned on first.
2. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief 379 for details.

Electrical Specifications

V_{DD} = +5.0V ±10%, V_{SS} = 0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	T_A = 25°C			-40°C TO 85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage Range, V_{SUPPLY}	Operating	4	-	6	4	-	6	V
	Power Down Mode	2	-	-	2	-	-	
Quiescent Supply Current, I_Q	Shutdown, ICM7228A, IMC7228B	-	1	100	-	1	100	µA
	Shutdown, 7228C	-	2.5	100	-	2.5	100	
Operating Supply Current, I_{DD}	Common Anode, ICM7228A/C Segments = ON; Outputs = OPEN	-	200	450	-	200	450	µA
	Common Anode, ICM7228A/C Segments = OFF; Outputs = OPEN	-	100	450	-	100	450	
	Common Cathode, ICM7228B Segments = ON; Outputs = OPEN	-	250	450	-	250	450	
	Common Cathode, ICM7228B Segments = OFF; Outputs = OPEN	-	175	450	-	175	450	
Digit Drive Current, I_{DIG}	Common Anode, ICM7228A/C V_{OUT} = V_{DD} - 2.0V	200	-	-	175	-	-	mA
	Common Cathode, ICM7228B V_{OUT} = V_{SS} + 1.0V	50	-	-	40	-	-	
Digit Leakage Current, I_{DLK}	Shutdown Mode, V_{OUT} = 2.0V Common Anode, ICM7228A/C	-	1	100	-	1	100	µA
	Shutdown Mode, V_{OUT} = 5.0V Common Cathode, 7228B	-	1	100	-	1	100	
Peak Segment Drive Current, I_{SEG}	Common Anode, ICM7228A/C V_{OUT} = V_{SS} + 1.0V	20	25	-	20	-	-	mA
	Common Cathode, 7228B V_{OUT} = V_{DD} - 2.0V	10	12	-	10	-	-	
Segment Leakage Current, I_{SLK}	Shutdown Mode, V_{OUT} = V_{DD} Common Anode, ICM7228A/C	-	1	50	-	1	50	µA
	Shutdown Mode, V_{OUT} = V_{SS} Common Cathode, ICM7228B	-	1	50	-	1	50	

Electrical Specifications V_{DD} = +5.0V ±10%, V_{SS} = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	$T_A = 25^oC$			-40^oC TO 85^oC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Leakage Current, I_{IL}	All Inputs Except Pin 9, ICM7228C, $V_{IN} = V_{SS}$	-	-	1	-	-	1	µA
	All Inputs Except Pin 9, ICM7228C, V_{IN} = 5.0V	-	-	-1	-	-	-1	
Display Scan Rate, f_{MUX}	Per Digit	-	390	-	-	390	-	Hz
Inter-Digit Blanking Time, t_{IDB}		2	10	-	2	-	-	µs
Logical “1” Input Voltage, V_{INH}	Three Level Input: Pin 9 ICM7228C, Hexadecimal V_{DD} = 5V	4.2	-	-	4.2	-	-	V
Floating Input, V_{INF}	Three Level Input: Pin 9 ICM7228C, Code B, V_{DD} = 5V	2.0	-	3.0	2.0	-	3.0	V
Logical “0” Input Voltage, V_{INL}	Three Level Input: Pin 9 ICM7228C, Shutdown, V_{DD} = 5V	-	-	0.8	-	-	0.8	V
Three Level Input Impedance, Z_{IN}	V_{CC} = 5V, Pin 9 of ICM7228C	50	-	-	50	-	-	kΩ
Logical “1” Input Voltage, V_{IH}	All Inputs Except, Pin 9 of ICM7228C, V_{DD} = 5V	2.0	-	-	2.0	-	-	V
Logical “0” Input Voltage, V_{IL}	All Inputs Except, Pin 9 of ICM7228C, V_{DD} = 5V	-	-	0.8	-	-	0.8	V
SWITCHING SPECIFICATIONS V_{DD} = +5.0V ±10%, V_{SS} = 0V, V_{IL} = +0.4V, V_{IH} = +2.4V								
Write Pulsewidth (Low), t_{WL}		200	100	-	250	-	-	ns
Write Pulsewidth (High), t_{WH}		850	540	-	1200	-	-	ns
Mode Hold Time, t_{MH}	ICM7228A, ICM7228B	0	-65	-	0	-	-	ns
Mode Setup Time, t_{MS}	ICM7228A, ICM7228B	250	150	-	250	-	-	ns
Data Setup Time, t_{DS}		250	160	-	250	-	-	ns
Data Hold Time, t_{DH}		0	-60	-	0	-	-	ns
Digit Address Setup Time, t_{AS}	ICM7228C	250	110	-	250	-	-	ns
Digit Address Hold Time, t_{AH}	ICM7228C	0	-60	-	0	-	-	ns

Timing Diagrams

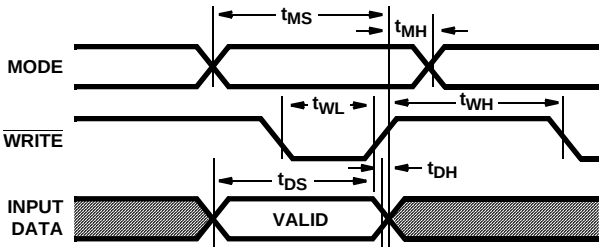


FIGURE 1. ICM7228A/B WRITE CYCLE

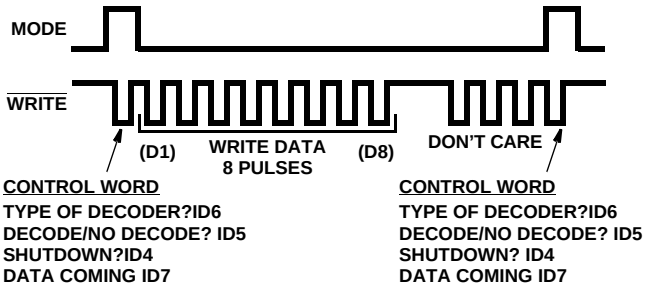


FIGURE 2. ICM7228A/B SEQUENTIAL 8-DIGIT RAM UPDATE

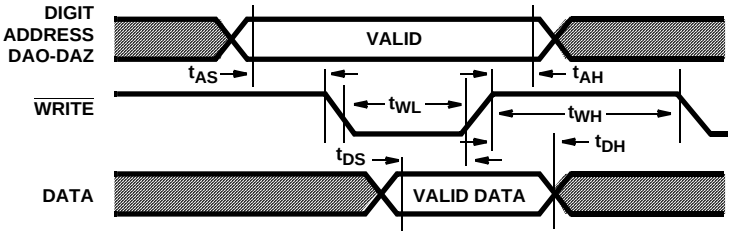


FIGURE 3. ICM7228C WRITE CYCLE

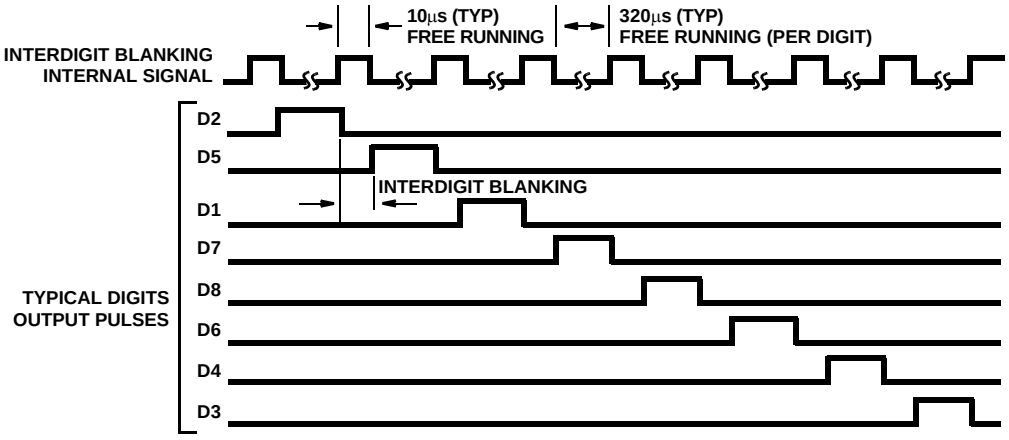


FIGURE 4. DISPLAY DIGITS MULTIPLEX (COMMON ANODE DISPLAY)

Typical Performance Curves

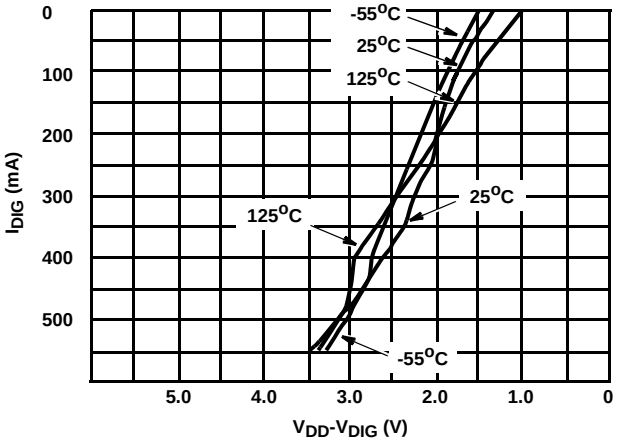


FIGURE 5. COMMON ANODE DIGIT DRIVER I_{DIG} vs (V_{DD} - V_{DIG})

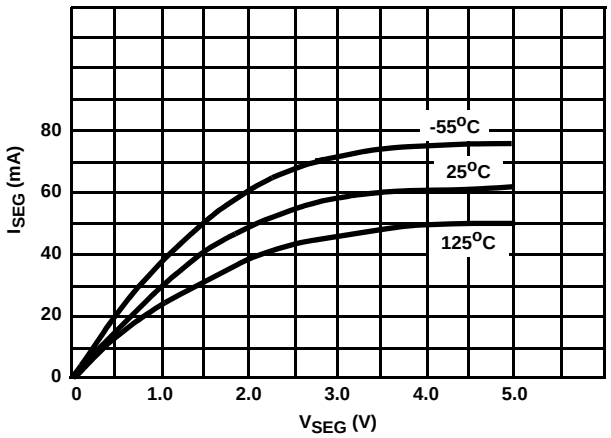


FIGURE 6. COMMON ANODE SEGMENT DRIVER I_{SEG} vs V_{SEG}

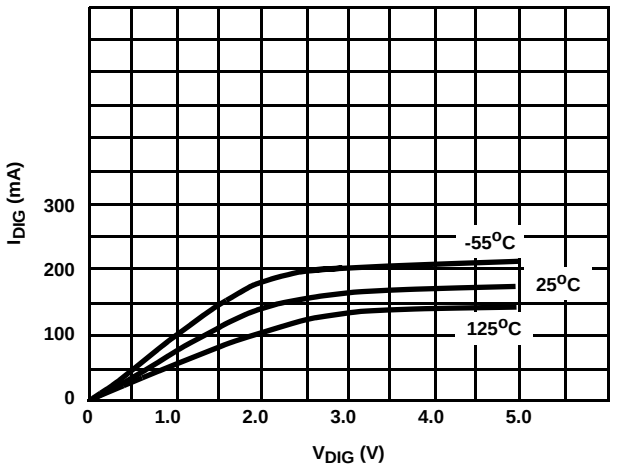


FIGURE 7. COMMON CATHODE DIGIT DRIVER I_{DIG} vs V_{DIG}

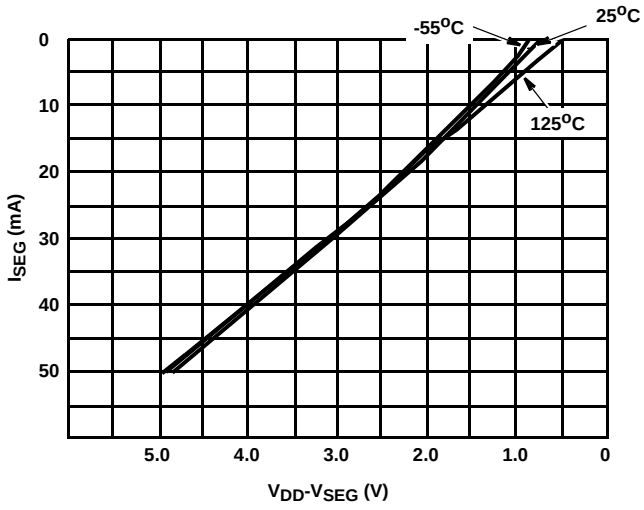


FIGURE 8. COMMON CATHODE SEGMENT DRIVER I_{SEG} vs (V_{DD} - V_{SEG})

TABLE 1. ICM7228A PIN ASSIGNMENTS AND DESCRIPTIONS

PIN NO.	NAME	FUNCTION	DESCRIPTION
1	SEG c	Output	LED Display Segments c, e, b and Decimal Point Drive Lines.
2	SEG e		
3	SEG b		
4	DP		
5	ID6, (HEXA/$\overline{\text{CODE B}}$)	Input	When “MODE” Low: Display Data Input, Bit 7. When “MODE” High: Control Bit, Decoding Scheme Selection: High, Hexadecimal Decoding; Low, Code B Decoding.
6	ID5, ($\overline{\text{DECODE}}$)	Input	When “MODE” Low: Display Data Input, Bit 6. When “MODE” High: Control Bit, Decode/No Decode Selection: High, No Decode; Low, Decode.
7	ID7, (DATA COMING)	Input	When “MODE” Low: Display Data Input, Bit 8, Decimal Point Data. When “MODE” High: Control Bit, Sequential Data Update Select: High, Data Coming; Low, No Data Coming.
8	$\overline{\text{WRITE}}$	Input	Data Input Will Be Written to Control Register or Display RAM on Rising Edge of WRITE.

TABLE 1. ICM7228A PIN ASSIGNMENTS AND DESCRIPTIONS (Continued)

PIN NO.	NAME	FUNCTION	DESCRIPTION
9	MODE	Input	Selects Data to Be Loaded to Control Register or Display RAM: High, Loads Control Register; Low, Loads Display RAM.
10	ID4, ($\overline{\text{SHUTDOWN}}$)	Input	When “MODE” Low: Display Data Input, Bit 5. When “MODE” High: Control Bit, Low Power Mode Select: High, Normal Operation; Low, Oscillator and Display Disabled.
11	ID1	Input	When “MODE” Low: Display Data Input, Bit 2. When “MODE” High and “ID7 (DATA COMING)” Low: Digit Address, Bit 2, Single Digit Update Mode.
12	ID0	Input	When “MODE” Low: Display Data Input, Bit 1. When “MODE” High and “ID7 (DATA COMING)” Low: Digit Address, LSB, Single Digit Update Mode.
13	ID2	Input	When “MODE” Low: Display Data Input, Bit 3. When “MODE” High and “ID7 (DATA COMING)” Low: Digit Address, MSB, Single Digit Update Mode.
14	ID3	Input	When “MODE” Low: Display Data Input, Bit 4. When “MODE” High: RAM Bank Select (Decode Modes Only): High, RAM Bank A; Low, RAM Bank B
15	DIGIT 1	Output	LED Display Digits 1, 2, 5 and 8 Drive Lines.
16	DIGIT 2		
17	DIGIT 5		
18	DIGIT 8		
19	V_{DD}	Supply	Device Positive Power Supply Rail.
20	DIGIT 4	Output	LED Display Digits 4, 7, 6 and 3 Drive Lines.
21	DIGIT 7		
22	DIGIT 6		
23	DIGIT 3		
24	SEG f	Output	LED Display Segments f, d, g and a Drive Lines.
25	SEG d		
26	SEG g		
27	SEG a		
28	V_{SS}	Supply	Device Ground or Negative Power Supply Rail.

TABLE 2. ICM7228B PIN ASSIGNMENTS AND DESCRIPTIONS

PIN NO.	NAME	FUNCTION	DESCRIPTION
1	DIGIT 4	Output	LED Display Digits 4, 6, 3 and 1 Drive Lines.
2	DIGIT 6		
3	DIGIT 3		
4	DIGIT 1		
5	ID6, (HEXA/$\overline{\text{CODE B}}$)	Input	When “MODE” Low: Display Data Input, Bit 7. When “MODE” High: Control Bit, Decoding Scheme Selection: High, Hexadecimal Decoding; Low, Code B Decoding.
6	ID5, ($\overline{\text{DECODE}}$)	Input	When “MODE” Low: Display Data Input, Bit 6. When “MODE” High: Control Bit, Decode/No Decode Selection: High, No Decode; Low, Decode.
7	ID7, (DATA COMING)	Input	When “MODE” Low: Display Data Input, Bit 8, Decimal Point Data. When “MODE” High: Control Bit, Sequential Data Update Select: High, Data Coming; Low, No Data Coming.

TABLE 2. ICM7228B PIN ASSIGNMENTS AND DESCRIPTIONS (Continued)

PIN NO.	NAME	FUNCTION	DESCRIPTION
8	$\overline{\text{WRITE}}$	Input	Data Input Will Be Written to Control Register or Display RAM on Rising Edge of WRITE.
9	MODE	Input	Selects Data to Be Loaded to Control Register or Display RAM: High, Loads Control Register; Low, Loads Display RAM.
10	ID4, ($\overline{\text{SHUTDOWN}}$)	Input	When “MODE” Low: Display Data Input, Bit 5. When “MODE” High: Control Bit, Low Power Mode Select: High, Normal Operation; Low, Oscillator and Display Disabled.
11	ID1	Input	When “MODE” Low: Display Data Input, Bit 2. When “MODE” High and “ID7 (DATA COMING)” Low: Digit Address, Bit 2, Single Digit Update Mode.
12	ID0	Input	When “MODE” Low: Display Data Input, Bit 1. When “MODE” High and “ID7 (DATA COMING)” Low: Digit Address, LSB, Single Digit Update Mode.
13	ID2	Input	When “MODE” Low: Display Data Input, Bit 3. When “MODE” High and “ID7 (DATA COMING)” Low: Digit Address, MSB, Single Digit Update Mode.
14	ID3	Input	When “MODE” Low: Display Data Input, Bit 4. When “MODE” High: RAM Bank Select (Decode Modes Only): High, RAM Bank A; Low, RAM Bank B.
15	DP	Output	LED Display Decimal Point and Segments a, b, and d Drive Lines
16	SEG a		
17	SEG b		
18	SEG d		
19	V_{DD}	Supply	Device Positive Power Supply Rail.
20	SEG c	Output	LED Display Segments c, e, f and g Drive Lines.
21	SEG e		
22	SEG f		
23	SEG g		
24	DIGIT 8	Output	LED Display Digits 8, 2, 5 and 7 Drive Lines.
25	DIGIT 2		
26	DIGIT 5		
27	DIGIT 7		
28	V_{SS}	Supply	Device Ground or Negative Power Supply Rail.

TABLE 3. ICM7228C PIN ASSIGNMENTS AND DESCRIPTIONS

PIN NO.	NAME	FUNCTION	DESCRIPTION
1	SEG c	Output	LED Display Segments c, e, band Decimal Point Drive Lines.
2	SEG e		
3	SEG b		
4	DP		
5	DA0	Input	Digit Address Input, Bit 1 LSB.
6	DA1	Input	Digit Address Input, Bit 2.
7	ID7, (INPUT $\overline{\text{DP}}$)	Input	Display Decimal Point Data Input, Negative True.
8	$\overline{\text{WRITE}}$	Input	Data Input Will Be Written to Display RAM on Rising Edge of $\overline{\text{WRITE}}$.

TABLE 3. ICM7228C PIN ASSIGNMENTS AND DESCRIPTIONS (Continued)

PIN NO.	NAME	FUNCTION	DESCRIPTION
9	HEXA/CODE B/SHUTDOWN	Input	Three Level Input. Display Function Control: High, Hexadecimal Decoding; Float, Code B Decoding; Low, Oscillator, and Display Disabled.
10	DA2	Input	Digit Address Input, Bit 3, MSB.
11	ID1	Input	Display Data Inputs.
12	ID0		
13	ID2		
14	ID3		
15	DIGIT 1	Output	LED Display Digits 1, 2, 5 and 8 Drive Lines.
16	DIGIT 2		
17	DIGIT 5		
18	DIGIT 8		
19	V_{DD}	Supply	Device Positive Power Supply Rail.
20	DIGIT 4	Output	LED Display Digits 4, 7, 6 and 3 Drive Lines.
21	DIGIT 7		
22	DIGIT 6		
23	DIGIT 3		
24	SEG f	Output	LED Display Segments f, d, g and a Drive Lines.
25	SEG d		
26	SEG g		
27	SEG a		
28	V_{SS}	Supply	Device Ground or Negative Power Supply Rail.

Detailed Description

System Interfacing and Data Entry Modes, ICM7228A and ICM7228B

The ICM7228A/B devices are compatible with the architectures of most microprocessor systems. Their fast switching characteristics makes it possible to access them as a memory mapped I/O device with no wait state necessary in most microcontroller systems. All the ICM7228A/B inputs, including MODE, feature a 250ns minimum setup and 0ns hold time with a 200ns minimum $\overline{\text{WRITE}}$ pulse. Input logic levels are TTL and CMOS compatible. Figure 9 shows a generic method of driving the ICM7228A/B from a microprocessor bus. To the microprocessor, each device appears to be 2 separate I/O locations; the Control Register and the Display RAM. Selection between the two is accomplished by the MODE input driven by address line A0. Input data is placed on the lD0 - lD7 lines. The $\overline{\text{WRITE}}$ input acts as both a device select and write cycle timing pulse. See Figure 1 and Switching Specifications Table for write cycle timing parameters.

The ICM7228A/B have three data entry modes: Control Register update without RAM update, sequential 8-digit update and single digit update. In all three modes a control word is first written by pulsing the WRITE input while the MODE input is high, thereby latching data into the Control Register. The logic level of individual bits in the Control Register select Shutdown, Decode/No Decode, Hex/Code B, RAM bank A/B and Display RAM digit address as shown in Tables 1 and 2.

The ICM7228A/B Display RAM is divided into 2 banks, called bank A and B. When using the Hexadecimal or code B display modes, these RAM banks can be selected separately. This allows two separate sets of display data to be stored and displayed alternately. Notice that the RAM bank selection is not possible in No-Decode mode, this is because the display data in the No-Decode mode has 8 bits, but in Decoded schemes (Hex/Code B) is only 4 bits (lD0 - lD3 data). It should also be mentioned that the decimal point is independent of selected bank, a turned on decimal point will remain on for either bank. Selection of the RAM banks is controlled by lD3 input. The lD3 logic level (during Control Register update) selects which bank of the internal RAM to be written to and/or displayed.

Control Register Update without RAM Update

The Control Register can be updated without changing the display data by a single pulse on the WRITE input, with MODE high and DATA COMING low. If the display is being decoded (Hex/Code B), then the value of lD3 determines which RAM bank will be selected and displayed for all eight digits.

Sequential 8-Digit Update

The logic state of DATA COMING (ID7) is also latched during a Control Register update. If the latched value of DATA COMING (ID7) is high, the display becomes blanked and a sequential 8-digit update is initiated. Display data can now be written into RAM with 8 successive WRITE pulses, starting with digit 1 and ending with digit 8 (See Figure 2). After all 8 RAM locations have been written to, the display turns on again and the new data is displayed. Additional write pulses are ignored until a new Control Register update is performed. All 8 digits are displayed in the format (Hex/Code B or No Decode) specified by the control word that preceded the 8 digit update. If a decoding scheme (Hex/Code B) is to be used, the value of ID3 during the control word update determines which RAM bank will be written to.

Single Digit Update

In this mode each digit data in the display RAM can be updated individually without changing the other display data. First, with MODE input high, a control word is written to the Control Register carrying the following information; DATA COMING (ID7) low, the desired display format data on ID4 - ID6, the RAM bank selected by ID3 (if decoding is selected) and the address of the digit to be updated on data lines ID0 - ID2 (See Table 4). A second write to the ICM7228A/B, this time with MODE input low, transfers the data at the ID0 - ID7 inputs into the selected digit's RAM location. In single digit update mode, each individual digit's data can be specified independently for being displayed in Decoded or No-Decode mode. For those digits which decoding scheme (Hex/Code B) is selected, only one can be effective at a time. Whenever a control word is written, the specified decoding scheme will be applied to all those digits which selected to be displayed in Decoded mode.

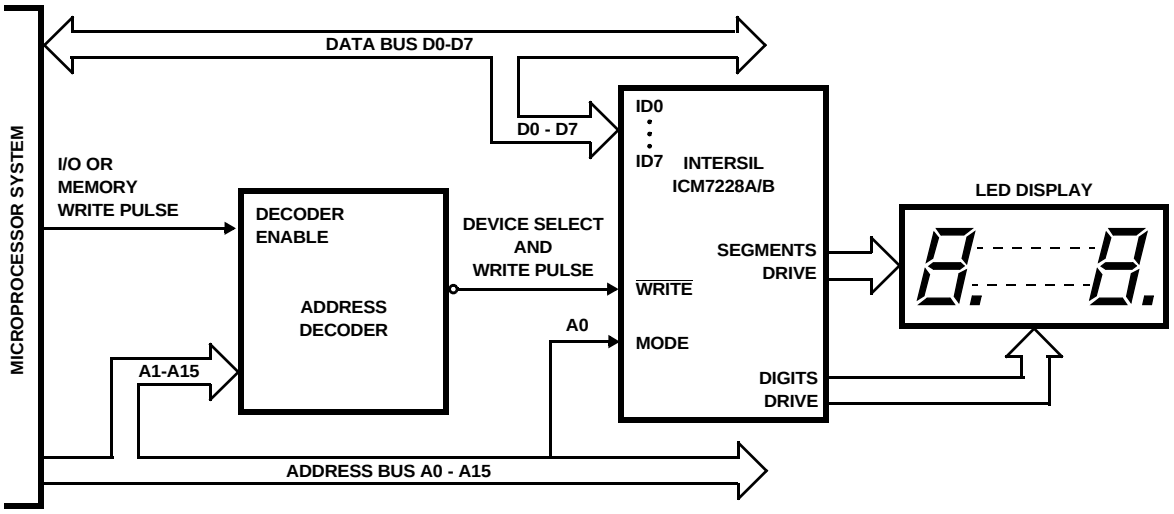


FIGURE 9. ICM7228A/B MICROPROCESSOR SYSTEM INTERFACING

TABLE 4. DIGITS ADDRESS, ICM7228A/B

INPUT DATA LINES			
1D2	ID2	ID0	SELECTED DIGIT
0	0	0	DIGIT 1
0	0	1	DIGIT 2
0	1	0	DIGIT 3
0	1	1	DIGIT 4
1	0	0	DIGIT 5
1	0	1	DIGIT 6
1	1	0	DIGIT 7
1	1	1	DIGIT 8

System Interfacing, ICM7228C

The ICM7228C is directly compatible with the architecture of most microprocessor systems. Its fast switching characteristics make it possible to access them as a memory mapped I/O device with no wait state necessary in most microcontroller systems. All the ICM7228C inputs, excluding HEXA/CODE B/SHUTDOWN, feature a 250ns minimum setup and 0ns hold time with a 200ns minimum WRITE pulse. Input logic levels are TTL and CMOS compatible. Figure 10 shows a generic method of driving the ICM7228C from a microprocessor bus. To the microprocessor, the 8 bytes of the Display RAM appear to be 8 separate I/O locations. Loading the ICM7228C is quite similar to a standard memory write cycle. The address of the digit to be updated is placed on lines DA0 - DA2, the data to be written is placed on lines ID0 - ID3 and ID7, then a low pulse on WRITE input will transfer the data in. See Figure 3 and Switching Characteristics Table for write cycle timing parameters.

The ICM7228C does not have any control register, and also does not provide the No Decode display format. Hexadecimal or Code B character selection and shutdown mode are directly controlled through the three level input at Pin 9, which is accordingly called HEXA/CODE B/$\overline{\text{SHUTDOWN}}$. See Table 3 for input and output definitions of the ICM7228C.

Display Formats

The ICM7228A and ICM7228B have three possible display formats; Hexadecimal, Code B and No Decode. Table 5 shows the character sets for the decode modes and their corresponding input code.

The display formats of the ICM7228A/B are selected by writing data to bits ID4, ID5 and ID6 of the Control Register (See Table 1 and 2 for input Definitions). Hexadecimal and Code B data is entered via ID0-lD3 and ID7 controls the decimal point.

TABLE 5. DISPLAY CHARACTER SETS

INPUT DATA CODE			DISPLAY CHARACTERS		
ID3	ID2	ID1	ID0	HEXADECIMAL	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2

TABLE 5. DISPLAY CHARACTER SETS (Continued)

INPUT DATA CODE			DISPLAY CHARACTERS		
ID3	ID2	ID1	ID0	HEXADECIMAL	CODE B
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(Blank)

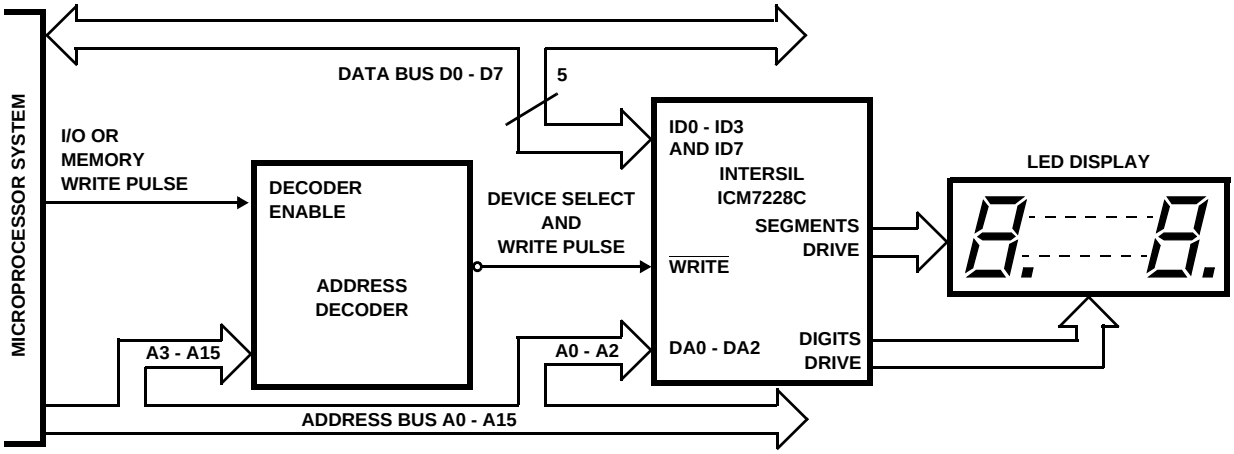


FIGURE 10. ICM7228C MICROPROCESSOR SYSTEM INTERFACING

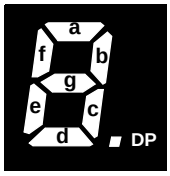


FIGURE 11. DIGITS SEGMENT ASSIGNMENTS

The No Decode mode of the ICM7228A and ICM7228B allows the direct segment-by-segment control of all 64 segments driven by the device. In the No Decode mode, the input data directly control the outputs as shown in Table 6.

TABLE 6. NO DECODE SEGMENT LOCATIONS

DATA INPUT	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Controlled Segment	Decimal Point	a	b	c	e	g	f	d

An input high level turns on the respective segment, except for the decimal point, which is turned on by an input low level on ID7.

The No Decode mode can be used in different applications such as bar graph or status panel driving where each segment controls an individual LED.

The ICM7228C has only the Hexadecimal and Code B character sets. The HEXA/CODE B/$\overline{\text{SHUTDOWN}}$ input, pin 9, requires a three level input. Pin 9 selects the Hexadecimal format when pulled high, the Code B format when floating or driven to mid-supply, and the shutdown mode when pulled low (See Table 3). Table 5 also applies to the ICM7228C.

Shutdown and Display Banking

When shutdown, the ICM7228 enters a low power standby mode typically consuming only 1μA of supply current for the ICM7228A/B and 2.5μA for the ICM7228C. In this mode the ICM7228 turns off the multiplex scan oscillator as well as the digit and segment drivers. However, input data can still be

entered when in the shutdown mode. Data is retained in memory even with the supply voltage as low as 2V.

The ICM7228A/B is shutdown by writing a control word with Shutdown (ID4) low. The ICM7228C is put into shutdown mode by driving pin 9, HEXA/CODE B/$\overline{\text{SHUTDOWN}}$, low.

The ICM7228 operating current with the display blanked is within 100μA - 200μA for all versions. All versions of the ICM7228 can be blanked by writing Hex FF to all digits and selecting Code B format. The ICM7228A and ICM7228B can also be blanked by selecting No Decode mode and writing Hex 80 to all digits (See Tables 5and 6).

Common Anode Display Drivers, ICM7228A and ICM7228C

The common anode digit and segment driver output schematics are shown in Figure 12. The common anode digit driver output impedance is approximately 4Ω. This provides a nearly constant voltage to the display digits. Each digit has a minimum of 200mA drive capability. The N-Channel segment driver's output impedance of 50Ω limits the segment current to approximately 25mA peak current per segment. Both the segment and digit outputs can directly drive the display, current limiting resistors are not required.

Individual segment current is not significantly affected by whether other segments are on or off. This is because the segment driver output impedance is much higher than that of the digit driver. This feature is important in bar graph applications where each bar graph element should have the same brightness, independent of the number of elements being turned on.

Common Cathode Display Driver, ICM7228B

The common cathode digit and segment driver output schematics are shown in Figure 13. The N-channel digit drivers have an output impedance of approximately 15Ω. Each digit has a minimum of 50mA drive capability. The segment drivers have an output impedance of approximately 100Ω with typically 10mA peak current drive for each segment. The common cathode display driver output currents are only $^1/_4$ of the common anode display driver currents. Therefore, the ICM7228A and ICM7228C common anode display drivers are recommended for those applications where high display brightness is desired. The ICM7228B common cathode display driver is suitable for driving bubble-lensed monolithic 7 segment displays. They can also drive individual LED displays up to 0.3 inches in height when high brightness is not required.

Display Multiplexing

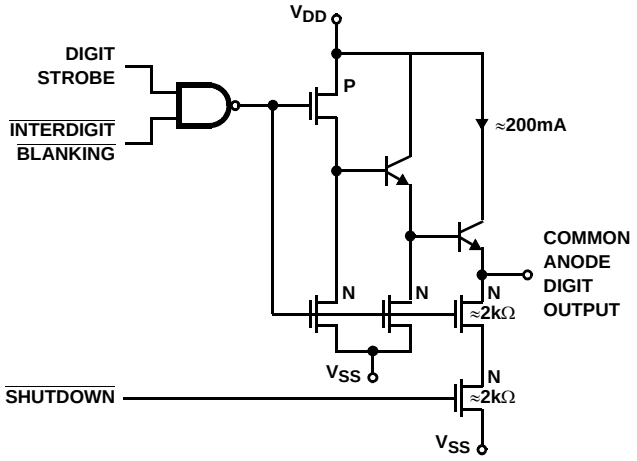
Each digit of the ICM7228 is on for approximately 320μs, with a multiplexing frequency of approximately 390Hz. The ICM7228 display drivers provide interdigit blanking. This ensures that the segment information of the previous digit is gone and the information of the next digit is stable before the next digit is driven on. This is necessary to eliminate display ghosting (a faint display of data from previous digit superimposed on the next digit). The interdigit blanking time is 10μs typical with a guaranteed 2μs minimum. The ICM7228 turns off both the digit drivers and the segment drivers during the interdigit blanking period. The digit multiplexing sequence is: D2, D5, D1, D7, D8, D6, D4 and D3. A typical digit's drive pulses are shown on Figure 4.

Due to the display multiplexing, the driving duty cycle for each digit is 12% (100 x $^1/_8$) This means the average current for each segment is $^1/_8$ of its peak current. This must be considered while designing and selecting the displays.

Driving Larger Displays

If very high display brightness is desired, the ICM7228 display driver outputs can be externally buffered. Figures 14 thru 16 show how to drive either common anode or common cathode displays using the ICM7228 and external driver circuit for higher current displays.

Another method of increasing display currents is to connect two digit outputs together and load the same data into both digits. This drives the display with the same peak current, but the average current doubles because each digit of the display is on for twice as long, i.e., $^1/_4$ duty cycle versus $^1/_8$.



NOTE: When SHUTDOWN goes low INTERDIGIT BLANKING also stays low.

FIGURE 12A. DIGIT DRIVER

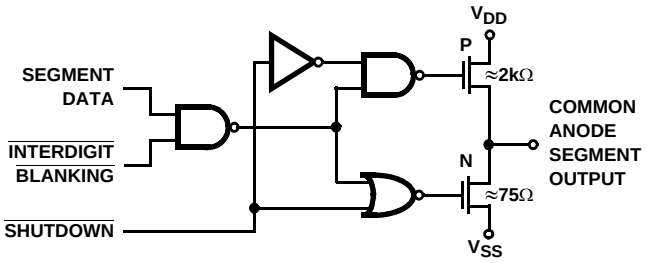


FIGURE 12B. SEGMENT DRIVER

FIGURE 12. COMMON ANODE DISPLAY DRIVERS

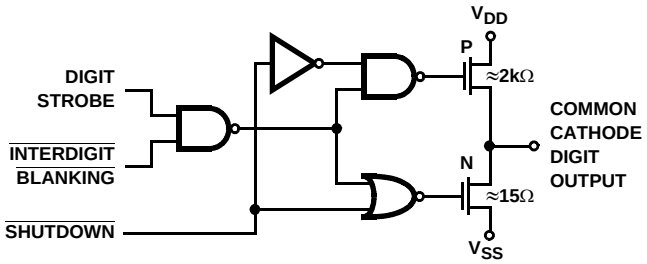
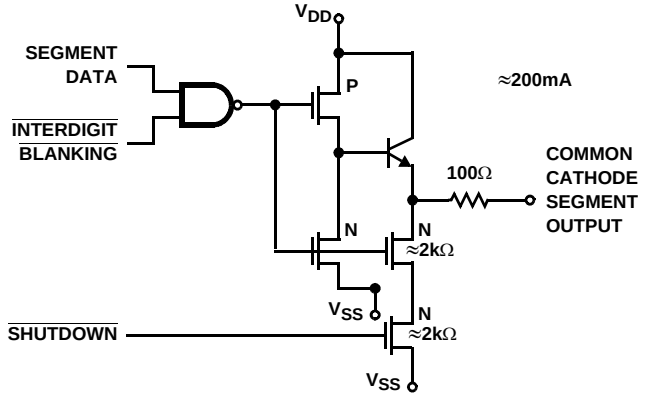


FIGURE 13A. DIGIT DRIVER



NOTE: When SHUTDOWN goes low INTERDIGIT BLANKING also stays low.

FIGURE 13B. SEGMENT DRIVER

FIGURE 13. COMMON CATHODE DISPLAY DRIVERS

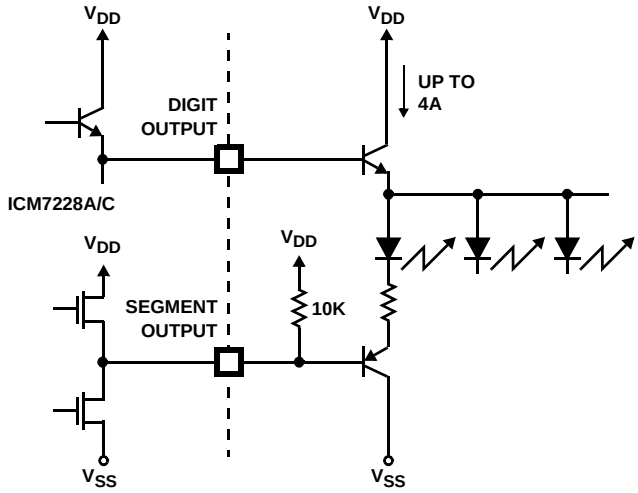


FIGURE 14. DRIVING HIGH CURRENT DISPLAY, COMMON ANODE ICM7228A/C TO COMMON ANODE

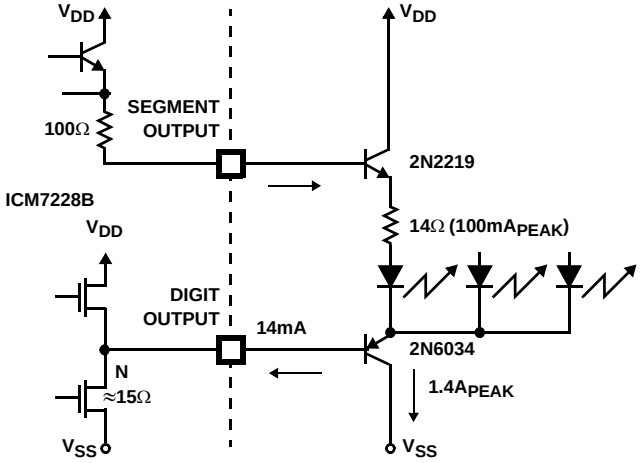


FIGURE 15. DRIVING HIGH CURRENT DISPLAY, COMMON CATHODE ICM7228B TO COMMON CATHODE DISPLAY

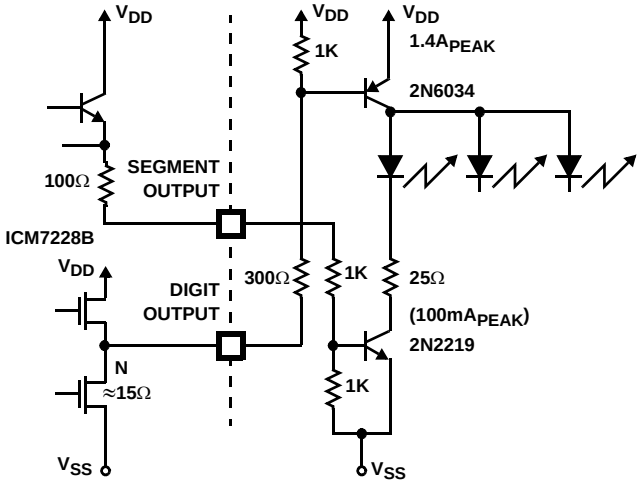


FIGURE 16. DRIVING HIGH CURRENT DISPLAY, COMMON CATHODE ICM7228B TO COMMON ANODE DISPLAY

Three Level Input, ICM7228C

As mentioned before, pin 9 is a three level input and controls three functions: Hexadecimal display decoding, Code B display decoding and shutdown mode. In many applications, pin 9 will be left open or permanently wired to one state. When pin 9 can not be permanently left in one state, the circuits illustrated in Figure 17 can be used to drive this three level input.

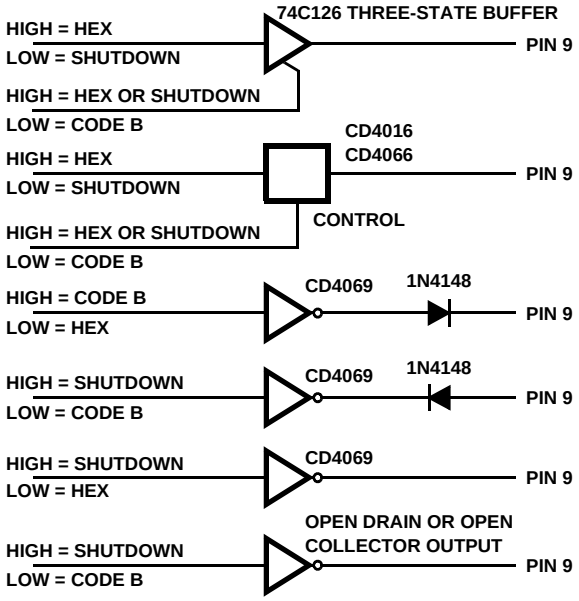


FIGURE 17. ICM7228C PIN 9 DRIVE CIRCUITS

Power Supply Bypassing

Connect a minimum of 47µF in parallel with 0.1µF capacitors between V_{DD} and V_{SS} of ICM7228. These capacitors should be placed in close proximity to the device to reduce the power supply ripple caused by the multiplexed LED display drive current pulses.

Test Circuit

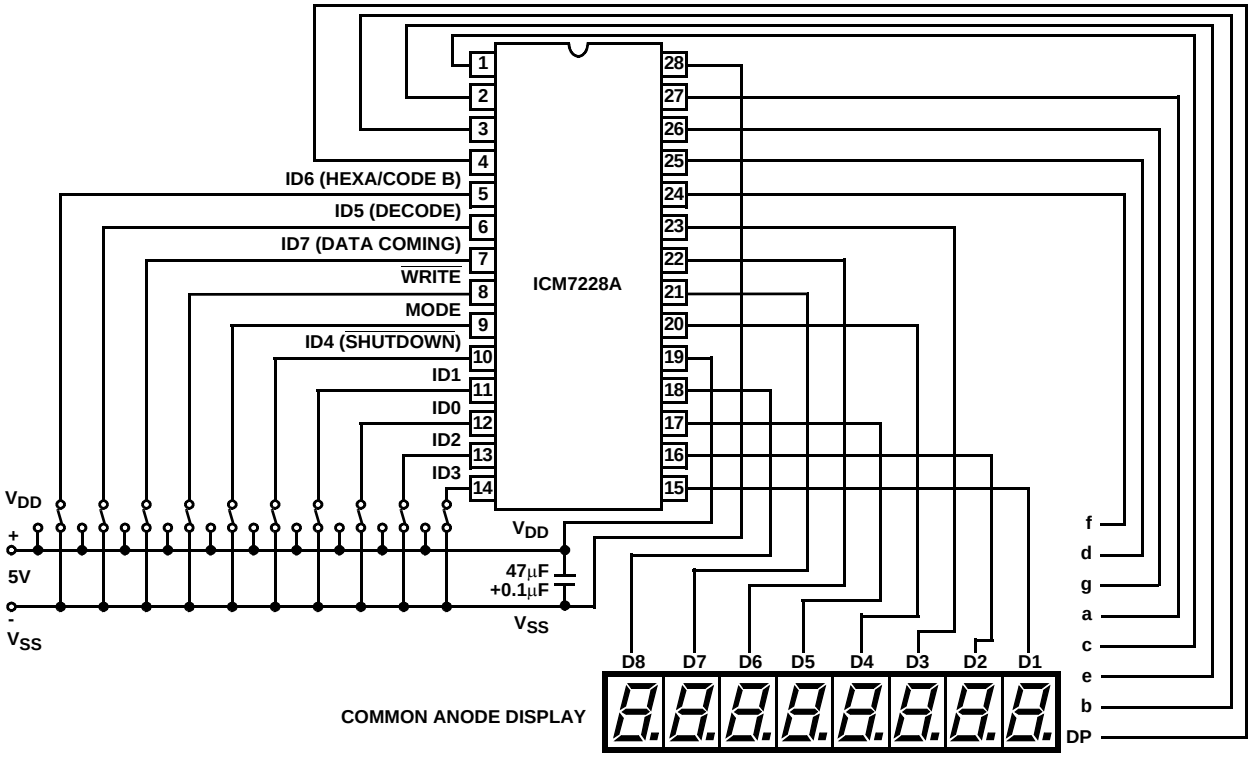
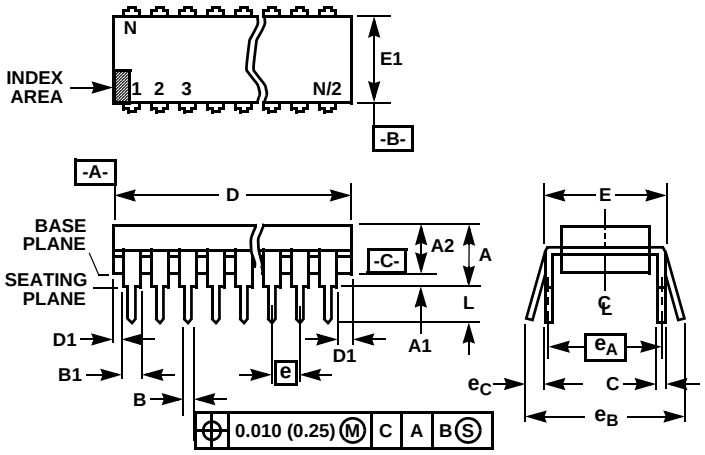


FIGURE 18. FUNCTIONAL TEST CIRCUIT #1

Dual-In-Line Plastic Packages (PDIP)



NOTES:

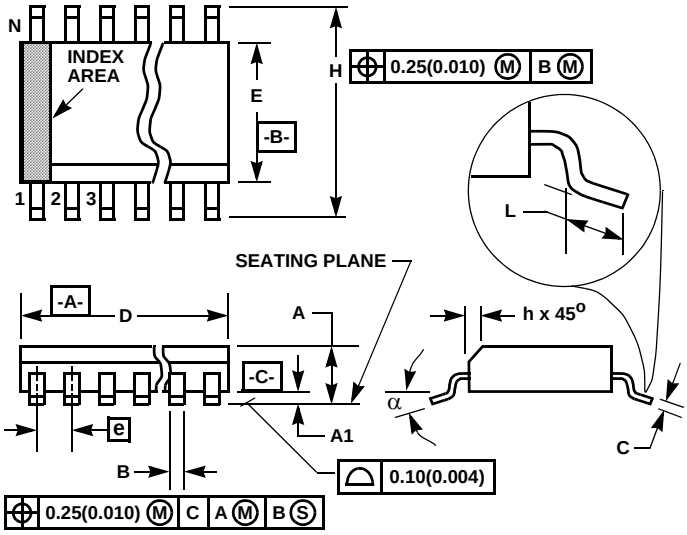
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-011-AB ISSUE B)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

Rev. 1 12/00

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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