Datasheet

PROGRAMMABLE TIMING CONTROL HUB FOR INTEL BASED SYSTEMS

9LRS3197

Recommended Application:

CK505 version 1-1 clock, with fully integrated voltage regulators and series resistors

Output Features:

- 2 - CPU differential low power push-pull pairs
- 1 - SRC differential low power push-pull pair
- 1 - SATA differential low power push-pull pair
- 1 - DOT differential low power push-pull pair
- 1 - REF, able to drive 3 loads, 14.318MHz
- 1 - 27MHz_SS/non_SS single-ended output pair

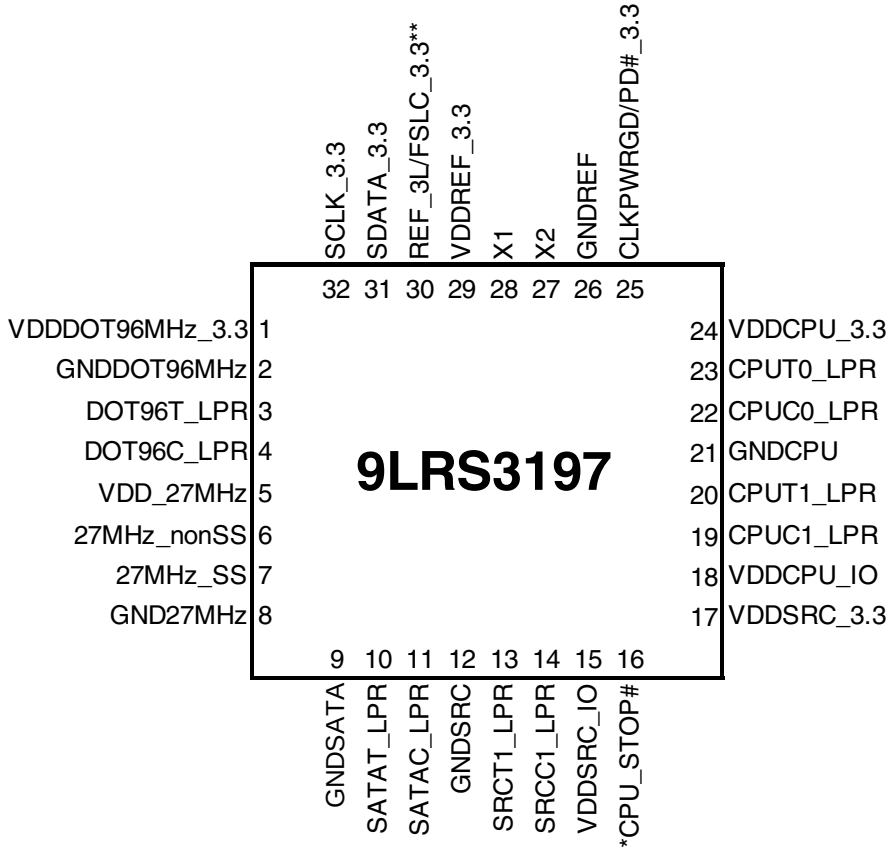
Features/Benefits:

- Supports spread spectrum modulation, 0 to -0.5% down spread for CPU and SRC clocks
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning

Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- SRC outputs cycle-cycle jitter < 125ps
- +/- 100ppm frequency accuracy on all clocks

Pin Configuration



* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

32-pin MLF

Pin Description

Pin#	Pin Name	Type	Pin Description
1	VDDDOT96MHz_3.3	PWR	Power pin for the DOT96MHz output 3.3V.
2	GNDDOT96MHz	PWR	Ground pin for the DOT96MHz output
3	DOT96T_LPR	OUT	True clock DOT96 output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
4	DOT96C_LPR	OUT	Complement clock DOT96 output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
5	VDD_27MHz	PWR	Power pin for the 27MHz output 3.3V.
6	27MHz_nonSS	OUT	27MHz non-spread output, 3.3V
7	27MHz_SS	OUT	27MHz spread output, 3.3V
8	GND27MHz	PWR	Ground pin for the 27MHz output
9	GNDSATA	PWR	Ground pin for the SATA output 3.3V.
10	SATAT_LPR	OUT	True clock of differential 0.8V push-pull SATA output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
11	SATAC_LPR	OUT	Complementary clock of differential 0.8V push-pull SATA output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
12	GNDSRC	PWR	Ground pin for the SRC outputs
13	SRCT1_LPR	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
14	SRCC1_LPR	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
15	VDDSRC_IO	PWR	1.05V to 3.3V from external power supply
16	*CPU_STOP#	IN	Stops all CPU clocks, except those set to be free running clocks
17	VDDSRC_3.3	PWR	Supply for SRC clocks, 3.3V nominal
18	VDDCPU_IO	PWR	1.05V to 3.3V from external power supply
19	CPUC1_LPR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
20	CPUT1_LPR	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
21	GNDCPU	PWR	Ground pin for the CPU outputs
22	CPUC0_LPR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
23	CPUT0_LPR	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
24	VDDCPU_3.3	PWR	Supply for CPU clocks, 3.3V nominal
25	CLKPWRGD/PD#_3.3	IN	Notifies CK505 to sample latched inputs, or iAMT entry/exit, or PWRDWN# mode
26	GNDREF	PWR	Ground pin for the REF outputs.
27	X2	OUT	Crystal output, Nominally 14.318MHz
28	X1	IN	Crystal input, Nominally 14.318MHz.
29	VDDREF_3.3	PWR	Power pin for the XTAL and REF clocks, nominal 3.3V
30	REF_3L/FSLC_3.3**	I/O	14.318 MHz reference clock, which can drive 3 loads / 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
31	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
32	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.

General Description

The **9LRS3197** is a CK505 clock synthesizer. The **9LRS3197** provides a single-chip solution for Intel based systems. The **9LRS3197** is driven with a 14.318MHz crystal.

Functional Block Diagram

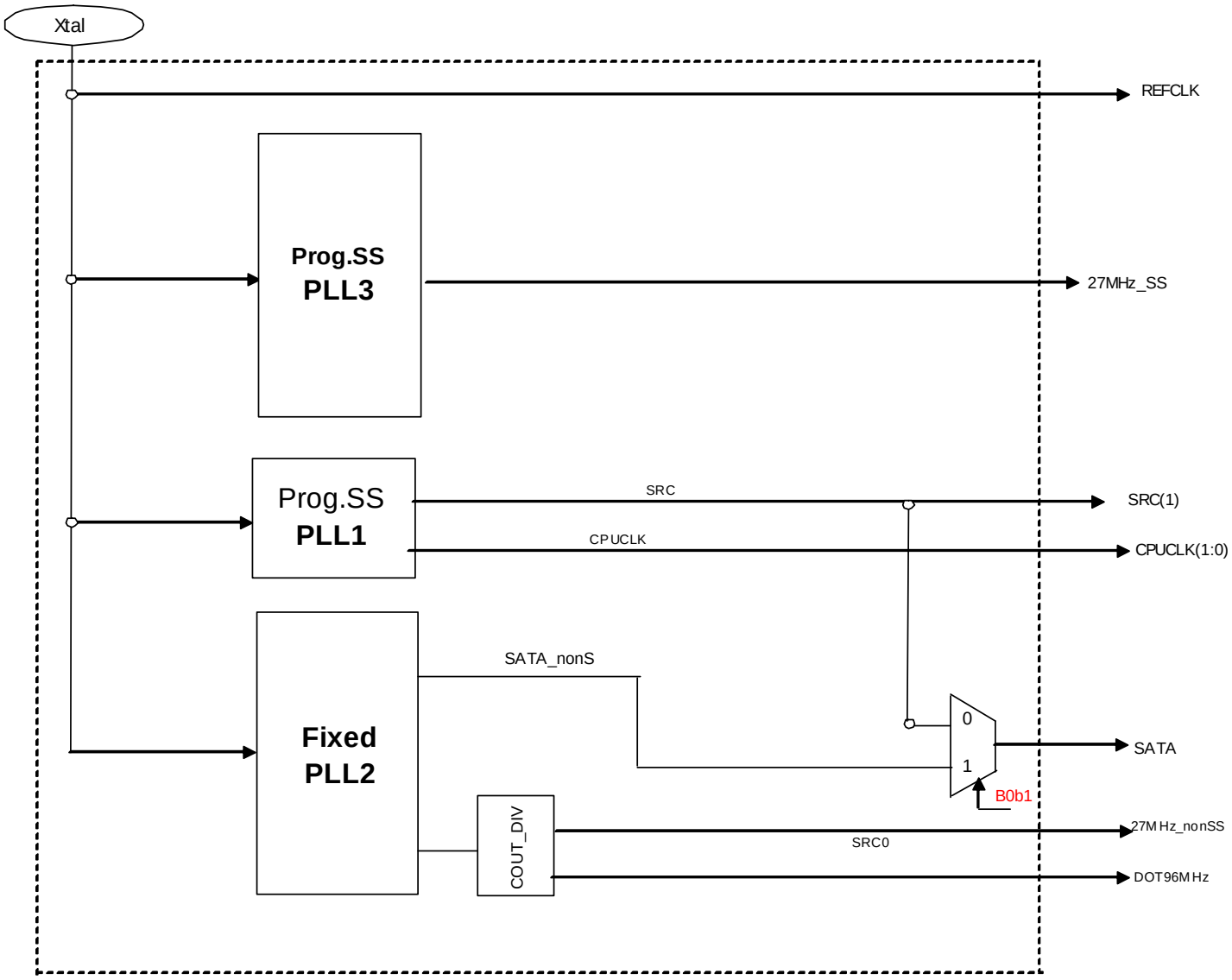


Table 1: CPU Frequency Select Table

FS_LC B0b7	CPU MHz	SRC MHz	REF MHz	DOT MHz
0 (Default)	133.33	100.00	14.318	96.00
1	100.00			

1. FS_LC is a low-threshold input.Please see V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.

Table 2: pin 6, 7 Configuration

B1b3	B1b2	B1b1	Pin 6	Pin 7	Spread	Comment
			MHz	MHz	%	
0	0	0	27MHz_nonSS	27MHz_SS	-1.75%	
0	0	1	27MHz_nonSS	27MHz_SS	+-0.5%	
0	**1**	**0**	**27MHz_nonSS**	**27MHz_SS**	**-0.5%**	**Default**
0	1	1	27MHz_nonSS	27MHz_SS	-1%	
1	0	0	27MHz_nonSS	27MHz_SS	-1.5%	
1	0	1	27MHz_nonSS	27MHz_SS	-2%	
1	1	0	27MHz_nonSS	27MHz_SS	-0.75%	
1	1	1	27MHz_nonSS	27MHz_SS	-1.25%	

IO_Vout Select Table

b2	b1	b0	IO_Vout
0	0	0	N/A
0	0	0	N/A
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	**0**	**1**	**0.8V**
1	1	0	0.9V
1	1	1	1.0V

*** Bold is default**

General SMBus serial interface information for the 9LRS3197

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the beginning byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	○		
	○		○
	○		○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			○
	○		○
	○		○
	○		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Byte 0 FS Readback and PLL Selection Register

Bit	Name	Description	Type	0	1	Default
7	FSLC	CPU Freq. Sel. Bit	R			Latch
6	Reserved	Reserved	RW	-	-	0
5	Reserved	Reserved	RW	-	-	1
4	iAMT_EN	Set via SMBus	RW (Sticky "1")	Legacy Mode	iAMT Enabled	0
3	Reserved	Reserved	RW			0
2	Reserved	Reserved	RW	Reserved	Reserved	0
1	SATA_SEL	Select source for SATA clock	RW	SATA (SRC2 100MHz_SS) = SRC_Main	SATA (100MHz non_SS) = SATA PLL	0
0	PD_Restore	1 = on Power Down de-assert return to last known state 0 = clear all SMBus configurations as if cold power-on and go to latches open state This bit is ignored and treated at '1' if device is in iAMT mode.	RW	Configuration Not Saved	Configuration Saved	1

Byte 1 DOT96 Select and PLL3 Quick Config Register,

Bit	Name	Description	Type	0	1	Default
7	Reserved	Reserved	RW	-	-	1
6	CK505 PLL1_SSC_SEL	Select 0.5% down or center SSC	RW	Down spread	Center spread	0
5	Reserved	Reserved	RW	-	-	1
4	PLL3_CF3	PLL3 Quick Config Bit 3	RW	See Table 2: pin 6/7 Configuration		0
3	PLL3_CF2	PLL3 Quick Config Bit 2	RW			0
2	PLL3_CF1	PLL3 Quick Config Bit 1	RW			1
1	PLL3_CF0	PLL3 Quick Config Bit 0	RW			0
0	Reserved	Reserved	RW	-	-	1

Byte 2 Output Enable Register

Bit	Name	Description	Type	0	1	Default
7	REF_3L_OE	Output enable for REF0, if disabled output is tri-stated	RW	Output Disabled	Output Enabled	1
6	Reserved	Reserved	RW	-	-	1
5	Reserved	Reserved	RW	-	-	1
4	Reserved	Reserved	RW	-	-	1
3	Reserved	Reserved	RW	-	-	1
2	Reserved	Reserved	RW	-	-	1
1	Reserved	Reserved	RW	-	-	1
0	Reserved	Reserved	RW	-	-	1

Byte 3 Output Enable Register

Bit	Name	Description	Type	0	1	Default
7	Reserved	Reserved	RW	-	-	1
6	Reserved	Reserved	RW	-	-	1
5	Reserved	Reserved	RW	-	-	1
4	Reserved	Reserved	RW	-	-	1
3	Reserved	Reserved	RW	-	-	1
2	Reserved	Reserved	RW	-	-	1
1	Reserved	Reserved	RW			1
0	Reserved	Reserved	RW	-	-	1

Byte 4 Output Enable and Spread Spectrum Disable Register

Bit	Name	Description	Type	0	1	Default
7	Reserved	Reserved	RW	-	-	1
6	SATA_OE	Output enable for SATA	RW	Output Disabled	Output Enabled	1
5	SRC1_OE	Output enable for SRC1	RW	Output Disabled	Output Enabled	1
4	DOT96_OE	Output enable for DOT96	RW	Output Disabled	Output Enabled	1
3	CPU1_OE	Output enable for CPU1	RW	Output Disabled	Output Enabled	1
2	CPU0_OE	Output enable for CPU0	RW	Output Disabled	Output Enabled	1
1	SSC_EN1 (MSB)	SSC_EN1 (MSB)	RW	00=All Spread OFF 01=Reserved 10=Reserved 11=All Spread ON		1
0	SSC_EN0 (LSB)	SSC_EN0 (LSB)	RW			1

Byte 5 Reserved Register

Bit	Name	Description	Type	0	1	Default
7	Reserved	Reserved	RW	-	-	1
6	Reserved	Reserved	RW	-	-	1
5	Reserved	Reserved	RW	-	-	1
4	Reserved	Reserved	RW	-	-	1
3	Reserved	Reserved	RW	-	-	1
2	Reserved	Reserved	RW	-	-	1
1	Reserved	Reserved	RW	-	-	1
0	Reserved	Reserved	RW	-	-	1

Byte 6 Slew Rate Control Register

Bit	Name	Description	Type	0	1	Default
7	Reserved	Reserved	RW	-	-	0
6	Reserved	Reserved	RW	-	-	0
5	REF Slew	Slew Rate Control	RW	2 V/ns	1 V/ns	0
4	Reserved	Reserved	RW	-	-	0
3	27MHz Slew	Slew Rate Control	RW	2 V/ns	1 V/ns	0
2	Reserved	Reserved	RW	-	-	0
1	Reserved	Reserved	RW	-	-	0
0	Reserved	Reserved	RW	-	-	0

Byte 7 Vendor ID/ Revision ID

Bit	Name	Description	Type	0	1	Default
7	Rev Code Bit 3	Revision ID	R	Vendor specific		0
6	Rev Code Bit 2		R			0
5	Rev Code Bit 1		R			0
4	Rev Code Bit 0		R			0
3	Vendor ID bit 3	Vendor ID ICS is 0001, binary	R			0
2	Vendor ID bit 2		R			0
1	Vendor ID bit 1		R			0
0	Vendor ID bit 0		R			1

Byte 8 Device ID and Output Enable Register

Bit	Name	Description	Type	0	1	Default
7	Device_ID3	Table of Device identifier codes, used for differentiating between CK505 package options, etc.	R	See Device ID Table		**1**
6	Device_ID2		R			**0**
5	Device_ID1		R			**0**
4	Device_ID0		R			**0**
3	Reserved	Reserved	RW	-	-	0
2	Reserved	Reserved	RW	-	-	0
1	27MHz_nonSS_OE	Output enable for 27MHz_nonSS	RW	Disabled	Enabled	1
0	27MHz_SS_OE	Output enable for 27MHz_SS	RW	Disabled	Enabled	1

Byte 9 Output Control Register

Bit	Name	Description	Type	0	1	Default
7	Reserved	Reserved	RW	-	-	0
6	Reserved	Reserved	**R**	-	-	0
5	Reserved	Reserved	RW	-	-	1
4	Reserved	Reserved	RW	-	-	0
3	Reserved	Reserved	RW	-	-	0
2	IO_VOUT2	IO Output Voltage Select (Most Significant Bit)	RW	See Table 3: V_IO Selection (Default is 0.8V)		1
1	IO_VOUT1	IO Output Voltage Select	RW			0
0	IO_VOUT0	IO Output Voltage Select (Least Significant Bit)	RW			1

Byte 10 Output Control Register

Bit	Name	Description	Type	0	1	Default
7	Reserved	Reserved	RW	-	-	0
6	Reserved	Reserved	RW	-	-	0
5	Reserved	Reserved	RW	-	-	0
4	Reserved	Reserved	RW	-	-	0
3	Reserved	Reserved	RW	-	-	0
2	Reserved	Reserved	RW	-	-	0
1	CPU 1 Stop Enable	Enables control of CPU1 with CPU_STOP#	RW	Free Running	Stoppable	1
0	CPU 0 Stop Enable	Enables control of CPU 0 with CPU_STOP#	RW	Free Running	Stoppable	1

Byte 11 Reserved Register

Bit	Name	Description	Type	0	1	Default
7	Reserved	Reserved	RW			0
6	Reserved	Reserved	RW			0
5	Reserved	Reserved	RW			0
4	Reserved	Reserved	RW			0
3	Reserved	Reserved	RW	-	-	0
2	CPU1_AMT_EN	M1 mode clk enable	RW	Disable	Enable	1
1	PCI-E_GEN2	Determines if PCI-E Gen2 compliant	**R**	non-Gen2	PCI-E Gen2 Compliant	1
0	Reserved	Reserved	RW	-	-	1

Byte 12 Byte Count Register

Bit	Name	Description	Type	0	1	Default
7	Reserved		RW			0
6	Reserved		RW			0
5	BC5	Read Back byte count register, max bytes = 32	RW			0
4	BC4		RW			0
3	BC3		RW			1
2	BC2		RW			1
1	BC1		RW			0
0	BC0		RW			1

Absolute Maximum Ratings - DC Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Maximum Supply Voltage	VDDxxx	Supply Voltage		4.6	V	7
Maximum Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply		3.8	V	7
Maximum Input Voltage	V_{IH}	3.3V Inputs		4.6	V	4,5,7
Minimum Input Voltage	V_{IL}	Any Input	GND - 0.5		V	4,7
Storage Temperature	Ts	-	-65	150	°C	4,7
Input ESD protection	ESD prot	Human Body Model	2000		V	6,7

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied, nor guaranteed.

[3] Maximum input voltage is not to exceed VDD

Electrical Characteristics - Input/Supply/Common Output DC Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Ambient Operating Temp	Tambient	-	0	70	°C	
Supply Voltage	VDDxxx	Supply Voltage	3.135	3.465	V	
Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply	0.9975	3.465	V	
Input High Voltage	V_{IHSE}	Single-ended 3.3V inputs	2	V_{DD} + 0.3	V	3
Input Low Voltage	V_{ILSE}	Single-ended 3.3V inputs	V_{SS} - 0.3	0.8	V	3
Low Threshold Input- FSC = '1' Voltage	V_{IH_FSC}	3.3 V +/-5%	0.7	3.5	V	
Low Threshold Input-Low Voltage	V_{IL_FSC}	3.3 V +/-5%	V_{SS} - 0.3	0.35	V	
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5	5	uA	2
Input Leakage Current	I_{INRES}	Inputs with pull up or pull down resistors $V_{IN} = V_{DD}$, V_{IN} = GND	-200	200	uA	
Output High Voltage	V_{OHSE}	Single-ended outputs, I_{OH} = -1mA	2.4		V	1
Output Low Voltage	V_{OLSE}	Single-ended outputs, I_{OL} = 1 mA		0.4	V	1
Operating Supply Current	$I_{DDOP3.3}$	Full Active, C_L = Full load; Idd 3.3V		125	mA	
	I_{DDOPIO}	Full Active, C_L = Full load; IDD IO		28	mA	
Input Frequency	F_i	V_{DD} = 3.3 V		15	MHz	
Pin Inductance	L_{pin}			7	nH	
Input Capacitance	C_{IN}	Logic Inputs	1.5	5	pF	
	C_{OUT}	Output pin capacitance		6	pF	
	C_{INX}	X1 & X2 pins		6	pF	
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock		1.8	ms	
Tfall_SE	T_{FALL}	Fall/rise time of all 3.3V control inputs from 20-80%		10	ns	
Trise_SE	T_{RISE}			10	ns	
SMBus Voltage	V_{DD}		2.7	5.5	V	
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}		0.4	V	
Current sinking at V_{OLSMB} = 0.4 V	I_{PULLUP}	SMB Data Pin	4		mA	
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)		1000	ns	
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)		300	ns	
Maximum SMBus Operating Frequency	F_{SMBUS}			100	kHz	
Spread Spectrum Modulation Frequency	f_{SSMOD}	Triangular Modulation	30	33	kHz	

Electrical Characteristics - Input/Supply/Common Output DC ParametersDC Parameters: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

[1]Signal is required to be monotonic in this region.

[2] input leakage current does not include inputs with pull-up or pull-down resistors

[3] 3.3V referenced inputs are: SCLK, SDATA, and CKPWRGD if selected.

[4] Intentionally blank

[5] Maximum VIH is not to exceed VDD

[6] Human Body Model

[7] Operation under these conditions is neither implied, nor guaranteed.

[8] Frequency Select pins which have tri-level input

AC Electrical Characteristics - Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Rising Edge Slew Rate	tSLR	Averaging on	2.5	5	V/ns	2, 3
Falling Edge Slew Rate	tFLR	Averaging on	2.5	5	V/ns	2, 3
Slew Rate Variation	tSLVAR	Averaging on		20	%	1, 6
Differential Voltage Swing	VSWING	Averaging off	300		mV	2
Crossing Point Voltage	VXABS	Averaging off	300	550	mV	1,4,5
Crossing Point Variation	VXABSVAR	Averaging off		140	mV	1,4,9
Maximum Output Voltage	VHIGH	Averaging off		1150	mV	1,7
Minimum Output Voltage	VLOW	Averaging off	-300		mV	1,8
Duty Cycle	DCYC	Averaging on	45	55	%	2
CPU Skew	CPUSKEW	Averaging on		100	ps	
SRC_SATA Skew	SRCSKEW	Differential Measurement		300	ps	1

NOTES on DIF Output AC Specs: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

[1]Measurement taken for single ended waveform on a component test board (not in system)

[2] Measurement taken from differential waveform on a component test board. (not in system)

[3] Slew rate emastured through V_swing voltage range centered about differential zero

[4] Vcross is defined at the voltage where Clock = Clock#, measured on a component test board (not in system)

[5] Only applies to the differential rising edge (Clock rising, Clock# falling)

[6] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage

[7] The max voltage including overshoot.

[8] The min voltage including undershoot.

[9] The total variation of all Vcross measurements in any particular system. Note this is a subset of V_cross min/mas (V_Cross absolute) allowed. The intent is to limit Vcross induced modulation by setting C_cross_delta to be smaller than V_Cross absolute

Clock Jitter Specifications - Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
CPU Jitter - Cycle to Cycle	$CPUJ_{C2C}$	Differential Measurement		85	ps	1,2
SRC Jitter - Cycle to Cycle	$SRCJ_{C2C}$	Differential Measurement		125	ps	1,2,3
SATA Jitter - Cycle to Cycle	$SATAJ_{C2C}$	Differential Measurement		125	ps	1,2
DOT Jitter - Cycle to Cycle	$DOTJ_{C2C}$	Differential Measurement		250	ps	1,2
SRC Phase Jitter	$t_{jphasePLL}$	PCIe Gen 1		86	ps (p-p)	1,2
	$t_{jphaseLo}$	PCIe Gen 2 10kHz < f < 1.5MHz		3	ps (RMS)	1,4
	$t_{jphaseHigh}$	PCIe Gen 2 1.5MHz < f < Nyquist (50MHz)		3.1	ps (RMS)	1,4

*TA = 0 - 70°C; Supply Voltage VDD = 3.3V+/-5%, Rs = 0ohms, CL = 2pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2]JItter specs are specified as measured on a clock characterization board. System designers need to take special care not to use these numbers, as the in-system performance will be somewhat degraded. The receiver EMTS (chispet or CPU) will have the receiver requirements.

[3] Phase jitter requirement: The deisgnated Gen2 outputs will meet the reference clock jitter requirememrnts from the PCI Express Gen2 Base Spec. The test is performed on a component test board under quiet conditttions with all outputs on.

[4]See http://www.pcisig.com for complete specs

Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100	100	ppm	2, 4
Clock period	Tperiod	14.318MHz output nominal	69.82033	69.86224	ns	2, 3
Absolute min/max period	Tabs	14.318MHz output nominal	69.83400	70.84800	ns	2
CLK High Time	THIGH		29.97543	38.46654	V	
CLK Low time	TLOW		29.57543	38.26654	V	
Output High Voltage	VOH	IOH = -1 mA	2.4		V	
Output Low Voltage	VOL	IOL = 1 mA		0.4	V	
Output High Current	IOH	VOH @MIN = 1.0 V, VOH@MAX = 3.135 V	-33	-33	mA	
Output Low Current	IOL	VOL @MIN = 1.95 V, VOL @MAX = 0.4 V	30	38	mA	
Rising Edge Slew Rate	tSLR	Measured between 0.8V and 2.0V	1	4	V/ns	1
Falling Edge Slew Rate	tFLR	Measured between 2.0V and 0.8V	1	4	V/ns	1
Duty Cycle	dt1	VT = 1.5 V	45	55	%	2
Jitter, Cycle to cycle	tjcyc-cyc	VT = 1.5 V		1000	ps	2

NOTES on SE outputs: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

[1]Edge rate is measured between 0.8V to 2.0V.

[2] Duty cycle, Peroid and Jitter are measured with respect to 1.5V

[3] The average period over any 1us period of time

[4] Using frequency counter with the measurment interval equal or greater that 0.15s, target frequencies are 14.318180 MHz, 33.333333MHz and 48.000000MHz

Electrical Characteristics - 27MHz_Spread / 27MHz_NonSpread

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-50	50	ppm	1,2
			-15	15		1,2,3
Clock period	T_{period}	27.000MHz output nominal	37.0365	37.0376		
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4		V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA		0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29		mA	1
		V_{OH}@MAX = 3.135 V		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29		mA	1
		V_{OL} @ MAX = 0.4 V		27	mA	1
Rising Edge Rate	$t_{slewr/r}$	Measured between 0.8V and 2.0V	1	4	V/ns	1
Falling Edge Rate	$t_{slewr/f}$	Measured between 2.0V and 0.8V	1	4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	55	%	1
Jitter	t_{ltj}	Long Term (10us)		800	ps	1,4
	t_{jpk-pk}		-250	250	ps	1
	$t_{jcyc-cyc}$	V_T = 1.5 V		500	ps	1

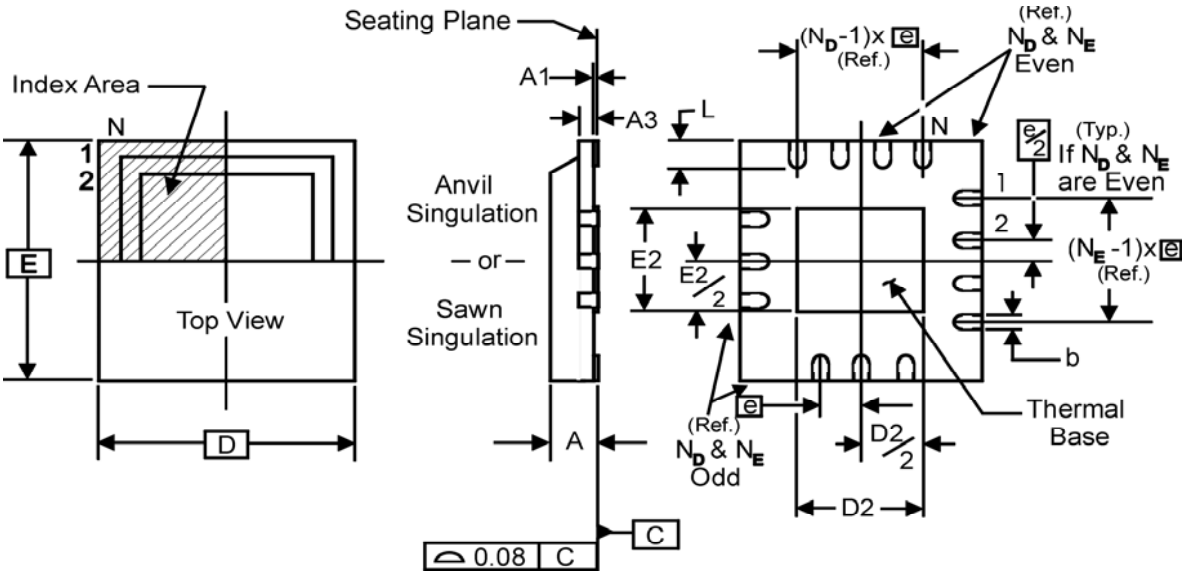
*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3] At nominal voltage and temperature

[4] 27MHz-Non-spread only



THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

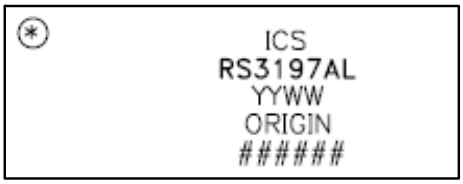
DIMENSIONS

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.20 Reference	
b	0.18	0.3
e	0.50 BASIC	

DIMENSIONS

SYMBOL	ICS 32L TOLERANCE
N	32
N_D	8
N_E	8
D x E BASIC	5.00 x 5.00
D2 MIN. / MAX.	3.0/ 3.3
E2 MIN. / MAX.	3.0/ 3.3
L MIN. / MAX.	0.30 / 0.50

Marking Diagram



Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9LRS3197AKLF	Trays	32-pin MLF	0 to +70° C
9LRS3197AKLFT	Tape and Reel	32-pin MLF	0 to +70° C

"A" is the device revision designator (will not correlate to the datasheet revision)
"LF" denotes Pb-free, RoHS compliant package

Revision History

Rev.	Issue Date	Description	Page #
A	01/17/11	Release to final	
B	07/29/11	Updated "Electrical Characteristics - Input/Supply/Common Output DC Parameters" table	
C	08/22/11	Updated Electrical parameters and ordering info table	9-12

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