Description

The 9SQL4958 is a member of IDT's 'Lite' family of server clocks. It generates 8 100MHz outputs that exceed the requirements of the CK420BQ CPU/SRC clocks. Each output has its own OE# pin for clock management and supports 2 different spread spectrum levels in addition to spread off. It also provides a copy of the 25MHz internal XO. The 9SQL4958 supports PCIe Common Clock (CC) and Independent Reference Clock (IR) architectures.

Recommended Application

PCIe Gen1, Gen2, Gen3, Gen4 Server Clock

Output Features

- 8 -100MHz Low-power HCSL (LP-HCSL) CPU/SRC pairs
- Integrated terminations for 85Ω Zo
- 1 - 3.3V LVCMOS REF output w/Wake-On-LAN (WOL) support

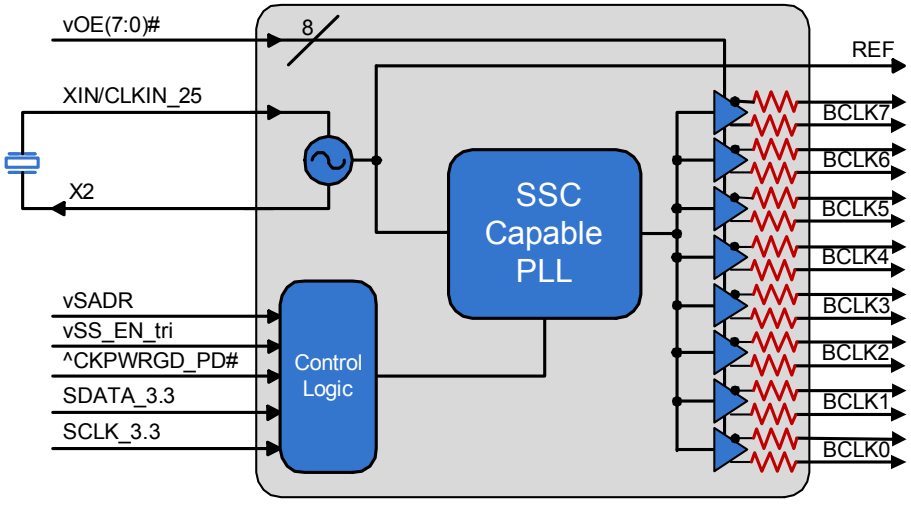
Key Specifications

- BCLK outputs
  - Cycle-to-cycle jitter <50ps
  - Output-to-output skew <50ps
  - PCIe Gen1, Gen2, Gen3, Gen4 CC compliant
  - PCIe Gen2, Gen3 IR compliant
  - QPI/UPI compliant
  - SAS12G compliant (SSC off)
  - 12k-20M phase jitter <2ps rms (SSC off)
- REF output:
  - Phase jitter <200fs rms (SSC off)
- ±50ppm frequency accuracy on all clocks

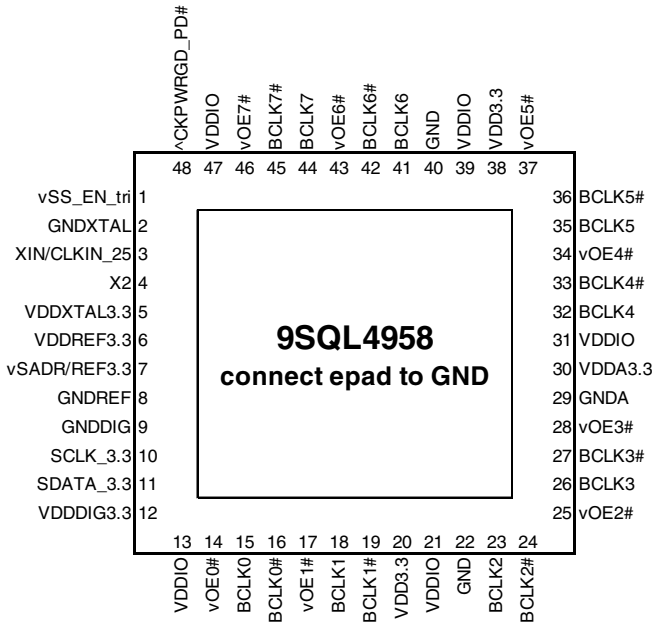
Features/Benefits

- Direct connection to 85Ω transmission lines; saves 32 resistors and 55mm^2 compared to standard HCSL
- 132mW typ. power consumption; eases thermal concerns @ 1/10 the power of CK420BQ
- Contains default configuration; SMBus interface not required for device operation
- OE# pins; support BLCK power management
- 25MHz input frequency; standard crystal frequency
- 25MHz REF output; eliminates XO from board
- Pin/SMBus selectable 0%, -0.25% or -0.5% spread on BLCK outputs; minimize EMI and phase jitter for each application
- BLCK outputs blocked until PLL is locked; clean system start-up
- Two selectable SMBus addresses; multiple devices can easily share an SMBus segment
- Space saving 48-pin 6x6mm VFQFPN; minimal board space

Block Diagram



Pin Configuration



48-pin VFQFPN, 6x6 mm, 0.4mm pitch

vv prefix indicates internal 60KOhm pull down resistor
v prefix indicates internal 120KOhm pull down resistor
^ prefix indicates internal 120KOhm pull up resistor

SMBus Address Selection Table

	SADR	Address	+ Read/Write Bit
State of SADR on first application of CKPWRGD_PD#	0	1101000	x
	1	1101010	x

Power Management Table[3]

CKPWRGD_PD#	SMBus OE bit	OEx# Pin	BCLKx		REF
			True O/P	Comp. O/P	
0	X	X	Low[1]	Low[1]	Hi-Z[2]
1	1	0	Running	Running	Running
1	1	1	Disabled[1]	Disabled[1]	Running
1	0	X	Disabled[1]	Disabled[1]	Disabled[4]

Notes

1. The output state is set by B11[1:0] (Low/Low default)
2. REF is Hi-Z until the 1st assertion of CKPWRGD_PD# high. After this, when CKPWRG_PD# is low, REF is disabled unless Byte3[5]=1, in which case REF is running..
3. Input polarities defined at default SMBus values.
4. See SMBus description for Byte 3, bit 4

Power Connections

Pin Number			Description
VDD	VDDIO	GND	
5		2	XTAL OSC
6		8	REF Power
12		9	Digital (dirty) Power
20,38	13,21,31,39, 47	22,29,40, 49	BCLK outputs
30		29	PLL Analog

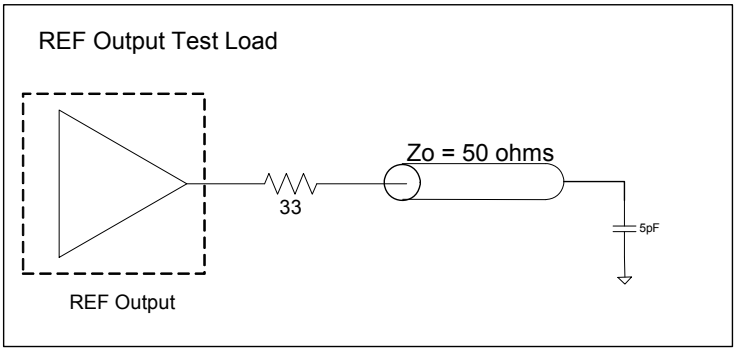
Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	vSS_EN_tri	LATCHED IN	Latched select input to select spread spectrum amount at initial power up : 1 = -0.5% spread, M = -0.25%, 0 = Spread Off
2	GNDXTAL	GND	GND for XTAL
3	XIN/CLKIN_25	IN	Crystal input or Reference Clock input. Nominally 25MHz.
4	X2	OUT	Crystal output.
5	VDDXTAL3.3	PWR	Power supply for XTAL, nominal 3.3V
6	VDDREF3.3	PWR	VDD for REF output. nominal 3.3V.
7	vSADR/REF3.3	LATCHED I/O	Latch to select SMBus Address/3.3V LVCMOS copy of X1/REFIN pin
8	GNDREF	GND	Ground pin for the REF outputs.
9	GNDDIG	GND	Ground pin for digital circuitry
10	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
11	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
12	VDDDIG3.3	PWR	3.3V digital power (dirty power)
13	VDDIO	PWR	Power supply for differential outputs
14	vOE0#	IN	Active low input for enabling output 0. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
15	BCLK0	OUT	True output of differential BCLK.
16	BCLK0#	OUT	Complement output of differential BCLK.
17	vOE1#	IN	Active low input for enabling output 1. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
18	BCLK1	OUT	True output of differential BCLK.
19	BCLK1#	OUT	Complement output of differential BCLK.
20	VDD3.3	PWR	Power supply, nominal 3.3V
21	VDDIO	PWR	Power supply for differential outputs
22	GND	GND	Ground pin.
23	BCLK2	OUT	True output of differential BCLK.
24	BCLK2#	OUT	Complement output of differential BCLK.
25	vOE2#	IN	Active low input for enabling output 2. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
26	BCLK3	OUT	True output of differential BCLK.
27	BCLK3#	OUT	Complement output of differential BCLK.
28	vOE3#	IN	Active low input for enabling output 3. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
29	GNDA	GND	Ground pin for the PLL core.
30	VDDA3.3	PWR	3.3V power for the PLL core.
31	VDDIO	PWR	Power supply for differential outputs
32	BCLK4	OUT	True output of differential BCLK.
33	BCLK4#	OUT	Complement output of differential BCLK.
34	vOE4#	IN	Active low input for enabling output 4. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
35	BCLK5	OUT	True output of differential BCLK.
36	BCLK5#	OUT	Complement output of differential BCLK.
37	vOE5#	IN	Active low input for enabling output 5. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
38	VDD3.3	PWR	Power supply, nominal 3.3V
39	VDDIO	PWR	Power supply for differential outputs

Pin Descriptions, cont.

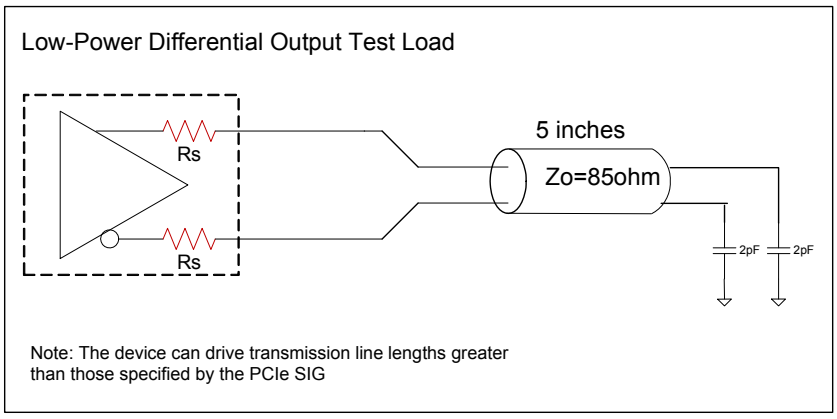
PIN #	PIN NAME	TYPE	DESCRIPTION
40	GND	GND	Ground pin.
41	BCLK6	OUT	True output of differential BCLK.
42	BCLK6#	OUT	Complement output of differential BCLK.
43	vOE6#	IN	Active low input for enabling output 6. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
44	BCLK7	OUT	True output of differential BCLK.
45	BCLK7#	OUT	Complement output of differential BCLK.
46	vOE7#	IN	Active low input for enabling output 7. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
47	VDDIO	PWR	Power supply for differential outputs
48	^CKPWRGD_PD#	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal 120kohm pull-up resistor.
49	EPAD	GND	Connect to Ground.

Test Loads



Terminations

Zo (Ω)	Rs (Ω)
85	0
100	7.5



Alternate Terminations

The 9SQL family can easily drive LVPECL, LVDS, and CML logic. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for details.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9SQL4958. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Supply Voltage	VDDxxx	Applies to all VDD pins	-0.5		3.9	V	1,2
Input Voltage	V_{IN}		-0.5		V_{DD} + 0.5V	V	1, 3
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins			3.9	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2500			V	1

Notes

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 4.5V.

Electrical Characteristics–SMBus Parameters

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SMBus Input Low Voltage	V_{ILSMB}	V_{DDSMB} = 3.3V			0.8	V	
SMBus Input High Voltage	V_{IHSMB}	V_{DDSMB} = 3.3V	2.1		3.6	V	
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{SMBMAX}	Maximum SMBus operating frequency			500	kHz	

Notes

[1] Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDxxx	Supply voltage for core, analog and single-ended LVCMOS outputs.	3.135	3.3	3.465	V	
IO Supply Voltage	VDDIO	Supply voltage for differential Low Power outputs.	0.9975	1.05-3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	Industrial range	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus	0.75 V_{DDx}		V_{DDx} + 0.3	V	
Input Low Voltage	V_{IL}		-0.3		0.25 V_{DDx}	V	
Input High Voltage	V_{IHtri}	Single-ended tri-level inputs ('_tri' suffix)	0.75 V_{DDx}		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IMtri}		0.4 V_{DDx}	0.5 V_{DDx}	0.6 V_{DDx}	V	
Input Low Voltage	V_{ILtri}		-0.3		0.25 V_{DDx}	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-50		50	uA	
Input Frequency	F_{in}	XTAL, or X1 input		25		MHz	
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.35	1.8	ms	1,2
SS Modulation Frequency	f_{MOD}	(Triangular Modulation)	30	31.6	33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1	2	3	clocks	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion		28	300	us	1,3
Tfall	t_F	Fall time of single-ended control inputs			5	ns	1,2
Trise	t_R	Rise time of single-ended control inputs			5	ns	1,2

Notes

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are >200 mV

Electrical Characteristics–BLCK Low-Power HCSL Outputs

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on, fast setting	2	2.7	4	V/ns	2,3
		Scope averaging, slow setting	1	1.9	3	V/ns	2,3
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	409	550	mV	1,4,5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		14	140	mV	1,4,9
Avg. Clock Period Accuracy	T_{PERIOD_AVG}		-50	0.0	+2550	ppm	2,10,13
Absolute Period	T_{PERIOD_ABS}	Includes jitter and Spread Spectrum Modulation	9.9491	10.0	10.1011	ns	2,6
Jitter, Cycle to cycle	$t_{jcyc-cyc}$			16	50	ps	2
Voltage High	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	761	850	mV	1
Voltage Low	V_{LOW}		-150	-7	150		1
Absolute Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		819	1150	mV	1,7,15
Absolute Min Voltage	Vmin		-300	-46			1,8,15
Duty Cycle	t_{DC}		45	49.2	55	%	2
Slew rate matching	ΔTrf			6	20	%	1,14
Skew, Output to Output	t_{sk3}	Averaging on, V_T = 50%		35	50	ps	2

Notes

[1] Measured from single-ended waveform.

[2] Measured from differential waveform.

[3] Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.

[4] Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

[5] Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

[6] Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative PPM tolerance, and spread spectrum modulation.

[7] Defined as the maximum instantaneous voltage including overshoot.

[8] Defined as the minimum instantaneous voltage including undershoot.

[9] Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system.

[10] Refer to Section 4.3.7.1.1 of the PCI Express Base Specification, Revision 3.0 for information regarding PPM considerations.

[11] System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL = 2 pF.

[12] T_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the VRB ±100 mV differential range.

[13] PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For 300 PPM, then we have an error budget of 100 Hz/PPM * 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 PPM applies to systems that do not employ Spread Spectrum Clocking, or that use common clock source. For systems employing Spread Spectrum Clocking, there is an additional 2,500 PPM nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,800 PPM.

[14] Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

[15] At default SMBus amplitude settings.

Electrical Characteristics–Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures[1, 2, 5]

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	SPECIFICATION LIMIT	UNITS	NOTES
Phase Jitter, PLL Mode	$t_{jphPCIeG1-CC}$	PCIe Gen 1		19	30	86	ps (p-p)	3
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz, 8-16MHz, CDR = 5MHz)		0.4	0.6	3	ps (rms)	
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz, 8-16MHz, CDR = 5MHz)		1.2	1.9	3.1	ps (rms)	
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz)		0.27	0.45	1	ps (rms)	
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz)		0.27	0.45	0.5	ps (rms)	

Electrical Characteristics–Filtered Phase Jitter Parameters - PCIe Separate Reference Independent Spread (SRIS) Architectures[1, 5, 6]

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	NOTES
	$t_{jphPCIeG1-SRIS}$	PCIe Gen 1		n/a		None	ps (rms)	2, 7
Phase Jitter, PLL Mode	$t_{jphPCIeG2-SRIS}$	PCIe Gen 2 (PLL BW of 16MHz , CDR = 5MHz)		0.7	1.2	2	ps (rms)	2
	$t_{jphPCIeG3-SRIS}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.5	0.65	0.7	ps (rms)	2
	$t_{jphPCIeG4-SRIS}$	PCIe Gen 4 (PLL BW of 2-4MHz, CDR = 10MHz)		n/a		None	ps (rms)	2, 7

Notes on PCIe Filter Phase Jitter Tables

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Based on PCIe Base Specification Rev4.0 version 0.7draft. See http://www.pcisig.com for latest specifications.

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] Additive jitter for RMS values is calculated by solving for b where [$b=sqrt(c^2-a^2)$], a is rms input jitter and c is rms total jitter.

[5] Driven by 9FGL0841 or equivalent

[6] IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures.

[7] According to the PCIe Base Specification Rev4.0 version 0.7 draft, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted *industry* limits using widely accepted *industry* filters are used to populate this table. There are no accepted filters or limits for IR clock architectures at PCIe Gen1 or Gen4 data rates

Electrical Characteristics–Phase Jitter - QPI/UPI, SAS[1, 2]

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	SPECIFICATION LIMIT	UNITS	NOTES
Phase Jitter, PLL Mode	t_{jphQPI_UPI}	QPI & UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.13	0.2	0.5	ps (rms)	
		QPI & UPI (100MHz, 8.0Gb/s, 12UI)		0.10	0.15	0.3	ps (rms)	
		QPI & UPI (100MHz, ?9.6Gb/s, 12UI)		0.08	0.12	0.2	ps (rms)	
Phase Jitter, SAS12G BCLK Outputs	$t_{jphSAS12G}$	100MHz, SSC Off, REF output enabled		0.50	0.55	1.2	ps (rms)	1,2

Notes

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Calculated from Intel-supplied Clock Jitter Tool

[3] For RMS values additive jitter is calculated by solving for b where [$b=sqrt(c^2-a^2)$], a is rms input jitter and c is rms total jitter.

Electrical Characteristics–12kHz-20MHz Phase Jitter

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	SPECIFICATION LIMIT	UNITS	NOTES
Phase Jitter, 12kHz-20MHz BCLK Outputs	$t_{jph12k-20M}$	100MHz, SSC Off, REF output enabled		1.5	2	n/a	ps (rms)	1

Notes

[1] Applies to all differential outputs, guaranteed by design and characterization.

Electrical Characteristics–Current Consumption

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I_{DDAOP}	VDDA, All outputs active @100MHz		13	18	mA	
	I_{DDOP}	All other VDD, except VDDA, All outputs active @100MHz		19	26	mA	
	I_{DDIOOP}	VDDIO, All outputs active @100MHz, Zo=85ohm		31	40	mA	
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I_{DDAPD}	VDDA, BCLK outputs off, REF output on		0.9	1.5	mA	1
	I_{DDPD}	All other VDD, except VDDA, BCLK outputs off, REF output running		6.5	9	mA	1
	I_{DDIOPD}	VDDIO, BCLK outputs off, REF output on, Zo=85ohm		0.05	0.1	mA	1
Powerdown Current (Power down state and Byte 3, bit 5 = '0')	I_{DDAPD}	VDDA, all outputs off		0.9	1.5	mA	
	I_{DDPD}	All other VDD, except VDDA, all outputs off		2.4	3	mA	
	I_{DDIOPD}	VDDIO, all outputs off, Zo=85ohm		0.05	0.1	mA	

Notes

[1] This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1)

Electrical Characteristics– REF

TA = T_{AMB}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values		0		ppm	1,2
Clock period	T_{period}	25 MHz output		40		ns	2
Output High Voltage	V_{IH}	I_{OH} = -2mA	0.8xV_{DDREF}			V	
Output Low Voltage	V_{IL}	I_{OL} = 2mA			0.2xV_{DDREF}	V	
Rise/Fall Slew Rate	t_{rf1}	Byte 3 = 1F, V_{OH} = VDD-0.45V, V_{OL} = 0.45V	0.5	0.8	1.1	V/ns	1
Rise/Fall Slew Rate	t_{rf1}	Byte 3 = 5F, V_{OH} = VDD-0.45V, V_{OL} = 0.45V	0.9	1.4	1.9	V/ns	1,3
Rise/Fall Slew Rate	t_{rf1}	Byte 3 = 9F, V_{OH} = VDD-0.45V, V_{OL} = 0.45V	1.3	2.0	2.7	V/ns	1
Rise/Fall Slew Rate	t_{rf1}	Byte 3 = DF, V_{OH} = VDD-0.45V, V_{OL} = 0.45V	1.7	2.6	3.5	V/ns	1
Duty Cycle	d_{t1X}	V_T = VDD/2 V	45	49.8	55	%	1,4
Duty Cycle Distortion	d_{tcd}	V_T = VDD/2 V	-1	0	0	%	1,5
Jitter, cycle to cycle	$t_{jcyc-cyc}$	V_T = VDD/2 V		70	250	ps	1,4
Noise floor	t_{jdBc1k}	1kHz offset			-137	dBc	1,4
Noise floor	$t_{jdBc10k}$	10kHz offset to Nyquist			-140	dBc	1,4
Jitter, phase	t_{jphREF}	12kHz to 5MHz, SSC Off		0.13	0.2	ps (rms)	1,4
Jitter, phase	t_{jphREF}	12kHz to 5MHz, SSC On		1.5	2	ps (rms)	1,4

Notes

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00 MHz

[3] Default SMBus Value

[4] When driven by a crystal.

[5] When driven by an external oscillator via the X1 pin, X2 should be floating.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Note: SMBus Read/Write Address is Latched on SADR pin.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Output Enable Register [1]

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	BCLK OE7	Output Enable	RW	See B11[1:0]	Pin Control	1
Bit 6	BCLK OE6	Output Enable	RW		Pin Control	1
Bit 5	BCLK OE5	Output Enable	RW		Pin Control	1
Bit 4	BCLK OE4	Output Enable	RW		Pin Control	1
Bit 3	BCLK OE3	Output Enable	RW		Pin Control	1
Bit 2	BCLK OE2	Output Enable	RW		Pin Control	1
Bit 1	BCLK OE1	Output Enable	RW		Pin Control	1
Bit 0	BCLK OE0	Output Enable	RW		Pin Control	1

1. A low on these bits will overide the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default)

SMBus Table: SS Readback and Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	SSENRB1	SS Enable Readback Bit1	**R**	00' for SS_EN_tri = 0, '01' for SS_EN_tri = 'M', '11 for SS_EN_tri = '1'		Latch
Bit 6	SSENRB1	SS Enable Readback Bit0	**R**			Latch
Bit 5	SSEN_SWCNTRL	Enable SW control of SS	RW	SS control locked	Values in B1[4:3] control SS amount.	0
Bit 4	SSENSW1	SS Enable Software Ctl Bit1	RW[1]	00' = SS Off, '01' = -0.25% SS, '10' = Reserved, '11'= -0.5% SS		0
Bit 3	SSENSW0	SS Enable Software Ctl Bit0	RW[1]			0
Bit 2	Reserved					X
Bit 1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.6V	01= 0.68V	1
Bit 0	AMPLITUDE 0		RW	10 = 0.75V	11 = 0.85V	0

1. Spread must be selected OFF or ON with the hardware latch pin. These bits should not be used to turn spread ON or OFF after power up. These bits can be used to change the spread amount, and B1[5] must be set to a 1 for these bits to have any effect on the part. If These bits are used to turn spread OFF or ON, the system will need to be reset.

SMBus Table: BCLK Slew Rate Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	SLEWRATESEL BCLK7	Adjust Slew Rate of BCLK7	RW	Slow Setting	Fast Setting	1
Bit 6	SLEWRATESEL BCLK6	Adjust Slew Rate of BCLK6	RW	Slow Setting	Fast Setting	1
Bit 5	SLEWRATESEL BCLK5	Adjust Slew Rate of BCLK5	RW	Slow Setting	Fast Setting	1
Bit 4	SLEWRATESEL BCLK4	Adjust Slew Rate of BCLK4	RW	Slow Setting	Fast Setting	1
Bit 3	SLEWRATESEL BCLK3	Adjust Slew Rate of BCLK3	RW	Slow Setting	Fast Setting	1
Bit 2	SLEWRATESEL BCLK2	Adjust Slew Rate of BCLK2	RW	Slow Setting	Fast Setting	1
Bit 1	SLEWRATESEL BCLK1	Adjust Slew Rate of BCLK1	RW	Slow Setting	Fast Setting	1
Bit 0	SLEWRATESEL BCLK0	Adjust Slew Rate of BCLK0	RW	Slow Setting	Fast Setting	1

Note: See "Low-Power HCSL Outputs" table for slew rates.

SMBus Table: Nominal Vhigh Amplitude Control/ REF Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	REF	Slew Rate Control	RW	00 = Slowest	01 =Slow	0
Bit 6			RW	10 = Fast	11 = Fastest	1
Bit 5	REF Power Down Function	Wake-on-Lan Enable for REF	RW	REF disabled in Power Down	REF runs in Power Down	0
Bit 4	REF OE	REF Output Enable	RW	Disabled[1]	Enabled	1
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	Reserved					X
Bit 0	Reserved					X

1. The disabled state depends on Byte11[1:0]. '00' = Low, '01'=HiZ, '10'=Low, '11'=HIgh

Byte 4 is Reserved

SMBus Table: Revision and Vendor ID Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	B rev = 0001		0
Bit 6	RID2		R			0
Bit 5	RID1		R			0
Bit 4	RID0		R			1
Bit 3	VID3	VENDOR ID	R	0001 = IDT		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

SMBus Table: Device Type/Device ID

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device Type1	Device Type	R	00 = 9SQL49xx		0
Bit 6	Device Type0		R			0
Bit 5	Device ID5	Device ID	R	001000 binary or 08 hex		0
Bit 4	Device ID4		R			0
Bit 3	Device ID3		R			1
Bit 2	Device ID2		R			0
Bit 1	Device ID1		R			0
Bit 0	Device ID0		R			0

SMBus Table: Byte Count Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is = 8 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

Bytes 8 and 9 are Reserved.

SMBus Table: PLL MN Enable, PD_Restore

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	PLL M/N En	M/N Programming Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
Bit 6	Power-Down (PD) Restore	Restore Default Config. In PD	RW	Clear Config in PD	Keep Config in PD	1
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	Reserved					X
Bit 0	Reserved					X

SMBus Table: Stop State Control

Byte 11	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	STP[1]	True/Complement BCLK Output Disable State	RW	00 = Low/Low	10 = High/Low	0
Bit 0	STP[0]		RW	01 = HiZ/HiZ	11 = Low/High	0

SMBus Table: Impedance Control

Byte 12	Name	Control Function	Type	0	1	Default
Bit 7	BCLK3_imp[1]	BCLK3 Zo	RW	00=33 ohm Zo	10=100 ohm Zo	see Note
Bit 6	BCLK3_imp[0]	BCLK3 Zo	RW	01=85 ohm Zo	11 = Reserved	
Bit 5	BCLK2_imp[1]	BCLK2 Zo	RW	00=33 ohm Zo	10=100 ohm Zo	
Bit 4	BCLK2_imp[0]	BCLK2 Zo	RW	01=85 ohm Zo	11 = Reserved	
Bit 3	BCLK1_imp[1]	BCLK1 Zo	RW	00=33 ohm Zo	10=100 ohm Zo	
Bit 2	BCLK1_imp[0]	BCLK1 Zo	RW	01=85 ohm Zo	11 = Reserved	
Bit 1	BCLK0_imp[1]	BCLK0 Zo	RW	00=33 ohm Zo	10=100 ohm Zo	
Bit 0	BCLK0_imp[0]	BCLK0 Zo	RW	01=85 ohm Zo	11 = Reserved	

SMBus Table: Impedance Control

Byte 13	Name	Control Function	Type	0	1	Default
Bit 7	BCLK7_imp[1]	BCLK7 Zo	RW	00=33 ohm Zo	10=100 ohm Zo	see Note
Bit 6	BCLK7_imp[0]	BCLK7 Zo	RW	01=85 ohm Zo	11 = Reserved	
Bit 5	BCLK6_imp[1]	BCLK6 Zo	RW	00=33 ohm Zo	10=100 ohm Zo	
Bit 4	BCLK6_imp[0]	BCLK6 Zo	RW	01=85 ohm Zo	11 = Reserved	
Bit 3	BCLK5_imp[1]	BCLK5 Zo	RW	00=33 ohm Zo	10=100 ohm Zo	
Bit 2	BCLK5_imp[0]	BCLK5 Zo	RW	01=85 ohm Zo	11 = Reserved	
Bit 1	BCLK4_imp[1]	BCLK4 Zo	RW	00=33 ohm Zo	10=100 ohm Zo	
Bit 0	BCLK4_imp[0]	BCLK4 Zo	RW	01=85 ohm Zo	11 = Reserved	

SMBus Table: Pull-up Pull-down Control

Byte 14	Name	Control Function	Type	0	1	Default
Bit 7	OE3_pu/pd[1]	OE3 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 6	OE3_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 5	OE2_pu/pd[1]	OE2 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 4	OE2_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 3	OE1_pu/pd[1]	OE1 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 2	OE1_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 1	OE0_pu/pd[1]	OE0 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 0	OE0_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1

SMBus Table: Pull-up Pull-down Control

Byte 15	Name	Control Function	Type	0	1	Default
Bit 7	OE7_pu/pd[1]	OE7 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 6	OE7_pu/pd0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 5	OE6_pu/pd[1]	OE6 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 4	OE6_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 3	OE5_pu/pd[1]	OE5 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 2	OE5_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 1	OE4_pu/pd[1]	OE4 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 0	OE4_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1

SMBus Table: Pull-up Pull-down Control

Byte 16	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	CKPWRGD_PD_pu/pd[1]	CKPWRGD_PD Pull-up(PuP)/	RW	00=None	10=Pup	1
Bit 0	CKPWRGD_PD_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	0

Bytes 17 is Reserved

SMBus Table: Polarity Control

Byte 18	Name	Control Function	Type	0	1	Default
Bit 7	OE7_polarity	Sets OE7 polarity	RW	Enabled when Low	Enabled when High	0
Bit 6	OE6_polarity	Sets OE6 polarity	RW	Enabled when Low	Enabled when High	0
Bit 5	OE5_polarity	Sets OE5 polarity	RW	Enabled when Low	Enabled when High	0
Bit 4	OE4_polarity	Sets OE4 polarity	RW	Enabled when Low	Enabled when High	0
Bit 3	OE3_polarity	Sets OE3 polarity	RW	Enabled when Low	Enabled when High	0
Bit 2	OE2_polarity	Sets OE2 polarity	RW	Enabled when Low	Enabled when High	0
Bit 1	OE1_polarity	Sets OE1 polarity	RW	Enabled when Low	Enabled when High	0
Bit 0	OE0_polarity	Sets OE0 polarity	RW	Enabled when Low	Enabled when High	0

SMBus Table: Polarity Control

Byte 19	Name	Control Function	Type	0	1	Default
Bit 7		Reserved				X
Bit 6		Reserved				X
Bit 5		Reserved				X
Bit 4		Reserved				X
Bit 3		Reserved				X
Bit 2		Reserved				X
Bit 1		Reserved				X
Bit 0	CKPWRGD_PD	Determines CKPWRGD_PD polarity	RW	Power Down when Low	Power Down when High	0

Recommended Crystal Characteristics (3225 package)

PARAMETER	VALUE	UNITS	NOTES
Frequency	25	MHz	1
Resonance Mode	Fundamental	-	1
Frequency Tolerance @ 25°C	±20	PPM Max	1
Frequency Stability, ref @ 25°C Over Operating Temperature Range	±20	PPM Max	1
Temperature Range (commerical)	0~70	°C	1
Temperature Range (industrial)	-40~85	°C	1
Equivalent Series Resistance (ESR)	50	Ω Max	1
Shunt Capacitance (C_O)	7	pF Max	1
Load Capacitance (C_L)	8	pF Max	1
Drive Level	0.3	mW Max	1
Aging per year	±5	PPM Max	1

Marking Diagram

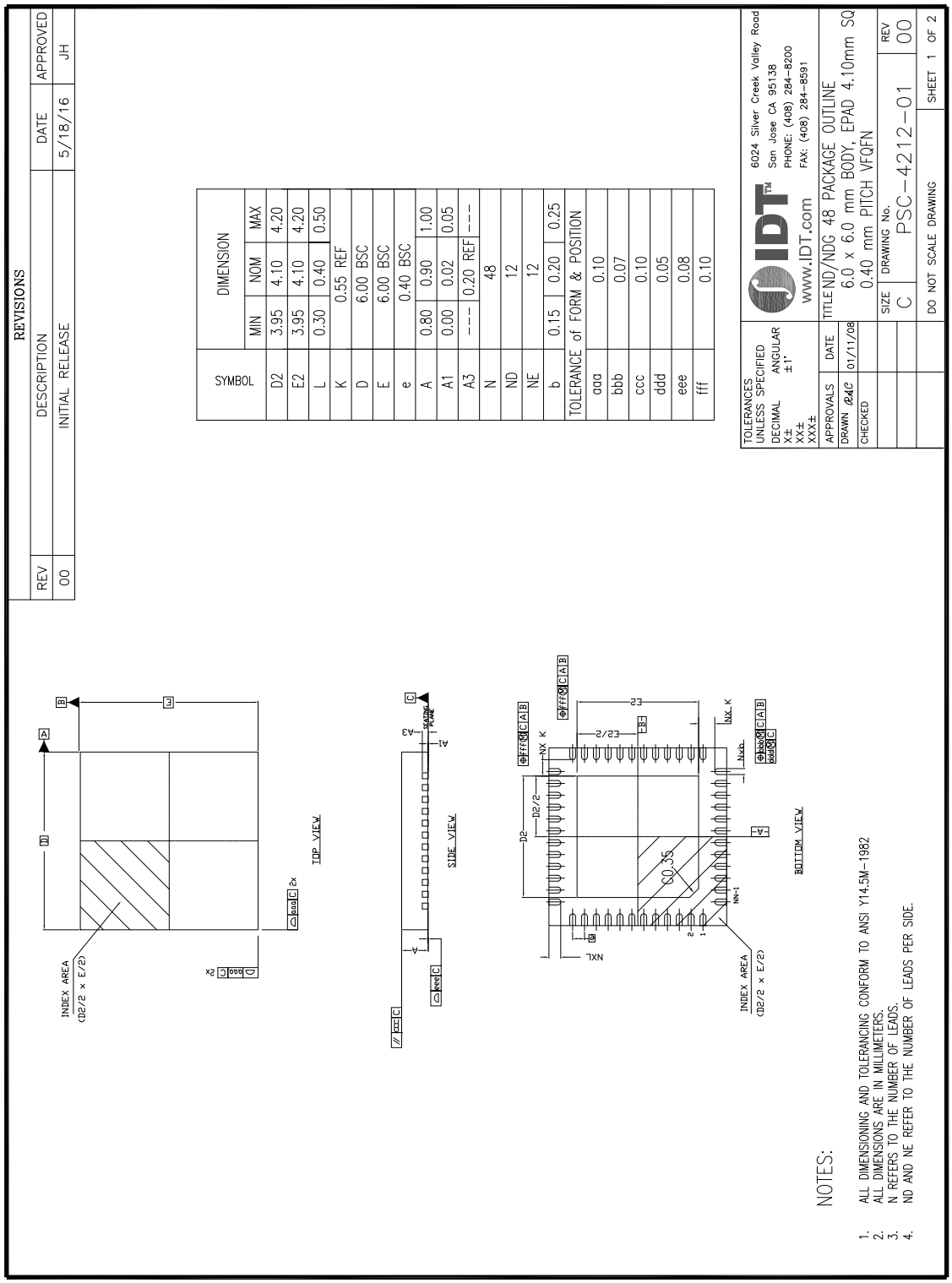
Notes:
1. “YYWW” is the last two digits of the year and week that the part was assembled.
2. “$” denotes the mark code.
3. “I” denotes industrial temperature range device.
4. “LOT” is the lot sequence number.

Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP.	UNITS	NOTES
Thermal Resistance	θ_{JC}	Junction to Case	NDG48	33	°C/W	1
	θ_{Jb}	Junction to Base		2.1	°C/W	1
	θ_{JA0}	Junction to Air, still air		37	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		30	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		27	°C/W	1
	θ_{JA5}	Junction to Air, 5 m/s air flow		26	°C/W	1

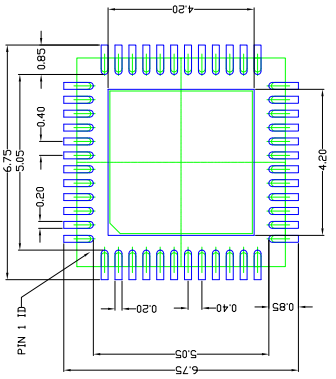
[1]ePad soldered to board

Package Outline and Dimensions (NDG48)



Package Outline and Dimensions (NDG48), cont.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/18/16	JH



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± ±1°
XX±
XXX±

APPROVALS DATE
DRAWN dxc 01/11/08
CHECKED

IDT™ 6024 Silver Creek Valley Road San Jose CA 95138
www.IDT.com PHONE: (408) 284-8200 FAX: (408) 284-8591

TITLE NDG/NDG 48 PACKAGE OUTLINE
6.0 x 6.0 mm BODY, EPAD 4.10mm SQ
0.40 mm PITCH VFQFN

SIZE C DRAWING No. PSC-4212-01 REV 00

DO NOT SCALE DRAWING SHEET 2 OF 2

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9SQL4958BNDGI	Trays	48-pin VFQFPN	-40 to +85° C
9SQL4958BNDGI8	Tape and Reel	48-pin VFQFPN	-40 to +85° C

"G" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
"B" is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Issue Date	Intiator	Description	Page #
A	10/28/2016	RDW	1. Updated electrical tables per PCIe Base Spec 4.0v7 of Oct. 2016 to add PCIe Gen4 CC and PCIe Gen2-3 IR to the data sheet. 2. Separated PCIe and QPI/UPI, SAS electrical tables 3. Updated front page text for clarity 4. Added note about hardware latching Spread Spectrum versus software control of on/off to Byte 1. 5. Updated block diagram for formatting, and test loads 6. Removed IDT Crystal Part numbers from DS. 7. Changed pin name of DIF outputs to BCLK to better indicate usage	Various

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