

ISL85415DEMO2Z

Demonstration Board

AN1945
Rev 1.00
June 1, 2015

Description

The ISL85415DEMO2Z kit is intended for use in point-of-load applications sourcing from 3V to 36V. The kit is used to demonstrate the performance of the [ISL85415](#) wide V_{IN} low quiescent current high efficiency synchronous buck regulator using an isolated secondary output.

The ISL85415 is offered in a 4mmx3mm 12 Ld DFN package with 1mm maximum height. The converter occupies 1.138cm² area.

Specifications

- This board has been configured and optimized for the following operating conditions:
- V_{IN} = 3V to 36V
- V_{OUT} = 0.6V to 12V
- I_{MAX} = 300mA with $\pm 1\%$ secondary output regulation (at $V_{OUT} = 3.3V$, $V_{IN} = 12V$)
- Board temperature: +25°C

References

- [ISL85415](#) Datasheet

Key Features

- Wide input voltage range 3V to 36V
- Synchronous operation for high efficiency
- Integrated high-side and low-side NMOS devices
- Programmable switching frequency (fixed or externally)
- Continuous output current up to 300mA (refer to [Figures 10](#) and [11](#))
- Internal or external soft-start
- Minimal external components required
- Power-good function available for primary output

Recommended Equipment

The following materials are recommended to perform testing:

- 0V to 50V power supply with at least 1A source current capability
- Electronic loads capable of sinking current up to 1A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope

Ordering Information

PART NUMBER	DESCRIPTION
ISL85415DEMO2Z	Demonstration board with Isolated Outputs

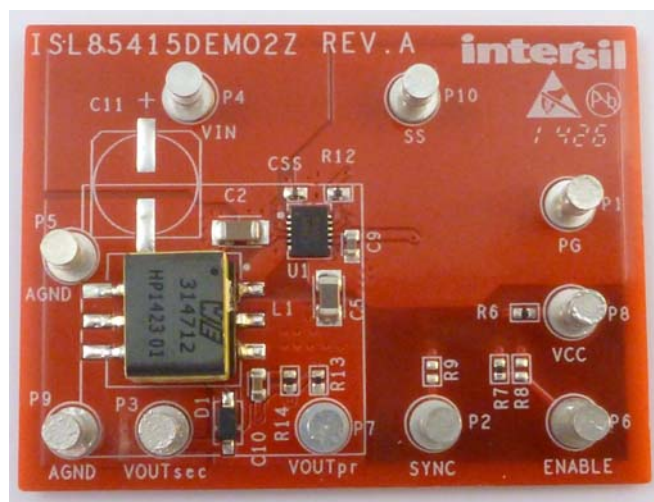


FIGURE 1. FRONT OF EVALUATION BOARD ISL85415DEMO2Z

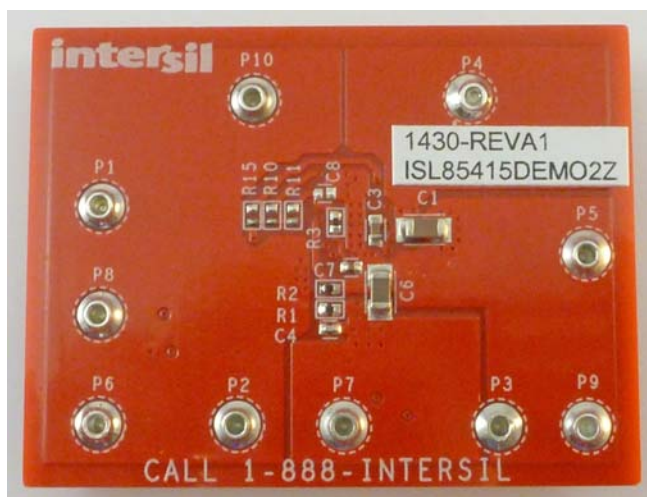


FIGURE 2. BACK OF EVALUATION BOARD ISL85415DEMO2Z

Quick Set up Guide

1. Ensure that the circuit is correctly connected to the supply and loads prior to applying any power.
2. Connect the bias supply to VIN, the plus terminal to VIN (P4) and the negative return to GND (P5).
3. Turn on the power supply.
4. Without any load applied on the output, verify that the output voltage is 3.3V for V_{OUT1} (P7).

PCB Layout Guidelines

The ISL85415EVAL2Z PCB layout has been optimized for electrical and thermal performance. Proper layout of the power converter will minimize EMI and noise while insuring first pass success of the design.

PCB layout is provided on the Intersil web site. A multilayer printed circuit board with GND plane is recommended. The most critical connections are to tie the PGND pin to the package GND pad and then use vias to directly connect the GND pad to the system GND plane. This connection of the GND pad to system plane insures a low impedance path for all return current, as well as an excellent thermal path to dissipate heat.

With this connection made, place the high frequency MLCC input capacitors C_1 , C_2 near the VIN pin and use vias directly at the capacitor pads to tie the capacitors to the system GND plane. Also, use vias directly at the C_5 , C_6 output capacitor pads to tie the capacitors to the system GND plane. These measures will minimize the high dV/dt and dI/dt loops. Minimize the PHASE connection by placing L_1 very close to the IC. Place a $1\mu F$ MLCC near the VCC pin and directly connect its return with a via to the system GND plane. Keep the power components path (L_1 , C_1 , C_2 , C_3 , C_5 , C_6) separated from the small signal nodes (FB, COMP) and the control components path (FS, SS) by placing the feedback divider close to the FB pin and do not route any feedback components near PHASE or BOOT. If external components are used for SS, COMP or FS, the same advice applies. Connect these control components and small signal noise components to the system GND. Keep the small signal nodes traces (FB, COMP) as short as possible.

Evaluating the Other Output Voltage

The ISL85415DEMO2Z kit output is preset to 3.3V; however, output voltages can be adjusted from 0.6V to 15V. The output voltage programming resistor, R_2 , will depend on the desired output voltage of the regulator and the value of the feedback resistor R_1 , as shown in [Equation 1](#).

$$R_2 = R_1 \left(\frac{0.6}{V_{OUT} - 0.6} \right) \quad (\text{EQ. 1})$$

If the output voltage desired is 0.6V, then R_1 is shorted. Please note that if V_{OUT} is less than 1.8V, the switching frequency and compensation must be changed for 300kHz operation due to minimum on-time limitation. Please refer to datasheet [ISL85415](#) for further information.

[Table 1](#) shows external component selection for different desired V_{OUT} .

The curves in [Figure 10](#) indicate the secondary output voltage regulation versus the load applied in the secondary output, without any load on the primary output for $V_{OUT} = 5V$, at different input voltages. The curves in [Figure 11](#) indicate the secondary output voltage regulation versus the load applied in the secondary output, without any load on the primary output for $V_{OUT} = 3.3V$, at different input voltages.

Frequency Control

The ISL85415 has an FS pin that controls the frequency of operation. Programmable frequency allows for optimization between efficiency and external component size. It also allows low frequency operation for low V_{OUTs} when minimum on-time would limit the operation otherwise. Default switching frequency is 500kHz when FS is tied to V_{CC} ($R_{10} = 0$). By removing R_{10} the switching frequency could be changed from 300kHz ($R_{12} = 340k$) to 2MHz ($R_{12} = 32.4k$). Please refer to datasheet [ISL85415](#) for calculating the value of R_{12} . Do not leave this pin floating.

Disabling/Enabling Function

The ISL85415DEMO2Z board has the EN pin tied to VIN via R_7 . This keeps the part enabled all the time. To disable the part, remove R_7 and populate R_8 with a 0Ω resistor.

SYNC Control

The ISL85415 evaluation board has a SYNC pin that allows external synchronization frequency to be applied. Default board configuration has $R_6 = 200k$ to V_{CC} , which defaults to PWM operation mode and also to the preselected switching frequency set by R_{12} (see [ISL85415](#) datasheet and previous section "Frequency Control" for details). If this pin is tied to GND, the IC will operate in PFM mode. For PFM operation, remove R_6 and populate R_9 with 0Ω resistor.

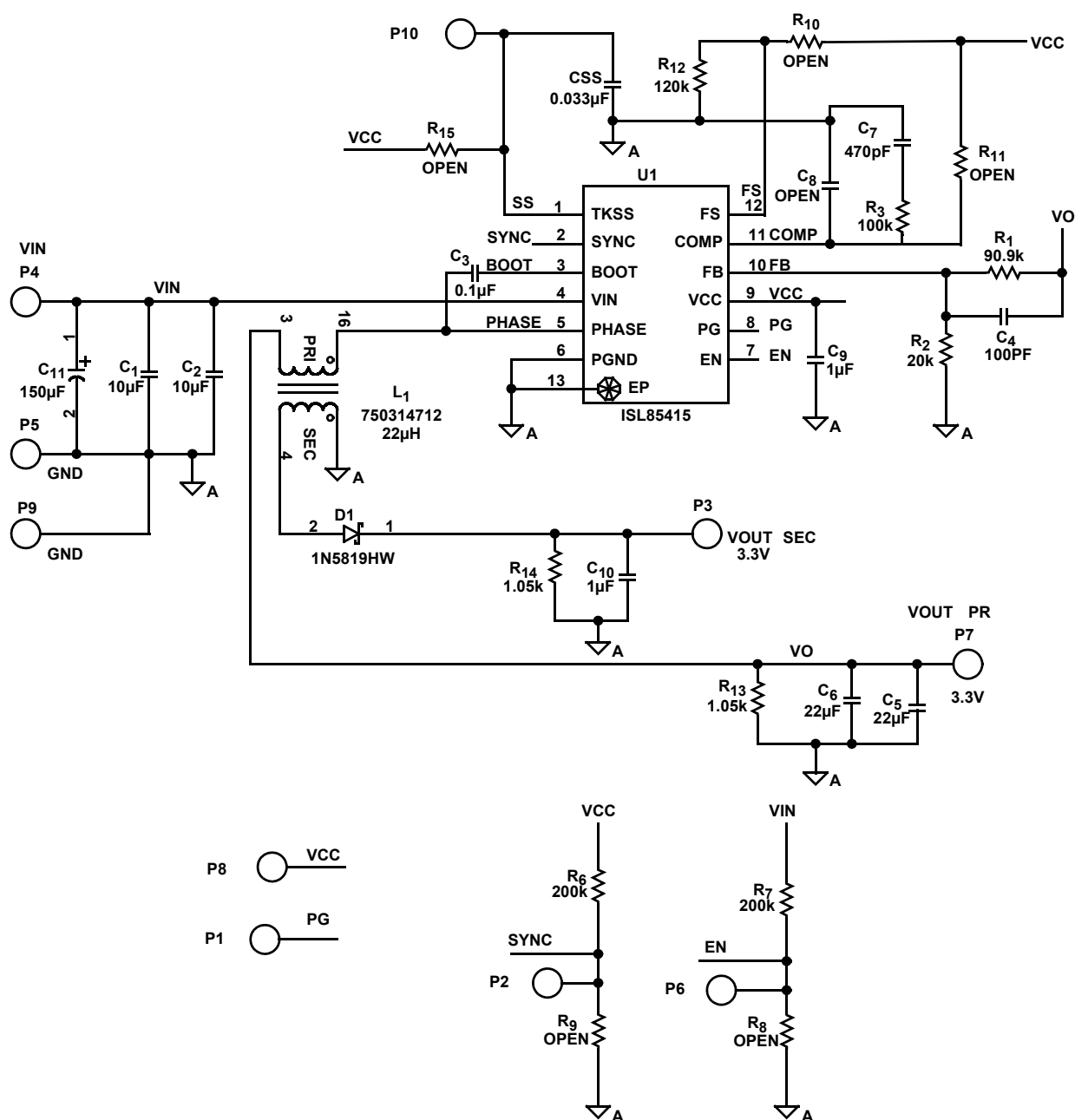
Soft-start/COMP Control

R_{15} selects between internal ($R_{15} = 0$) and external soft-start. R_{11} selects between internal ($R_{11} = 0$) and external compensation. Please refer to the Pin Description table of the [ISL85415](#) datasheet.

TABLE 1. EXTERNAL COMPONENT SELECTION

V_{OUT} (V)	L_1 (μH)	C_{OUT} (μF)	R_1 ($k\Omega$)	R_2 ($k\Omega$)	C_{FB} (pF)	R_{FS} ($k\Omega$)	R_{COMP} ($k\Omega$)	C_{COMP} (pF)
12	45	10	90.9	4.75	22	115	100	470
5	22	2x22	90.9	12.4	100	120	100	470
3.3	22	2x22	90.9	20	100	120	100	470
2.5	22	2x22	90.9	28.7	100	120	100	470
1.8	22	22	100	50	22	120	50	470

ISL85415DEMO2Z Schematic



NOTE: If the IC is used in an application where the input test leads have large parasitic inductance, the input electrolytic capacitor C₁₁ may be added to prevent transient voltages on the input pin.

FIGURE 3. ISL85415DEMO2Z SCHEMATIC

ISL85415DEMO2Z Bill of Materials

MANUFACTURER PART	QTY	UNIT	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER
EEE-FK1H151P	1	ea.	C11 (OPTIONAL)	CAP, SMD, 10.3mm, 150μF, 50V, 20%, ROHS, ALUM.ELEC.	PANASONIC
GRM188R71E105KA12D	1	ea.	C10	CAP, SMD, 0603, 1μF, 25V, 10%, X7R, ROHS	MURATA
04025A101FAT2A	1	ea.	C4	CAP, SMD, 0402, 100pF, 50V, 1%, NP0, ROHS	AVX
GRM36X7R333K016AQ	1	ea.	CSS	CAP, SMD, 0402, 33nF, 16V, 10%, X7R, ROHS	MURATA
ECJ-0EB1H471K	1	ea.	C7	CAP, SMD, 0402, 470pF, 50V, 10%, X7R, ROHS	PANASONIC
	0	ea.	C8	CAP, SMD, 0402, DNP-PLACE HOLDER, ROHS	
06035C104KAT2A	1	ea.	C3	CAP, SMD, 0603, 0.1μF, 50V, 10%, X7R, ROHS	AVX
GRM188R61C105KA12D	1	ea.	C9	CAP, SMD, 0603, 1μF, 16V, 10%, X5R, ROHS	MURATA
C3216X5R1H106K	2	ea.	C1, C2	CAP, SMD, 1206, 10μF, 50V, 10%, X5R, ROHS	TDK
ECJ-DV50J226M	2	ea.	C5, C6	CAP, SMD, 1206, 22μF, 6.3V, 20%, X5R, ROHS	PANASONIC
1514-2	5	ea.	P3, P4, P5, P7, P9	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE
5002	5	ea.	P1, P2, P6, P8, P10	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	KEYSTONE
1N5819HW-7-F	1	ea.	D1	DIODE-RECTIFIER, SMD, 2P, SOD-123, 40V, 1A, ROHS	DIODES, INC.
ISL85415FRZ	1	ea.	U1	IC-500mA BUCK REGULATOR, 12P, DFN, 3X4, ROHS	INTERSIL
750314712	1	ea.	L1	TRANSFORMER- CUSTOM, SMD, 6P, 10.16 x11.66, 22μH, 10%, 2.5A, ROHS	WURTH ELECTRONICS MIDCOM INC.
	0	ea.	R8-R11, R15	RES, SMD, 0402, DNP, DNP, DNP, TF, ROHS	
ERJ2RKF1003	1	ea.	R3	RES, SMD, 0402, 100k, 1/16W, 1%, TF, ROHS	PANASONIC
ERJ-2RKF1051X	2	ea.	R13, R14	RES, SMD, 0402, 1.05k, 1/16W, 1%, TF, ROHS	PANASONIC
MCR01MZPF1203	1	ea.	R12	RES, SMD, 0402, 120k, 1/16W, 1%, TF, ROHS	ROHM
ERJ2RKF2001	1	ea.	R2	RES, SMD, 0402, 20k, 1/16W, 1%, TF, ROHS	PANASONIC
MCR01MZPF2003	2	ea.	R6, R7	RES, SMD, 0402, 200k, 1/16W, 1%, TF, ROHS	ROHM
CRCW040290K9FKED	1	ea.	R1	RES, SMD, 0402, 90.9k, 1/16W, 1%, TF, ROHS	VISHAY/DALE
D810 (212403-012)	1	ea.	PLACE ASSY IN BAG	BAG, STATIC, 3X5, ZIP LOC	INTERSIL COMMON STOCK
LABEL-DATE CODE	1	ea.	AFFIX TO BACK OF PCB	LABEL-DATE CODE_LINE 1: YRWK/REV#, LINE 2: BOM NAME	INTERSIL
ISL85415DEMO2ZREVAPCB	1	ea.		PWB-PCB, ISL85415DEMO2Z, REVA, ROHS	IMAGINEERING INC

ISL85415DEMO2Z Board Layout

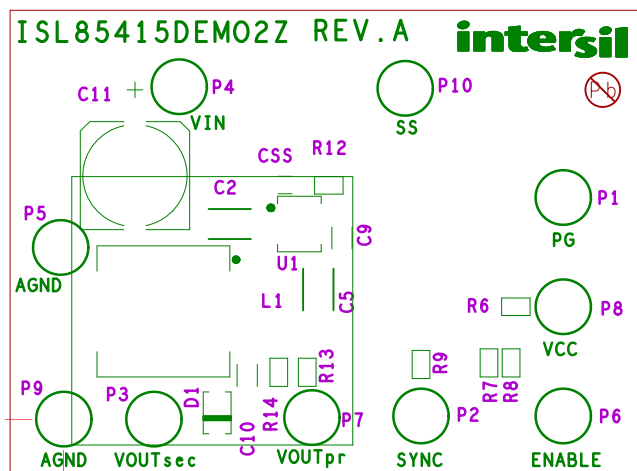


FIGURE 4. SILKSCREEN TOP

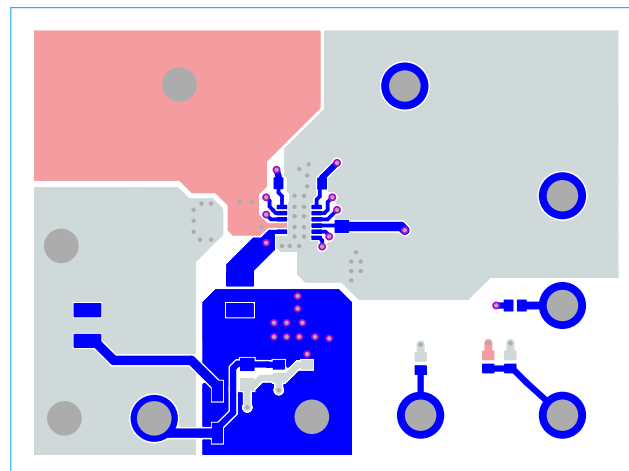


FIGURE 5. TOP LAYER

ISL85415DEMO2Z Board Layout (Continued)

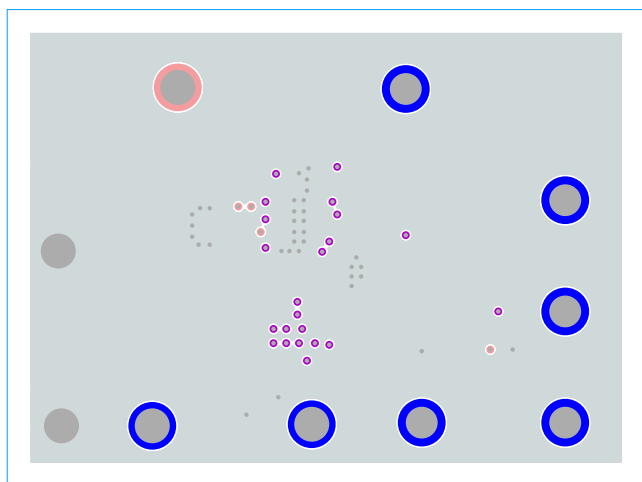


FIGURE 6. LAYER 2

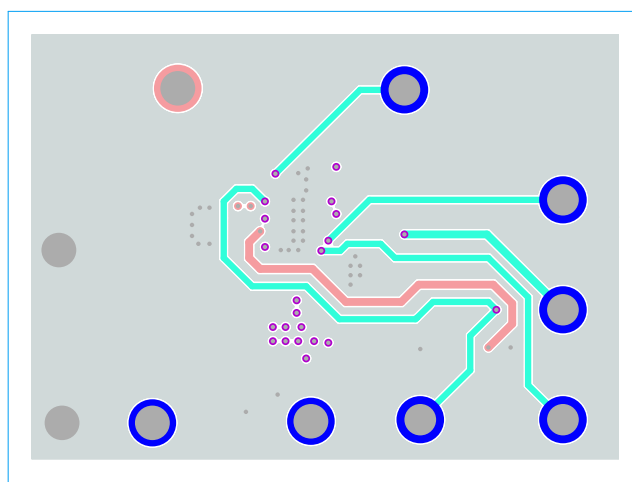


FIGURE 7. LAYER 3

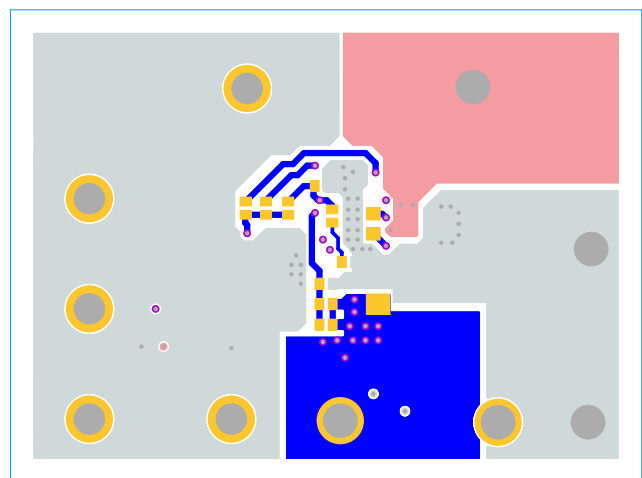


FIGURE 8. BOTTOM LAYER

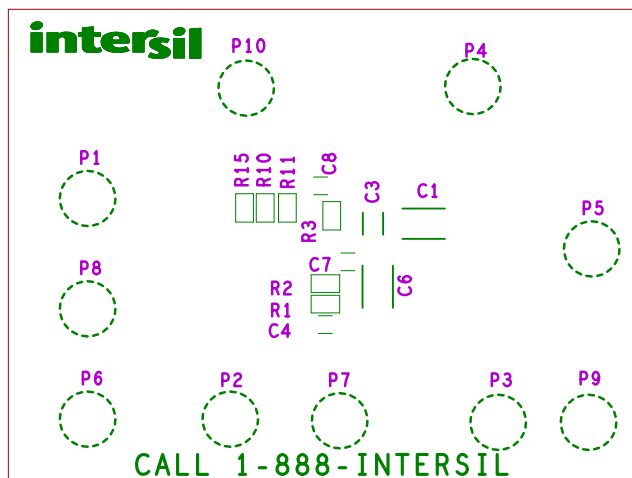


FIGURE 9. SILKSCREEN BOTTOM

Typical Performance Curves $f_{SW} = 800\text{kHz}$, $T_A = +25^\circ\text{C}$.

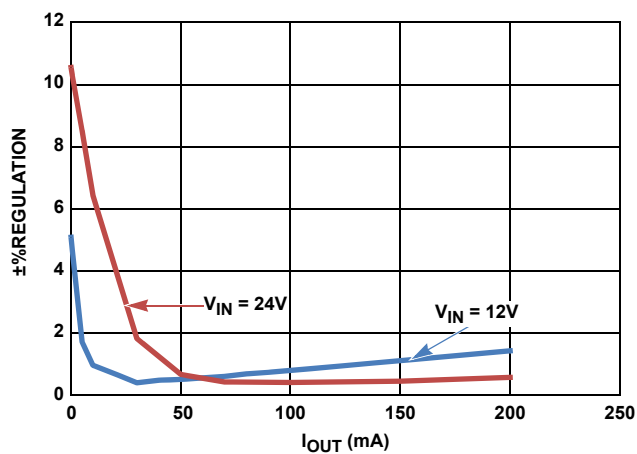


FIGURE 10. $V_{OUT} = 5\text{V}$, $\% \text{REGULATION}$ vs I_{OUT}

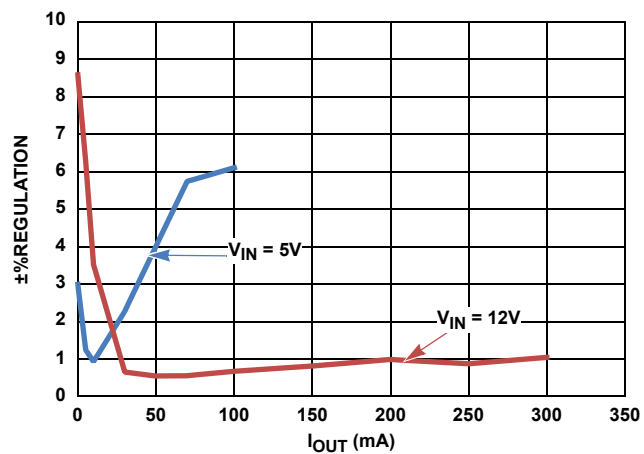


FIGURE 11. $V_{OUT} = 3.3\text{V}$, $\% \text{REGULATION}$ vs I_{OUT}

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(Rev.4.0-1 November 2017)



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