X28HC64

64k, 8k x 8-Bit 5 Volt, Byte Alterable EEPROM

FN8109
Rev 4.00
June 27, 2016

The X28HC64 is an 8k x 8 EEPROM, fabricated with Intersil's proprietary, high performance, floating gate CMOS technology. Like all Intersil programmable nonvolatile memories, the X28HC64 is a 5V only device. It features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28HC64 supports a 64-byte page write operation, effectively providing a 32µs/byte write cycle, and enabling the entire memory to be typically written in 0.25 seconds. The X28HC64 also features $\overline{\text{DATA}}$ Polling and Toggle Bit Polling, two methods providing early end of write detection. In addition, the X28HC64 includes a user-optional software data protection mode that further enhances Intersil's hardware write protect capability.

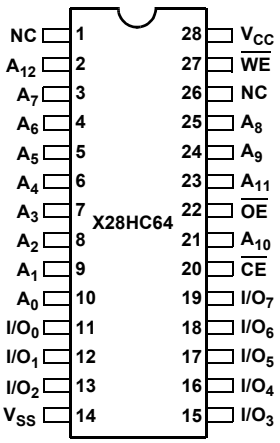
Intersil EEPROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

Features

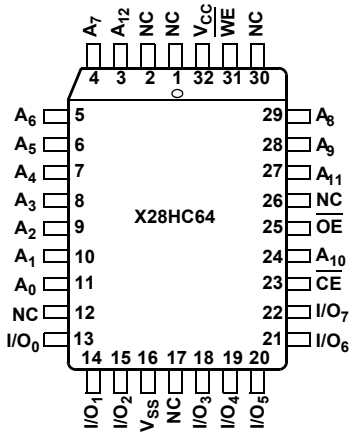
- 70ns access time
- Simple byte and page write
  - Single 5V supply
  - No external high voltages or V_{P-P} control circuits
  - Self-timed
  - No erase before write
  - No complex programming algorithms
  - No overerase problem
- Low power CMOS
  - 40mA active current maximum
- 200µA standby current maximum
- Fast write cycle times
  - 64-byte page write operation
  - Byte or page write cycle: 2ms typical
  - Complete memory rewrite: 0.25s typical
  - Effective byte write cycle time: 32µs typical
- Software data protection
- End of write detection
  - DATA polling
  - Toggle bit
- High reliability
  - Endurance: 100,000 cycles
  - Data retention: 100 years
- JEDEC approved byte-wide pinout
- Pb-free available (RoHS compliant)

Pin Configurations

X28HC64
(28 LD PDIP, SOIC)
TOP VIEW



X28HC64
(32 LD PLCC)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	TEMPERATURE RANGE (°C)	ACCESS TIME (ns)	PACKAGE	PKG. DWG. #
X28HC64J-70 (Notes 1, 6) (No longer available, recommended replacement: X28HC64JZ-70)	X28HC64J-70 CY	0 to +70	70	32 Ld PLCC	N32.45x55
X28HC64JIZ-70 (Notes 1, 4, 6)	X28HC64JI-70 ZCY	-40 to +85		32 Ld PLCC (RoHS Compliant)	N32.45x55
X28HC64JZ-70 (Notes 1, 4, 6)	X28HC64J-70 ZCY	0 to +70		32 Ld PLCC (RoHS Compliant)	N32.45x55
X28HC64SIZ-70 (Notes 4, 6)	X28HC64SI-70 CYZ	-40 to +85		28 Ld SOIC (300 mil) (RoHS Compliant)	M28.3
X28HC64SZ-70 (Notes 4, 6)	X28HC64S-70 CYZ	0 to +70		28 Ld SOIC (300 mil) (RoHS Compliant)	M28.3
X28HC64J-90 (Notes 1, 6) (No longer available, recommended replacement: X28HC64JIZ-90)	X28HC64J-90 CY	0 to +70	90	32 Ld PLCC	N32.45x55
X28HC64JI-90 (Notes 1, 3, 6) (No longer available, recommended replacement: X28HC64JIZ-90)	X28HC64JI-90 CY	-40 to +85		32 Ld PLCC	N32.45x55
X28HC64JIZ-90 (Notes 1, 4, 6)	X28HC64JI-90 ZCY	-40 to +85		32 Ld PLCC (RoHS Compliant)	N32.45x55
X28HC64PIZ-90 (Notes 4, 5)	X28HC64PI-90 CYZ	-40 to +85		28 Ld PDIP (RoHS Compliant)	E28.6
X28HC64PZ-90 (Notes 4, 5)	X28HC64P-90 CYZ	0 to +70		28 Ld PDIP (RoHS Compliant)	E28.6
X28HC64J-12 (Notes 1, 6) (No longer available, recommended replacement: X28HC64JZ-12)	X28HC64J-12 CY	0 to +70	120	32 Ld PLCC	N32.45x55
X28HC64JI-12 (Notes 1, 6) (No longer available, recommended replacement: X28HC64JIZ-12)	X28HC64JI-12 CY	-40 to +85		32 Ld PLCC	N32.45x55
X28HC64JIZ-12 (Notes 1, 4, 6)	X28HC64JI-12 ZCY	-40 to +85		32 Ld PLCC (RoHS Compliant)	N32.45x55
X28HC64JZ-12* (Notes 1, 4, 6)	X28HC64J-12 ZCY	0 to +70		32 Ld PLCC (RoHS Compliant)	N32.45x55
X28HC64PIZ-12 (Notes 4, 5)	X28HC64PI-12 CYZ	-40 to +85		28 Ld PDIP (RoHS Compliant)	E28.6
X28HC64PZ-12 (Notes 4, 5)	X28HC64P-12 CYZ	0 to +70		28 Ld PDIP (RoHS Compliant)	E28.6
X28HC64SIZ-12 (Notes 2, 4, 6)	X28HC64SI-12 CYZ	-40 to +85		28 Ld SOIC (300 mil) (RoHS Compliant)	M28.3
X28HC64SZ-12 (Notes 4, 6)	X28HC64S-12 CYZ	0 to +70		28 Ld SOIC (300 mil) (RoHS Compliant)	M28.3

NOTES:

1. Add “T1” suffix for 750 unit tape and reel option.
2. Add “T1” suffix for 1000 unit tape and reel option.
3. Add “T2” suffix for 750 unit tape and reel option.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.
6. For Moisture Sensitivity Level (MSL), please see product information page for X28HC64. For more information on MSL, please see tech brief TB363.

Pin Descriptions

SYMBOL	DESCRIPTION
A_0-A_{12}	Address Inputs. The Address inputs select an 8-bit memory location during a read or write operation.
I/O_0-I/O_7	Data Input/Output. Data is written to or read from the X28HC64 through the I/O pins.
$\overline{WE}$	Write Enable. The Write Enable input controls the writing of data to the X28HC64.
$\overline{CE}$	Chip Enable. The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.
$\overline{OE}$	Output Enable. The Output Enable input controls the data output buffers and is used to initiate read operations.
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

Block Diagram

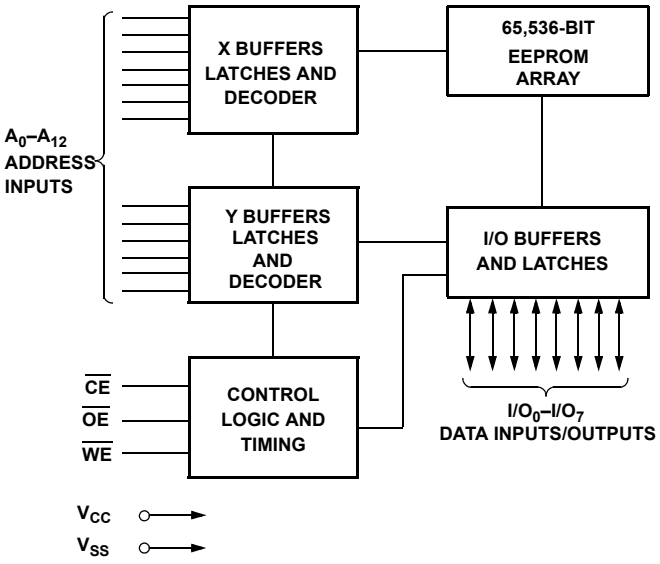


FIGURE 1. BLOCK DIAGRAM

Device Operation

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28HC64 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 2ms.

Page Write Operation

The page write feature of the X28HC64 allows the entire memory to be written in 0.25 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28HC64 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_6 through A_{12}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The X28HC64 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 2.

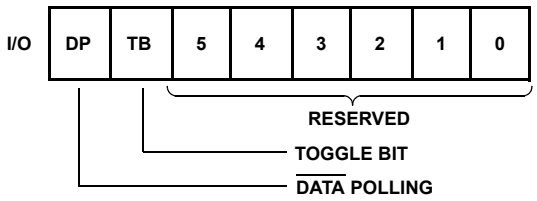


FIGURE 2. STATUS BIT ASSIGNMENT

$\overline{\text{DATA}}$ Polling (I/O_7)

The X28HC64 features $\overline{\text{DATA}}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{\text{DATA}}$ Polling allows a simple bit test operation to determine the status of the X28HC64, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

$\overline{\text{DATA}}$ Polling can effectively reduce the time for writing to the X28HC64. The timing diagram in Figure 3 illustrates the sequence of events on the bus. The software flow diagram in Figure 4 illustrates one method of implementing the routine.

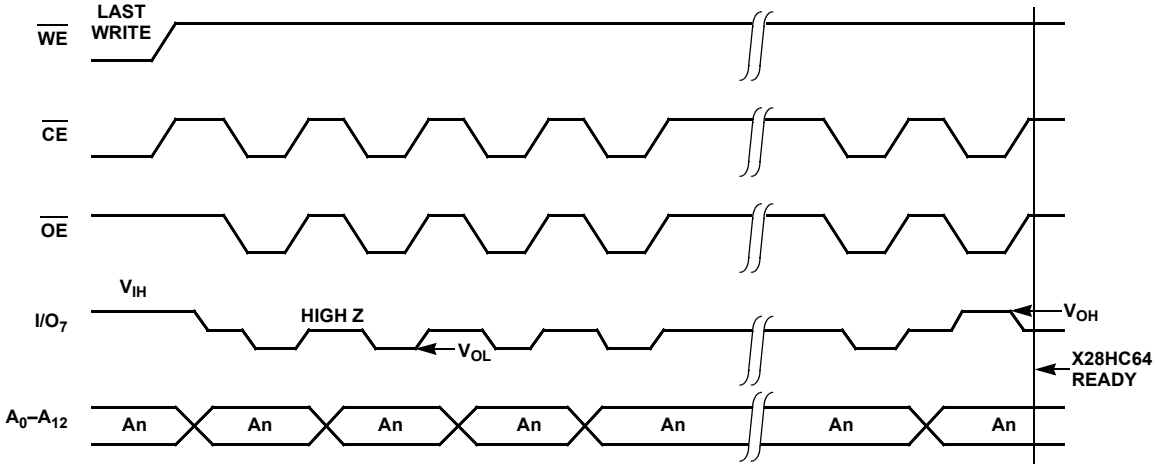


FIGURE 3. $\overline{\text{DATA}}$ POLLING BUS SEQUENCE

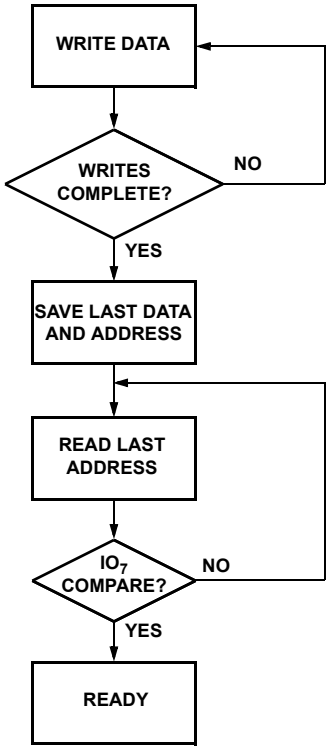


FIGURE 4. $\overline{\text{DATA}}$ POLLING SOFTWARE FLOW

Toggle Bit (I/O_6)

The X28HC64 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete, the toggling will cease and the device will be accessible for additional read or write operations.

The Toggle Bit can eliminate the chore of saving and fetching the last address and data in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28HC64 memories that is frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 5 illustrates the sequence of events on the bus. The software flow diagram in Figure 6 illustrates a method for polling the Toggle Bit.

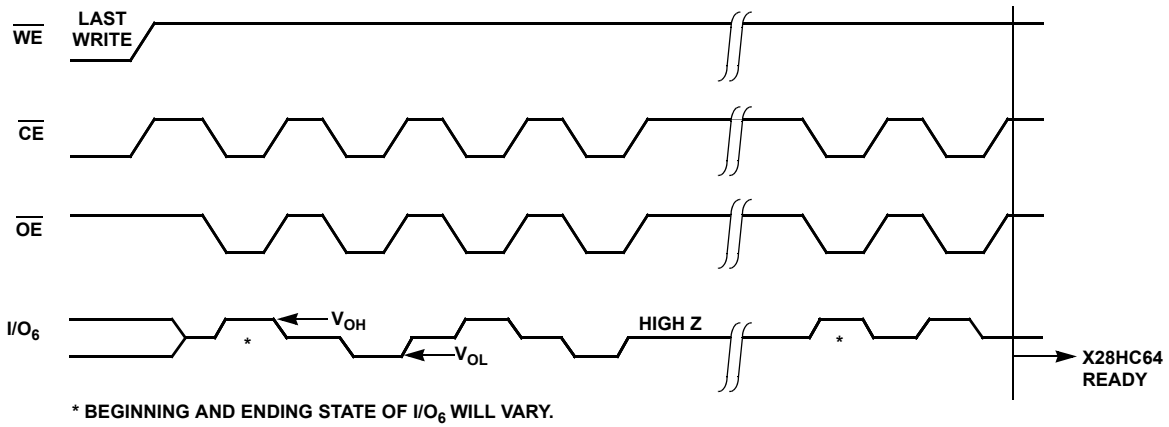


FIGURE 5. TOGGLE BIT BUS SEQUENCE

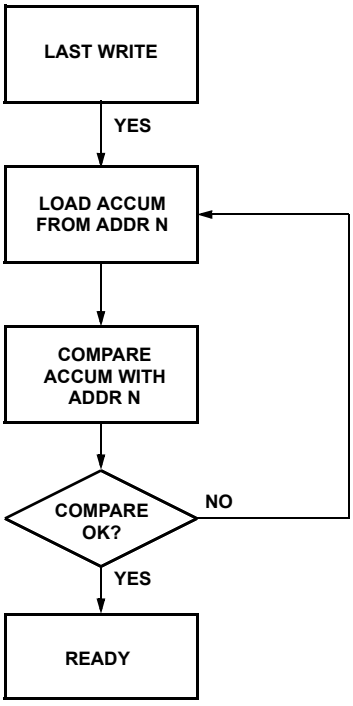


FIGURE 6. TOGGLE BIT SOFTWARE FLOW

Hardware Data Protection

The X28HC64 provides two hardware features that protect nonvolatile data from inadvertent writes.

- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is 3V typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

Software Data Protection

The X28HC64 offers a software controlled data protection feature. The X28HC64 is shipped from Intersil with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/power-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28HC64 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device, unless the reset command is issued.

Once the software protection is enabled, the X28HC64 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device.

Software Algorithm

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figures 7 and 8 for the sequence. The 3-byte sequence opens the page write window, enabling the host to write from 1 to 64 bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used, the X28HC64 will automatically disable further writes unless another command is issued to deactivate it. If no further commands are issued, the X28HC64 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

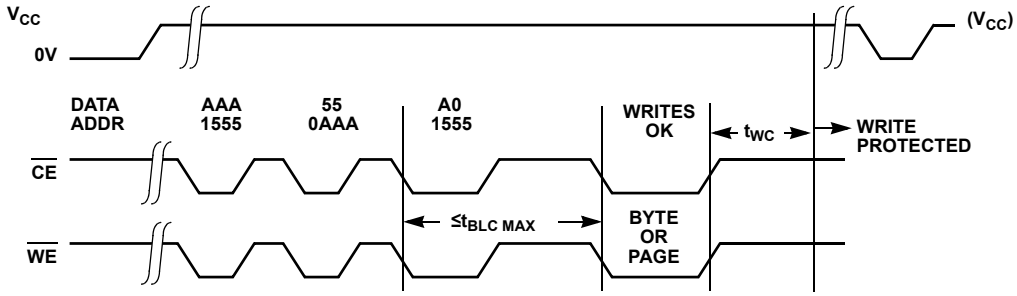


FIGURE 7. TIMING SEQUENCE—BYTE OR PAGE WRITE

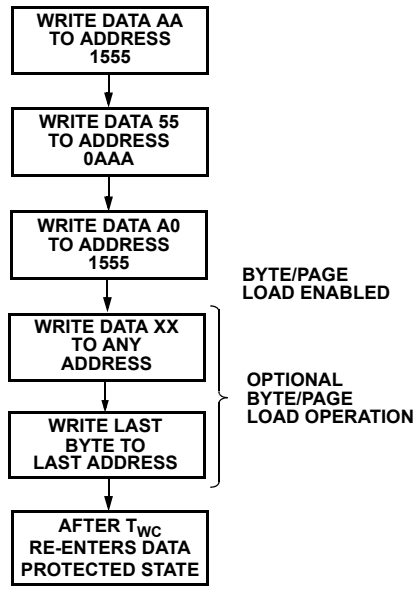


FIGURE 8. WRITE SEQUENCE FOR SOFTWARE DATA PROTECTION

Resetting Software Data Protection

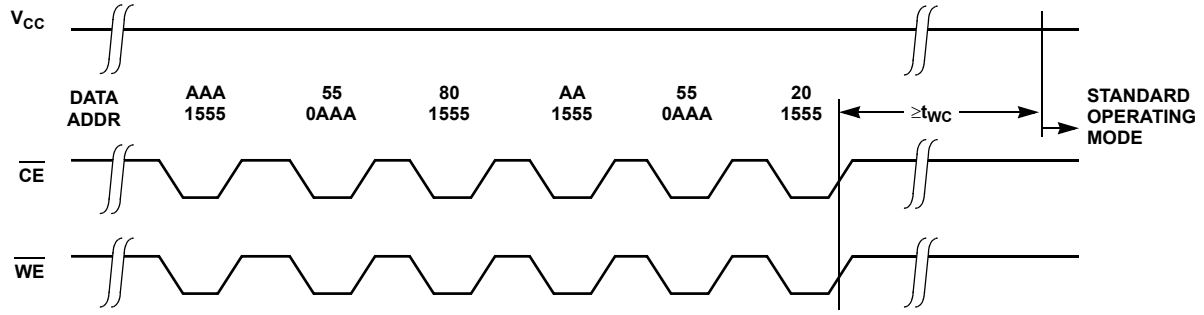


FIGURE 9. RESET SOFTWARE DATA PROTECTION TIMING SEQUENCE

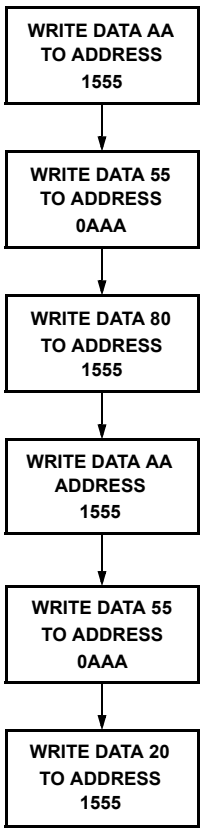


FIGURE 10. SOFTWARE SEQUENCE TO DEACTIVATE SOFTWARE DATA PROTECTION

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an EEPROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28HC64 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

System Considerations

Because the X28HC64 is frequently used in large memory arrays, it is provided with a two-line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation, and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit, it is recommended that $\overline{CE}$ be decoded from the address bus, and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation, this assures that all deselected devices are in their standby mode, and that only the selected device(s) is/are outputting data on the bus.

Because the X28HC64 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

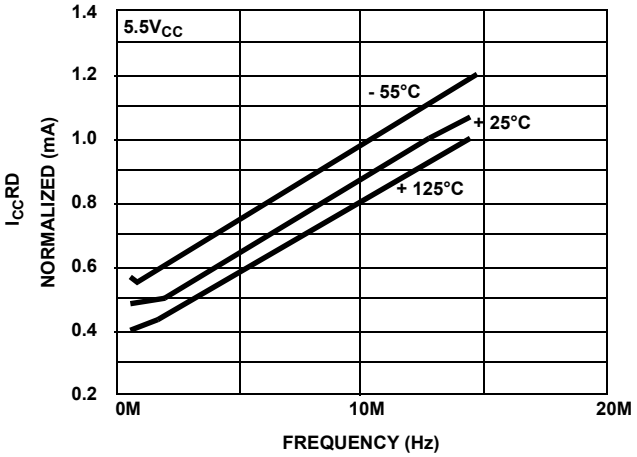


FIGURE 11. NORMALIZED I_{CC}(RD) BY TEMPERATURE OVER FREQUENCY DATA PROTECTION

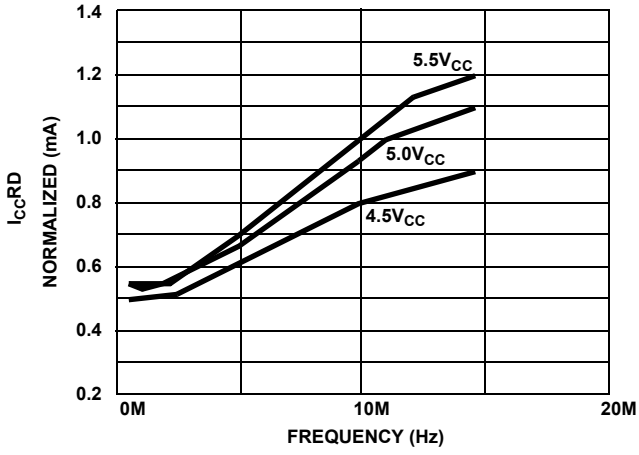


FIGURE 12. NORMALIZED I_{CC}(RD) AT 25% OVER THE V_{CC} RANGE AND FREQUENCY

Absolute Maximum Ratings

Temperature Under Bias
- X28HC64 . . . . . -10°C to +85°C
- X28HC64I . . . . . -65°C to +135°C

Storage Temperature . . . . . -65°C to +150°C
Voltage on any Pin with Respect to V_{SS} . . . . . -1V to +7V
DC Output Current 5mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld PLCC Package (Notes 7, 9)	41	19
28 Ld SOIC Package (Notes 7, 9)	46	19
28 Ld PDIP Package (Notes 8, 9)	53	21

Pb-Free Reflow Profile . . . . . see TB493

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Recommended Operating Conditions

Commercial Temperature Range . . . . . 0°C to +70°C
Industrial Temperature Range . . . . . -40°C to +85°C
Supply Voltage Range
- X28HC64 . . . . . 5V ±10%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

7. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
8. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
9. For θ_{JC}, the "case temp" location is taken at the package top center.

DC Electrical Specifications

Over recommended operating conditions, unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 10)	TYP (Note 11)	MAX (Note 10)	UNIT
V_{CC} Current (Active) (TTL Inputs)	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = open, address inputs = TTL levels at f = 10MHz		15	40	mA
V_{CC} Current (Standby) (TTL Inputs)	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = open, other inputs = V_{IH}		1	2	mA
V_{CC} Current (Standby) (CMOS Inputs)	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.3V, $\overline{OE}$ = GND, All I/O's = open, other inputs = V_{CC} - 0.3V		100	200	µA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}			±10	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}			±10	µA
Input LOW Voltage (Note 12)	V_{IL}		-1		0.8	V
Input HIGH Voltage (Note 12)	V_{IH}		2		V_{CC} + 1	V
Output LOW Voltage	V_{OL}	I_{OL} = 5mA			0.4	V
Output HIGH Voltage	V_{OH}	I_{OH} = -5mA	2.4			V

NOTES:

10. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
11. Typical values are for T_A = +25°C and nominal supply voltage.
12. V_{IL} minimum and V_{IH} maximum are for reference only and are not tested.

Endurance and Data Retention

The endurance and data retention specifications are established by characterization and are not production tested.

PARAMETER	MIN	MAX	UNIT
Minimum Endurance	100,000		Cycles
Data Retention	100		Years

Power-Up Timing

PARAMETER	SYMBOL	TYP (Note 11)	UNIT
Power-Up to Read Operation (Note 13)	t_{PUR}	100	µs
Power-Up to Write Operation (Note 13)	t_{PUW}	5	ms

Capacitance $T_A = +25°C$, f = 1MHz, V_{CC} = 5V

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT
Input/output Capacitance (Note 13)	$C_{I/O}$	$V_{I/O}$ = 0V	10	pF
Input Capacitance (Note 13)	C_{IN}	V_{IN} = 0V	6	pF

NOTE:
13. This parameter is periodically sampled and not 100% tested.

TABLE 1. AC CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

TABLE 2. MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and write inhibit	High Z	Standby
X	L	X	Write inhibit	-	-
X	X	H	Write inhibit	-	-

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Equivalent AC Load Circuits

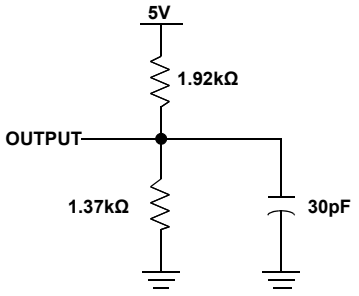


FIGURE 13. EQUIVALENT AC LOAD CIRCUITS

AC Electrical Specifications

Read Cycle Limits

Over the recommended operating conditions unless otherwise specified.

PARAMETER	SYMBOL	X28HC64-70		X28HC64-90		X28HC64-12		UNIT
		MIN (Note 10)	MAX (Note 10)	MIN (Note 10)	MAX (Note 10)	MIN (Note 10)	MAX (Note 10)	
Read Cycle Time	t_{RC}	70		90		120		ns
Chip Enable Access Time	t_{CE}		70		90		120	ns
Address Access Time	t_{AA}		70		90		120	ns
Output Enable Access Time	t_{OE}		35		40		50	ns
$\overline{CE}$ LOW to Active Output (Note 14)	t_{LZ}	0		0		0		ns
$\overline{OE}$ LOW to Active Output (Note 14)	t_{OLZ}	0		0		0		ns
$\overline{CE}$ HIGH to High Z Output (Note 14)	t_{HZ}		30		30		30	ns
$\overline{OE}$ HIGH to High Z Output (Note 14)	t_{OHZ}		30		30		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

NOTE:

14. t_{LZ} minimum, t_{HZ}, t_{OLZ} minimum, and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} maximum and t_{OHZ} maximum are measured from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

Read Cycle

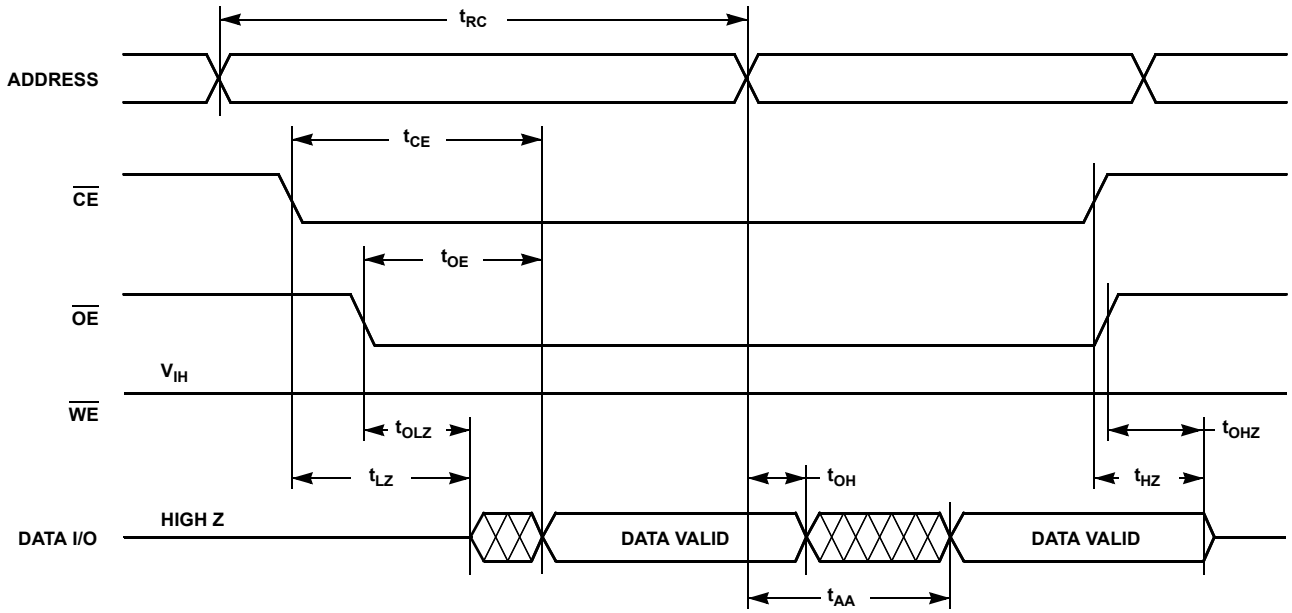


FIGURE 14. READ CYCLE

Write Cycle Limits

PARAMETER	SYMBOL	MIN (Note 10)	TYP (Note 11)	MAX (Note 10)	UNIT
Write Cycle Time (Note 15)	t_{WC}		2	5	ms
Address Set-Up Time	t_{AS}	0			ns
Address Hold Time	t_{AH}	50			ns
Write Set-Up Time	t_{CS}	0			ns
Write Hold Time	t_{CH}	0			ns
$\overline{CE}$ Pulse Width	t_{CW}	50			ns
$\overline{OE}$ High Set-Up Time	t_{OES}	0			ns
$\overline{OE}$ High Hold Time	t_{OEH}	0			ns
$\overline{WE}$ Pulse Width	t_{WP}	50			ns
$\overline{WE}$ HIGH Recovery (Note 16)	t_{WPH}	50			ns
Data Valid (Note 16)	t_{DV}			1	µs
Data Setup	t_{DS}	50			ns
Data Hold	t_{DH}	0			ns
Delay to Next Write (Note 16)	t_{DW}	10			µs
Byte Load Cycle	t_{BLC}	0.15		100	µs

NOTES:

15. t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

16. t_{WPH} and t_{DW} are periodically sampled and not 100% tested.

$\overline{WE}$ Controlled Write Cycle

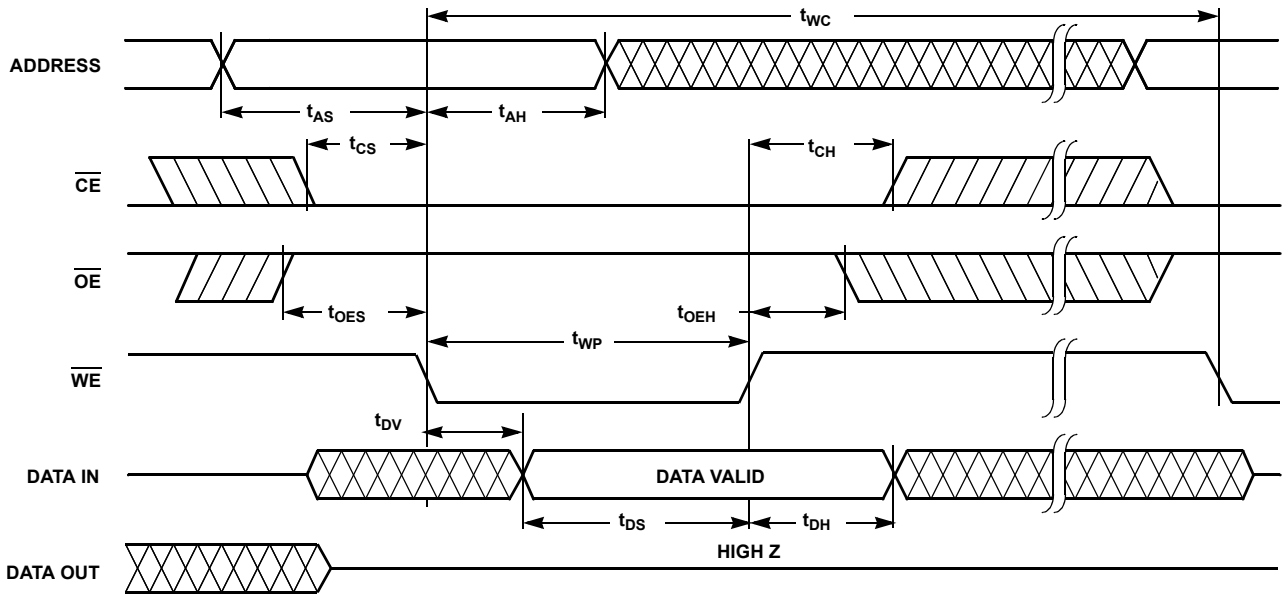


FIGURE 15. $\overline{WE}$ CONTROLLED WRITE CYCLE

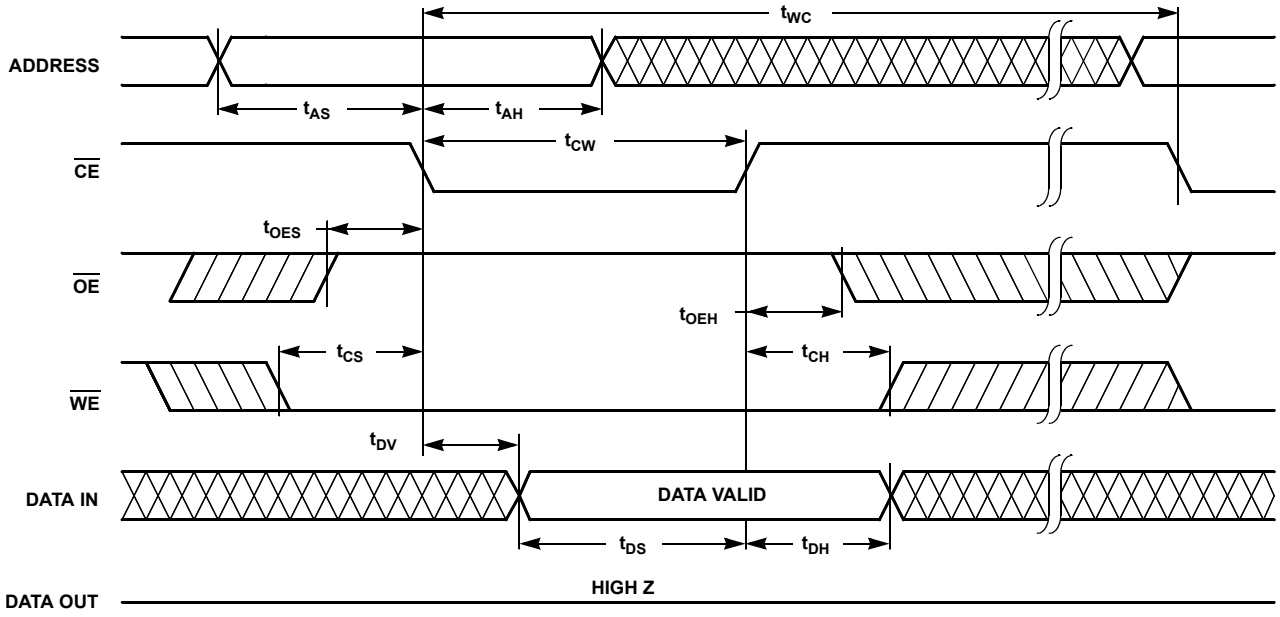
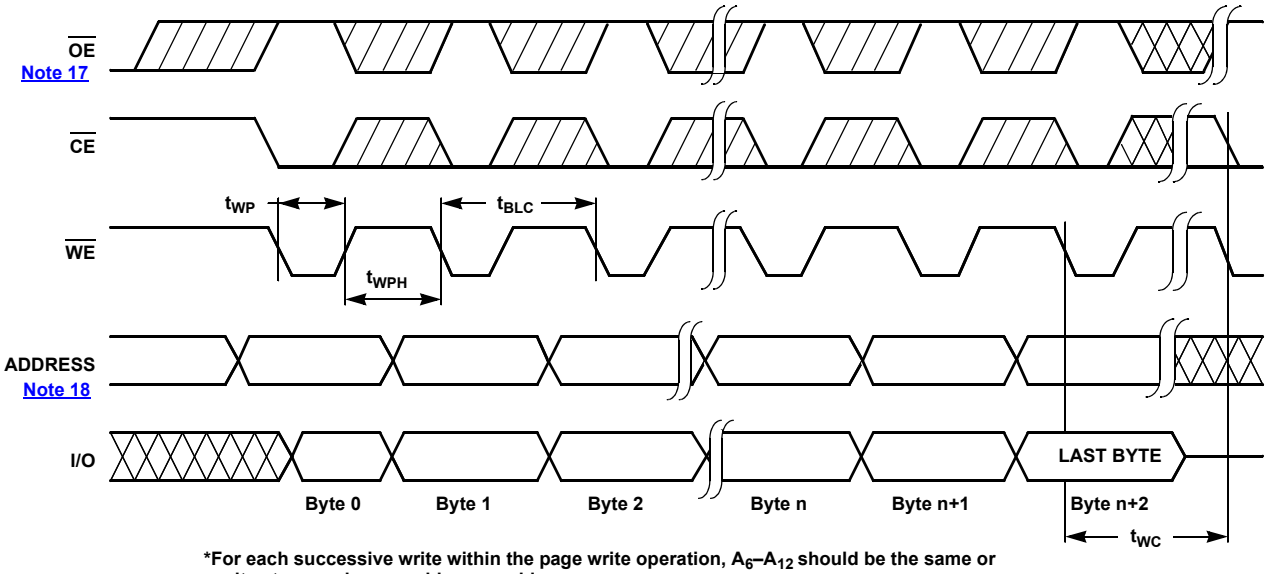


FIGURE 16. $\overline{CE}$ CONTROLLED WRITE CYCLE



*For each successive write within the page write operation, A_6–A_{12} should be the same or writes to an unknown address could occur.

FIGURE 17. PAGE WRITE CYCLE

NOTES:

17. Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

18. The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

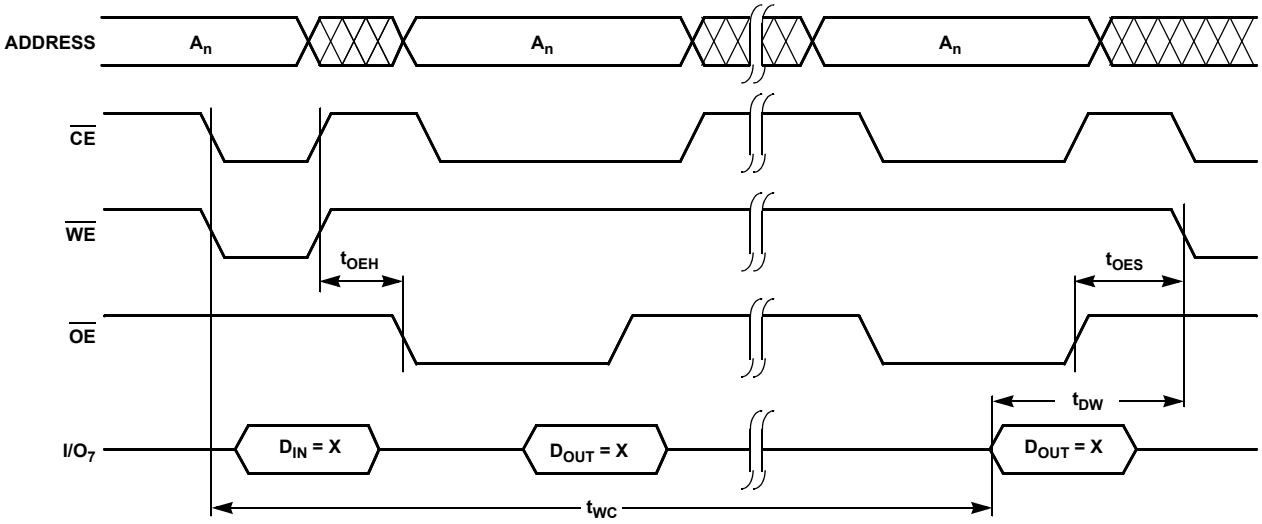
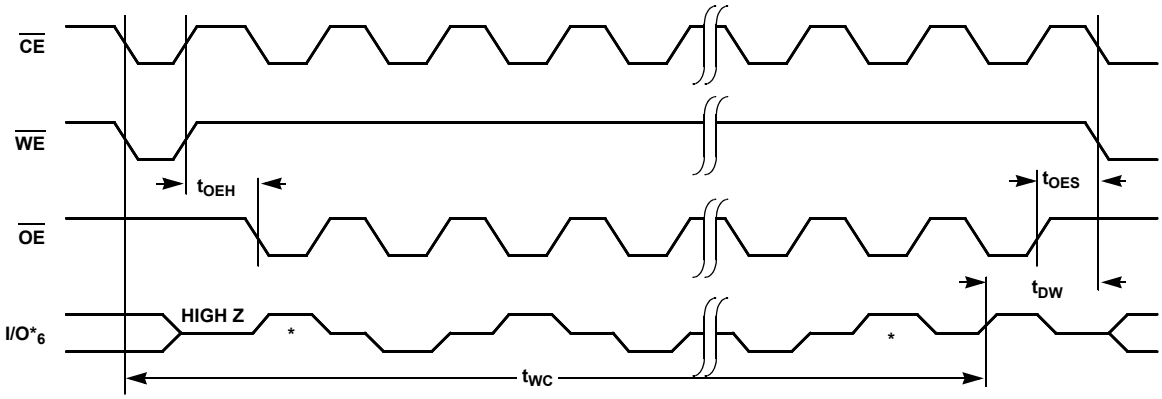


FIGURE 18. $\overline{DATA}$ POLLING TIMING DIAGRAM (Note 19)



* I/O_6 beginning and ending state will vary, depending upon actual t_{WC}.

FIGURE 19. TOGGLE BIT TIMING DIAGRAM (Note 19)

NOTE:

19. Polling operations are by definition read cycles and are therefore subject to read cycle timings.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
June 27, 2016	FN8109.4	Updated entire datasheet applying Intersil's new standards. Updated the Ordering Information table by adding Note 2, updated other tape and reel notes, updated all of the part marking and added Note 6. Added Thermal Information (Theta JA, Theta JC, and applicable notes) on page 9. Added "The endurance and data retention specifications are established by characterization and are not production tested" to the "Endurance and Data Retention" table.
August 18, 2015	FN8109.3	- Updated Ordering Information Table on page 2. - Added Revision History and About Intersil sections. - Updated POD M28.3 to latest revision changes are as follow: Added land pattern.

About Intersil

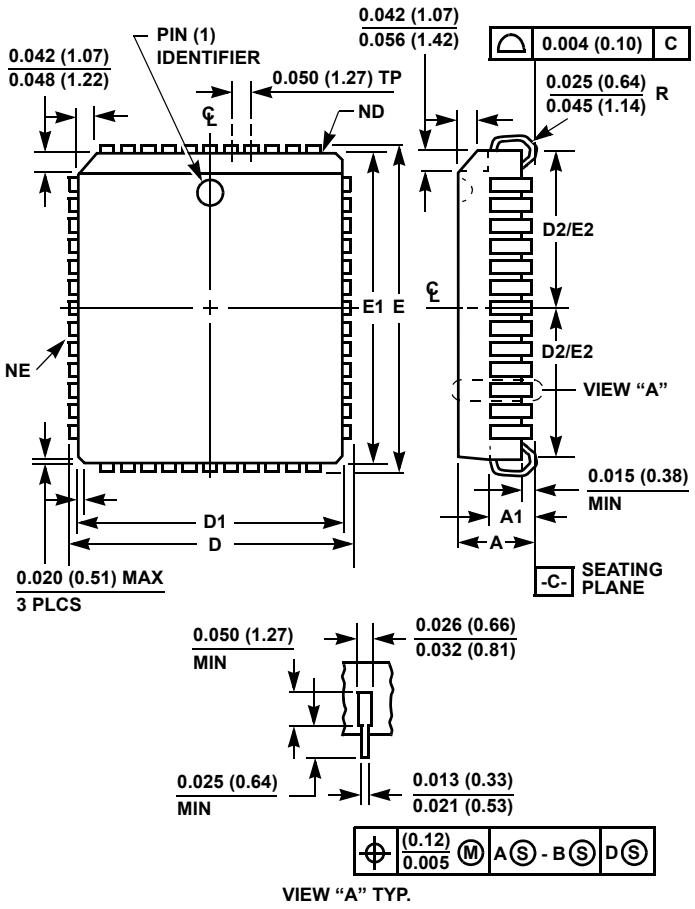
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

Plastic Leaded Chip Carrier Packages (PLCC)



N32.45x55 (JEDEC MS-016AE ISSUE A)

32 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

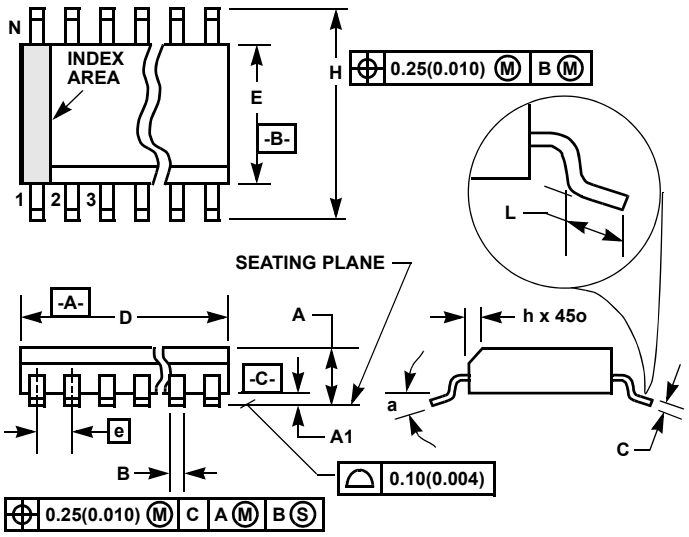
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.125	0.140	3.18	3.55	-
A1	0.060	0.095	1.53	2.41	-
D	0.485	0.495	12.32	12.57	-
D1	0.447	0.453	11.36	11.50	3
D2	0.188	0.223	4.78	5.66	4, 5
E	0.585	0.595	14.86	15.11	-
E1	0.547	0.553	13.90	14.04	3
E2	0.238	0.273	6.05	6.93	4, 5
N	28		28		6
ND	7		7		7
NE	9		9		7

Rev. 0 7/98

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.
7. ND denotes the number of leads on the two shorts sides of the package, one of which contains pin #1. NE denotes the number of leads on the two long sides of the package.

Small Outline Plastic Packages (SOIC)

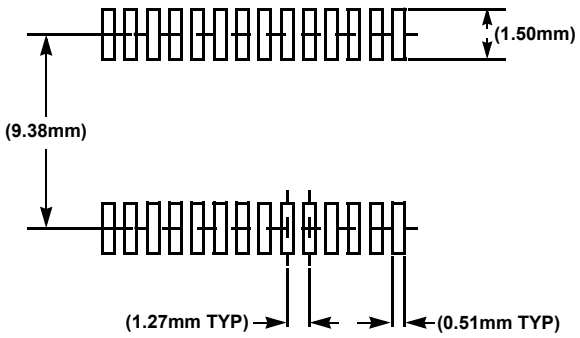


M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 1, 1/13

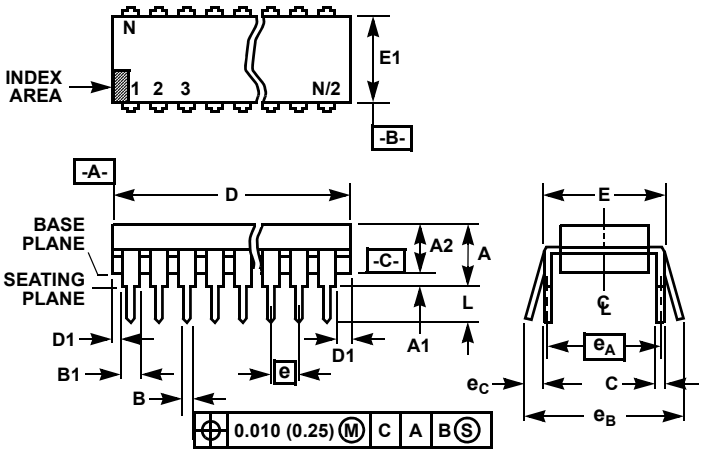
TYPICAL RECOMMENDED LAND PATTERN



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-011-AB ISSUE B)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

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