

# Rail to Rail I/O 375 nA/Amp Dual/Quad CMOS Op Amps with Power Down

### **General Description**

### **Pin Configurations**

The SLG88103/4 is a wide voltage range, 375 nA Dual/Quad Channel CMOS Input Operational Amplifier capable of rail-to-rail input and output operation. Each Amplifier can be individually powered down.

# **Features**

- Low Quiescent Current: 375 nA per Amplifier (typ)
- Low Offset Voltage: ±200 µV (typ) •
- Zero-Crossover
- Low Offset Drift: 1 µV/°C (typ)
- DC Precision: •
  - PSRR: 115 dB
  - CMRR: 100 dB
  - A<sub>OI</sub>: 120 dB
- Gain-Bandwidth Product: 10 kHz (typ)
- Rail to Rail Input/Output
- Supply Voltage: 1.71 V to 5.5 V
- Tiny Package:
- 10-pin 2 x 2 mm STDFN
- 20-pin 2 x 3.5 mm STQFN
- Industrial Temperature Range: -40 °C to 85 °C

# **Typical Applications**

- **Battery-Powered Devices** •
- Portable Devices •
- Wearable Products
- Gas Sensors
- Pressure Sensors
- Medical Monitors •
- Smoke Detectors •
- Active RFID Reader
- ٠ **Energy Harvester**

### Example Application Circuit: Non-Inverting Amplifier + GreenPAK with Wake-Sleep Controller



#### 10 - - -PD1 1 VDD OUT1 2 ٦ OUT2 9 <sup>r</sup> IN-1 3 8 -IN-2 IN+1 ٦4 7 ' IN+2 VSS 5 6 [ PD2 10-pin STDFN (Top View)

SLG88103

# SLG88104





# **Pin Description**

Piı	n #			
20L STQFN	10L STDFN	Pin Name	Туре	Pin Description
1	2	OUT1	0	Analog Output (Op Amp 1)
2	3	IN-1	I	Inverting Input (Op Amp 1)
3	4	IN+1	I	Non-inverting Input (Op Amp 1)
4	5	VSS	GND	Negative Power Supply
5	6	PD2	I	Power Down Input (Op Amp 2) When PD pin is high, the respective amplifier is powered down.
6	9	OUT2	0	Analog Output (Op Amp 2)
7	8	IN-2	I	Inverting Input (Op Amp 2)
8	7	IN+2	I	Non-inverting Input (Op Amp 2)
9		VSS	GND	Negative Power Supply
10		PD3	I	Power Down Input (Op Amp 3) When PD pin is high, the respective amplifier is powered down.
11		IN+3	I	Non-inverting Input (Op Amp 3)
12		IN-3	I	Inverting Input (Op Amp 3)
13		OUT3	0	Analog Output (Op Amp 3)
14	10	VDD	PWR	Power Supply
15		PD4	I	Power Down Input (Op Amp 4) When PD pin is high, the respective amplifier is powered down.
16		IN+4	I	Non-inverting Input (Op Amp 4)
17		IN-4	I	Inverting Input (Op Amp 4)
18		OUT4	0	Analog Output (Op Amp 4)
19		VDD	PWR	Power Supply
20	1	PD1	I	Power Down Input (Op Amp 1) When PD pin is high, the respective amplifier is powered down.

# **Ordering Information**

Part Number	Туре	Production Flow		
SLG88103V	10-pin STDFN	Industrial, -40 °C to 85 °C		
SLG88103VTR	10-pin STDFN (Tape and Reel)	Industrial, -40 °C to 85 °C		
SLG88104V	20-pin STQFN	Industrial, -40 °C to 85 °C		
SLG88104VTR	20-pin STQFN (Tape and Reel)	Industrial, -40 °C to 85 °C		



### **Absolute Maximum Ratings**

Parameter	Description	Min.	Тур.	Max.	Unit	
V <sub>DD</sub>	Voltage on VDD pin relative to GND	-0.3		6.0	V	
T <sub>A</sub>	Operating Range	-40		85	°C	
$\theta_{JA}$	Thermal Resistance	80 °C				
Τ <sub>S</sub>	Storage Temperature	-65		150	°C	
TJ	Junction Temperature			150	°C	
ESD <sub>HBM</sub>	ESD Protection (Human Body Model)	2000			V	
ESD <sub>CDM</sub>	ESD Protection (Charged Device Model)	500			V	
MSL	Moisture Sensitivity Level	1				
Note: Stresses only and specifica	s greater than those listed under "Absolute Maximum Ratings" may cause I functional operation of the device at these or any other conditions at ation is not implied. Exposure to absolute maximum rating conditions for	e permanent da pove those inc extended peri	amage to the d licated in the ods may affect	evice. This is a operational se t reliability.	a stress rating ections of this	

# **Electrical Characteristics**

 $T_A = 25 \text{ °C}, V_{DD} = 1.71 \text{ V to } 5.5 \text{ V}, V_{SS} = \text{GND}, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 \text{ M}\Omega \text{ to } V_L, \text{ unless otherwise stated}.$ 

-	-		אני	IVIAX	Unit	
Input Offset						
		$V_{CM} = V_{DD}/2$	-1000	±200	1000	μV
V <sub>OS</sub> I	Input Offset Voltage	V <sub>CM</sub> = V <sub>DD</sub> /2; T <sub>A</sub> = -40 °C to 85 °C	-1100	±250	1100	μV
		V <sub>CM</sub> = V <sub>SS</sub> ; T <sub>A</sub> = -40 °C to 85 °C	-2400	±350	2400	μV
dVoo/dT	Offset Drift with Temperature	V <sub>CM</sub> = V <sub>DD</sub> /2; T <sub>A</sub> = -40 °C to 85 °C	-4	±1	4	μV/°C
		V <sub>CM</sub> = V <sub>SS</sub> ; T <sub>A</sub> = -40 °C to 85 °C	-10	±2	10	μV/°C
dV/Time	10 Vear Offset Drift	T <sub>A</sub> = 85°C; V <sub>DD</sub> = 3.3 V	-30		+30	μV
uv <sub>OS</sub> /Time		T <sub>A</sub> = 85°C; V <sub>DD</sub> = 5.0 V	-40		+40	μV
PSRR	Power Supply Rejection Ratio	V <sub>CM</sub> = V <sub>DD</sub> /2 T <sub>A</sub> = -40 °C to 85 °C	95	115		dB
		V <sub>CM</sub> = V <sub>SS</sub> T <sub>A</sub> = -40 °C to 85 °C	85	100		dB
CS (	Channel Separation	V <sub>DD</sub> = 5 V, f = 10 Hz		120		dB
00 0		V <sub>DD</sub> = 5 V, f = 1 kHz		95		dB
Input Voltage R	Range					
V <sub>CMR</sub> I	Input Common-Mode Voltage Range	T <sub>A</sub> = -40 °C to 85 °C	$V_{SS}$		$V_{DD}$	V
		V <sub>SS</sub> + 0.8 V < V <sub>CM &lt;</sub> V <sub>DD</sub> - 0.8 V, T <sub>A</sub> = -40 °C to 85 °C	65	100		dB
CMRR (	Common-Mode Rejection Ratio	$V_{SS} < V_{CM} < V_{SS} + 0.8 V,$ $V_{DD} - 0.8 V < V_{CM} < V_{DD},$ $T_A = -40 ^{\circ}C \text{ to } 85 ^{\circ}C$	50	75		dB
Input Bias Curr	rent and Impedance					
	Input Bias Current <sup>1</sup>			2		pА
'B I		T <sub>A</sub> = 85 °C		320	500	pА



# Electrical Characteristics (continued)

$T_A = 25 \text{ °C}, V_{DD} = 1.71 \text{ V to } 5.5 \text{ V}, V_S$	$_{SS} = GND, V_{CM} = V_{DD}/2,$	V <sub>OUT</sub> = V <sub>DD</sub> /2, V <sub>L</sub> = V <sub>DD</sub> /2, F	$R_L = 1 M\Omega$ to $V_L$ , unless otherwise stated.
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I <sub>OS</sub>	Input Offset Current <sup>2</sup>					
R <sub>CM</sub>	Input Offset Current-			±0.3		pА
R <sub>CM</sub>		T <sub>A</sub> = 85 °C		±20		pА
D	Common Mode Input Resistance			10 <sup>13</sup>		Ω
DIFF	Differential Input Resistance			10 <sup>13</sup>		Ω
C <sub>CM</sub>	Input Capacitance Common-Mode			4.3		pF
C <sub>DIFF</sub>	Input Capacitance Differential			6		pF
Open-Loop Ga	in		<u> </u>		<u> </u>	
		$R_L = 1 MΩ;$ V <sub>SS</sub> + 0.1 V ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> - 0.1 V	100	120		dB
A <sub>OL</sub>	DC Open Loop Voltage Gain	$R_L = 50 k\Omega;$ V <sub>SS</sub> + 0.5 V ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> - 0.5 V	100	120		dB
		$R_L = 50 k\Omega; T_A = 85 °C;$ V <sub>SS</sub> + 0.1 V ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> - 0.1 V	80	100		dB
Output						
V <sub>OH</sub> , V <sub>OL</sub>	Maximum Voltage Swing	R <sub>L</sub> = 50 kΩ	V <sub>SS</sub> + 5		V <sub>DD</sub> - 5	mV
V <sub>OSR</sub>	Linear Output Swing Range	V <sub>OVR</sub> from Rail	V <sub>SS</sub> + 100		V <sub>DD</sub> - 100	mV
	Short-circuit Current	V <sub>DD</sub> = 1.71 V	3.8	4.5		mA
isc		V <sub>DD</sub> = 3.0 V to 5.5 V	8.5	10		mA
C <sub>LOAD</sub>	Capacitive Load Drive		See Typ	oical Perf	ormance C	harts
Power Supply			_			
V <sub>DD</sub> :	Supply Voltage	Guaranteed by PSRR Test	1.71		5.5	V
				0.38	0.55	μΑ
l <sub>Q</sub> (	Quiescent Current (Per Amplifier)	T <sub>A</sub> = -40 °C to 85 °C		0.4	0.8	μΑ
		PDx = V <sub>DD</sub>		1		nA
Frequency Res	sponse					
GBW	Gain Bandwidth Product	G = +1 V/V		10		kHz
PM !	Phase Margin	G = +1 V/V		54		۰
SR 5	Slew Rate	R <sub>L</sub> = 50 kΩ	2.4	5.0		V/ms
t <sub>OR</sub>	Overload Recovery Time	$T_A$ = -40 °C to 85 °C; $R_L$ = 50 k $\Omega$		350		μs
Noise						
e <sub>n</sub>	Input Voltage Noise	f = 0.1 to 10 Hz		6.5		$\mu V_{P-P}$
V <sub>n</sub>	Input Voltage Noise Density	f =1 kHz		195		nV/√Hz
I <sub>n</sub> !	Input Current Noise Density	f =1 kHz		< 10		fA/√Hz



### **Typical Performance Charts**

 $T_{A} = 25 \text{ °C}, V_{DD} = 5.0 \text{ V}, V_{SS} = \text{GND}, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_{L} = V_{DD}/2, R_{L} = 1 \text{ M}\Omega \text{ to } V_{L}, C_{L} = 80 \text{ pF}, \text{ unless otherwise stated}.$ 



Fig 1. Input Offset Voltage Drift Distribution  $V_{CM} = V_{SS}$ ;  $V_{DD} = 1.71$  V and 5.5 V;  $T_A = 25^{\circ}C$ .



Fig 2. Input Offset Voltage vs. Common Mode Input Voltage V<sub>DD</sub> = 5.5 V.





Input Offset Voltage Temperature Drift (µV/°C)





Fig 5. Input Offset Voltage vs. Common Mode Input Voltage V<sub>DD</sub> = 1.71 V.



Fig 6. DC Open Loop Gain vs. Common Mode Input Voltage V<sub>DD</sub> = 3.3 V.

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 $T_{A} = 25 \text{ °C}, V_{DD} = 5.0 \text{ V}, V_{SS} = \text{GND}, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_{L} = V_{DD}/2, R_{L} = 1 \text{ M}\Omega \text{ to } V_{L}, C_{L} = 80 \text{ pF, unless otherwise stated.}$ 

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# SLG88103/4

5.0

80

100

5.5



 $T_{A} = 25 \text{ °C}, V_{DD} = 5.0 \text{ V}, V_{SS} = \text{GND}, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_{L} = V_{DD}/2, R_{L} = 1 \text{ M}\Omega \text{ to } V_{L}, C_{L} = 80 \text{ pF}, \text{ unless otherwise stated}.$ 

V<sub>DD</sub> = 5.5 V.

100

80

 $G = 1 V/V; R_{L} = 50 k\Omega$ 



 $T_{A} = 25 \text{ °C}, V_{DD} = 5.0 \text{ V}, V_{SS} = \text{GND}, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_{L} = V_{DD}/2, R_{L} = 1 \text{ M}\Omega \text{ to } V_{L}, C_{L} = 80 \text{ pF, unless otherwise stated.}$ 









Time (250µs/div)









Fig 27. Overload Recovery Time vs. Power Supply Voltage  $R_L$ = 50 k $\Omega$ ; G = 1 V/V.



Fig 28. DC Open Loop Gain vs. Power Supply Voltage  $R_L$  = 50 k $\Omega$ 



Fig 29. Output Voltage Swing from Rail vs.  $I_{OUT}$ V<sub>DD</sub> = 1.71 V and 5.5 V.



Fig 30. Output Response to Power Down Signal G = 1 V/V;  $R_L = 50 k\Omega$ ;  $C_L = 20 pF$ ;  $V_{IN} = V_S/2$ .



### **Applications Information**

The SLG88103/4 operates on a 1.71 V to 5.5 V power supply over a wide industrial temperature range from -40 °C to 85 °C. This dual/quad op amp chip has two/four active low enable pins used to individually power-up / power-down each op amp. Its common-mode range extends from 0 to  $V_{DD}$  and its output swings from rail-to-rail.

#### Input Protection

Voltage spikes need to be controlled at the inputs of each operational amplifier in order to avoid damaging the device. Electrical events like electrostatic discharge can produce large voltages at these nodes. The SLG88103/4 has internal circuitry to protect the device from these events. If  $V_{IN}$  exceeds  $V_{DD}$  or drops below  $V_{SS}$ , additional currents will flow through the internal ESD diodes and can damage the device even if the supplies are turned off.

In this case we recommend placing a resistor in series to the input to limit current through the internal ESD diodes to 5 mA (or preferably less).



Fig 31. ESD Protection .

#### **Driving Capacitive Loads**

Capacitive loads degrade circuit stability by decreasing the phase margin and bandwidth of the operational amplifier circuit. The SLG88103/4 can drive capacitive loads up to 10 nF at low loads. The amplifier's output impedance and the capacitive load add phase lag to the system. This phase lag creates gain peaking in the frequency response and peaking/ringing in the output's transient response. When large capacitive loads need to be driven, isolation resistors need to be used to increase the phase margin. This is done by increasing the output load impedance at higher frequencies. After selecting an isolation resistor value, verify that the frequency peaking and transient overshoot and ringing have been reduced.



Fig 32. Capacitive Load Test Circuit.



#### Low Power Considerations

The SLG88103/4 features low quiescent current at 375 nA per amplifier, as well as extremely high-impedance CMOS inputs. To take most advantage of such low power features, high impedance external components should be used. We recommend using low-leakage capacitors (such as ceramic). Other types of capacitors (such as aluminum dielectric) can leak at uA levels and consume more quiescent power than the op-amp itself! High value resistors are needed to keep power consumption low, as well as to avoid gain loss and non-linearities due to loading effects on the ultra-low power-stage of the op amp. On the other hand, higher resistances increase thermal noise and sensitivity to external interference. We recommend impedances between 100 k $\Omega$  and 500 k $\Omega$  in gain/feedback networks to achieve balanced performance given the ultra-low power characteristics of SLG88103/4.

#### PCB Layout

For proper PCB layout, place a 100 nF decoupling capacitor close to the VDD pin of the SLG88103/4. To improve sensitive system performance, keep trace lengths similar on the positive and negative inputs of the op amp. Keep feedback resistors as close to the op amp and as short as possible. In addition, remove the PCB ground plane from under the inputs and outputs of the op amp.

For low current applications, board leakage currents on sensitive, high impedance inputs can degrade signal integrity. To maximize system performance, use guard rings / shields around these high impedance op amp inputs. For non-inverting op amps, IN+ should have a guard ring driven to the voltage of IN- by a low impedance source. Similarly, the guard ring around IN- should be driven to IN+ for an inverting amplifier. The IN- and IN+ nodes for non-inverting and inverting amplifiers respectively can be used as low impedance voltage sources. This is because these nodes are effectively low impedance nodes due to op amp feedback properties. For a non-inverting amplifier, leakage current on IN+ will produce a voltage on the input that will be amplified to the op amp's output. On the other hand, the op amp will fight changes in voltage on IN- to match the voltage potential at IN+. These guard rings should be used on both sides of the PCB to help sink stray currents on the PCB before the currents can reach the input pins of the op amp and to minimize stray capacitance.

#### Proper Setup for Unused Op Amps

For an unused op amp on the SLG88103/4, connect the op amp as a voltage follower with the input tied to ground and it's enable pin tied to VDD. An example circuit using one of the op amps is shown below.



Fig 33. Unused Op Amp Setup.

#### **Application Examples**

The SLG88103/4 excels in low-power applications that operate at low frequencies. Please see the "Application Notes" section of this datasheet for application examples which use the SLG88103/4.



#### Design Resources

#### 1. Spice Macro Model

The most recent SPICE model is available on the Renesas website. This model is intended for simulation purposes only and shouldn't be used in place of hardware testing to verify proper functionality in a full system.

#### 2. Application Notes

For more information on the topics discussed in this datasheet and applications of this device, please see the following applications notes available online at our Application Notes page. New Application Notes are added regularly.

AN-1106 Custom Instrumentation Amplifier Design

#### 3. Design Support

Please contact a Renesas Representative at our Contact page for more information on the SLG88103/4. They will be happy to assist you by answering additional questions and by offering design support for projects relating to the SLG88103/4 and Renesas's GreenPAK devices.

#### 4. Op Amp + GreenPAK EVB

The OP AMP+GreenPAK EVB provides convenient breakout access for various IC's in Renesas's Op Amp and GreenPAK product families. Please see the OP AMP+EVB Layout Guide for more information on which GreenPAK devices and op amps can be placed on this PCB.

HO O OL 100 TE O	
GEBOG LOOOH	
	HOOOL 190 190 10 10 10 10 10 10 10
190 III 0 2 190 III 0	
0 0 0 3 7 180 0 0 0	
	[0 10 06 LO 0 0H] [0 0 02, 130 0 0]
	HO G OL 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 . 8 °13 0	
S . S 10 6 S . S	

Fig 34. Op Amp + GreenPAK EVB.



Package Top Marking System Definition - SLG88103



PP - Part ID Field WW - Date Code Field<sup>1</sup> N - Lot Traceability Code Field<sup>1</sup> A - Assembly Site Code Field<sup>2</sup> R - Part Revision Code Field<sup>2</sup>

Note 1: Each character in code field can be alphanumeric A-Z and 0-9 Note 2: Character in code field can be alphabetic A-Z



Package Top Marking System Definition - SLG88104



PPPPP - Part ID Field WW - Date Code Field<sup>1</sup> NNN - Lot Traceability Code Field<sup>1</sup> A - Assembly Site Code Field<sup>2</sup> RR - Part Revision Code Field<sup>2</sup>

Note 1: Each character in code field can be alphanumeric A-Z and 0-9 Note 2: Character in code field can be alphabetic A-Z



### Package Drawing and Dimensions - SLG88103

10 Lead STDFN Package JEDEC MO-252



Unit: mm										
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max			
A	0.50	0.55	0.60	D	1.95	2.00	2.05			
A1	0.005	-	0.050	E	1.95	2.00	2.05			
A2	0.10	0.15	0.20	L	0.55	0.60	0.65			
b	0.13	0.18	0.23	С	0.15 REF					
е	(	).40 BSC	;							



### Package Drawing and Dimensions - SLG88104



Unit: mm										
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max			
Α	0.50	0.55	0.60	D	3.45	3.50	3.55			
A1	0.005	-	0.050	E	1.95	2.00	2.05			
A2	0.10	0.15	0.20	L	0.65	0.70	0.75			
b	0.13	0.18	0.23	L1	0.45	0.50	0.55			
е	(	).40 BSC	•	С	0.15 REF					
S	(	).21 REF								



### **Recommended Land Pattern - SLG88103**



# Unit: um

# **Recommended Reflow Soldering Profile**

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.2 mm<sup>3</sup> (nominal). More information can be found at www.jedec.org.





# **Recommended Reflow Soldering Profile**

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.85 mm<sup>3</sup> (nominal). More information can be found at www.jedec.org.



# **Tape and Reel Specifications**

Package Type	# of	Nominal Package Size [mm]	Max Units		Reel &	Leader (min)		Trailer (min)		Таре	Part
	# of Pins		per Reel	per Box	Hub Size [mm]	Pockets	Length [mm]	Pockets	Length [mm]	Width [mm]	Pitch [mm]
STDFN 10L 2x2mm 0.4P COL Green	10	2 x 2 x 0.55	3000	3000	178 / 60	100	400	100	400	8	4
STQFN 20L 2x3.5mm 0.4P Green	20	2 x 3.5 x 0.55	5000	10000	330 /100	42	336	42	336	12	8

# Carrier Tape Drawing and Dimensions - SLG88103

Package Type	PocketBTM Length	PocketBTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	В0	K0	P0	P1	D0	Е	F	w
STDFN 10L 2x2mm 0.4P COL Green	2.2	2.2	0.83	4	4	1.55	1.75	3.5	8



Refer to EIA-481 specification



# **Carrier Tape Drawing and Dimensions Dimensions - SLG88104**

Package Type	PocketBTM Length	PocketBTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	В0	K0	P0	P1	D0	Е	F	w
STQFN 20L 2x3.5mm 0.4P Green	2.2	3.8	0.8	4	8	1.5	1.75	5.5	12



Refer to EIA-481 specification



# **Revision History**

Date	Version	Change
2/17/2022	1.03	Renesas rebranding Fixed typos
4/25/2017	1.02	Replaced Input Current vs.V <sub>CM</sub> Chart
3/13/2017	1.01	Replaced Slew Rate vs. Ambient Temperature Chart Fixed Chart formatting for some charts. Fixed typos
3/1/2017	1.00	Production Release

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