R1LV1616R Series

16Mb Advanced LPSRAM (1M wordx16bit / 2M wordx8bit)

REJ03C0101-0400Z
Rev.4.00
2007.09.12

Description

The R1LV1616R Series is a family of low voltage 16-Mbit static RAMs organized as 1048576-words by 16-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies.

The R1LV1616R Series is suitable for memory applications where a simple interfacing , battery operating and battery backup are the important design objectives.

The R1LV1616R Series is packaged in a 52pin micro thin small outline mount device[µTSOP / 10.79mm x 10.49mm with the pin-pitch of 0.4mm], a 48pin thin small outline mount device[TSOP / 12mm x 20mm with the pin-pitch of 0.5mm] or a 48balls fine pitch ball grid array [f-BGA / 7.5mmx8.5mm with the ball-pitch of 0.75mm and 6x8 array] . It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

Features

- Single 2.7-3.6V power supply
- Small stand-by current:2µA (3.0V, typ.)
- Data retention supply voltage =2.0V
- No clocks, No refresh
- All inputs and outputs are TTL compatible
- Easy memory expansion by CS1#, CS2, LB# and UB#
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE# prevents data contention on the I/O bus
- Process technology: 0.15um CMOS

Ordering Information

Type No.	Access time	Package
R1LV1616RSD-5S%	55 ns (Note0)	350-mil 52-pin plastic µ - TSOP(II) (normal-bend type) (52PTG)
R1LV1616RSD-7S%	70 ns	
R1LV1616RSD-8S%	85 ns	
R1LV1616RBG-5S%	55 ns (Note0)	7.5mmx8.5mm f-BGA 0.75mm pitch 48ball
R1LV1616RBG-7S%	70 ns	
R1LV1616RBG-8S%	85 ns	
R1LV1616RSA-5S%	55 ns (Note0)	12mm x 20mm plastic TSOP(I) (normal-bend type) (48P3R)
R1LV1616RSA-7S%	70 ns	
R1LV1616RSA-8S%	85 ns	

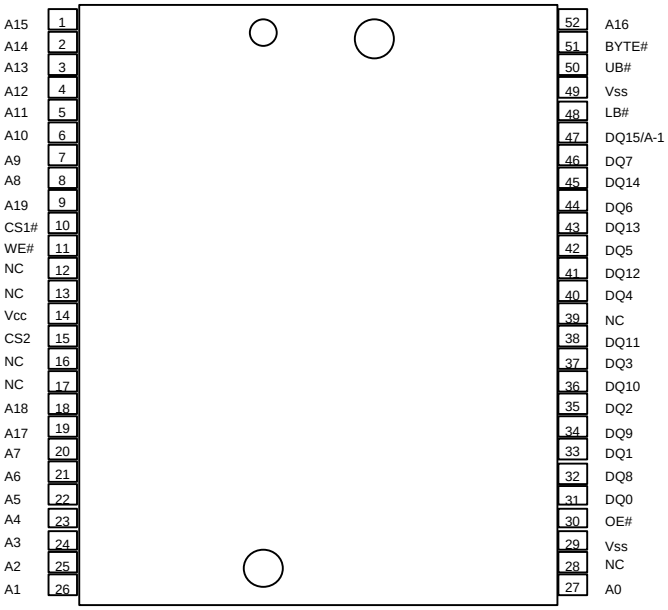
Note0. 55ns parts can be supported under the condition of the input timing limitation toward SRAM on customer's system. Please contact our sales office in your region, in case of the inquiry for 55ns parts.

% - Temperature version; see table below

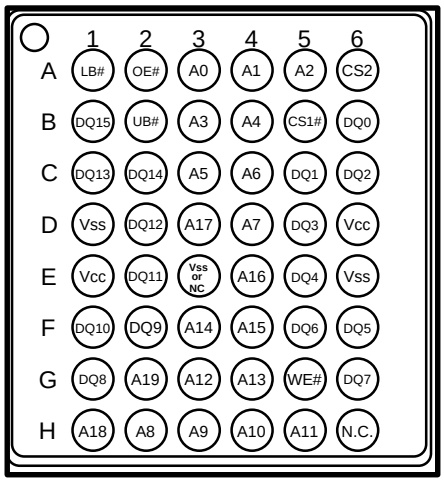
%	Temperature Range
R	0 ~ +70 ºC
I	-40 ~ +85 ºC

Pin Arrangement

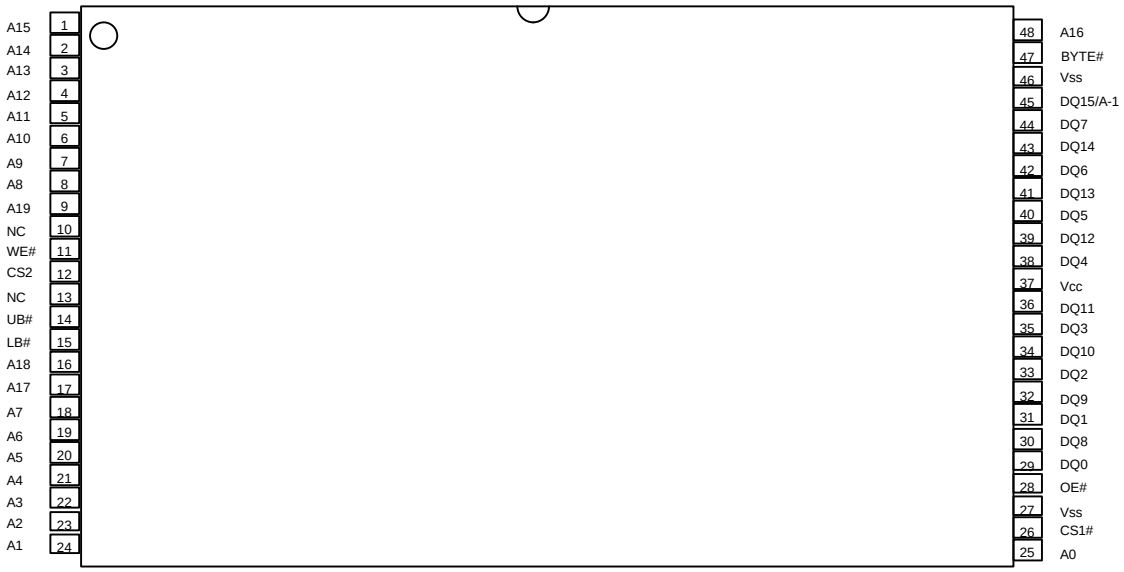
52-pin µTSOP



48-pin fBGA



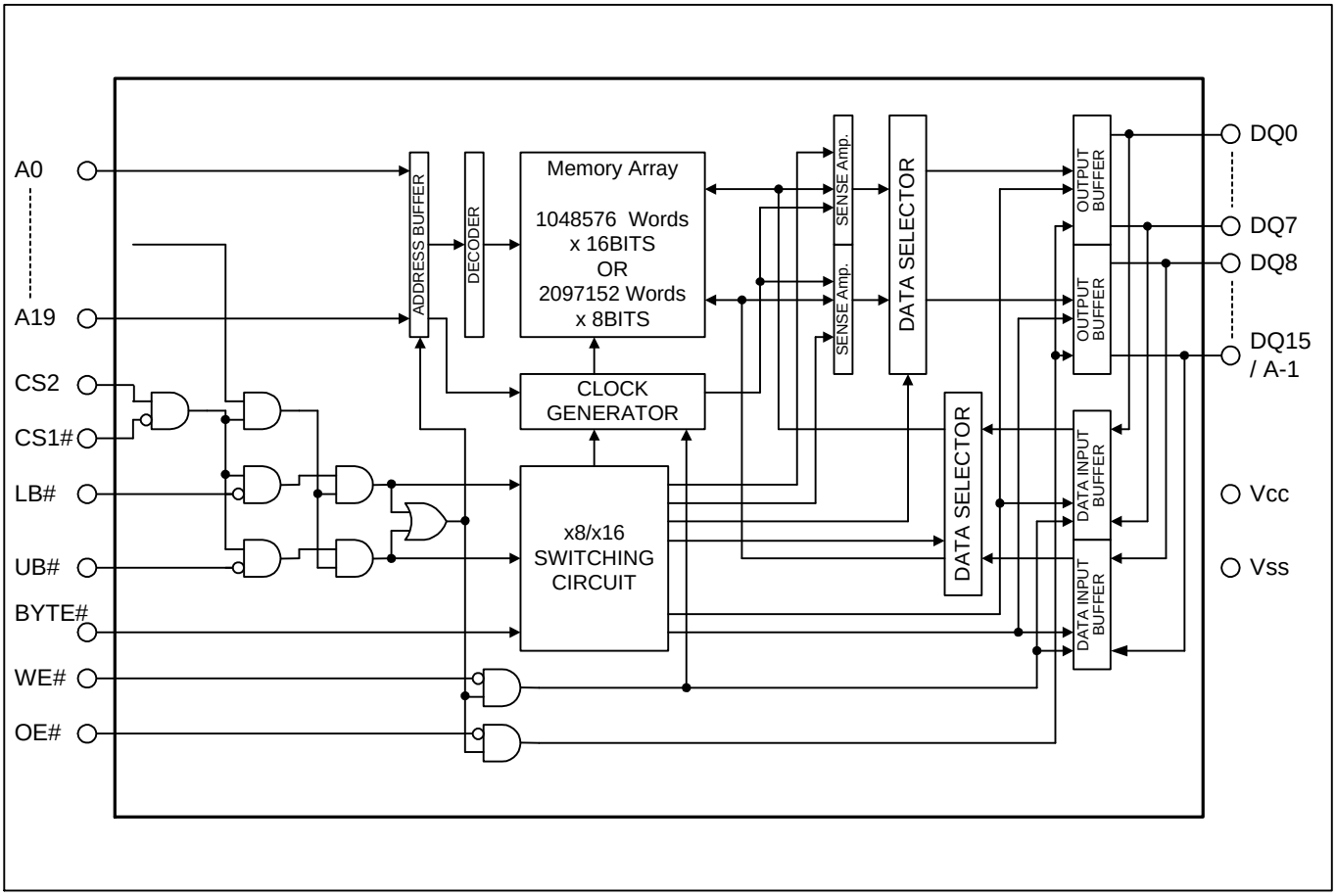
48-pin TSOP



Pin Description

Pin name	Function
A0 to A19	Address input
DQ 0 to DQ15	Data input/output
CS1# &CS2	Chip select
WE#	Write enable
OE#	Output enable
LB#	Lower byte select
UB#	Upper byte select
Vcc	Power supply
Vss	Ground
BYTE#	Byte (x8 mode) enable input
NC	Non connection

Block Diagram



Note. BYTE# pin supported by only TSOP and uTSOP types.

Operating Table

CS1#	CS2	BYTE#	LB#	UB#	WE#	OE#	DQ0-7	DQ8-14	DQ15	Operation
H	X	X	X	X	X	X	High-Z	High-Z	High-Z	Stand by
X	L	X	X	X	X	X	High-Z	High-Z	High-Z	Stand by
X	X	H	H	H	X	X	High-Z	High-Z	High-Z	Stand by
L	H	H	L	H	L	X	Din	High-Z	High-Z	Write in lower byte
L	H	H	L	H	H	L	Dout	High-Z	High-Z	Read from lower byte
L	H	X	X	X	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	H	L	L	X	High-Z	Din	Din	Write in upper byte
L	H	H	H	L	H	L	High-Z	Dout	Dout	Read from upper byte
L	H	H	L	L	L	X	Din	Din	Din	Write
L	H	H	L	L	H	L	Dout	Dout	Dout	Read
L	H	L	L	L	L	X	Din	High-Z	A-1	Write
L	H	L	L	L	H	L	Dout	High-Z	A-1	Read

Note 1. H:VIH L:VIL X: VIH or VIL
2. BYTE# pin supported by only TSOP and uTSOP types. When apply BYTE# =“L” , please assign LB#=UB#=“L”.

Absolute Maximum Ratings

Parameter	Symbol	Value		Unit
Power supply voltage relative to Vss	Vcc	-0.5 to +4.6		V
Terminal voltage on any pin relation toVss	V_T	-0.5*1 to Vcc+0.3*2		V
Power dissipation	P_T	0.7		W
Operation temperature	Topr	R ver.	0 to +70	ºC
		I ver.	-40 to +85	ºC
Storage temperature	Tstg	-65 to +150		ºC
Storage temperature range under bias	Tbias	R ver.	0 to +70	ºC
		I ver.	-40 to +85	ºC

Note 1. -2.0V in case of AC (Pulse width ≤ 30ns)
2. Maximum voltage is +4.6V

Recommended Operating Conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage		Vcc	2.7	3.0	3.6	V	
		Vss	0	0	0	V	
Input high voltage		V_{IH}	2.4	-	Vcc+0.2	V	
Input low voltage		V_{IL}	-0.2	-	0.4	V	1
Ambient temperature range	R ver.	Ta	0	-	+70	ºC	2
	I ver.		-40	-	+85	ºC	2

Note 1. –2.0V in case of AC (Pulse width ≤ 30ns)
2. Ambient temperature range depends on R/I-version. Please see table on page 2.

DC Characteristics

Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test conditions*2	
Input leakage current	$\|I_{LI}\|$	-	-	1	µA	Vin=Vss to Vcc	
Output leakage current	$\|I_{LO}\|$	-	-	1	µA	CS1# =V_{IH} or CS2=V_{IL} or OE# = V_{IH} or WE# =V_{IL} or LB# =UB# =V_{IH},$V_{I/O}$=Vss to Vcc	
Average operating current	I_{CC1}	-	25	40	mA	Min. cycle, duty =100% I I/O = 0 mA, CS1# =V_{IL}, CS2=V_{IH} Others = V_{IH} / V_{IL}	
	I_{CC2}	-	2	5	mA	Cycle time = 1 µs, I I/O = 0 mA, CS1#≤ 0.2V, CS2 ≥ V_{CC}-0.2V V_{IH} ≥ V_{CC}-0.2V , V_{IL} ≤ 0.2V, duty=100%	
Standby current	I_{SB}	-	0.1	0.3	mA	CS2=V_{IL}	
Standby current	I_{SB1}	-	2	6	µA	~+25ºC	V in ≥ 0V (1) 0V≤CS2≤0.2V or (2) CS2≥Vcc-0.2V, CS1# ≥Vcc-0.2V or (3)LB# =UB# ≥Vcc-0.2V, CS2≥Vcc-0.2V, CS1# ≤0.2V Average value
		-	4	12	µA	~+40ºC	
		-	-	25	µA	~+70ºC	
		-	-	40	µA	~+85ºC	
Output hige voltage	V_{OH}	2.4	-	-	V	I_{OH} = -1mA	
Output Low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA	

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (Ta= 25ºC), and not 100% tested.
2. BYTE# pin supported by only TSOP and uTSOP types.
BYTE# ≥ Vcc-0.2V or BYTE# ≤ 0.2V

Capacitance

(Ta = +25ºC, f =1MHz)

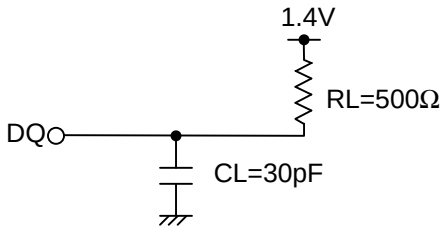
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	-	-	10	pF	V in = 0V	1
Input / output capacitance	C I/O	-	-	10	pF	V I/O = 0V	1

Note 1:This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc=2.7~3.6V, Ta = 0~+70ºC / -40~+85ºC *)

- Input pulse levels: VIL= 0.4V,VIH=2.4V
- Input rise and fall time : 5ns
- Input and output timing reference levels : 1.4V
- Output load : See figures (Including scope and jig)



Note: Temperature range depends on R/I-version. Please see table on page 2.

Read Cycle

Parameter	Symbol	R1LV1616R**-5S (Note0)		R1LV1616R**-7S		R1LV1616R**-8S		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	55	-	70	-	85	-	ns	
Address access time	t_{AA}	-	70	-	70	-	85	ns	
Chip select access time	t_{ACS1}	-	55	-	70	-	85	ns	
	t_{ACS2}	-	55	-	70	-	85	ns	
Output enable to output valid	t_{OE}	-	35	-	35	-	45	ns	
Output hold from address change	t_{OH}	10	-	10	-	10	-	ns	
LB#,UB# access time	t_{BA}	-	55	-	70	-	85	ns	
Chip select to output in low-Z	t_{CLZ}	10	-	10	-	10	-	ns	2,3
LB#,UB# enable to low-Z	t_{BLZ}	5	-	5	-	5	-	ns	2,3
Output enable to output in low-Z	t_{OLZ}	5	-	5	-	5	-	ns	2,3
Chip deselect to output in high-Z	t_{CHZ1}	0	20	0	25	0	30	ns	1,2,3
	t_{CHZ2}	0	20	0	25	0	30	ns	1,2,3
LB#,UB# disable to high-Z	t_{BHZ}	0	20	0	25	0	30	ns	1,2,3
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	0	30	ns	1,2,3

Write Cycle

Parameter	Symbol	R1LV1616R**-5S (Note0)		R1LV1616R**-7S		R1LV1616R**-8S		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	55	-	70	-	85	-	ns	
Address valid to end of write	t_{AW}	50	-	65	-	70	-	ns	
Chip selection to end of write	t_{CW}	55	-	65	-	70	-	ns	5
Write pulse width	t_{WP}	40	-	55	-	60	-	ns	4
LB#,UB# valid to end of write	t_{BW}	50	-	65	-	70	-	ns	
Address setup time	t_{AS}	0	-	0	-	0	-	ns	6
Write recovery time	t_{WR}	0	-	0	-	0	-	ns	7
Data to write time overlap	t_{DW}	25	-	35	-	40	-	ns	
Data hold from write time	t_{DH}	0	-	0	-	0	-	ns	
Output active from end of write	t_{OW}	5	-	5	-	5	-	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	0	30	ns	1,2
Write to output in high-Z	t_{WHZ}	0	20	0	25	0	30	ns	1,2

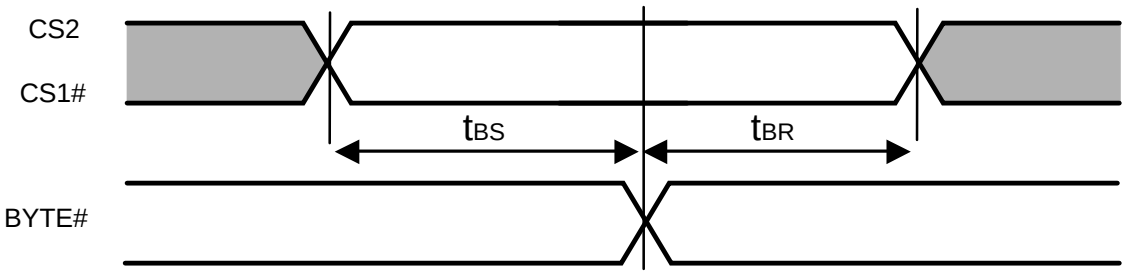
Note0. 55ns parts can be supported under the condition of the input timing limitation toward SRAM on customer's system. Please contact our sales office in your region, in case of the inquiry for 55ns parts.
In case of t_{AA} =70ns, t_{RC} =70ns.

1. t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. AT any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and form device to device.
4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.
   A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low .
   A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high. t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of CS1# going low or CS2 going high to end of write.
6. t_{AS} is measured the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

Byte enable (supported by only 48-pin TSOP and 52-pin µTSOP)

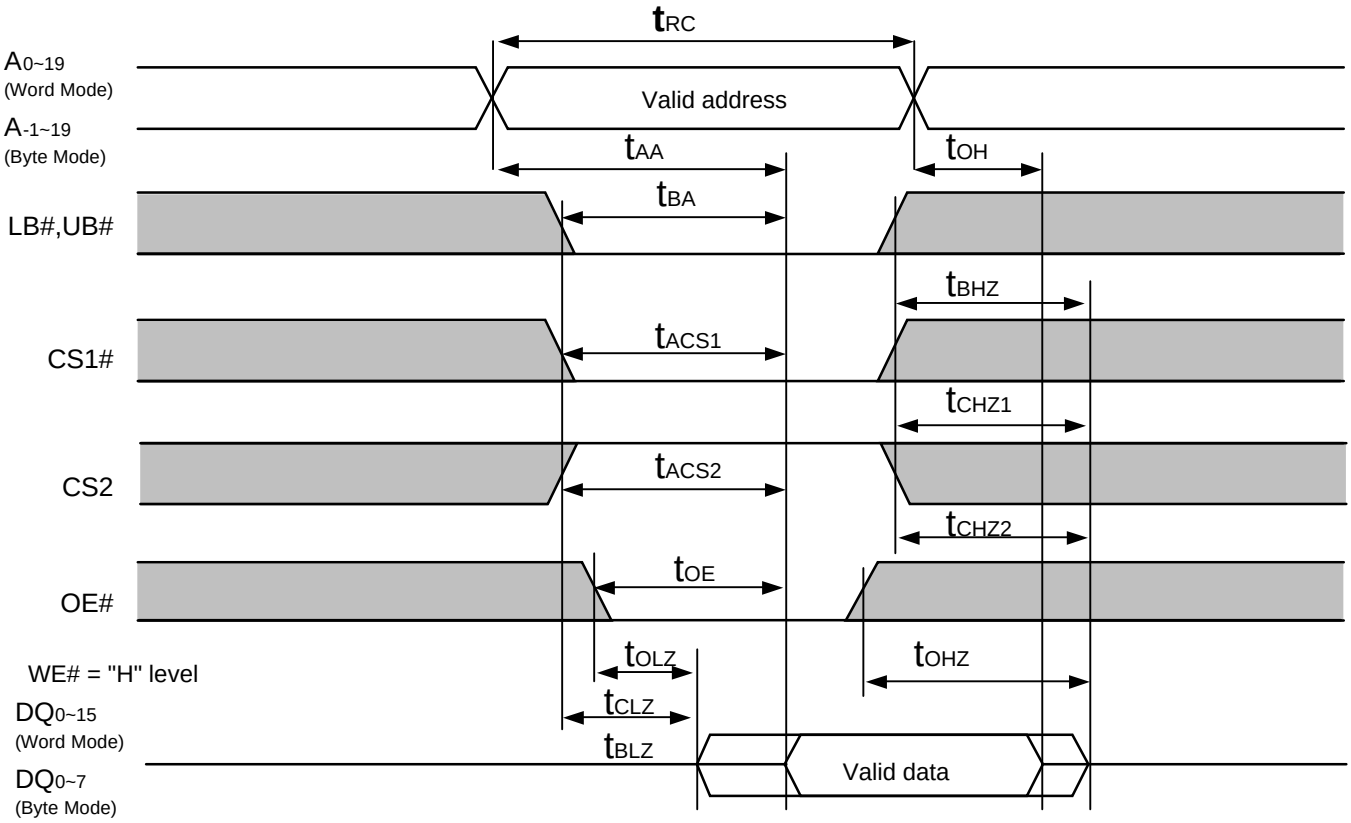
Parameter	Symbol	R1LV1616R**-5S		R1LV1616R**-7S		R1LV1616R**-8S		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Byte setup time	t_{BS}	5	-	5	-	5	-	ms	
Byte recovery time	t_{BR}	5	-	5	-	5	-	ms	

BYTE# Timing Waveform

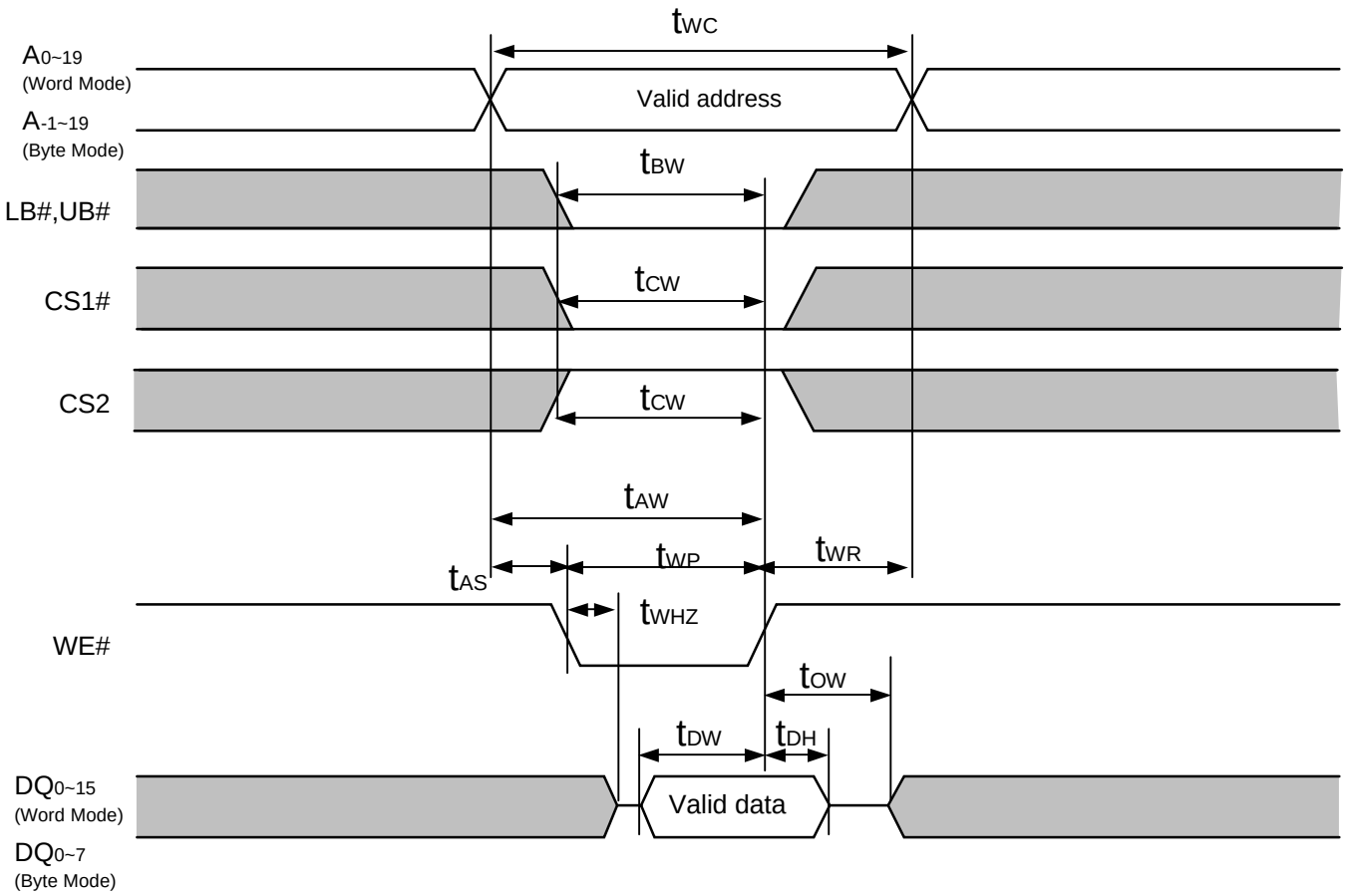


Timing Waveform

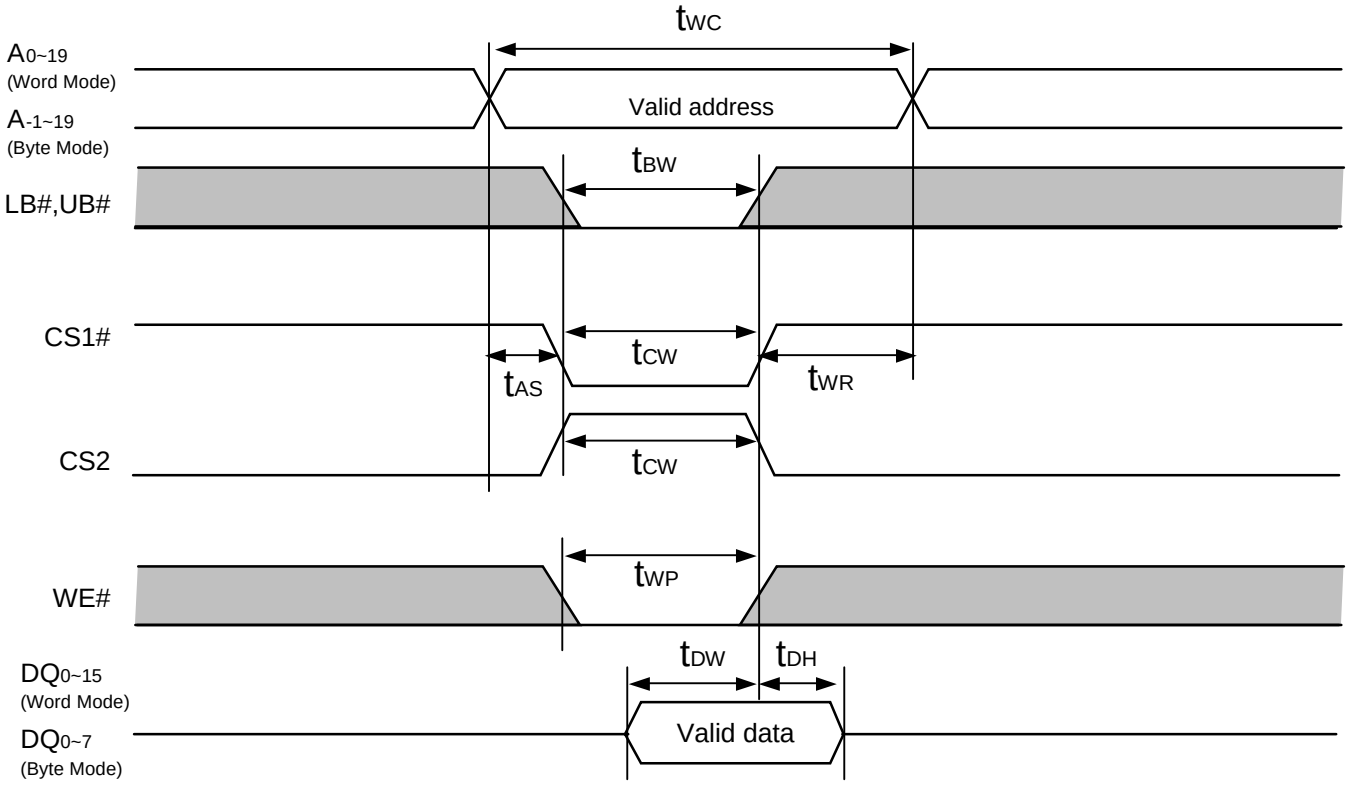
Read Cycle



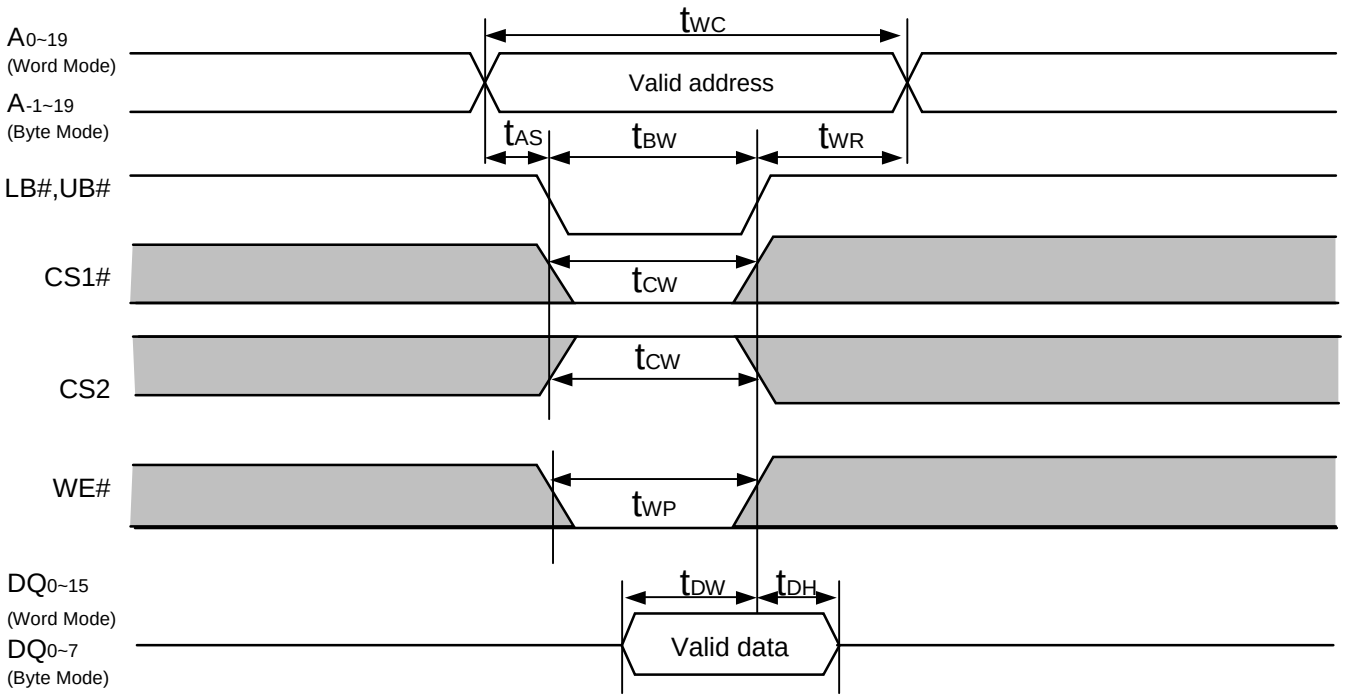
Write Cycle (1) (WE# Clock)



Write Cycle (2) (CS1# ,CS2 Clock, OE#=V_{IH})



Write Cycle (3) (LB#,UB# Clock, OE#=V_{IH})

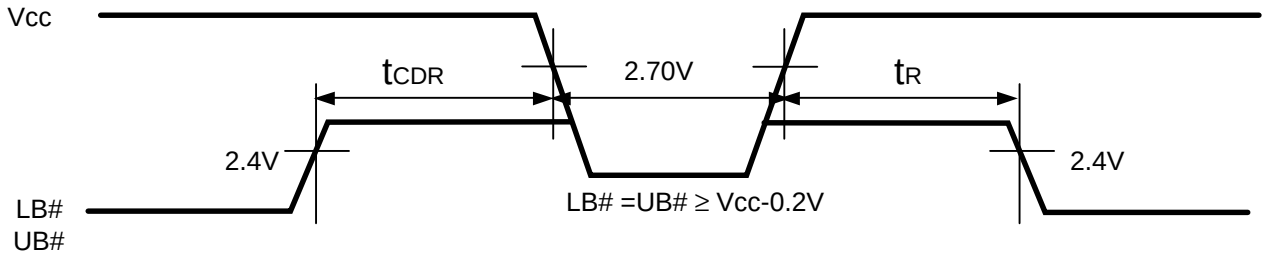


Data Retention Characteristics

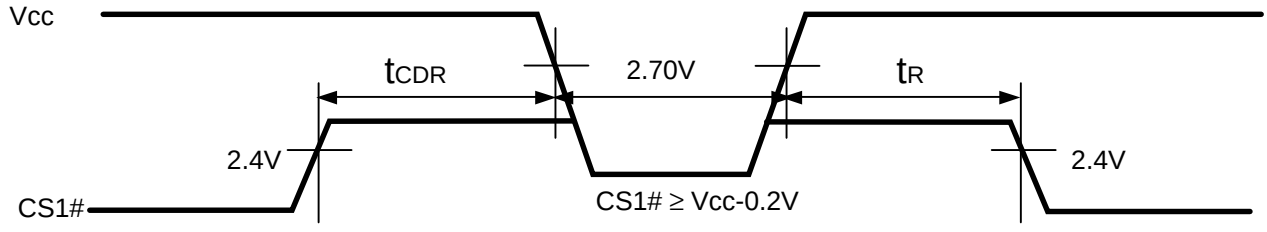
Parameter	Symbol	MIn.	Typ.*1	Max.	Unit	Test conditions*2,3	
Vcc for data retention	V_{DR}	2.0	-	3.6	V	V in ≥ 0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS2 ≥ Vcc-0.2V, CS1# ≥ Vcc-0.2V or (3) LB# =UB# ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V, CS1# ≤ 0.2V	
Data retention current	I_{CCDR}	-	2	6	µA	~+25ºC	Vcc=3.0V,Vin≥0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS2 ≥ Vcc-0.2V, CS1# ≥ Vcc-0.2V or (3) LB# =UB# ≥Vcc-0.2V, CS2 ≥ Vcc-0.2V, CS1# ≤ 0.2V Average value
		-	4	12	µA	~+40ºC	
		-	-	25	µA	~+70ºC	
		-	-	40	µA	~+85ºC	
Chip deselect to data retention time	t_{CDR}	0	-	-	ns	See retention waveform	
Operation recovery time	t_R	5	-	-	ms		

Note 1. Typical parameter of I_{CCDR} indicates the value for the center of distribution at Vcc=3.0V and not 100% tested.
2. BYTE# pin supported only by TSOP and uTSOP types. BYTE# ≥ Vcc-0.2V or BYTE# ≤ 0.2V
3. Also CS2 controls address buffer, WE# buffer ,CS1# buffer ,OE# buffer ,LB# ,UB# buffer and Din buffer .If CS2 controls data retention mode,Vin levels (address, WE# ,OE#,CS1#,LB#,UB#,I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ Vcc-0.2V or 0V ≤ CS2 ≤ 0.2V. The other input levels (address, WE# ,OE#,CS1#,LB#,UB#,I/O) can be in the high impedance state.

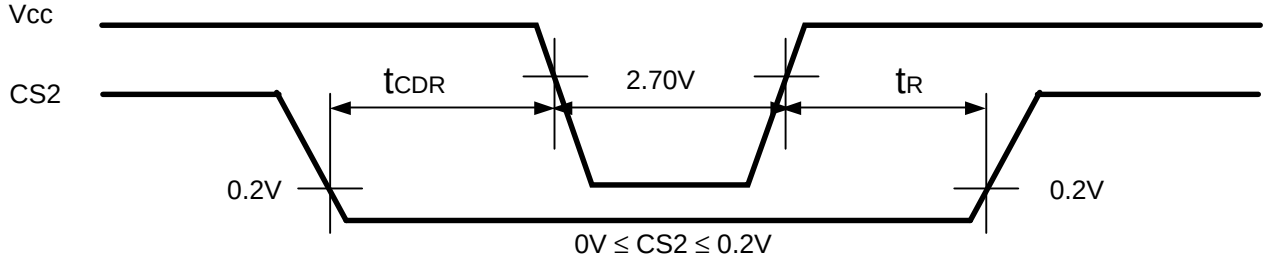
Data Retention timing Waveform (1) (LB#,UB# Controlled)



Data Retention timing Waveform (2) (CS1# Controlled)



Data Retention timing Waveform (3) (CS2 Controlled)



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To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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