To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using the R8C CPU core and is packaged in a 48-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, it is capable of executing instructions at high speed. This Furthermore, the data flash (1 KB x 2 blocks) is embedded in the R8C/21 Group.
The difference between R8C/20 and R8C/21 Groups is only the existence of the data flash. Their peripheral functions are the same.

1.1 Applications

Automotive, etc.

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/20 Group and Table 1.2 outlines the Functions and Specifications for R8C/21 Group.

Table 1.1 Functions and Specifications for R8C/20 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to **Table 1.3 Product Information for R8C/20 Group**
Peripheral Function	Ports	I/O ports: 41 pins, Input port: 3 pins
	Timers	Timer RA: 8 bits x 1 channel, Timer RB: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits x 2 channel (Circuits of input capture and output compare) Timer RE: With compare match function
	Serial interface	1 channel (UART0) Clock synchronous I/O, UART 1 channel (UART1) UART
	Clock synchronous serial interface	1 channel I2C bus interface(2), Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits x 1 channel (with prescaler) Reset start selectable
	Interrupt	Internal: 11 sources, External: 5 sources, Software: 4 sources, Priority level: 7 levels
	Clock generation circuits	2 circuits XIN clock generation circuit (with on-chip feedback resistor) On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has frequency adjustment function.
	Oscillation stop detection function	Stop detection of XIN clock oscillation
	Voltage detection circuit	On-chip
	Power-on reset circuit include	On-chip
Electric Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz)(J version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz)(K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Current consumption	Typ. 11.0 mA (VCC = 5 V, f(XIN) = 20 MHz, High-speed on-chip oscillator stopping) Typ. 5.3 mA (VCC = 5 V, f(XIN) = 10 MHz, High-speed on-chip oscillator stopping)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	100 times
Operating Ambient Temperature		-40 to 85°C
		-40 to 125°C (option(1))
Package		48-pin mold-plastic LQFP

NOTES:
1. When using options, be sure to inquire about the specification.
2. I2C bus is a registered trademark of Koninklijke Philips Electronics N.V.

Table 1.2 Functions and Specifications for R8C/21 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to **Table 1.4 Product Information for R8C/21 Group**
Peripheral Function	Ports	I/O ports: 41 pins, Input port: 3 pins
	Timers	Timer RA: 8 bits x 1 channel, Timer RB: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits x 2 channel (Circuits of input capture and output compare) Timer RE: With compare match function
	Serial interface	1 channel (UART0) Clock synchronous I/O, UART 1 channel (UART1) UART
	Clock synchronous serial interface	1 channel I^2C bus interface(2), Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (Timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits x 1 channel (with prescaler) Reset start selectable
	Interrupts	Internal: 11 sources, External: 5 sources, Software: 4 sources, Priority level: 7 levels
	Clock generation circuits	2 circuits XIN clock generation circuit (with on-chip feedback resistor) On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has frequency adjustment function.
	Oscillation stop detection function	Stop detection of XIN clock oscillation
	Voltage detection circuit	On-chip
	Power-on reset circuit include	On-chip
Electric Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz)(J version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz)(K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Current consumption	Typ. 11.0 mA (VCC = 5 V, f(XIN) = 20 MHz, High-speed on-chip oscillator stopping) Typ. 5.3 mA (VCC = 5 V, f(XIN) = 10 MHz, High-speed on-chip oscillator stopping)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	10,000 times (data flash)
		1,000 times (program ROM)
Operating Ambient Temperature		-40 to 85°C
		-40 to 125°C (option(1))
Package		48-pin mold-plastic LQFP

NOTES:
1. When using options, be sure to inquire about the specification.
2. I^2C bus is a registered trademark of Koninklijke Philips Electronics N.V.

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

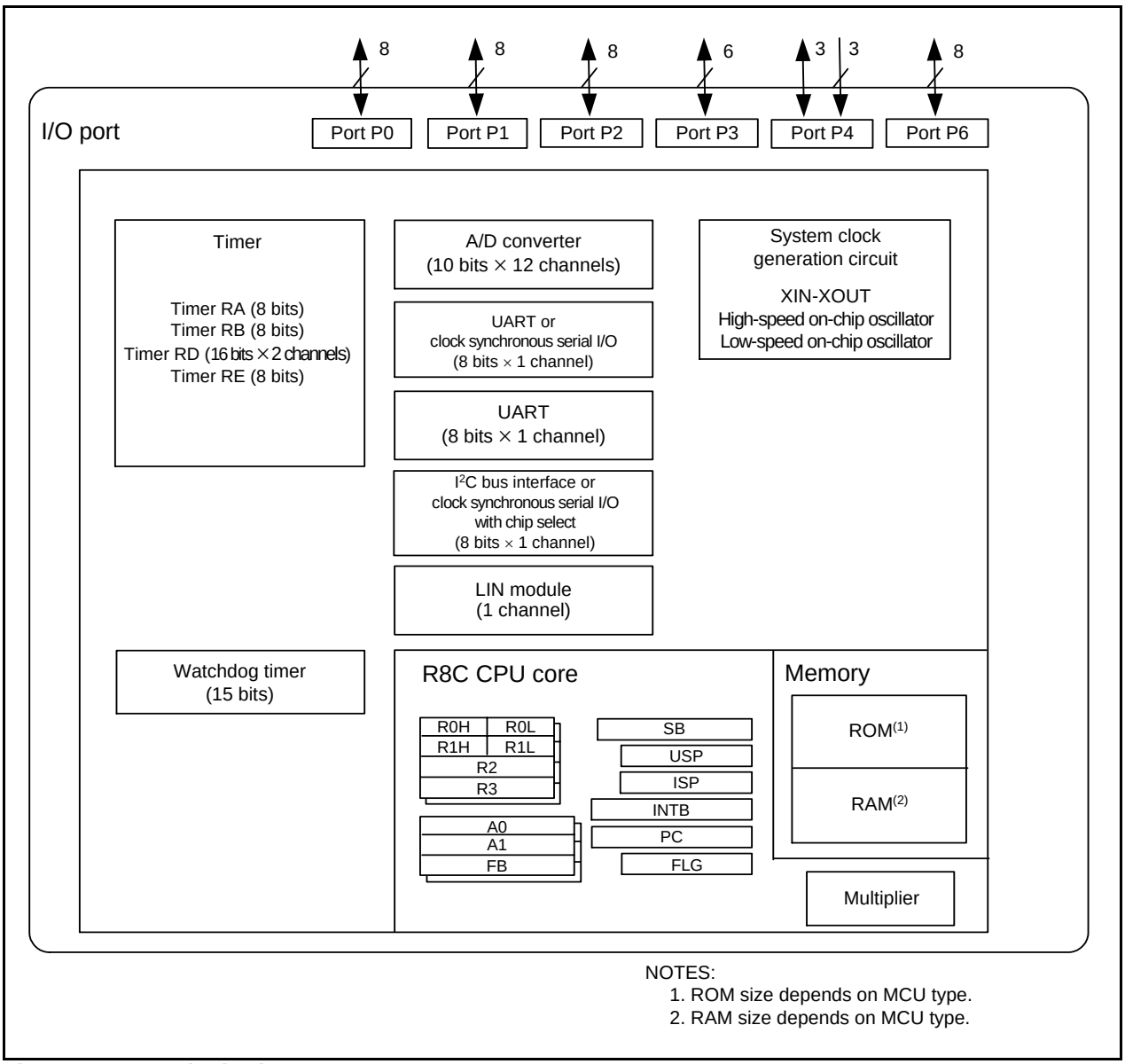


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists Product Information for R8C/20 Group and Table 1.4 lists Product Information for R8C/21 Group.

Table 1.3 Product Information for R8C/20 Group **Current of Aug. 2008**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks	
R5F21206JFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	J version	Flash memory version
R5F21207JFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21208JFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F2120AJFP	96 Kbytes	5 Kbytes	PLQP0048KB-A		
R5F2120CJFP	128 Kbytes(1)	6 Kbytes	PLQP0048KB-A		
R5F21206KFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	K version	
R5F21207KFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21208KFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F2120AKFP	96 Kbytes	5 Kbytes	PLQP0048KB-A		
R5F2120CKFP	128 Kbytes(1)	6 Kbytes	PLQP0048KB-A		

NOTE:
1. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **23. Notes on Emulator Debugger** of Hardware Manual.

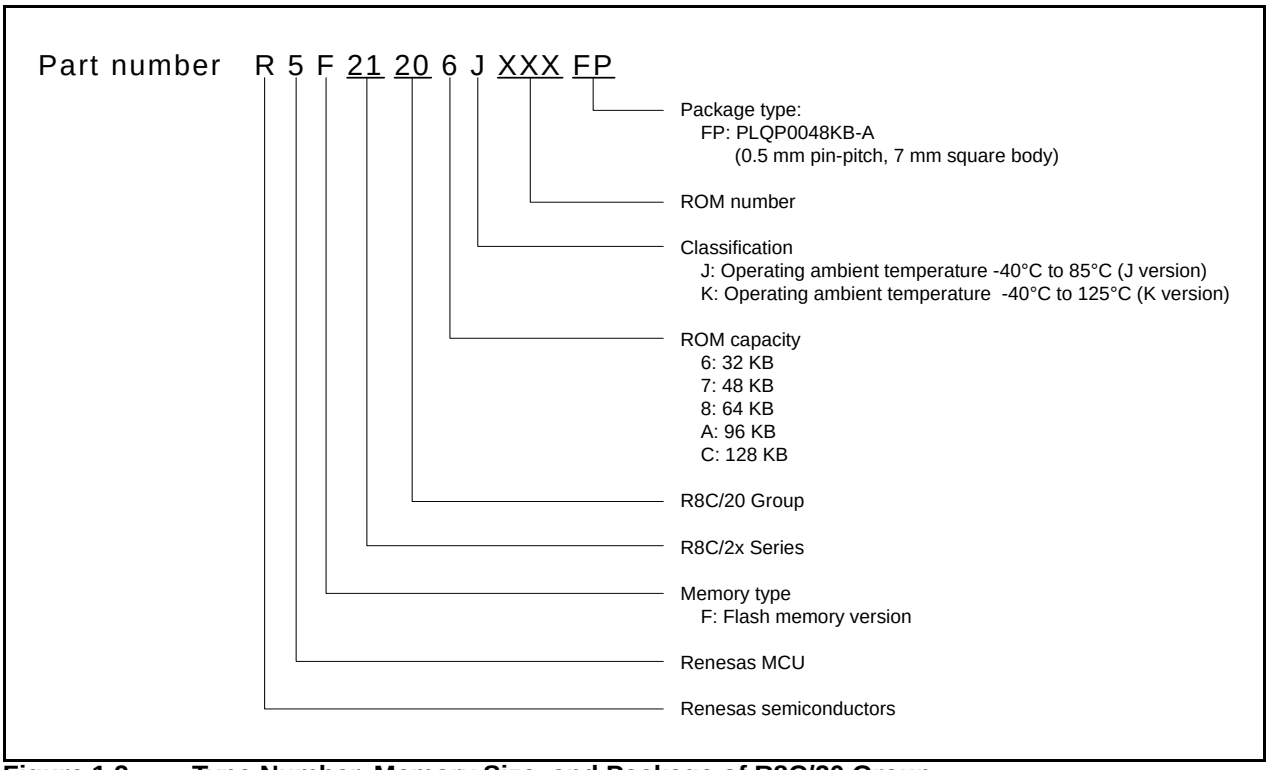


Figure 1.2 Type Number, Memory Size, and Package of R8C/20 Group

Table 1.4 Product Information for R8C/21 Group **Current of Aug. 2008**

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data Flash				
R5F21216JFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	J version	Flash memory version
R5F21217JFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21218JFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F2121AJFP	96 Kbytes	1 Kbyte X 2	5 Kbytes	PLQP0048KB-A		
R5F2121CJFP	128 Kbytes(1)	1 Kbyte X 2	6 Kbytes	PLQP0048KB-A		
R5F21216KFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	K version	
R5F21217KFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21218KFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F2121AKFP	96 Kbytes	1 Kbyte X 2	5 Kbytes	PLQP0048KB-A		
R5F2121CKFP	128 Kbytes(1)	1 Kbyte X 2	6 Kbytes	PLQP0048KB-A		

NOTE:
1. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **23. Notes on Emulator Debugger** of Hardware Manual.

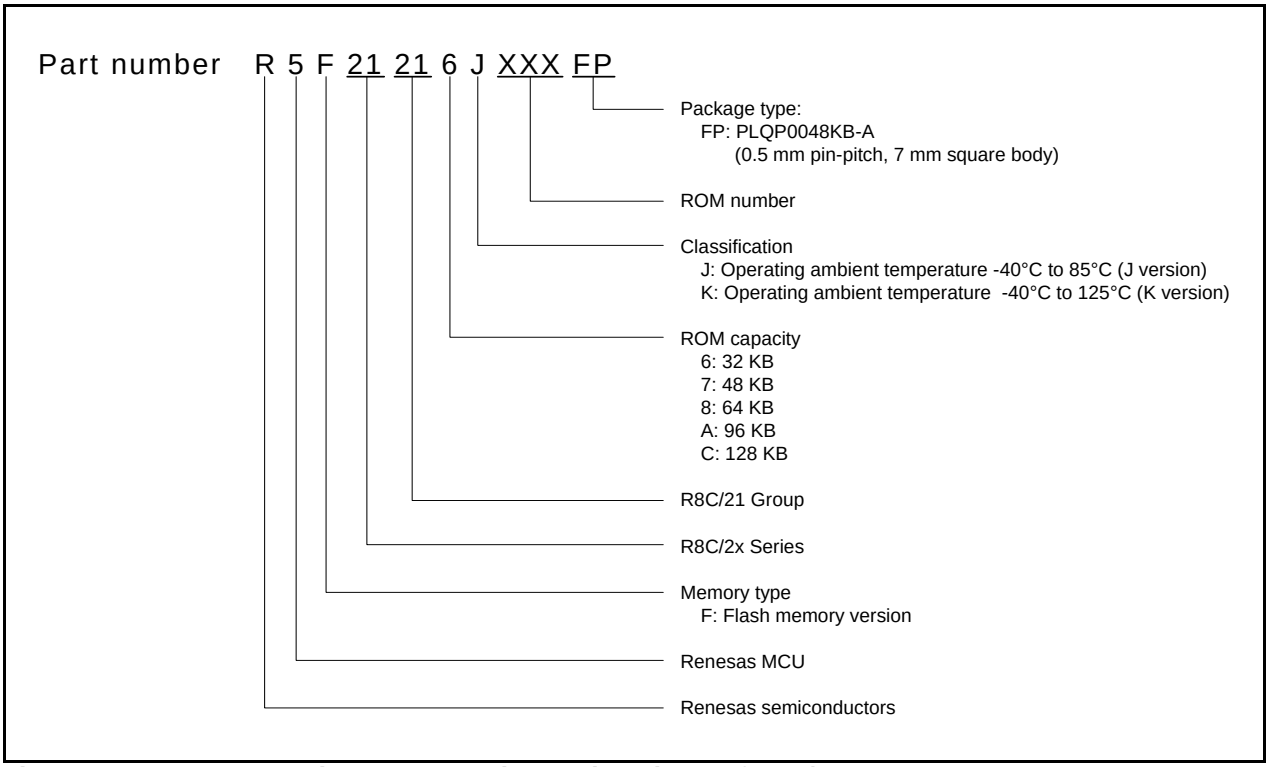


Figure 1.3 Type Number, Memory Size, and Package of R8C/21 Group

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments (Top View).

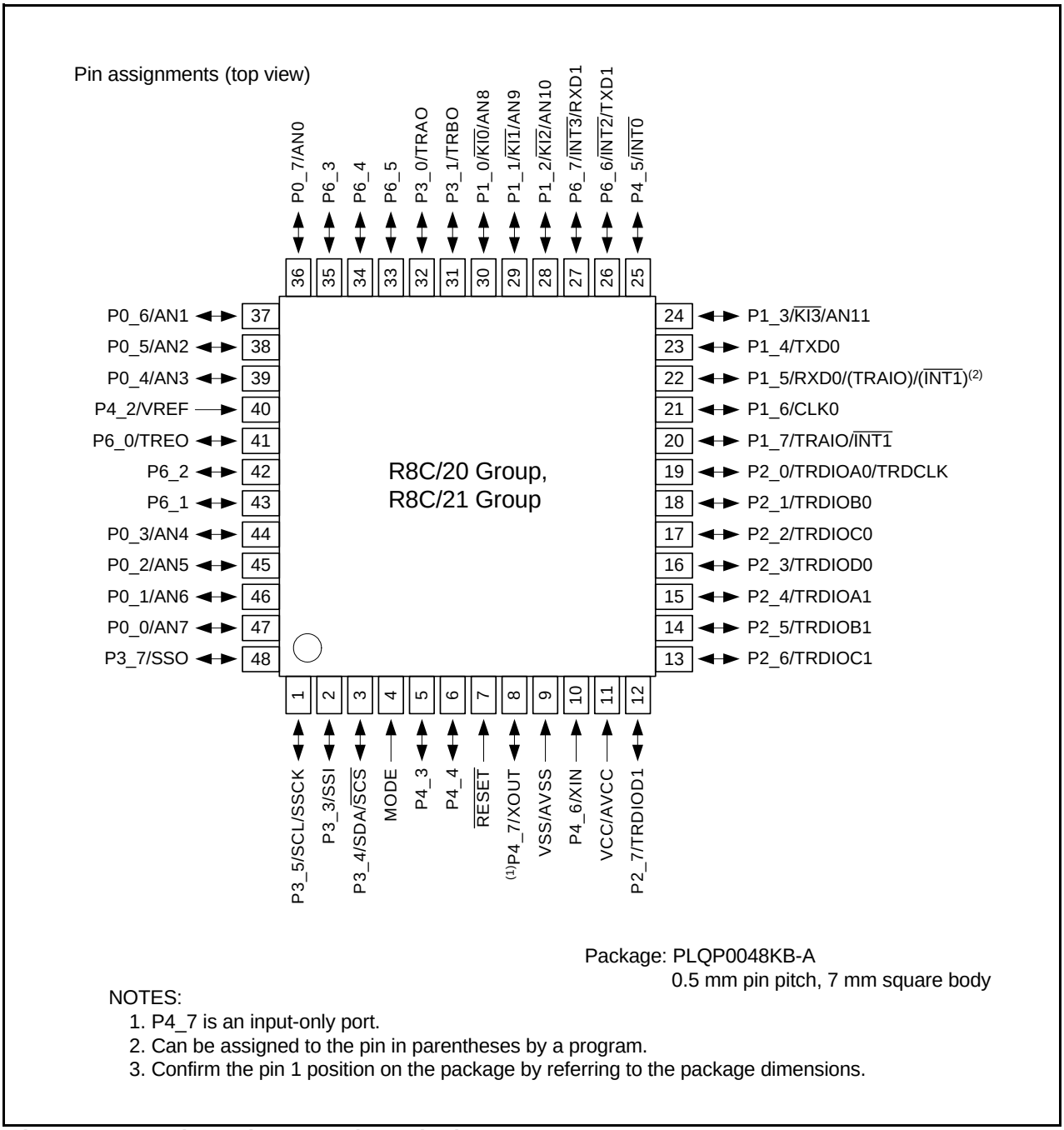


Figure 1.4 Pin Assignments (Top View)

1.6 Pin Functions

Table 1.5 lists the Pin Functions and Table 1.6 lists the Pin Name Information by Pin Number.

Table 1.5 Pin Functions

Type	Symbol	I/O Type	Description
Power Supply Input	VCC VSS	I	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog Power Supply Input	AVCC, AVSS	I	Applies the power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset Input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN Clock Input	XIN	I	These pins are provided for the XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
XIN Clock Output	XOUT	O	
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ Timer RD input pins. $\overline{\text{INT1}}$ Timer RA input pins.
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRAO	O	Timer RA output pin.
Timer RB	TRBO	O	Timer RB output pin.
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O ports.
	TRDCLK	I	External clock input pin.
Timer RE	TREO	O	Divided clock output pin.
Serial Interface	CLK0	I/O	Transfer clock I/O pin.
	RXD0, RXD1	I	Serial data input pins.
	TXD0, TXD1	O	Serial data output pins.
I^2C Bus Interface	SCL	I/O	Clock I/O pin.
	SDA	I/O	Data I/O pin.
Clock Synchronous Serial I/O with Chip Select	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
Reference Voltage Input	VREF	I	Reference voltage input pin to A/D converter.
A/D Converter	AN0 to AN11	I	Analog input pins to A/D converter.
I/O Port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, P6_0 to P6_7	I/O	CMOS I/O ports. Each port contains an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by a program.
Input Port	P4_2, P4_6, P4_7	I	Input only ports.

I: Input O: Output I/O: Input and output

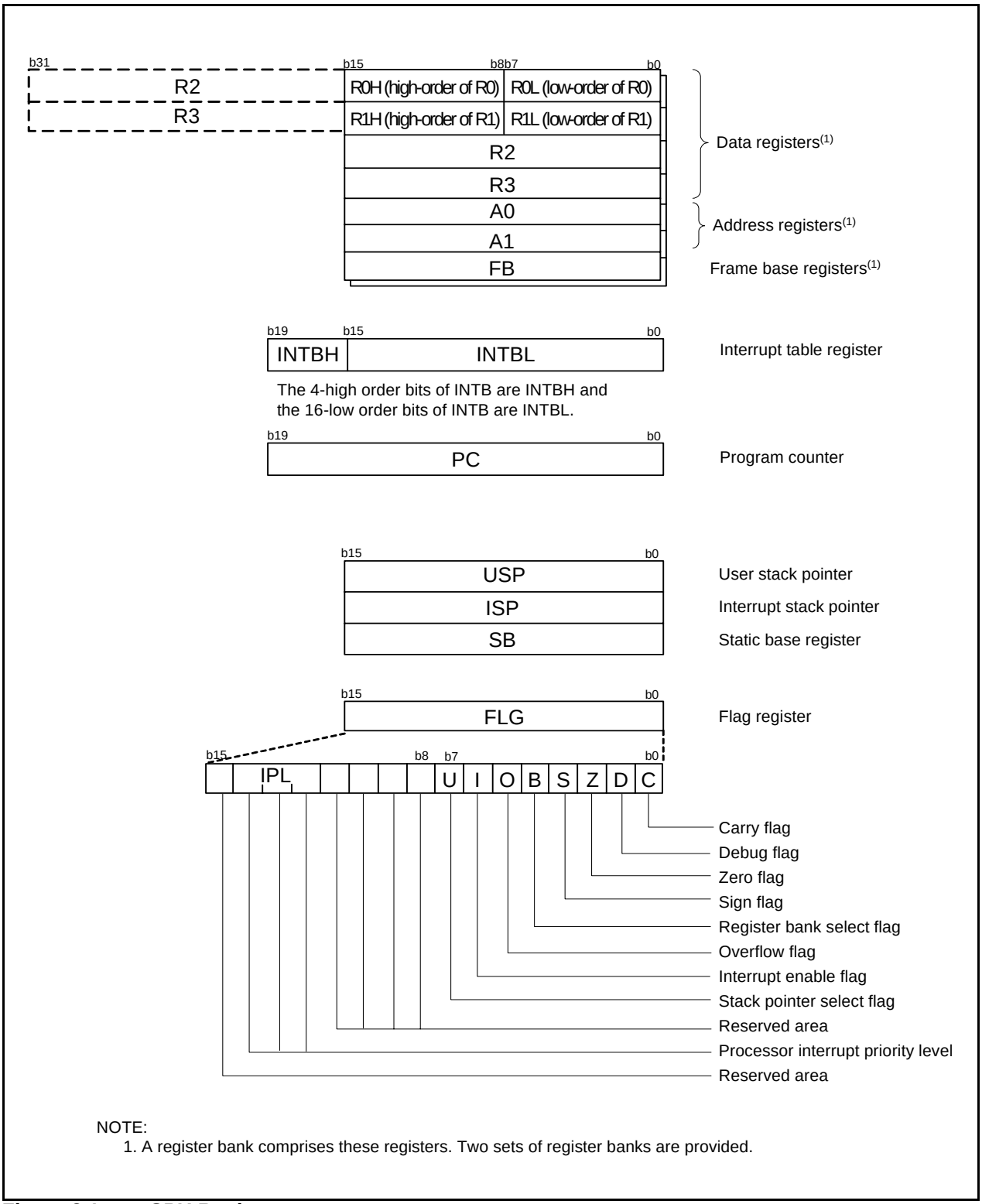
Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I^2C Bus Interface	A/D Converter
1		P3_5				SSCK	SCL	
2		P3_3				SSI		
3		P3_4				$\overline{SCS}$	SDA	
4	MODE							
5		P4_3						
6		P4_4						
7	$\overline{RESET}$							
8	XOUT	P4_7						
9	VSS/AVSS							
10	XIN	P4_6						
11	VCC/AVCC							
12		P2_7		TRDIOD1				
13		P2_6		TRDIOC1				
14		P2_5		TRDIOB1				
15		P2_4		TRDIOA1				
16		P2_3		TRDIOD0				
17		P2_2		TRDIOC0				
18		P2_1		TRDIOB0				
19		P2_0		TRDIOA0/TRDCLK				
20		P1_7	$\overline{INT1}$	TRAIO				
21		P1_6			CLK0			
22		P1_5	($\overline{INT1}$)(1)	(TRAIO)(1)	RXD0			
23		P1_4			TXD0			
24		P1_3	$\overline{KI3}$					AN11
25		P4_5	$\overline{INT0}$	$\overline{INT0}$				
26		P6_6	$\overline{INT2}$		TXD1			
27		P6_7	$\overline{INT3}$		RXD1			
28		P1_2	$\overline{KI2}$					AN10
29		P1_1	$\overline{KI1}$					AN9
30		P1_0	$\overline{KI0}$					AN8
31		P3_1		TRBO				
32		P3_0		TRAO				
33		P6_5						
34		P6_4						
35		P6_3						
36		P0_7						AN0
37		P0_6						AN1
38		P0_5						AN2
39		P0_4						AN3
40	VREF	P4_2						
41		P6_0		TREO				
42		P6_2						
43		P6_1						
44		P0_3						AN4
45		P0_2						AN5
46		P0_1						AN6
47		P0_0						AN7
48		P3_7				SSO		

NOTE:
1. Can be assigned to the pin in parentheses by a program.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1, and FB comprise a register bank. Two sets of register banks are provided.



NOTE:
1. A register bank comprises these registers. Two sets of register banks are provided.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3.
R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies R3R1 as R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0.
A1 can be combined with A0 to be used a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB, a 20-bit register, indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each.
The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU status.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation resulted in 0; otherwise, 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, 0.

2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is 0. The register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when the operation resulted in an overflow; otherwise, 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
An interrupt is disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

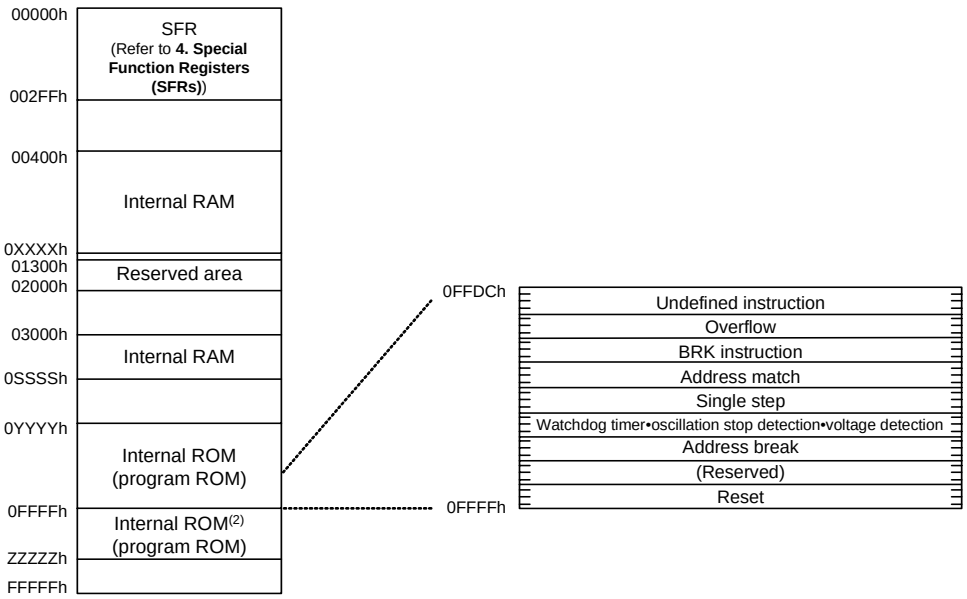
2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/20 Group

Figure 3.1 shows a Memory Map of R8C/20 Group. The R8C/20 Group has 1 Mbyte of address space from address 00000h to FFFFFh.
The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFR) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future user and cannot be accessed by users.



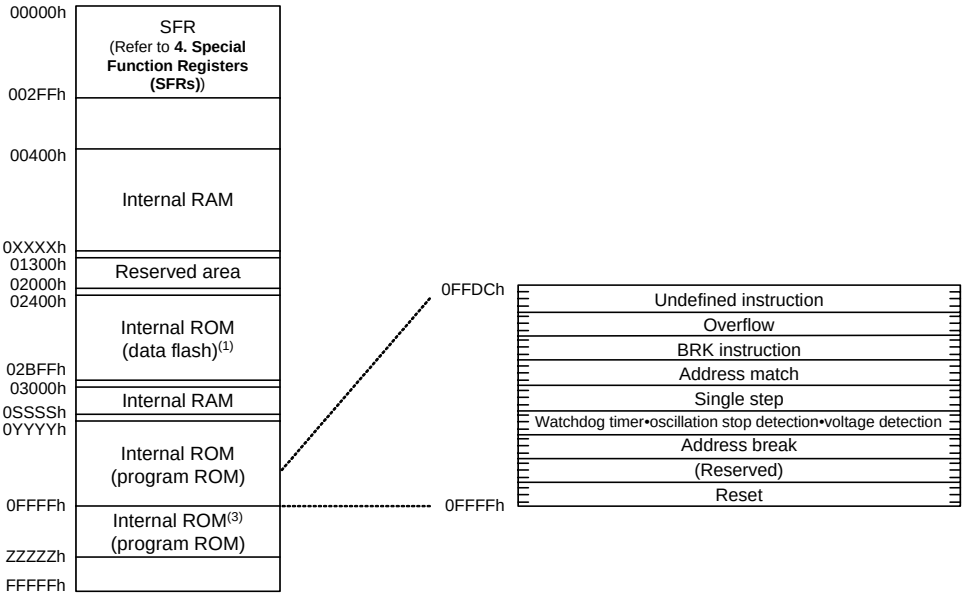
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **23. Notes on Emulator Debugger** of Hardware Manual.

Part Number	Internal ROM			Internal RAM		
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh	Address 0SSSSh
R5F21206JFP, R5F21206KFP	32 Kbytes	08000h	-	2 Kbytes	00BFFh	-
R5F21207JFP, R5F21207KFP	48 Kbytes	04000h	-	2.5 Kbytes	00DFFh	-
R5F21208JFP, R5F21208KFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh	-
R5F2120AJFP, R5F2120AKFP	96 Kbytes	04000h	1BFFFh	5 Kbytes	00FFFh	037FFh
R5F2120CJFP, R5F2120CKFP	128 Kbytes	04000h	23FFFh	6 Kbytes	00FFFh	03BFFh

Figure 3.1 Memory Map of R8C/20 Group

3.2 R8C/21 Group

Figure 3.2 shows a Memory Map of R8C/21 Group. The R8C/21 Group has 1 Mbyte of address space from address 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFR) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated them. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.
3. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **23. Notes on Emulator Debugger** of Hardware Manual.

Part Number	Internal ROM			Internal RAM		
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh	Address 0SSSSh
R5F21216JFP, R5F21216KFP	32 Kbytes	08000h	-	2 Kbytes	00BFFh	-
R5F21217JFP, R5F21217KFP	48 Kbytes	04000h	-	2.5 Kbytes	00DFFh	-
R5F21218JFP, R5F21218KFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh	-
R5F2121AJFP, R5F2121AKFP	96 Kbytes	04000h	1BFFFh	5 Kbytes	00FFFh	037FFh
R5F2121CJFP, R5F2121CKFP	128 Kbytes	04000h	23FFFh	6 Kbytes	00FFFh	03BFFh

Figure 3.2 Memory Map of R8C/21 Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function.
Table 4.1 to Table 4.6 list the SFR Information.

Table 4.1 SFR Information (1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protect Mode Register	CSPR	00h 10000000b[8]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[6]	VCA2	00h[3] 01000000b[4]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register[7]	VW1C	0000X000b[3] 0100X001b[4]
0037h	Voltage Monitor 2 Circuit Control Register[5]	VW2C	00h
0038h			
0039h			
003Fh			

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1.
4. Power-on reset, voltage monitor 1 reset or the LVD0ON bit in the OFS register is set to 0.
5. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b2 and b3.
6. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b7.
7. Software reset, the watchdog timer rest, and the voltage monitor 2 reset do not affect other than the b0 and b6.
8. The CSPROINI bit in the OFS register is 0.

Table 4.2 SFR Information (2)(1)

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register/IIC Bus Interrupt Control Register(2)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.3 SFR Information (3)(1)

Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
00A9h	UART1 Bit Rate Register	U1BRG	XXh
00AAh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AFh			XXh
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H/IIC Bus Control Register 1(2)	SSCRH/ICCR1	00h
00B9h	SS Control Register L/IIC Bus Control Register 2(2)	SSCRL/ICCR2	01111101b
00BAh	SS Mode Register/IIC Bus Mode Register 1(2)	SSMR/ICMR	00011000b
00BBh	SS Enable Register/IIC Bus Interrupt Enable Register(2)	SSER/ICIER	00h
00BCh	SS Status Register/IIC Bus Status Register(2)	SSSR/ICSR	00h/0000X000b
00BDh	SS Mode Register 2/Slave Address Register(2)	SSMR2/SAR	00h
00BEh	SS Transmit Data Register/IIC Bus Transmit Data Register(2)	SSTDR/ICDRT	FFh
00BFh	SS Receive Data Register/IIC Bus Receive Data Register(2)	SSRDR/ICDRR	FFh

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.4 SFR Information (4)(1)

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h	UART1 Function Select Register	U1SR	XXh
00F6h			
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX00XX00b
00FEh			
00FFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.5 SFR Information (5)(1)

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Counter Data Register	TRESEC	00h
0119h	Timer RE Compare Data Register	TREMIN	00h
011Ah			
011Bh			
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h			
0121h			
0122h			
0123h			
0124h			
0125h			
0126h			
0127h			
0128h			
0129h			
012Ah			
012Bh			
012Ch			
012Dh			
012Eh			
012Fh			
0130h			
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.6 SFR Information (6)(1)

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}/AV_{CC}	Supply voltage		-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	-40°C ≤ Topr ≤ 85°C	300	mW
		85°C < Topr ≤ 125°C	125	mW
T_{opr}	Operating ambient temperature		-40 to 85 (J version) / -40 to 125 (K version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage			2.7	–	5.5	V
V_{SS}/AV_{CC}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all Pins $I_{OH\ (peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak output “H” current			–	–	-10	mA
$I_{OH(avg)}$	Average output “H” current			–	–	-5	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all Pins $I_{OL\ (peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak output “L” currents			–	–	10	mA
$I_{OL(avg)}$	Average output “L” current			–	–	5	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
–	System clock	OCD2 = 0 When XIN clock is selected.	3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
		OCD2 = 1 When on-chip oscillator clock is selected.	FRA01 = 0 When low-speed on-chip oscillator clock is selected.	–	125	–	kHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected. 3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	–	–	20	MHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected.	–	–	10	MHz

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} = AVCC	–	–	10	Bits
–	Absolute Accuracy	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AVCC = 5.0 V	–	–	±3	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AVCC = 5.0 V	–	–	±2	LSB
		10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AVCC = 3.3 V	–	–	±5	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AVCC = 3.3 V	–	–	±2	LSB
R_{ladder}	Resistor ladder		V_{ref} = AVCC	10	–	40	kΩ
t_{conv}	Conversion time	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AVCC = 5.0 V	3.3	–	–	µs
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AVCC = 5.0 V	2.8	–	–	µs
V_{ref}	Reference voltage			2.7	–	AVCC	V
V_{IA}	Analog input voltage(2)			0	–	AVCC	V
–	A/D operating clock frequency	Without sample & hold		0.25	–	10	MHz
		With sample & hold		1	–	10	MHz

NOTES:
1. VCC = AVCC = 2.7 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. When analog input voltage exceeds reference voltage, A/D conversion result is 3FFh in 10-bit mode, FFh in 8-bit mode.

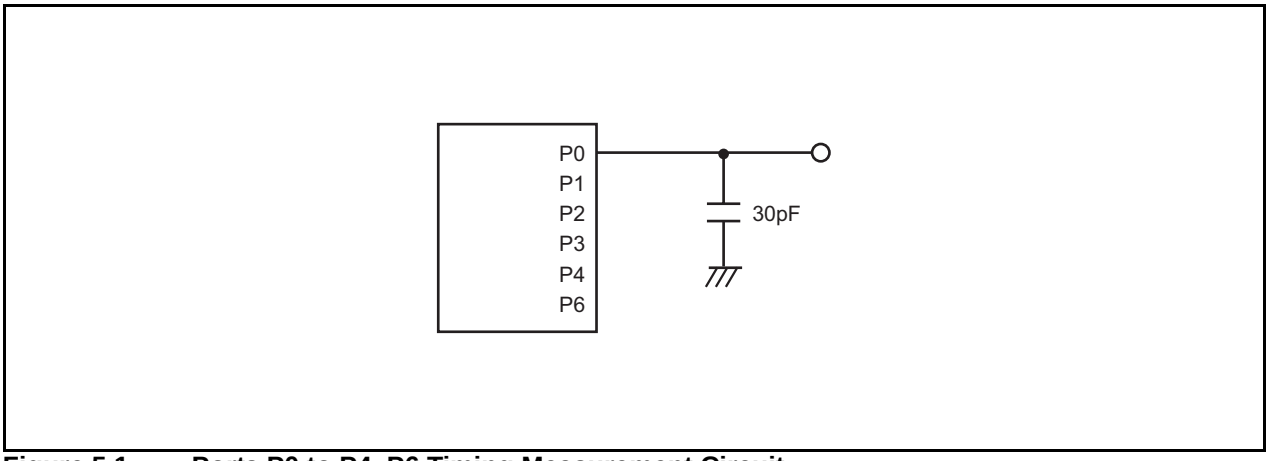


Figure 5.1 Ports P0 to P4, P6 Timing Measurement Circuit

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/20 Group	100(3)	–	–	times
		R8C/21 Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until erase suspend		–	–	97 + CPU clock × 6 cycle	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times.
   For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure endurance can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data Flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (Program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (Program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (Program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (Program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until erase suspend		–	–	97 + CPU clock × 6 cycle	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		-40	–	85(8)	°C
–	Data hold time(9)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times.
   For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. MInimum endurance to guarantee all electrical characteristics after program and erase (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times are the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure endurance can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
6. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. 125°C for K version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

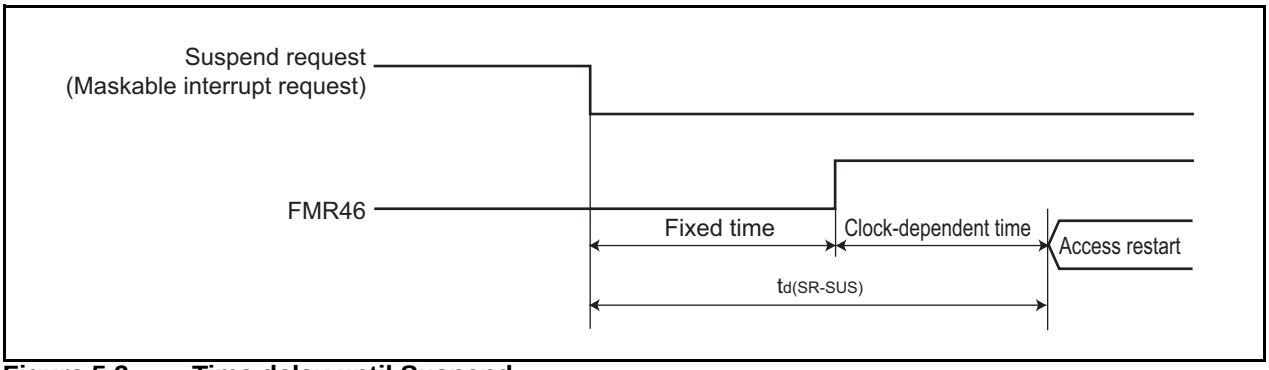


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level(3, 4)		2.70	2.85	3.00	V
$t_{d(Vdet1-A)}$	Voltage monitor 1 reset generation time(5)		–	40	200	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	100	µs
Vccmin	MCU operating voltage minimum value		2.70	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and Topr = -40°C to 85°C (J version) / -40°C to 125°C (K version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
3. Hold $V_{det2} > V_{det1}$.
4. This parameter shows the voltage detection level when the power supply drops. The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
5. Time until the voltage monitor 1 reset is generated after the voltage passes V_{det1} when V_{CC} falls. When using the digital filter, its sampling time is added to $t_{d(Vdet1-A)}$. When using the voltage monitor 1 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det1} when the power supply falls.

Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics

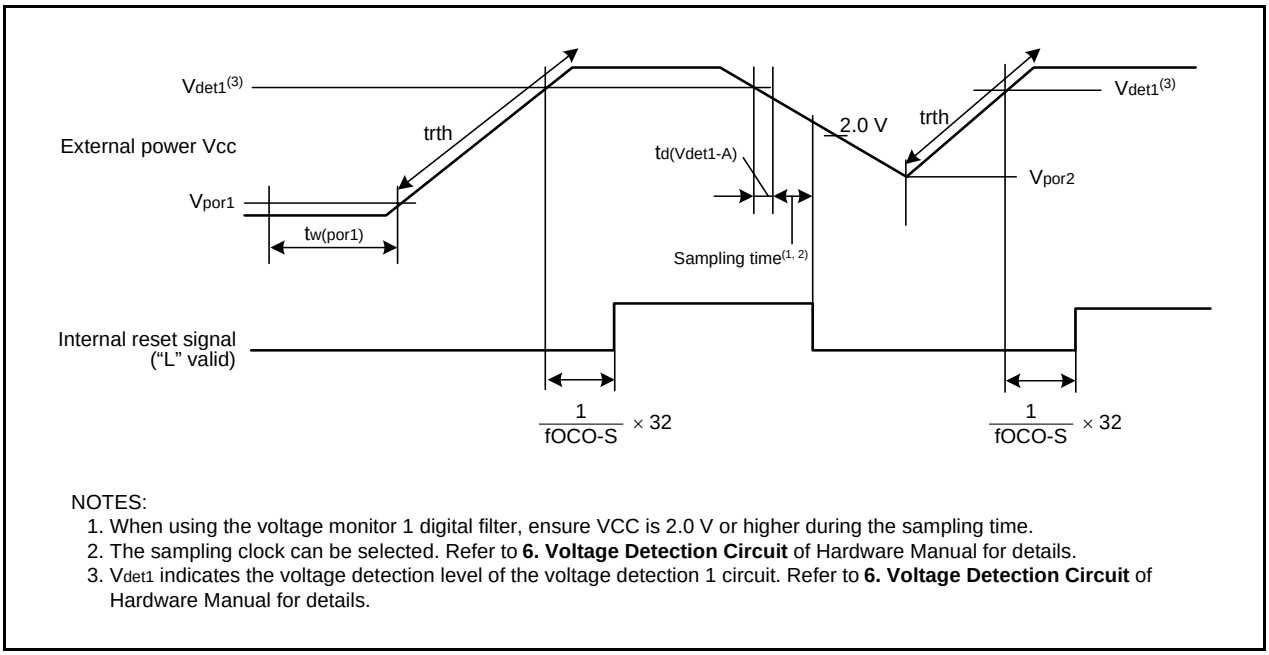
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level(4)		3.3	3.6	3.9	V
$t_{d(Vdet2-A)}$	Voltage monitor 2 reset/interrupt request generation time(2, 5)		–	40	200	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and Topr = -40°C to 85°C (J version) / -40°C to 125°C (K version).
2. Time until the voltage monitor 2 reset/interrupt request is generated since the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
4. Hold $V_{det2} > V_{det1}$.
5. When using the digital filter, its sampling time is added to $t_{d(Vdet2-A)}$. When using the voltage monitor 2 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det2} when the power supply falls.

Table 5.8 Power-on Reset Circuit, Voltage Monitor 1 Reset Circuit Electrical Characteristics(3)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage(4)		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 1 valid voltage		0	–	Vdet1	V
trth	External power V_{CC} rise gradient	$V_{CC} \leq 3.6$ V	20(2)	–	–	mV/msec
		$V_{CC} > 3.6$ V	20(2)	–	2,000	mV/msec

NOTES:
1. Topr = -40°C to 85°C (J version) / -40°C to 125°C (K version), unless otherwise specified.
2. This condition (the minimum value of external power V_{CC} rise gradient) does not apply if $V_{por2} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0, the VW1C0 and VW1C6 bits in the VW1C register to 1 respectively, and the VCA26 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain tw(por1) for 30s or more if -20°C ≤ Topr ≤ 125°C, maintain $t_{w(por1)}$ for 3,000s or more if -40°C ≤ Topr < -20°C.



NOTES:
1. When using the voltage monitor 1 digital filter, ensure VCC is 2.0 V or higher during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

Table 5.9 High-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 4.75 V to 5.25 V, 0°C ≤ Topr ≤ 60°C(2)	39.2	40	40.8	MHz
		V_{CC} = 3.0 V to 5.25 V, -20°C ≤ Topr ≤ 85°C(2)	38.8	40	41.2	MHz
		V_{CC} = 3.0 V to 5.5 V, -40°C ≤ Topr ≤ 85°C(2)	38.4	40	41.6	MHz
		V_{CC} = 3.0 V to 5.5 V, -40°C ≤ Topr ≤ 125°C(2)	38.0	40	42.0	MHz
		V_{CC} = 2.7 V to 5.5 V, -40°C ≤ Topr ≤ 125°C(2)	37.6	40	42.4	MHz
–	The value of the FRA1 register when the reset is deasserted		08h	40	F7h	–
–	High-speed on-chip oscillator adjustment range	Adjust the FRA1 register to -1 bit (the value when the reset is deasserted)	–	+ 0.3	–	MHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption when high-speed on-chip oscillator oscillating	V_{CC} = 5.0 V, Topr = 25°C	–	600	–	µA

NOTES:
1. V_{CC} = 2.7 V to 5.5 V, Topr = -40°C to 85°C (J version) / -40°C to 125°C (K version), unless otherwise specified.
2. The standard value shows when the reset is deasserted for the FRA1 register.

Table 5.10 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		40	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption when low-speed on-chip oscillator oscillating	V_{CC} = 5.0 V, Topr = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.7 V to 5.5 V, Topr = -40°C to 85°C (J version) / -40°C to 125°C (K version), unless otherwise specified.

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and Topr = -40°C to 85°C (J version) / -40°C to 125°C (K version), unless otherwise specified.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts since the interrupt is acknowledged to exit stop mode.

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}(2)
t_{SA}	SSI slave access time			–	–	1t_{CYC} + 100	ns
t_{OR}	SSI slave out open time			–	–	1t_{CYC} + 100	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

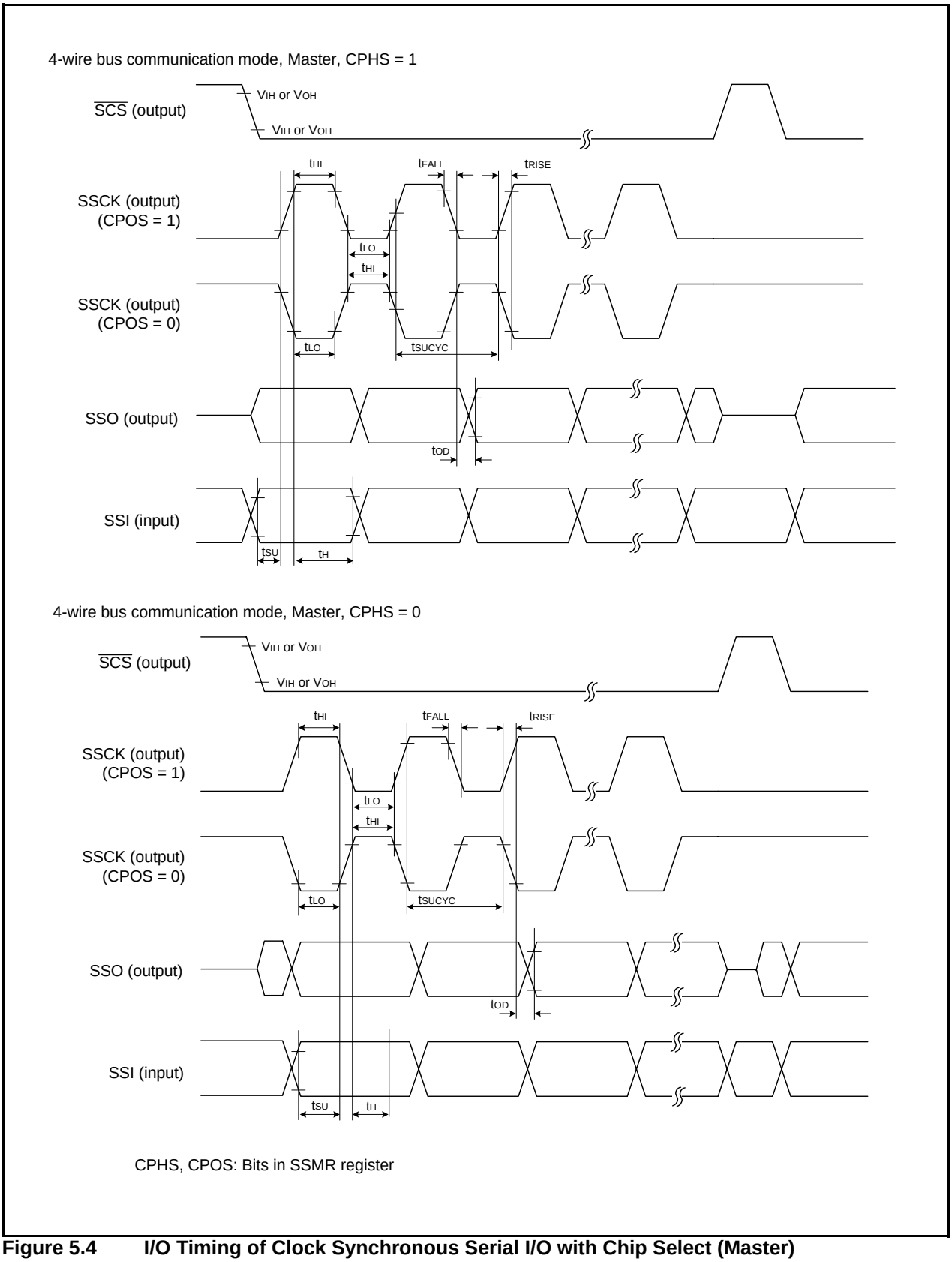


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

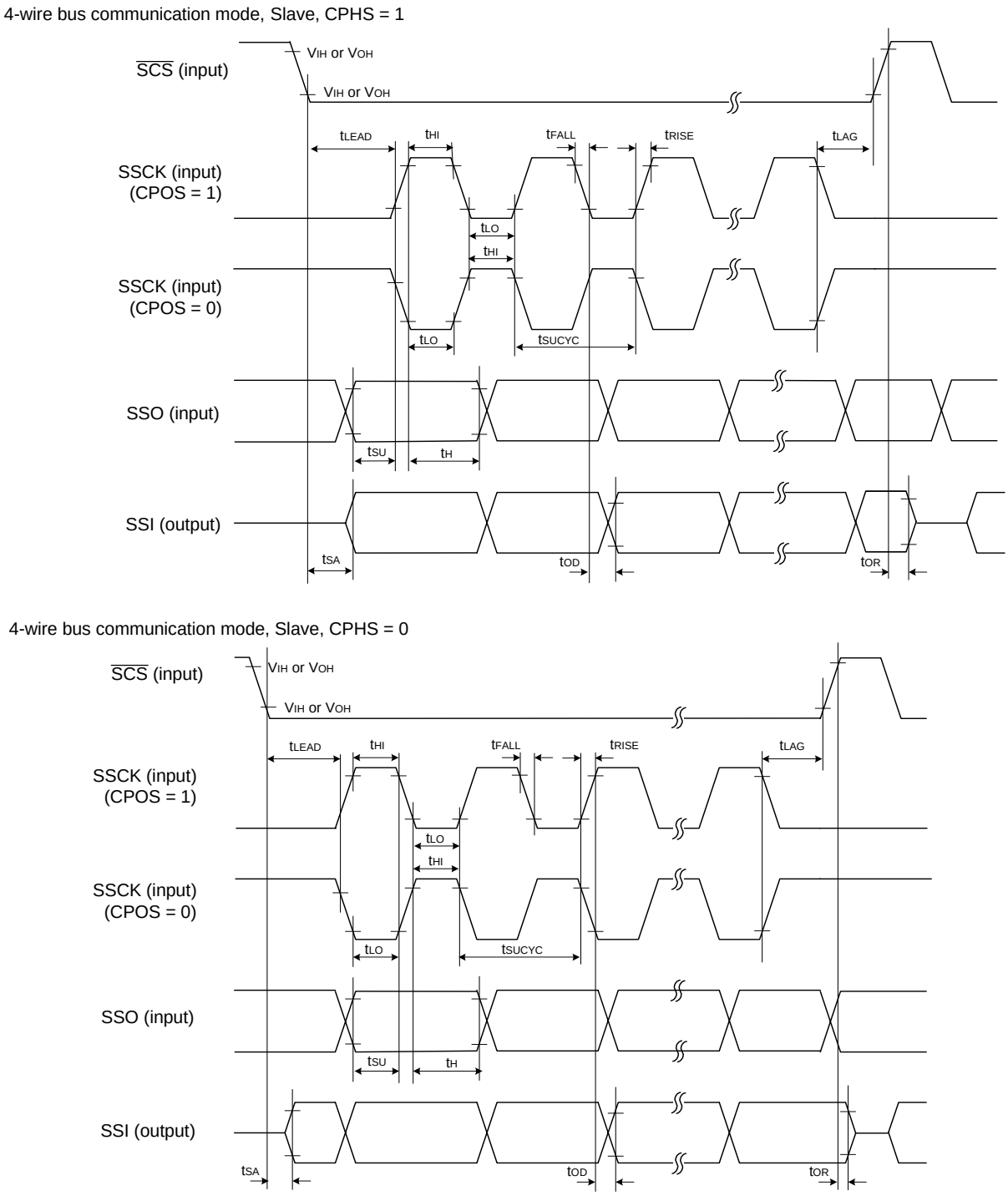


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

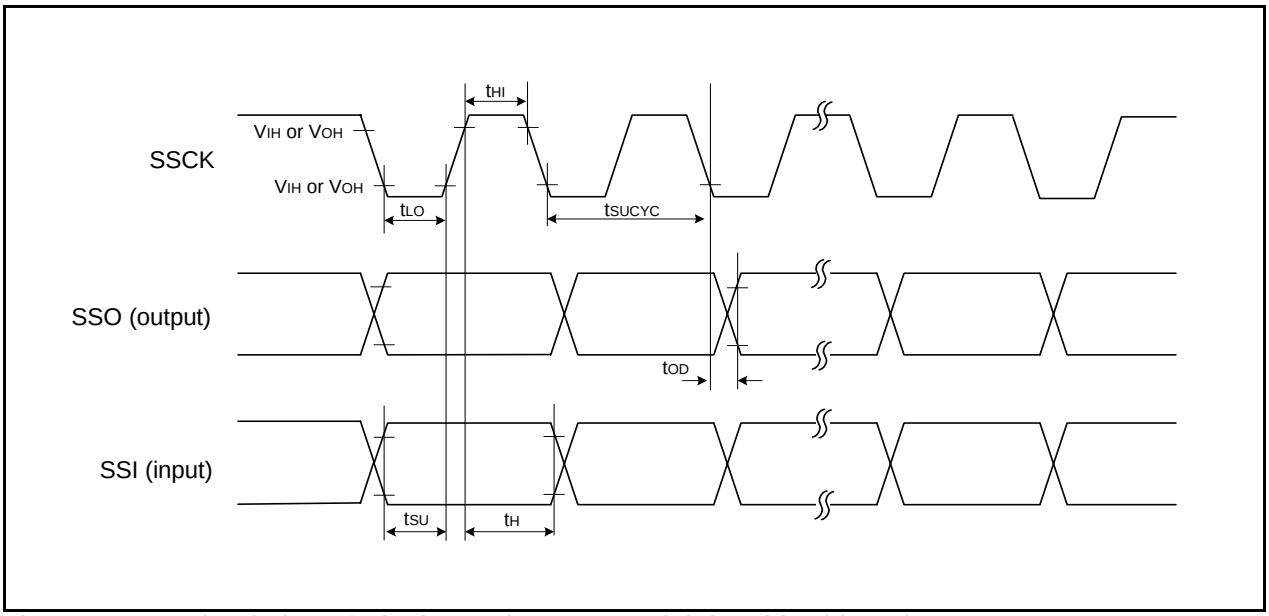
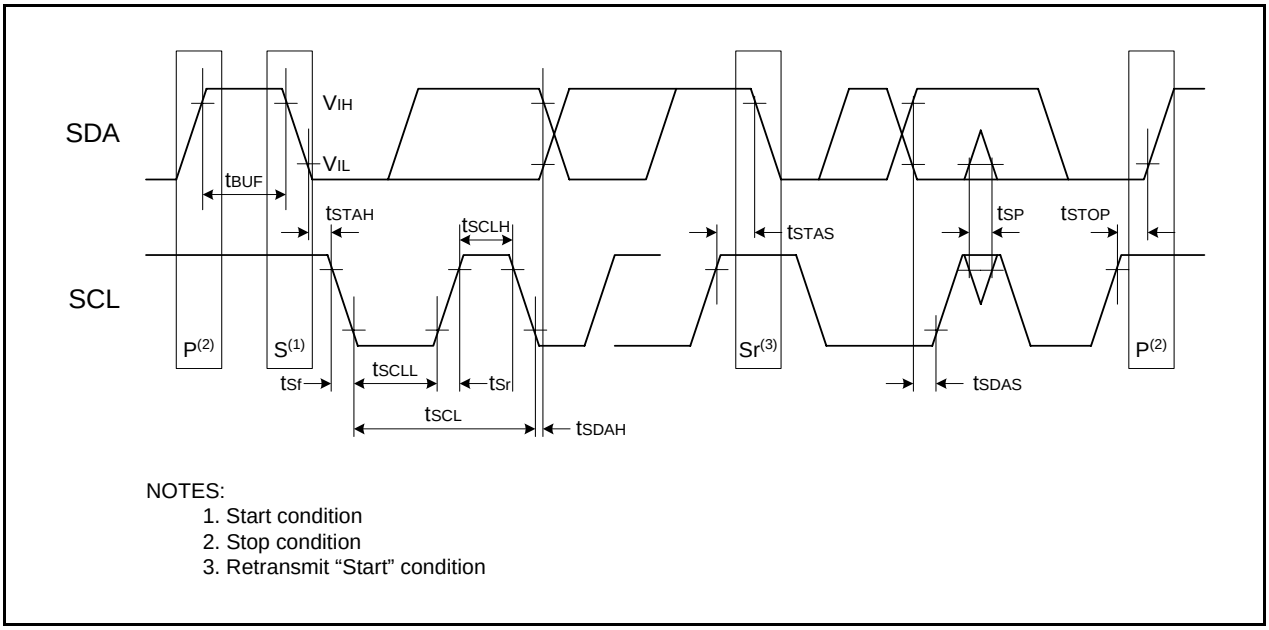


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.13 Timing Requirements of I²C Bus Interface(1)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC}$ + 600(2)	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC}$ + 300(2)	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC}$ + 300(2)	–	–	ns
t_{sf}	SCL, SDA input falling time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}$(2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$(2)	–	–	ns
t_{STAH}	Start condition input hole time		$3t_{CYC}$(2)	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{SOAS}	Data input setup time		$1t_{CYC}$ + 20(2)	–	–	ns
t_{SDAH}	Data input hold time		0	–	–	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)



NOTES:
1. Start condition
2. Stop condition
3. Retransmit “Start” condition

Figure 5.7 I/O Timing of I²C Bus Interface

Table 5.14 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” Voltage	Except XOUT	I_{OH} = -5 mA		V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = -200 μA		V_{CC} – 0.3	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -1 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -500 μA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output “L” Voltage	Except XOUT	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 μA		–	–	0.45	V
		XOUT	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 μA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		$\overline{RESET}$			0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5 V		–	–	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5 V		–	–	-5.0	μA
R_{PULLUP}	Pull-Up Resistance		VI = 0 V, V_{CC} = 5 V		30	50	167	kΩ
R_{fXIN}	Feedback Resistance	XIN			–	1.0	–	MΩ
V_{RAM}	RAM Hold Voltage		During stop mode		2.0	–	–	V

NOTE:
1. V_{CC} = 4.2 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.15 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = -40 to 85°C (J version) / -40 to 125°C (K version), Unless Otherwise Specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) In single-chip mode, the output pins are open and other pins are Vss	High-clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	11.0	22.0	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	8.8	17.6	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.8	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5.0	–	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.8	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.8	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.8	11.6	mA
			XIN clock off High-speed on-chip oscillator on fOCO= 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	143	286	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA20 = 0 VCA26 = VCA27 = 0	–	53	106	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA20 = 0 VCA26 = VCA27 = 0	–	38	76	µA
		Stop mode Topr = 25°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.8	3.0	µA
		Stop mode Topr = 85°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	1.2	–	µA
		Stop mode Topr = 125°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	4.0	–	µA

Timing Requirements (Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.16 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns

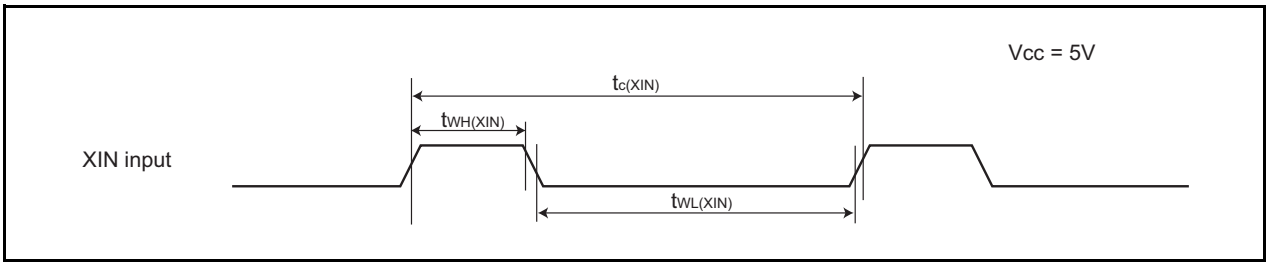


Figure 5.8 XIN Input Timing Diagram when Vcc = 5 V

Table 5.17 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

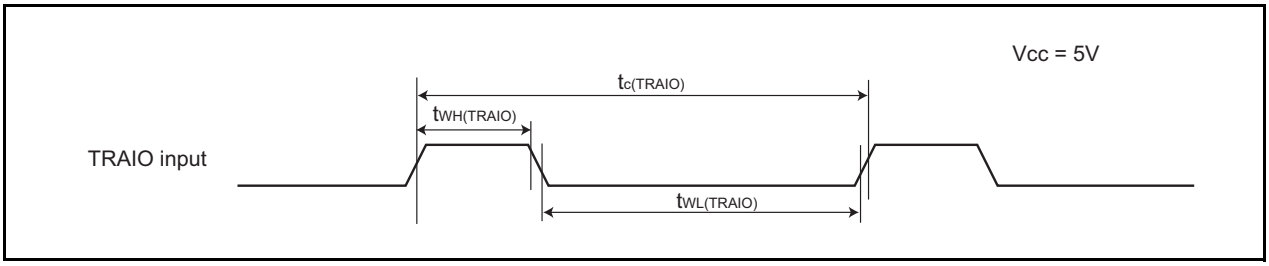


Figure 5.9 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.18 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	100	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

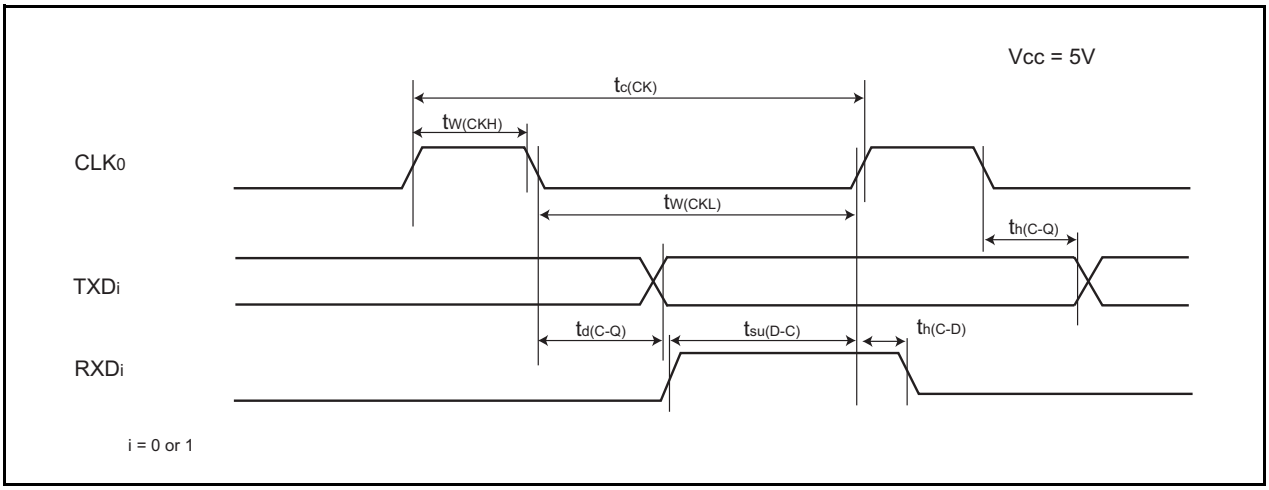


Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.19 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

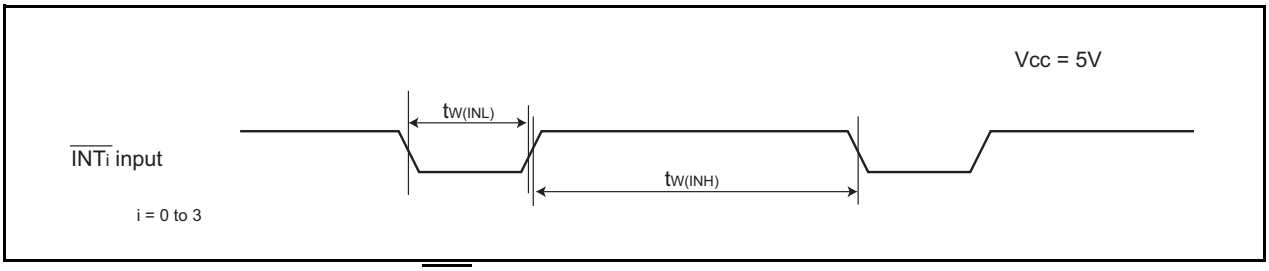


Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V (i = 0 to 3)

Table 5.20 Electrical Characteristics (3) [Vcc = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except XOUT	I_{OH} = -1 mA		V_{CC} – 0.5	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -0.1 mA	V_{CC} – 0.5	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -50 μA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except XOUT	I_{OL} = 1 mA		–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.3	–	V
		$\overline{RESET}$			0.1	0.4	–	V
I_{IH}	Input “H” current		VI = 3 V, V_{CC} = 3 V		–	–	4.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3 V		–	–	-4.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3 V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	3.0	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		2.0	–	–	V

NOTE:
1. V_{CC} = 2.7 to 3.3 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.21 Electrical Characteristics (4) [Vcc = 3 V]
(Topr = -40 to 85°C (J version) / -40 to 125°C (K version), Unless Otherwise Specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) In single-chip mode, the output pins are open and other pins are Vss	High-clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10.5	21.0	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	8.3	16.6	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.3	10.6	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4.5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.3	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.3	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.6	11.2	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.4	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	138	276	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA20 = 0 VCA26 = VCA27 = 0	–	48	96	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA20 = 0 VCA26 = VCA27 = 0	–	35	70	µA
		Stop mode Topr = 25°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.7	3.0	µA
		Stop mode Topr = 85°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	1.1	–	µA
		Stop mode Topr = 125°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	3.8	–	µA

Timing Requirements (Unless Otherwise Specified: Vcc = 3 V, Vss = 0V at Topr = 25°C) [Vcc = 3 V]

Table 5.22 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns

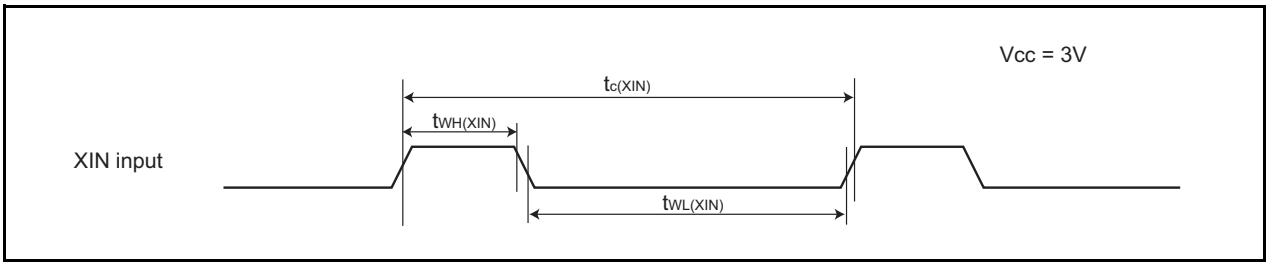


Figure 5.12 XIN Input Timing Diagram when Vcc = 3 V

Table 5.23 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input Cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

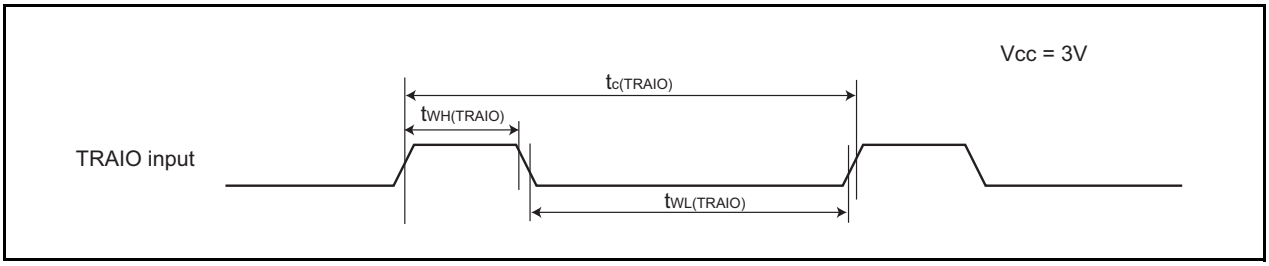


Figure 5.13 TRAIO Input Timing Diagram when Vcc = 3 V

Table 5.24 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	150	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

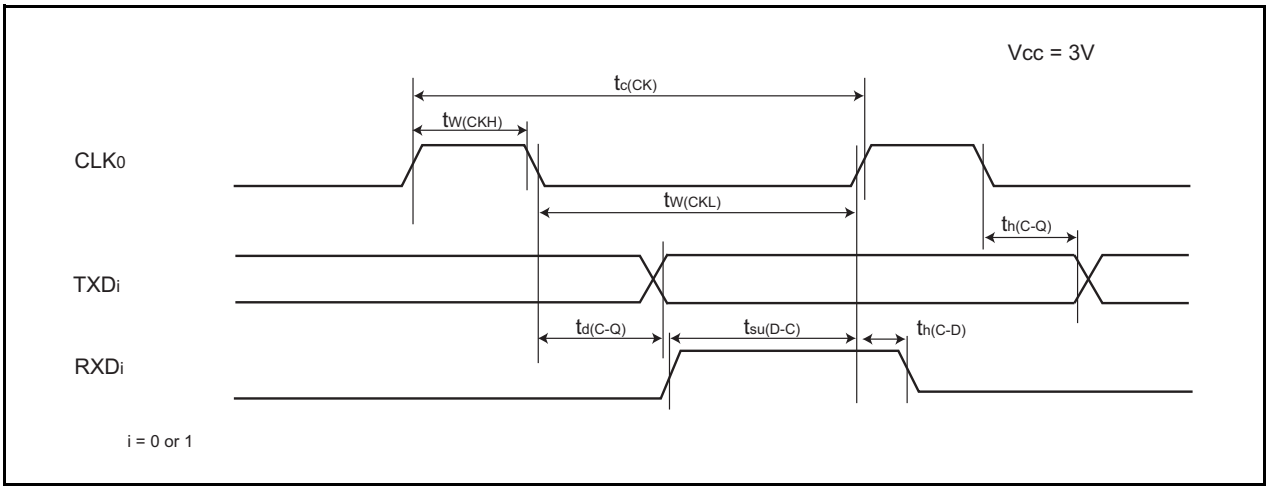


Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.25 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

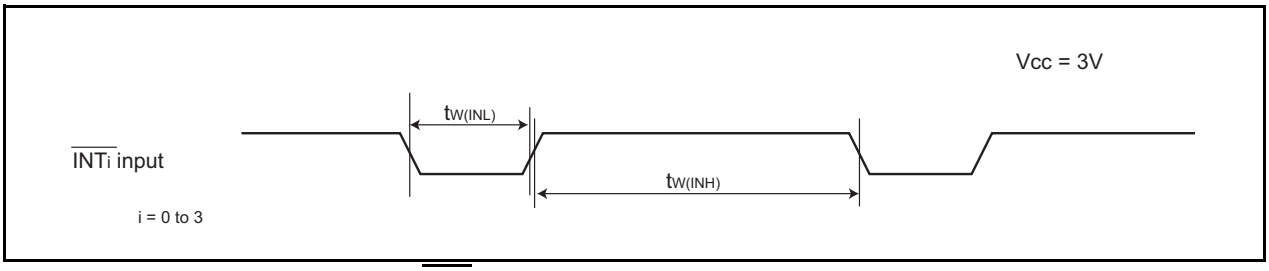
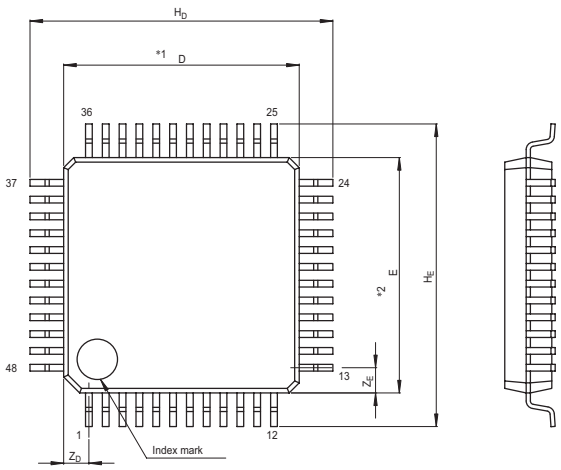


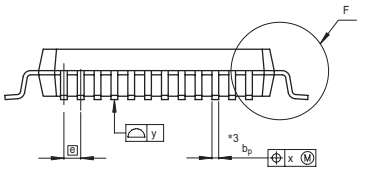
Figure 5.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V (i = 0 to 3)

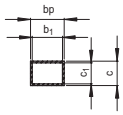
Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

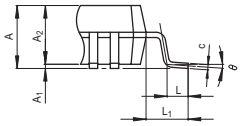
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g







Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	R8C/20 Group, R8C/21 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Mar 08, 2005	–	First Edition issued
0.20	Sep 29, 2005	–	Words standardized - Clock synchronous serial interface → Clock synchronous serial I/O - Chip-select clock synchronous interface(SSU) → Clock synchronous serial I/O with chip select - I^2C bus interface(IIC) → I^2C bus interface
		2, 3	Table1.1 R8C/20 Group Performance, Table1.2 R8C/21 Group Performance Serial Interface revised: - Clock Synchronous Serial Interface: 1 channel I^2C bus Interface (3), Clock synchronous serial I/O with chip select - Power-On Reset Circuit added - Power Consumption value determined
		5, 6	Table 1.3 Product Information of R8C/20 Group, Table 1.4 Product Information of R8C/21 Group Date revised.
		7	Figure 1.4 Pin Assignment Pin name revised: - P3_5/$\overline{\text{SSC}}$K(/SCL) → P3_5/ SCL/$\overline{\text{SSC}}$K - P3_4/$\overline{\text{SCS}}$(/SDA) → P3_4/ SDA /$\overline{\text{SCS}}$ - VSS → VSS/AVSS - VCC → VCC/AVCC - P1_5/$\overline{\text{RXD0}}$/(TRAIO/$\overline{\text{INT1}}$) → P1_5/$\overline{\text{RXD0}}$/(TRAIO)/($\overline{\text{INT1}}$) - P6_6/$\overline{\text{INT2}}$/(TXD1) → P6_6/$\overline{\text{INT2}}$/TXD1 - P6_7/$\overline{\text{INT3}}$/(RXD1) → P6_7/$\overline{\text{INT3}}$/RXD1 - NOTE2 added
		8	Table 1.5 Pin Description - Analog Power Supply Input: line added - I^2C Bus Interface (IIC) → I^2C Bus Interface - SSU → Clock Synchronous Serial I/O with Chip Select
		9	Table 1.6 Pin Name Information by Pin Number revised - Pin Number 1: (SCL) → SCL - Pin Number 2: (SDA) → SDA - Pin Number 9: VSS → VSS/AVSS - Pin Number 11: VCC → VCC/AVCC - Pin Number 26: (TXD1) → TXD1 - Pin Number 27: (RXD1) → RXD1
		15	Table 4.1 SFR Information (1) revised - 0013h: XXXXXX00b → 00h
		17	Table 4.3 SFR Information (3) revised - 00BCh: 0000X000b → 00h/0000X000b
		18	Table 4.4 SFR Information (4) revised - 00D6h: 00000XXXb → 00h - 00F5h: UART1 Function Select Register added
		19	Table 4.5 SFR Information (5) revised - 0104h: TRATR → TRA

REVISION HISTORY	R8C/20 Group, R8C/21 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.20	Sep 29, 2005	20	Table 4.6 SFR Information (6) revised - 0145h: POCR0 → TRDPOCR0 - 0146h, 0147h: TRDCNT0 → TRD0 - 0148h, 0149h: GRA0 → TRDGRA0 - 014Ah, 014Bh: GRB0 → TRDGRB0 - 014Ch, 014Dh: GRC0 → TRDGRC0 - 014Eh, 014Fh: GRD0 → TRDGRD0 - 0155h: POCR1 -> TRDPOCR1 - 0156h, 0157h: TRDCNT1 → TRD1 - 0158h, 0159h: GRA1 → TRDGRA1 - 015Ah, 015Bh: GRB1 → TRDGRB1 - 015Ch, 015Dh: GRC1 → TRDGRC1 - 015Eh, 015Fh: GRD1 → TRDGRD1
		22	5. Electrical Characteristics added
1.00	Nov 15, 2006	All pages	“Preliminary” and “Under development” deleted
		2	Table 1.1 Functions and Specifications for R8C/20 Group revised. NOTE1 deleted.
		3	Table 1.2 Functions and Specifications for R8C/21 Group revised. NOTE1 deleted.
		5	Table 1.3 Product Information for R8C/20 Group; “R5F2120AJFP (D)”, “R5F2120CJFP (D)”, “R5F2120AKFP (D)”, “R5F2120CKFP (D)”, and NOTE added. Figure 1.2 Type Number, Memory Size, and Package of R8C/20 Group; “A: 96 KB” and “C: 128 KB” added.
		6	Table 1.4 Product Information for R8C/21 Group; “R5F2121AJFP (D)”, “R5F2121CJFP (D)”, “R5F2121AKFP (D)”, “R5F2121CKFP (D)”, and NOTE added. Figure 1.3 Type Number, Memory Size, and Package of R8C/21 Group; “A: 96 KB” and “C: 128 KB” added.
		13	Figure 3.1 Memory Map of R8C/20 Group revised.
		14	Figure 3.2 Memory Map of R8C/21 Group revised.
		15	Table 4.1 SFR Information (1)(1); NOTE8; “The CSPROINI bit in the OFS register is set to 0.” → “The CSPROINI bit in the OFS register is 0.” revised.
		21	Table 5.1 Absolute Maximum Ratings; Power dissipation revised. Table 5.2 Recommended Operating Conditions; System clock revised.
		26	Table 5.8 Voltage Monitor 1 Reset Circuit Electrical Characteristics → Table 5.8 Power-on Reset Circuit, Voltage Monitor 1 Reset Circuit Electrical Characteristics(1) replaced. Table 5.8 revised. NOTE3 added. Table 5.9 Power-on Reset Circuit Electrical Characteristics deleted. Figure 5.3 Power-on Reset Circuit Electrical Characteristics revised.
		27	Table 5.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics → Table 5.9 High-Speed On-Chip Oscillator Circuit Electrical Characteristics revised.

REVISION HISTORY	R8C/20 Group, R8C/21 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Nov 15, 2006	33	Table 5.15 Electrical Characteristics (1) [VCC = 5 V] → Table 5.14 Electrical Characteristics (1) [VCC = 5 V] revised. RAM Hold Voltage, Min.; “1.8” → “2.0” corrected.
		34	Table 5.16 Electrical Characteristics (2) [Vcc = 5 V] → Table 5.15 Electrical Characteristics (2) [Vcc = 5 V] revised. Wait mode revised.
		37	Table 5.21 Electrical Characteristics (3) [VCC = 3 V → Table 5.20 Electrical Characteristics (3) [VCC = 3 V] revised. RAM hold voltage, Min.;“1.8” → “2.0” corrected.
		38	Table 5.22 Electrical Characteristics (4) [Vcc = 3 V] → Table 5.21 Electrical Characteristics (4) [Vcc = 3 V] revised. Wait mode revised.
2.00	Aug 27, 2008	–	“RENESAS TECHNICAL UPDATE” reflected: TN-16C-A172A/E
		5, 6	Table 1.3, Table 1.4 revised Figure 1.2, Figure 1.3; ROM number “XXX” added
		13, 14	Figure 3.1, Figure 3.2; “Expanding area” deleted
		21	Table 5.2; NOTE2 revised
		23	Table 5.4; NOTE2 and NOTE4 revised
		24	Table 5.5; NOTE2 and NOTE5 revised
		25	Table 5.6; “td(Vdet1-A)” added, NOTE5 added Table 5.7; “td(Vdet2-A)” and NOTE2 revised, NOTE5 added
		26	Table 5.8; “trth” and NOTE2 revised Figure 5.3 revised

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

Colophon .7.2

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Renesas Electronics:

R5F2121AJFP#U0 R5F21217KFP#U1 R5F2121AKFP#U0 R5F21216KFP#U1 R5F21218JFP#U1 R5F2120CKFP#U0 R5F2121CKFP#U0 R5F21206JFP#U1 R5F21206KFP#U1 R5F21216JFP#U1 R5F21208JFP#U1 R5F21208KFP#U1 R5F21217JFP#U1 R5F2120AKFP#U0 R5F2120CJFP#U0 R5F2121CJFP#U0 R5F2120AJFP#U0 R5F21207JFP#U1