RA2A1 Group

Evaluation Kit for RA2A1 Microcontroller Group
EK-RA2A1 v1
User's Manual

Renesas RA Family
RA2 Series

Renesas Electronics

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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Contact information

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Precautions

This Evaluation Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

• Ensure attached cables do not lie across the equipment.

• Reorient the receiving antenna.

• Increase the distance between the equipment and the receiver.

• Connect the equipment into an outlet on a circuit different from that which the receiver is connected.

• Power down the equipment when not in use.

• Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

• The user is advised that mobile phones should not be used within 10 m of the product when in use.

• The user is advised to take ESD precautions when handling the equipment.

The Evaluation Kit does not represent an ideal reference design for an end product and does not fulfill the regulatory standards for an end product.

Renesas RA Microcontrollers

EK-RA2A1 v1

Contents

1.   Kit Overview

The EK-RA2A1 v1 enables developers to get started with initial firmware development.

- Renesas RA2A1 Microcontroller Group
  — R7FA2A1AB3CFM
  — 64-pin LQFP package
  — 48 MHz Arm® Cortex®-M23 core (Armv8-M architecture) with Arm MPU
  — 32 KB SRAM
  — 256 KB code flash memory
  — 8 KB data flash memory
- Connectivity
  — A Device USB connector for the Main MCU
  — S124 MCU based SEGGER J-Link® On-Board interface for debugging and programming of the RA2A1 MCU. A 10-pin JTAG/SWD interface is also provided for connecting optional external debuggers and programmers.
  — Two PMOD connectors, allowing use of appropriate PMOD compliant peripheral plug-in modules for rapid prototyping
  — Pin headers for access to power and signals for the Main MCU
- Multiple clock sources
  — Main MCU oscillator crystals, providing precision 12.000 MHz and 32,768 Hz external reference clocks
  — Additional low-precision clocks are available internal to the Main MCU
- MCU reset push-button switch
- MCU boot configuration jumper
- General purpose I/O ports
  — One jumper to allow measuring of Main MCU current
  — Copper jumpers on PCB bottom side for configuration and access to selected MCU signals
- Operating voltage
  — External 5V input through the Debug USB connector supplies the on-board power regulator, which provides 3.3V to power the board logic and interfaces. External 5V or 3.3V may be also supplied through alternate locations on the Evaluation Kit Board.
- A two-color board status LED indicating availability of regulated power and connection status of the J-Link interface
- A red User LED, controlled by the Main MCU firmware
- A User Push-Button switch, User Capacitive Touch Button sensor, and an optional User Potentiometer, all of which are controlled by the Main MCU firmware
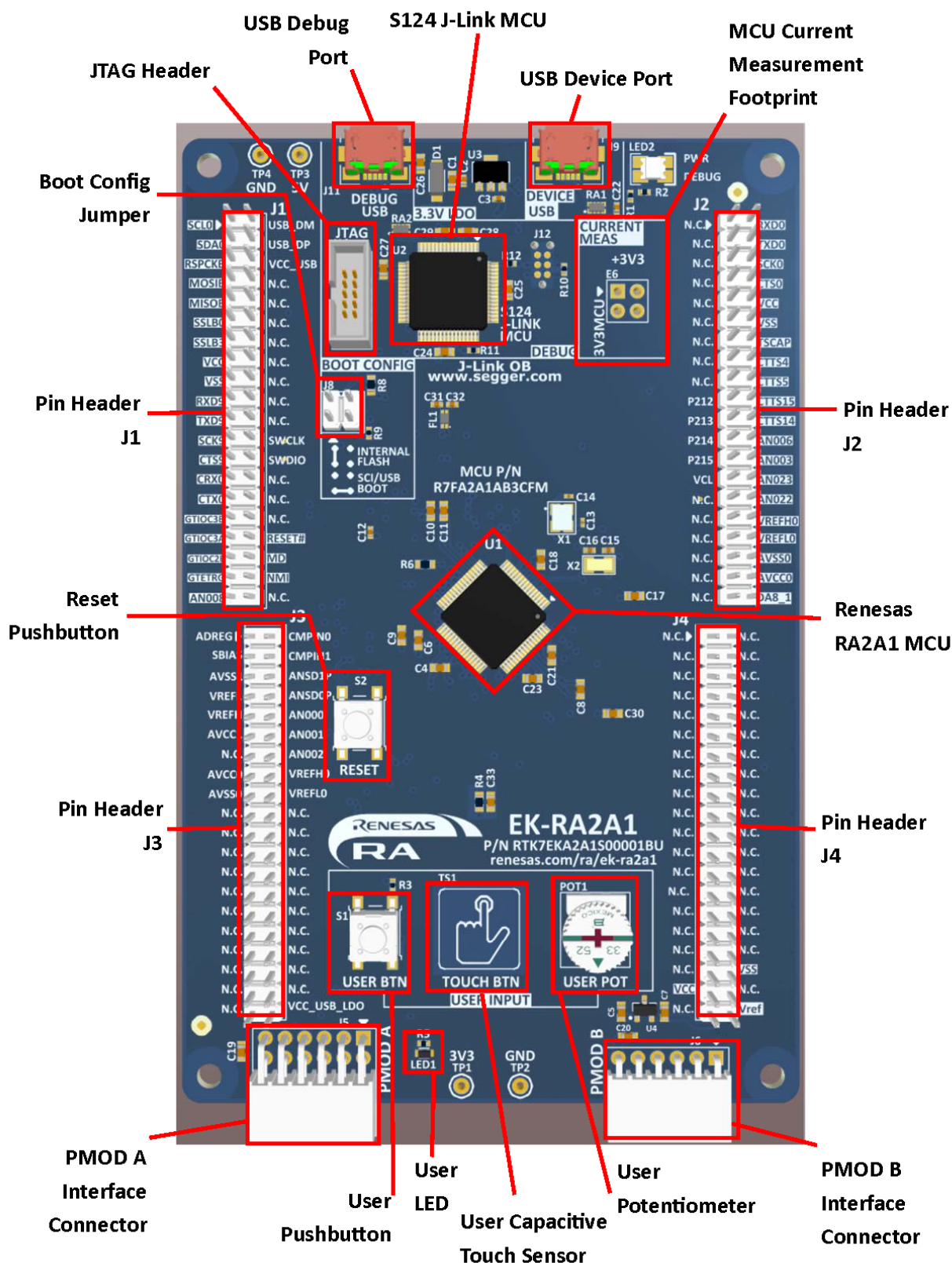
Figure 1.   EK-RA2A1 v1 Top Side

Figure 2.   EK-RA2A1 v1 Bottom Side
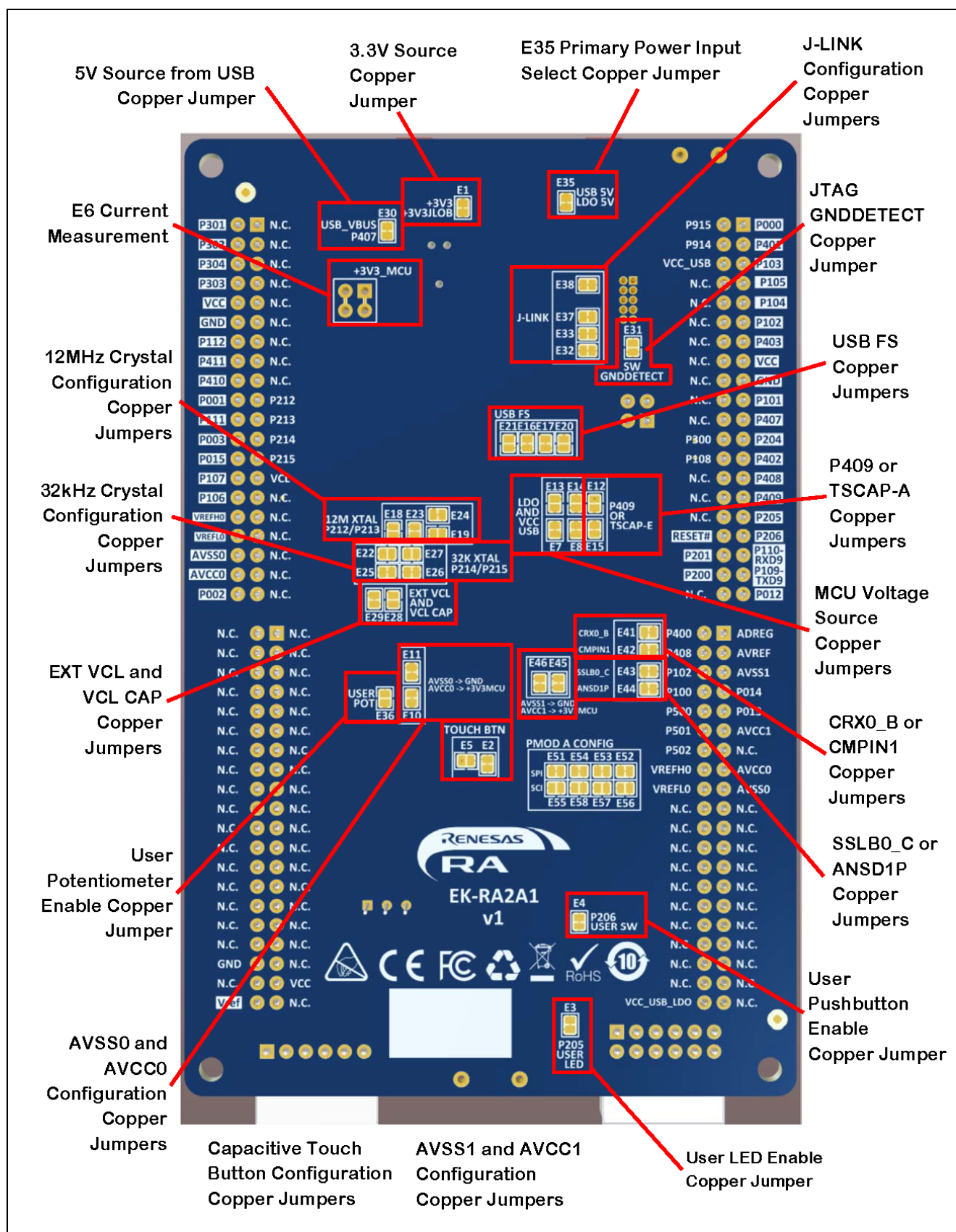
1.1   Assumptions and Advisory Notes

1. It is assumed that the user has a basic understanding of microcontrollers and embedded systems hardware
2. It is recommended that the user refers to the EK-RA2A1 - Quick Start Guide to become acquainted with the kit and the Quick Start example the EK-RA2A1 comes preprogrammed with.
3. Flexible Software Package (FSP) and Integrated Development Environment (IDE) such as e^2 studio are required to develop embedded applications on EK-RA2A1. Instructions to download and install software are provided in the Quick Start Guide.
4. Additionally, the instructions to import example projects, build them and program the EK-RA2A1 are also provided in the Quick Start Guide.

2.   Kit Contents

The following components are included in the kit:

1. One EK-RA2A1 board
2. One USB Type-A to USB Micro-B cable

Figure 3.   EK-RA2A1 v1 Kit Contents

3.   Ordering Information

EK-RA2A1 Orderable Part Number: RTK7EKA2A1S00001BU

4.   Hardware Details

4.1   Jumpers Settings

4.1.1   Copper Jumpers

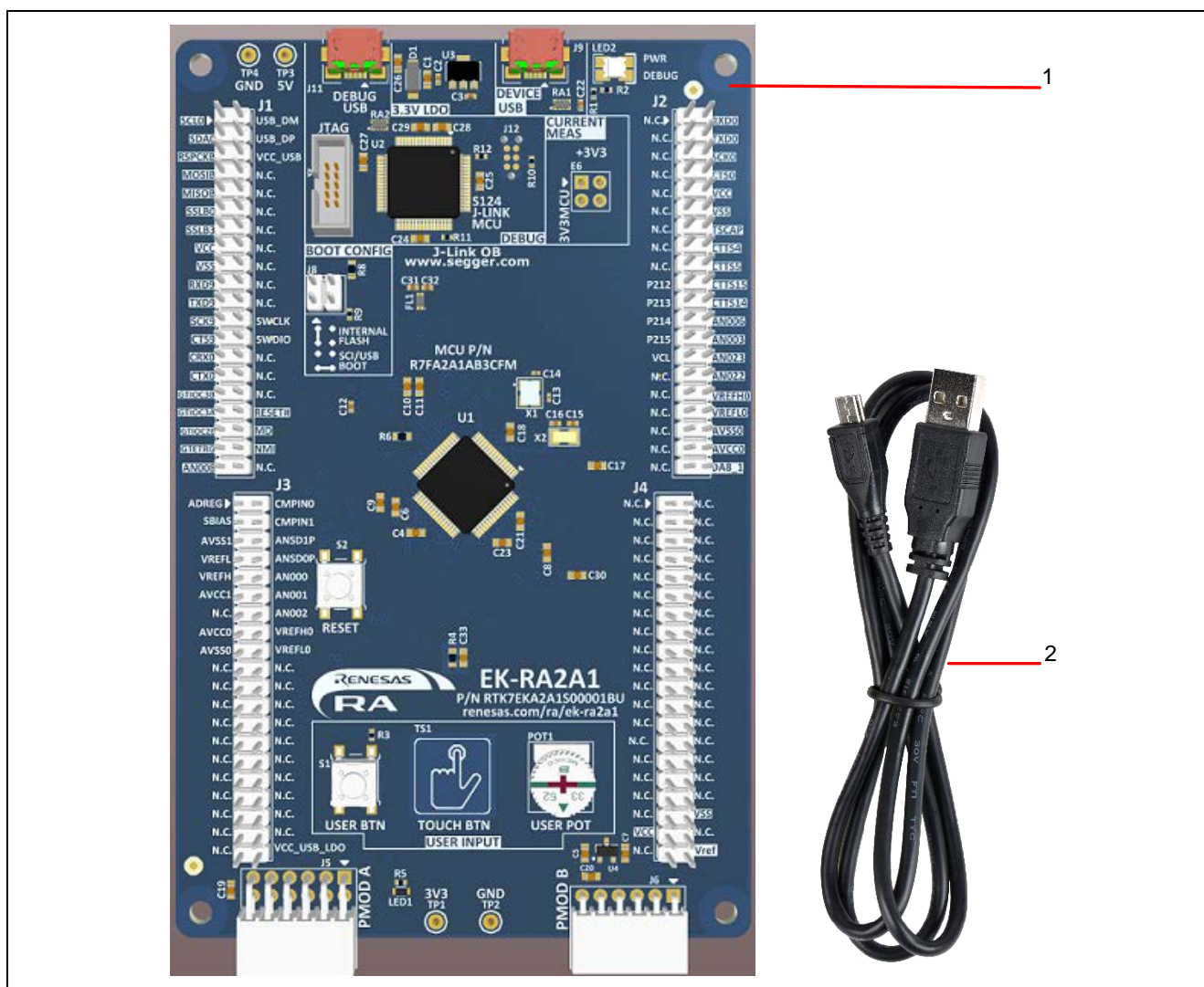Copper jumpers are of two types, designated **trace-cut** and **solder-bridge**.

A **trace-cut jumper** is provided with a narrow copper trace connecting its pads. The silk screen overlay printing around a trace-cut jumper is a solid box. To isolate the pads, cut the trace between pads adjacent to each pad, then remove the connecting copper foil either mechanically or with the assistance of heat. Once the etched copper trace is removed, the trace-cut jumper is turned into a solder-bridge jumper for any later changes.

A **solder-bridge jumper** is provided with two isolated pads that may be joined together by one of three methods:

- Solder may be applied to both pads to develop a bulge on each and the bulges joined by touching a soldering iron across the two pads.
- A small wire may be placed across the two pads and soldered in place.
- A SMT resistor, size 0805, 0603, or 0402, may be placed across the two pads and soldered in place. A zero-ohm resistor shorts the pads together.

The silk screen overlay printing around a solder-bridge jumper is a box with a gap in the lines adjacent to the isolation region between the pads.

For any copper jumper, the connection is considered **closed** if there is an electrical connection between the pads (default for trace-cut jumpers.) The connection is considered **open** if there is no electrical connection between the pads (default for the solder-bridge jumpers.)
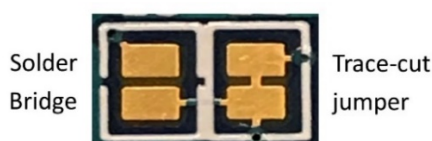

Figure 4.   Copper Jumpers

4.1.2   Default Board Configuration

The following table describes the default settings for each jumper on the EK-RA2A1. This includes traditional pin jumpers (J*x* designation) and copper jumpers (E*x* designation.)

The Circuit Group for each jumper is the designation found in the board schematic. See section 7, Design and Manufacturing Information. Functional details for many of the listed jumpers may be found in section 5.4, Connectivity and Settings, and section 5.6, Additional Features.

Table 1.   Default Jumper Settings

Location	Circuit Group	Default Open/Closed	Function
J8	MCU Mode Config	Shunt on pins 1-2	Sets the MCU Mode to boot from Internal Flash
E18	12M Crystal	Open	Connects P213/XTAL on MCU to J2-21
E19		Open	Connects P212/EXTAL on MCU to J2-19
E23		Closed	Connects 12.000 MHz Crystal to MCU
E24		Closed	Connects 12.000 MHz Crystal to MCU
E1	3.3V Linear Regulator	Closed	Alternate 3.3V source (+3V3JLOB)
E22	32K Crystal	Open	Connects P215/XCIN on MCU to J2-25
E25		Closed	Connects 32.768 kHz Crystal to MCU
E26		Closed	Connects 32.768 kHz Crystal to MCU
E27		Open	Connects P214/XCOUT on MCU to J2-23
E10	AVCC0-> +3V3MCU	Closed	Connects +3V3MCU to AVCC0
E11	AVSS0->GND	Closed	Connects Ground to AVSS1

Location	Circuit Group	Default Open/Closed	Function
E2	Capacitive Touch Button	Closed	Enable/Disable Capacitive Touch Button (connects P001 on MCU to Capacitive Touch Button)
E5		Open	Connects P001 on MCU to J2-20
E28	EXT VCL and VCL CAP	Open	Connects VCL to MCU
E29		Closed	Connects MCU pin 15 (VCL) to capacitor
E32	J-Link	Closed	Connects the S124 MCU to the J-Link signal JLED
E33		Closed	Connects the S124 MCU to the J-Link signal RESET#
E37		Closed	Connects the S124 MCU to the J-Link signal P100/SWDIO
E38		Closed	Connects the S124 MCU to the J-Link signal P300/SWCLK
E35	J-Link OB USB	Closed	Connects the J-Link OB USB 5V input to the primary 5V->3.3V voltage regulator
E31	JTAG Connector	Open	JTAG Ground Detect. Connects the JTAG connector pin 9 to Ground.
E13	LDO and VCC USB	Open	Connects VCC_USB_LDO to MCU pin 41
E14		Open	Connects VCC_USB_LDO to MCU pin 40
E7		Closed	Connects +3V3MCU to MCU pin 41
E8		Closed	Connects +3V3MCU to MCU pin 40
E12	P409/CAN or TSCAP-E	Open	Connects P409/CAN on MCU to J1-29
E30	USB Device Interface	Closed	Connects the Device USB 5V input to the MCU
E16	USB FS	Closed	Connects P915/USB_DM on MCU to signal USB_N
E17		Closed	Connects P914/USB_DP on MCU to signal USB_P
E20		Open	Connects P914/USB_DP on MCU to signal USBPH_P
E21		Open	Connects P915/USB_DM on MCU to signal USBPH_N
E3	User LED	Closed	Enable/Disable User LED
E36	User Potentiometer	Open	Enable/Disable User Potentiometer
E4	User Push-Button	Closed	Enable/Disable User Push-Button switch
E6	+3V3_MCU	Closed	Dual Jumper. Pins 1 and 3 connect +3V3 to +3V3MCU. Pins 2 and 4 are not used.
E41	CRX0_B (P408) -> J1	Closed	Connects P408 on MCU to J1-27
E42	CMPIN1 (P408) -> J3	Closed	Connects P408 on MCU to J3-4
E43	SSLB0_C (P102) -> J1	Closed	Connects P102 on MCU to J1-11
E44	ANSD1P (P102) -> J3	Closed	Connects P102 on MCU to J3-6
E45	AVCC1 -> +3V3MCU	Closed	Connects +3V3MCU to AVCC1
E46	AVSS1 -> GND	Closed	Connects AVSS1 to Ground

5.   Hardware Layout

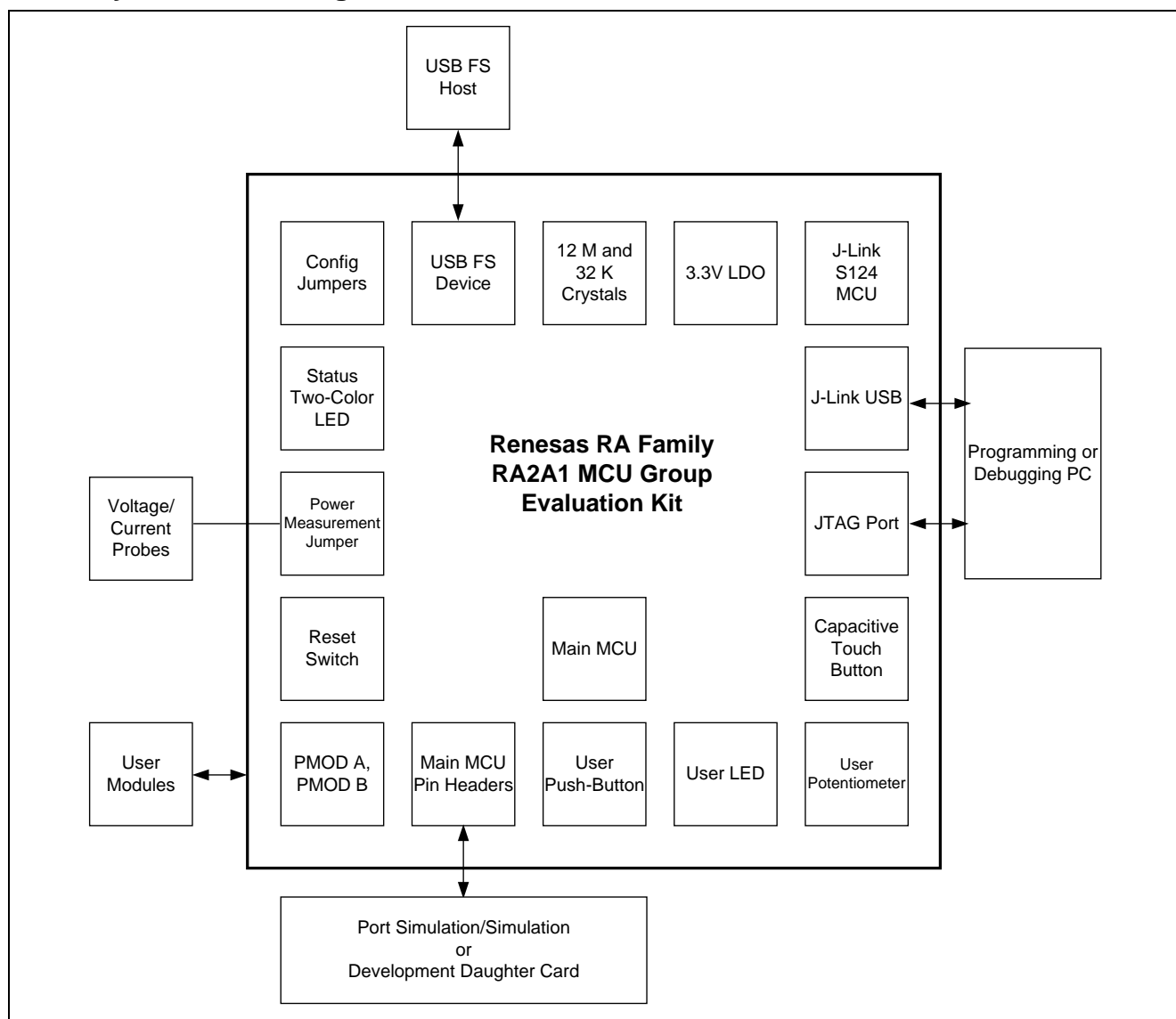## 5.1   System Block Diagram

Figure 5.   EK-RA2A1 Block Diagram

5.2   Power Requirements

The EK-RA2A1 is designed for 3.3V operation. This also means that 5V PMOD devices cannot be used together with the EK-RA2A1 unless they are powered separately.

The total current available from the LDO regulator for all connected circuits is 600 mA or less, depending on the 5V power source used.

5.2.1   Power Supply Options

EK-RA2A1 board can be powered in several different ways as described in this section.
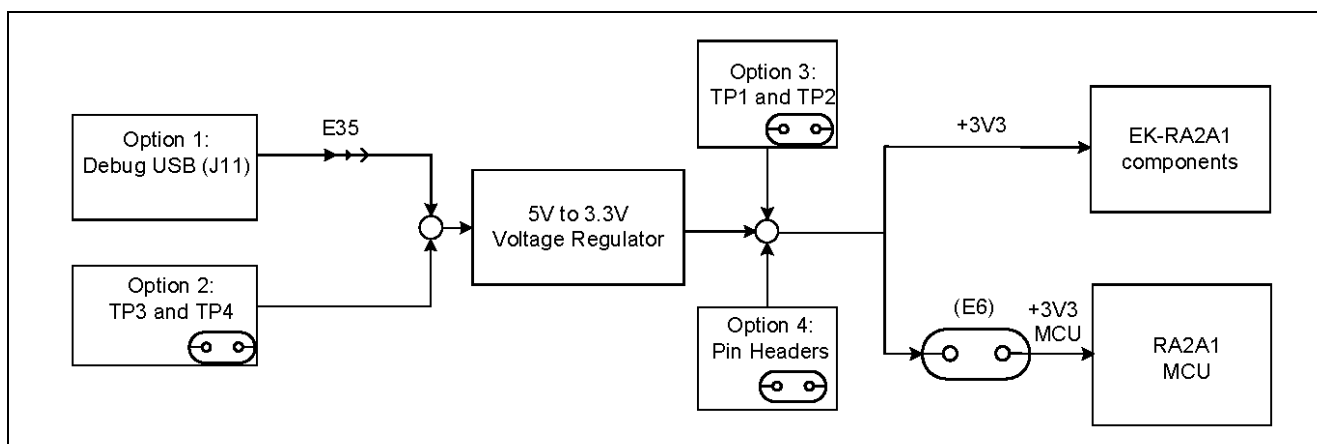

Figure 6.   Power Supply Options

5.2.1.1   Option 1: Debug USB (default)

The default power source is 5V, supplied from an external USB host to the USB Debug connector labelled **DEBUG USB** on the top surface of the board. A low drop-out regulator (LDO) is used to convert the 5V signal to 3.3V, which then is used to power the MCU and any connected devices.

Copper jumper E35 selects the source for the primary power input to the LDO regulator. By default, this jumper is configured to provide power through the Debug USB connector. Copper jumper E35 is closed for this configuration.

5.2.1.2   Option 2: Test Points TP3 and TP4

EK-RA2A1 board can also be powered by installing a 5V power source across TP3 (positive input) and TP4 (negative input). Copper jumper E35 must be opened to enable powering the board using these test points.

> ⚠ **The on-board Low Dropout Regulator (see section 5.3 Major Components) has an input voltage range of +3.3V to +5.5V, and a built-in current limit of 600 mA. Make sure any external power source connected to TP3 and TP4 meets these requirements.**

Figure 7.   USB Debug Connector (J11), TP3, and TP4 on the Evaluation Kit Board

5.2.1.3   Option 3: Test Points TP1 and TP2

EK-RA2A1 board can also be powered by installing a 3.3V source across TP1 (positive input) and TP2 (negative input). Copper jumper E35 must be open to enable powering the board using these test points.
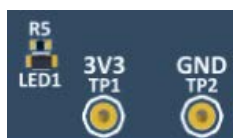
Figure 8.   TP1, TP2, and LED1 on the Evaluation Kit Board

> ⚠ **These test points supply voltage directly to the RA2A1 MCU, the S124 J-Link MCU, and other on-board circuitry. Use caution to ensure that any voltage connected in this manner meets the power requirements for the active features. Power sources that are outside of the published operating range for the active devices may cause degraded performance or damage the board.**

5.2.1.4 Option 4: Pin Headers

EK-RA2A1 board can also be powered through the following pin-headers.

- J1 (pin J1-15 for +3.3V, pin J1-17 for Return)
- J2 (pin J2-10 for +3.3V, pin J2-12 for Return)
- J4 (pin J4-37 for +3.3V, pin J4-36 for Return)

Copper jumper E35 must be open for any of these configurations.

⚠️ **The pin headers supply voltage directly to the RA2A1 MCU, the S124 J-Link MCU, and the other on-board circuitry. Use caution to ensure that any voltage connected in this manner meets the power requirements for the active features. Power sources that are outside of the published operating range for the active devices may cause degraded performance or damage the board.**

See section 5.5, Pin Headers for more information on the Pin Headers.
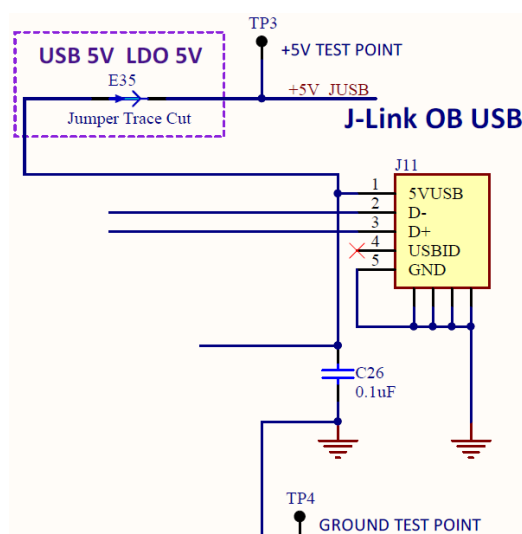
Figure 9.   5V Power Input Circuit

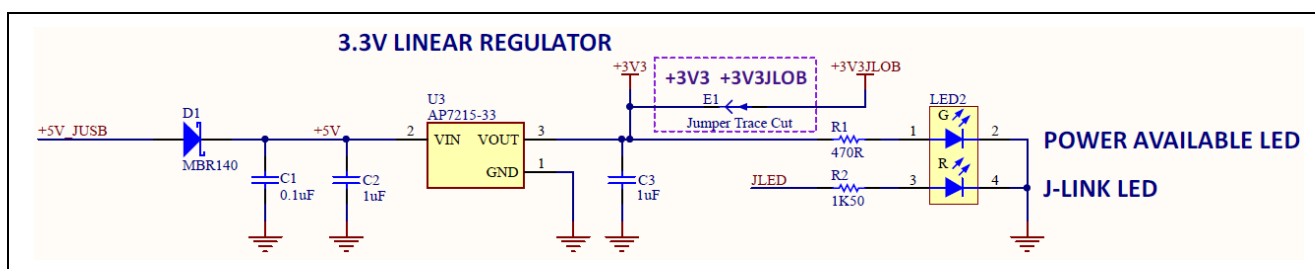**Figure 10.   3.3V Power Regulator Circuit**

5.2.2 Power-Up the Board

When powered, the green LED to the right of the DEVICE USB connector (LED2) lights up.

The red LED in the same LED package functions as a status indicator for the J-Link On-Board debug interface on the board. If both LEDs in the LED2 package are lit, LED2 appears orange.

Figure 11.   LED2 on the Evaluation Kit Board (Top Side)

5.2.3 Measuring Current Consumption

Pads 1 and 3 of copper jumper E6, which is a trace-cut jumper, allow measurement of +3V3 MCU supply current. Trace is connected by default and should be cut to enable power measurement. Care must be taken when cutting the trace to not cause damage to PCB layers below the trace.

The actual current consumed by the RA2A1 MCU is dependent on many factors, including ambient temperature, internal clock speed, input voltage level, and device activity. The actual current consumed by the MCU can vary from less than 1 mA to nearly 40 mA. Refer to the *RA2A1 Microcontroller Group User's Manual* for more information on the electrical characteristics of the MCU.
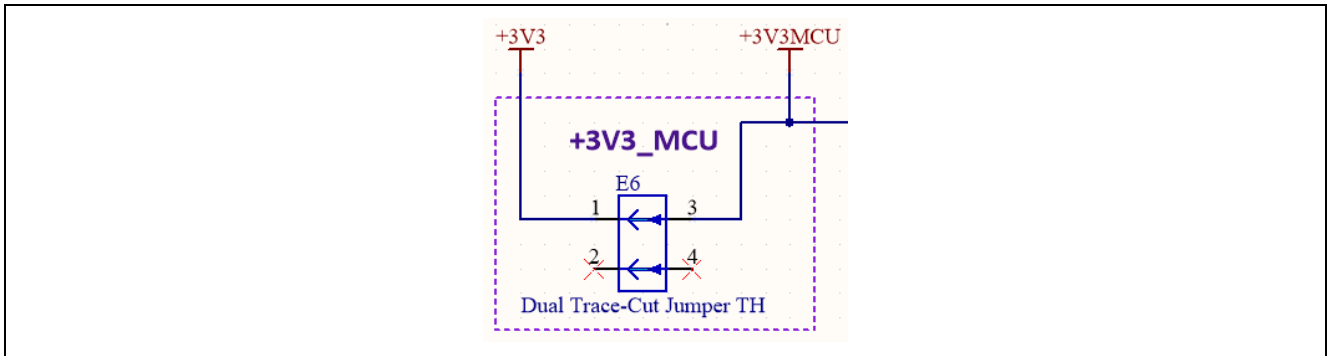

Figure 12. MCU Current Measurement Circuit
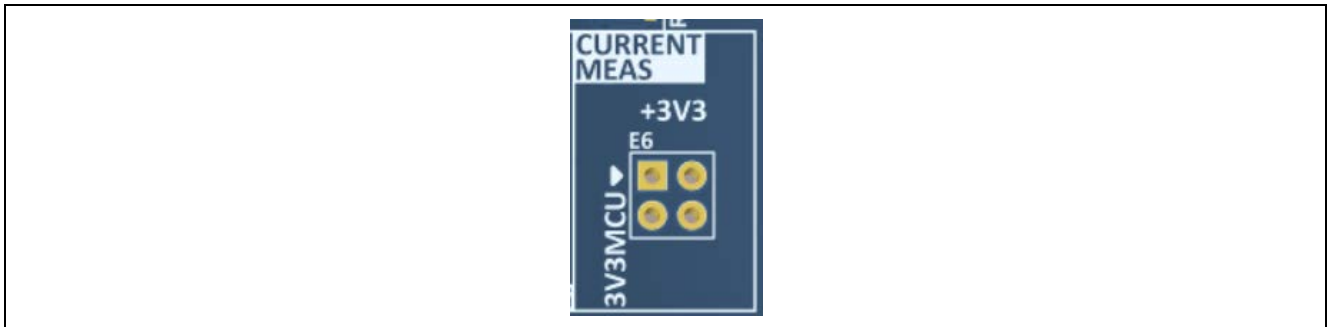
Figure 13.   E6 on Evaluation Kit Board (Top Side)
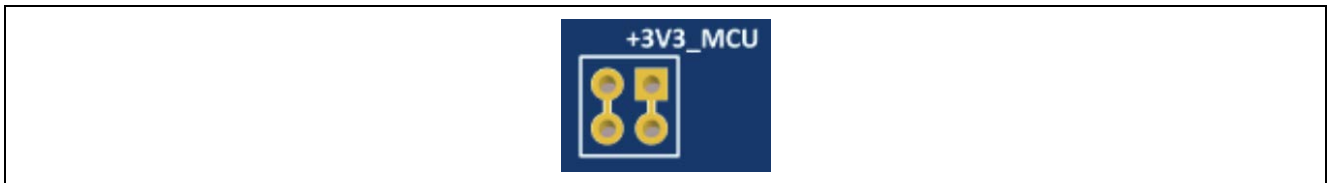
Figure 14.   E6 on Evaluation Kit Board (Bottom Side)

Once the shorting traces have been removed, there are several options to measure current:
- Pins can be installed that allow connection of a precision multi-meter or bench meter, or leaded current shunt to allow oscilloscope or data logger connection. When not measuring current, this allows easily installed and removed shunts to be used to short the jumper terminals.
- Another option is to install current sense resistors between pads 1 and 3 for +3V3MCU. Precision non-inductive film or foil resistors are recommended for use in this application, and the value of each resistor should be carefully considered.

  For example, if the expected current requirement for the +3V3 MCU supply voltage is 10 mA, and the user would expect to measure a 10 mV drop across the current measurement resistor, then a 1.0-ohm resistor should be selected and installed. The actual value selected should be based on the operating conditions of the MCU for the specific user application and the sensitivity of the measurement equipment used.

5.3   Major Components

- Main MCU
    - RA2A1 MCU, part number R7FA2A1AB3CFM (U1)
        - Main MCU
- J-Link MCU
    - S124 MCU, part number R7FS124773A01CFM#AA0 (U2)
        - J-Link MCU
- USB Connectors
    - FCI, part number 10118192-0001LF (J9, J11)
        - Micro USB 2.0 Female connector
        - Primary communication with Main MCU and J-Link MCU
- Push-Buttons
    - C&K, part number PTS645SM43SMTR92 LFS (S1, S2)
        - Momentary push-button switch
        - Used for system reset and user defined functions
- LDO Regulator
    - Diodes Inc., part number AP7215-33YG-13 (U3)
        - Low-drop out linear regulator
        - Generates system 3.3V from J-Link USB 5V input
- PMOD A Connector
    - Samtec, part number SSW-106-02-F-D-RA (J5)
        - 12-pin right angle connector for PMOD A
- PMOD B Connector
    - Samtec, part number SSW-106-02-FM-S-RA (J6)
        - 6-pin right angle connector for PMOD B
- Pin Headers
    - Sullins, part number PRPC020DAAN-RC (J1, J2, J3, J4)
        - 40 position pin header, 0.1" pitch
        - Provides signal breakout and access for Main MCU signals
- System LED
    - Dialight, part number 598-8610-207F (LED2)
        - Dual color red/green LED
        - System status indicator for power and J-Link status
- User LED
    - Lite-On, part number LTST-C191KRKT (LED1)
        - User defined
        - Single color red LED as needed for user environment
- User Potentiometer
    - Bourns, part number 3352T-1-1-3LF (POT1)
        - User defined
        - Provides variable resistance as needed for user environment
        - Not populated by default

5.4   Connectivity and Settings

Throughout this section, feature configuration using copper jumpers is described. See section 4.1.1, Copper Jumpers for information on using copper jumpers.

5.4.1   Device USB

The DEVICE USB Micro-B connection jack connects the Main MCU to an external USB Host, FS capable, allowing communications for testing and use of the Main MCU firmware. Power for the board cannot be received from this connector. The DEVICE USB interface can detect the presence of power from the USB Host PC. USB Host power received at the DEVICE USB interface is not connected to the 5V power bus.

Table 2.   DEVICE USB connector (J9)

USB device connector		EK-RA2A1
Pin	Description	Signal/Bus
1	+5VDC, connected to a sense voltage 2/3 divider to allow Main MCU sensing of Host presence	+5VUSB P407/USB_VBUS = 2/3(5VUSB)
2	Data-	P915/USB_DM
3	Data+	P914/USB_DP
4	USB ID, jack internal switch, cable inserted	N.C.
5	Ground	GND

Connections in Table 2 are based on the condition of copper jumpers E16, E17, E20, E21, and E30 matching their as-manufactured status. As-manufactured, E16 and E17 are closed, E20 and E21 are open, and E30 is closed.

Alternatively, the Device USB signals to the Main MCU may be connected to MCU Pin Header J1. To enable this configuration, copper jumpers E16 and E17 should be open, and E20 and E21 should be closed.

5.4.2   Debug USB

The DEBUG USB Micro-B connection jack connects the S124 J-Link MCU to an external USB Host, FS capable, allowing re-programming and debugging of the Main MCU firmware. Power for the board may be received from this connector.

The J-Link OB interface is multiplexed with the JTAG interface, and can collectively be referred to as the Programming Interface. While the J-Link OB interface and the JTAG interface do not conflict, the J-Link OB signals may be isolated from the programming interface by changing the associated copper jumpers.

J-Link Disconnect Copper Jumpers E32, E33, E37, and E38 connect the J-Link signals to the MCU programming interface. To isolate the J-Link signals from the JTAG interface, the copper jumpers must be open. To allow use of the J-Link interface, each copper jumper must be closed.

J-Link MCU Power Copper Jumper, E1, connects the main +3.3V power to the J-Link +3.3V power. The default condition for E1 is closed, which connects the J-Link MCU power to the main +3.3V power. If J-Link signals are disconnected, the power to the J-Link MCU should also be removed by changing E1 to open.

Table 3.   DEBUG USB Connector (J11)

DEBUG USB Connector		EK-RA2A1
Pin	Description	Signal/Bus
1	+5VDC	+5V_JUSB
2	Data-	U2 USB_DM (U2-18)
3	Data+	U2 USB_DP (U2-19)
4	USB ID, jack internal switch, cable inserted	N.C.
5	Ground	GND

5.4.3   SWD (JTAG)

A 10-pin Cortex Debug Connector is provided at J10.

Note: The RA2A1 MCU does not have JTAG support, only SWD.

Table 4. **SWD Connector (J10)**

JTAG Connector		EK-RA2A1
Pin	**SWD pin name**	**Signal/Bus**
1	VTref	+3V3
2	SWDIO	U1 P108/SWDIO (U1-33)
3	GND	GND
4	SWCLK	U1 P300/SWCLK (U1-32)
5	GND	GND
6	N.C.	N.C.
7	N.C.	N.C.
8	N.C.	N.C.
9	GNDDetect	N.C. (short E31 to connect to GND)
10	nSRST	U1 RESET# (U1-25)

The Cortex® Debug Connector is fully described in the *Arm® CoreSight™ Architecture Specification*.

The J-Link MCU Power copper jumper and J-Link Disconnects copper jumpers may be open for proper operation of the SWD interface to prevent interactions with the J-Link MCU. See section 5.4.1, Device USB for details.

If a SWD (JTAG) adapter is in use that properly interprets the Arm® Cortex® 10-pin Debug connector assignment of pin 9 to GND, SWD GNDDetect copper jumper E31 should be closed. If the SWD adapter used is one of several that may be confused or damaged by the presence of GND at pin 9, E31 should be open (as shipped).

The J-Link OB interface is multiplexed with the SWD interface, and can collectively be referred to as the Programming Interface. While the J-Link OB interface and the SWD interface do not conflict, the J-Link OB signals may be isolated from the programming interface by changing the copper jumpers as described in section 5.4.2, Debug USB.

5.4.4 LEDs

Two LEDs are provided on the EK-RA2A1 board. U1 is the Main MCU, and directly controls LED1. See Figure 8 for LED1 location and Figure 15 for the LED1 circuit. U2 is the J-Link MCU, and controls the red LED in LED2. See Figure 11 for LED2 location and Figure 10 for LED2 circuit.
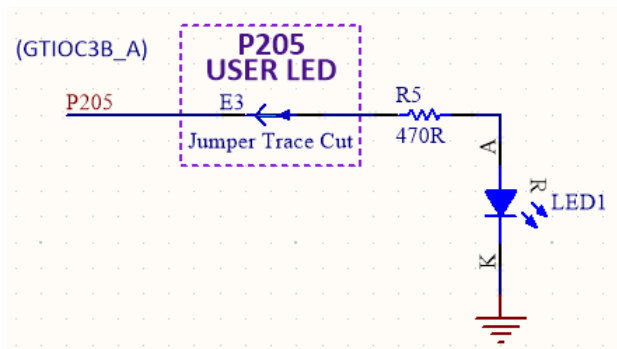
Figure 15. LED1 Control Circuit

The behavior of the LEDs is described in the following table.

Table 5. **LED Functions**

Designator	Color	Function	MCU control port	MCU pin
LED1	Red	User LED	U1 P205	U1-23
LED2	Red	J-Link Indicator	JLED (U2 P103)	U2-45
LED2	Green	3.3V Power Available	+3V3	N.A.

To disconnect the User LED from the MCU signal P205, copper jumper E3 must be open.

5.4.5   Switches

Two miniatures, momentary, mechanical push-button type SMT switches are mounted on the PCB. Pressing the RESET Switch generates a reset signal to restart the Main MCU. To disconnect the User Switch from the MCU signal P206/IRQ6_A, copper jumper E4 must be open.

Note: The correct port number for User SW (E4) is P206 as shown in the following schematic diagram. The board photograph (v1.2) showing P105 for the User SW (E4) (snippet shown to the right) is incorrect and should be P206 instead.

Table 6.   Switches on the Evaluation Kit Board

Designator	Function	MCU Control Port	MCU Pin
S1	User Switch	U1 P206/IRQ6_A	U1-22
S2	MCU Reset Switch	RESET#	U1-25
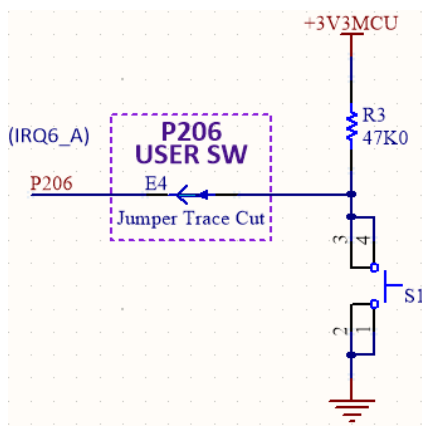
Figure 16.   User Switch Circuit

Figure 17.   User Switch (S1)
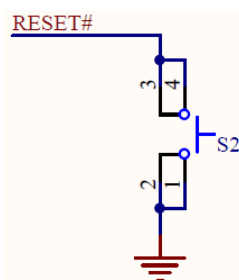
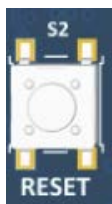**Figure 18.   Reset Switch Circuit**

Figure 19.   Reset Switch (S2) on Board

5.4.6   PMOD A

A 12-pin PMOD type 2A connector is provided at PMOD A. The interface is powered for 3.3V modules only. The Main MCU acts as the SPI master, and the connected module acts as an SPI slave device. This interface may additionally be re-configured in firmware as several other PMOD types.

Signals on PMOD A are shared with the Main MCU pin header J2. Care must be taken to ensure that shared signals are not used concurrently.

Table 7.   PMOD A Connector (J5)

PMOD A Connector		EK-RA2A1
Pin	Description	Signal/Bus
1	SS (low to select slave)	U1 P112, SSLA0_B (U1-36)
2	MOSI	U1 P303, MOSIA_B (U1-29)
3	MISO	U1 P304, MISOA_B (U1-28)
4	SCK	U1 P111, RSPCKA_B (U1-35)
5	GND	GND
6	VCC	+3V3
7	INT (slave to master)	U1 P301, IRQ5_A (U1-31)
8	RESET (master to slave)	U1 P015, GPIO (U1-52)
9	Not Specified	U1 P107, GPIO (U1-41)
10	Not Specified	U1 P106, GPIO (U1-42)
11	GND	GND
12	VCC	+3V3

Limits of the 3.3V regulator on the PCB, and limits of the power source supplying that regulator (especially for USB Host devices), including the to-be-connected PMOD device, must be considered prior to connecting a module to a PMOD connector.

5.4.7   PMOD B

A 6-pin PMOD type 4 connector is provided at PMOD B. The interface is powered for 3.3V modules only. The Main MCU acts as the UART DCE, and the connected module acts as the UART DTE. This interface may additionally be re-configured in firmware as some other PMOD types.

Signals on PMOD B are shared with Main MCU pin header J1 and J2. Care must be taken to ensure that shared signals are not used concurrently.
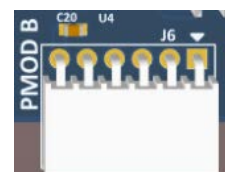
Table 8.   PMOD B Connector (J6)

PMOD B Connector		EK-RA2A1
Pin	Description	Signal/Bus
1	CTS (from module)	U1 P410, CTS0_A (U1-13)
2	TXD	U1 P411, TXD0_F (U1-12)
3	RXD	U1 P204, RXD0_C (U1-24)
4	RTS (from Main MCU)	U1 P401, GPIO (U1-2) (for RTS by Main MCU firmware)
5	GND	GND
6	VCC	+3V3

Limits of the 3.3V regulator , and limits of the power source supplying that regulator (especially for USB Host devices), including the to-be-connected PMOD device, must be considered prior to connecting a module to a PMOD connector.

5.4.8 User Capacitive Touch Button

A capacitive sensor region for use as a Capacitive Touch button is provided in the board USER INPUT region. To disconnect the Capacitive Touch Button from the MCU, copper jumper E2 must be open. To connect MCU signal P001 to pin header J3, copper jumper E5 must be closed.

Note: Capacitor C33 is optional. This design does not include a dielectric overlay, so C33 is added to reduce the sensitivity of the Capacitive Touch Button. This capacitor is not required by the MCU specification.

Table 9.   Capacitive Touch Button Sensor

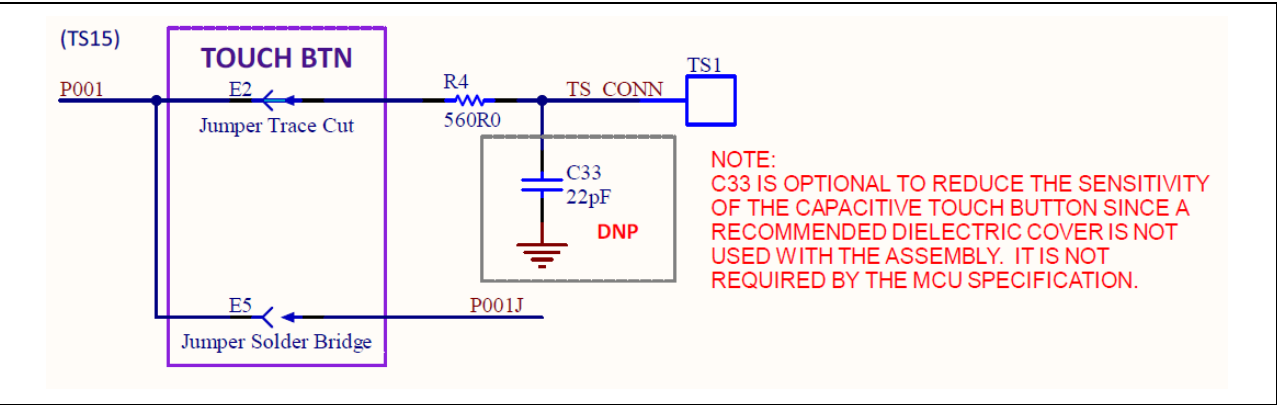| Designator	Function	MCU Control Port	MCU Pin
TS1	Capacitive Touch Button	U1 P001 (TS15)	U1-62
-	TSCAP Support	U1 P409 (TSCAP-E)	U1-14

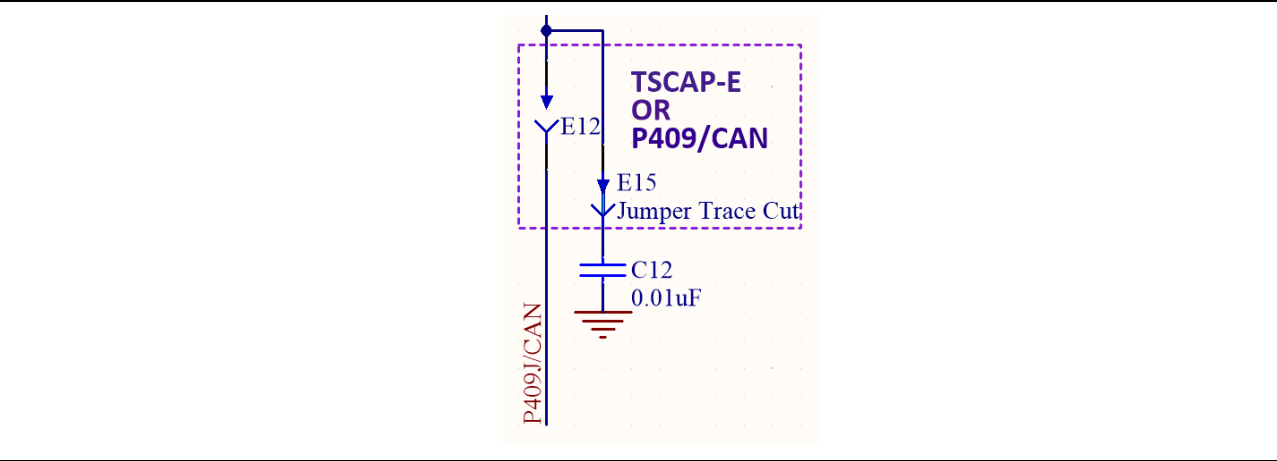**Figure 20.   Capacitive Touch Button Circuit**

Figure 21.   Capacitive Touch TSCAP Circuit

Figure 22.   Capacitive Touch Button on Evaluation Kit Board (Top)

5.5   Pin Headers

Pin headers, J1, J2, J3, and J4, provide access to all Main MCU interface signals, and to voltages for all Main MCU power ports.

On EK-RA2A1, 40 pins of the pin headers are set aside for **fixed function** assignment. These pins are odd-numbered pins of J1 and even-numbered pins of J2.

Pin Header Fixed Function Pins are labeled with dark text on a white background. Pins that are not Fixed Function pins are labeled with white text on a dark background. On the top side of the board is the functional label for the fixed location. On the bottom side of the board is the port information for the same pin.

Figure 23.   Fixed Function Pin Label Example

Primary Fixed Function Pins share the same functionality across EK-RA6M1, EK-RA6M2, EK-RA4M1, and EK-RA2A1 boards.

Secondary Fixed Function Pins share common pin assignments with other Renesas RA Family Evaluation Kits that have Main MCUs with the same functionality. The Secondary Fixed Function Pins are also labeled with the top side having a functional label, and bottom side having a port label.
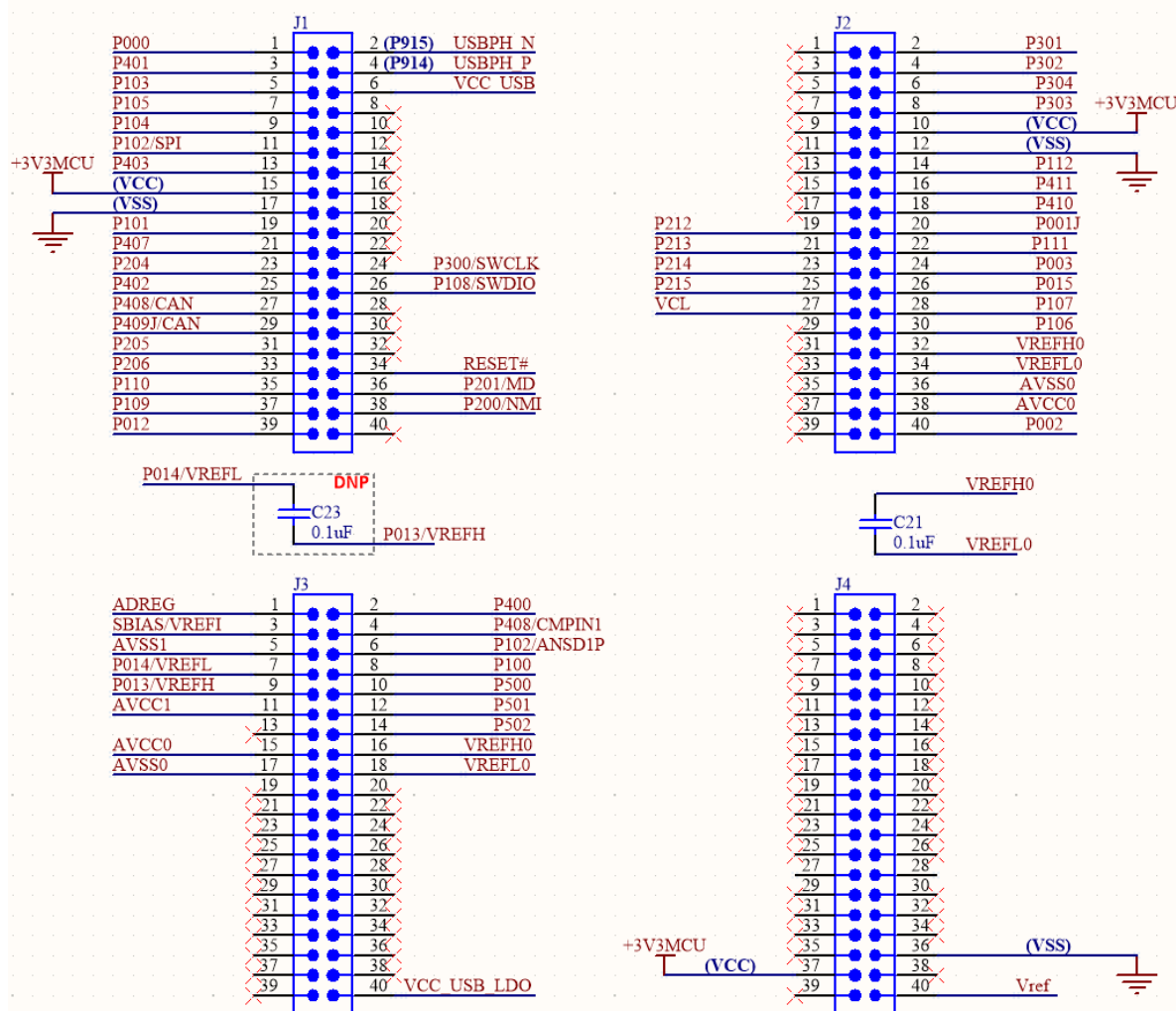
Figure 24.   EK-RA2A1 Pin Headers Circuit

5.5.1   Pin Header J1

Pin Header J1 is a 2-column by 20-row through-hole header on 2.54 mm centers.

Table 10.   Pin Header J1 Pin Assignment

64p Pin	Port/Signal	J1 Pins		Port/Signal	64p Pin
63	P000/SCL0_C (IIC)	1	2	P915/USB_DM	38
2	P401/SDA0_C (IIC)	3	4	P914/USB_DP	39
45	P103/RSPCKB_C (SPI)	5	6	VCC_USB	40
43	P105/MOSIB_C (SPI)	7	8	(None)	NC
44	P104/MISOB_C (SPI)	9	10	(None)	NC
46	P102/SSLB0_C (SPI)	11	12	(None)	NC
4	P403/SSLB3_A (SPI)	13	14	(None)	NC
11	VCC	15	16	(None)	NC
8	VSS	17	18	(None)	NC
47	P101/RXD9_C (SCI 2nd)	19	20	(None)	NC
16	P407/TXD9_A (SCI 2nd)	21	22	(None)	NC
24	P204/SCK9_B (SCI 2nd)	23	24	P300/SWCLK	32
3	P402/CTS_RTS (SCI 2nd)	25	26	P108/SWDIO	33
15	P408/CRX0_B (CAN)	27	28	(None)	NC
14	P409/CTX0_B (CAN)	29	30	(None)	NC
23	P205/GTIOC3B_A	31	32	(None)	NC
22	P206/GTIOC3A_A	33	34	RES	25
34	P110/RXD9	35	36	P201/MD	26
64	P109/TXD9	37	38	P200/NMI	27
55	P012/AN008	39	40	(None)	NC

Color Key

Primary Fixed Function Pins
Secondary Fixed Function Pins

5.5.2   Pin Header J2

Pin Header J2 is a 2-column by 20-row through-hole header on 2.54 mm centers.

Table 11.   Pin Header J2 Pin Assignment

64p Pin	Port/Signal	J2 Pins		Port/Signal	64p Pin
NC	(None)	1	2	P301/RXD0_B (SCI 1st)	31
NC	(None)	3	4	P302/TXD0_B (SCI 1st)	30
NC	(None)	5	6	P304/SCK0_B (SCI 1st)	28
NC	(None)	7	8	P303/CTS_RTS (SCI 1st)	29
NC	(None)	9	10	VCC	11
NC	(None)	11	12	VSS	8
NC	(None)	13	14	P112/TSCAP_B/CLKOUT_B	36
NC	(None)	15	16	P411/TS04	12
NC	(None)	17	18	P410/TS05	13
20	P212/EXTAL	19	20	P001/TS15	62

64p Pin	Port/Signal	J2 Pins		Port/Signal	64p Pin
19	P213/XTAL	21	22	P111/TS14	35
17	P214/XCOUT	23	24	P003/AN006	60
16	P215/XCIN	25	26	P015/AN003	52
15	VCL	27	28	P107/AN023	41
14	VBAT	29	30	P106/AN022	42
NC	(None)	31	32	VREFH0	59
NC	(None)	33	34	VREFL0	58
NC	(None)	35	36	AVSS0	57
NC	(None)	37	38	AVCC0	56
NC	(None)	39	40	P002/DA8_1	61

Color Key

Primary Fixed Function pins
Secondary Fixed Function pins

5.5.3 Pin Header J3

Pin header J3 is a 2-column by 20-row through-hole header on 2.54 mm centers.

Table 12.   Pin Header J3 Pin Assignment

64p Pin	Port/Signal	J3 Pins		Port/Signal	64p Pin
37	ADREG	1	2	P400/CMPIN0	1
38	SBIAS/AVREF	3	4	P408/CMPIN1	15
40	AVSS1	5	6	P102/ANSD1P	46
53	P014/VREFL	7	8	P100/ANSD0P	48
54	P013/VREFH	9	10	P500/AN000	49
39	AVSS1	11	12	P501/AN001	50
NC	(None)	13	14	P502/AN002	51
56	AVCC0	15	16	VREFH0	59
57	AVSS0	17	18	VFERL0	58
NC	(None)	19	20	(None)	NC
NC	(None)	21	22	(None)	NC
NC	(None)	23	24	(None)	NC
NC	(None)	25	26	(None)	NC
NC	(None)	27	28	(None)	NC
NC	(None)	29	30	(None)	NC
NC	(None)	31	32	(None)	NC
NC	(None)	33	34	(None)	NC
NC	(None)	35	36	(None)	NC
NC	(None)	37	38	(None)	NC
NC	(None)	39	40	VCC_USB_LDO	41

Color Key

Analog Front End Pins
Secondary Fixed Function Pins

5.5.4 Pin Header J4

Pin Header J4 is a 2-column by 20-row through-hole header on 2.54 mm centers.

Table 13.   Pin Header J4 Pin Assignment

64p Pin	Port/Signal	J4 Pins		Port/Signal	64p Pin
NC	(None)	1	2	(None)	NC
NC	(None)	3	4	(None)	NC
NC	(None)	5	6	(None)	NC
NC	(None)	7	8	(None)	NC
NC	(None)	9	10	(None)	NC
NC	(None)	11	12	(None)	NC
NC	(None)	13	14	(None)	NC
NC	(None)	15	16	(None)	NC
NC	(None)	17	18	(None)	NC
NC	(None)	19	20	(None)	NC
NC	(None)	21	22	(None)	NC
NC	(None)	23	24	(None)	NC
NC	(None)	25	26	(None)	NC
NC	(None)	27	28	(None)	NC
NC	(None)	29	30	(None)	NC
NC	(None)	31	(None)	(None)	NC
NC	(None)	33	(None)	(None)	NC
NC	(None)	35	36	VSS	8
11	VCC	37	(None)	(None)	NC
NC	(None)	39	40	Vref 2.048V	Vref

Color Key

Secondary Fixed Function pins
Analog Voltage Reference 2.048V

5.6   Additional Features

5.6.1   Analog Reference Voltages

Footprints for the installation of capacitors C21 and C23 are provided on the board. These two capacitors provide noise-bypass capability for ports VREFH0/VREFL0 and for ports P013(VREFH)/P014(VREFL) correspondingly. See Figure 24 for the circuit design.

Port pair P013/P014 may be assigned as GPIO, where bypass capacitor C21 would damage signal quality. When P013/P014 are to be assigned as VREFH/VREFL, installation of capacitor C21 can reduce reference voltage noise and improve ADC measurement and DAC output quality.

5.6.2   On-Board Clock Crystals

The EK-RA2A1 board includes two precision crystal clock sources. A precision 12.000 MHz crystal is installed at location X1, and a precision 32.768 kHz crystal is installed at location X2. These crystal clock sources are connected to the Main MCU by default.

The MCU pins for the 12 MHz clock crystal may be connected to P212 and P213. To disconnect the 12 MHz crystal, open copper jumpers E23 and E24, and close copper jumpers E18 and E19.

The MCU pins for the 32.768 kHz clock crystal may be connected to P214 and P215. To disconnect the 32.768 kHz crystal, open copper jumpers E25 and E26, and close copper jumpers E22 and E27.
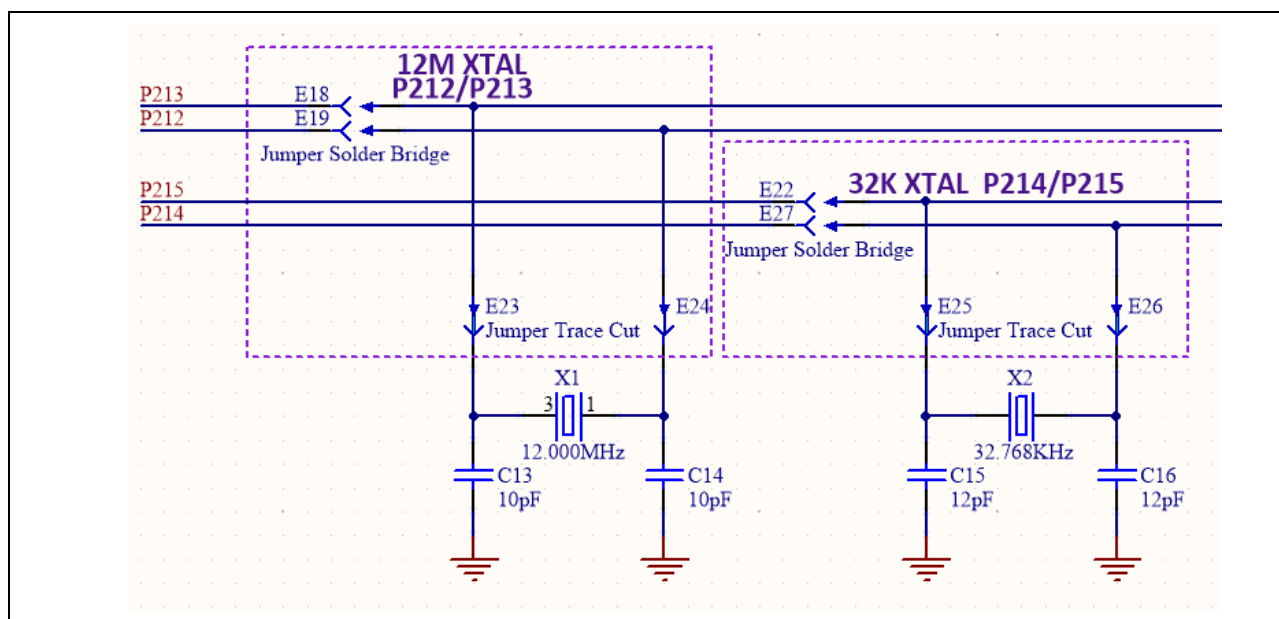

Figure 25.   Crystal Clock Sources

5.6.3   User Potentiometer

A footprint for installation of a potentiometer and a recommended noise-bypass capacitor are provided on the board. The footprint was designed for installation of a Bourns P/N 3352T-1-103LF, or equivalent, as the potentiometer, and a Samsung P/N CL10B104KB8NNNC, or similar, as the noise-bypass capacitor.

When the User Potentiometer is installed, copper jumper E36 must be closed to connect the User Potentiometer to the MCU.

Table 14.   User Potentiometer on the Evaluation Kit Board

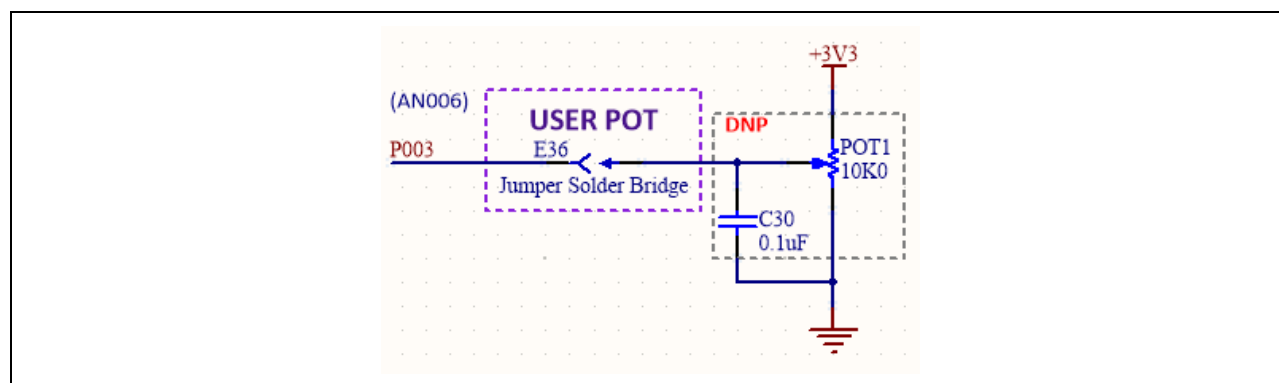| Designator	Function	MCU Control Port	MCU Pin
POT1	User Potentiometer	U1 P003 (AN006)	U1-60

Figure 26   User Potentiometer Circuit

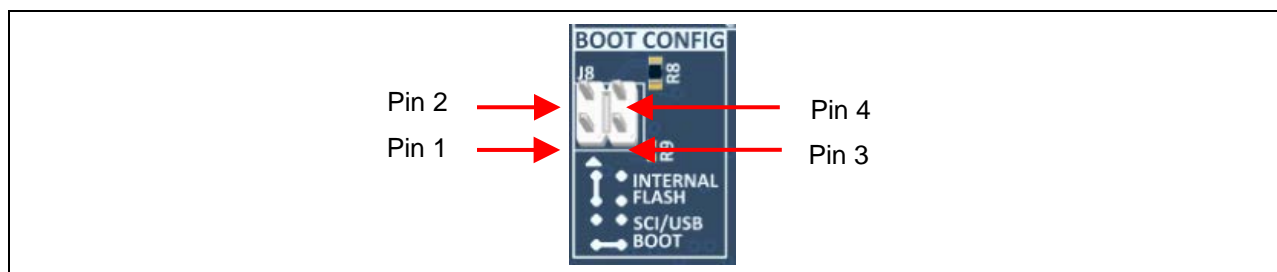**Figure 27． User Potentiometer on Evaluation Kit Board (Top)**

5.6.4 Boot Configuration

The BOOT CONFIG jumper, J8, is used to configure the operating mode of the RA2A1 MCU at boot.

Table 15.   Boot Configuration

| Boot Configuration	J8 Shunt Location
Normal Boot (default)	Pins 1 and 2
SCI/USB Boot	Pins 1 and 3

Figure 28.   Boot Config Jumper J8

5.6.5 Miscellaneous Signals

5.6.5.1 AVCC0/AVSS0 and AVCC1/AVSS1

By default, AVCC0 and AVCC1 are connected to +3V3MCU, and AVSS0 and AVSS1 are connected to the system ground. To disconnect the reference voltage from AVCC0 and AVSS0, copper jumpers E10 and E11 must be open. To disconnect the reference voltage from AVCC1 and AVSS1, copper jumpers E45 and E46 must be open.

Figure 29.   AVCC0/AVSS0 Circuit
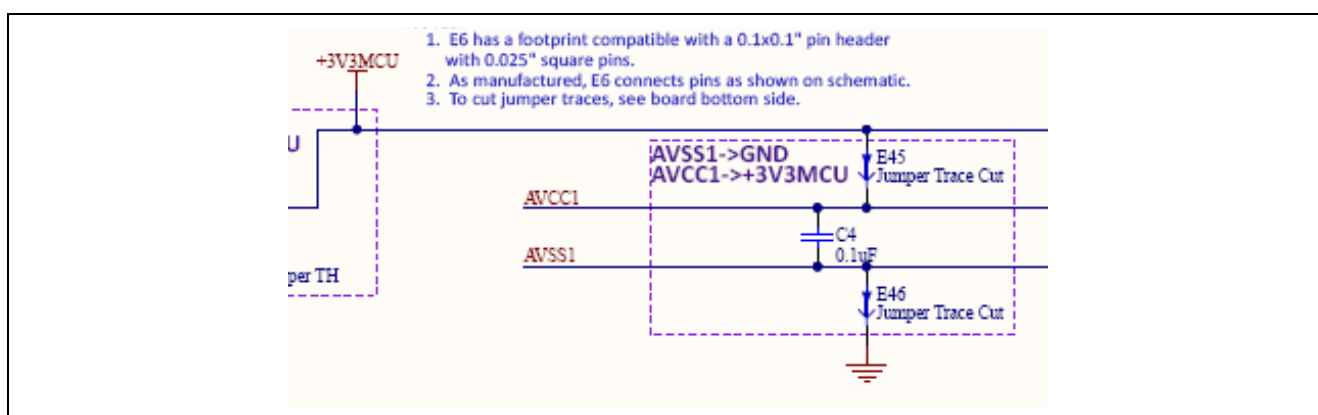
Figure 30.   AVCC1/AVSS1 Circuit

5.6.5.2 VCL

By default, the Main MCU pin VCL is connected to reference capacitor C17. To connect this pin to MCU pin header J2, solder bridge E28 must be closed. To disconnect the reference capacitor C17, copper jumper E29 must be open.
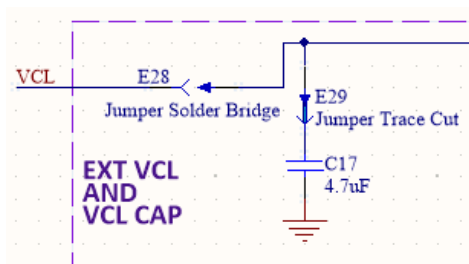

Figure 31.   External Capacitor to VCL Circuit

5.6.5.3 VCC_USB_LDO

By default, the Main MCU pin VCC_USB_LDO is connected to the +3V3 MCU supply voltage. Alternatively, this pin may be connected to MCU Pin Header J3. To do this, copper jumper E7 must be open, and copper jumper E13 must be closed.
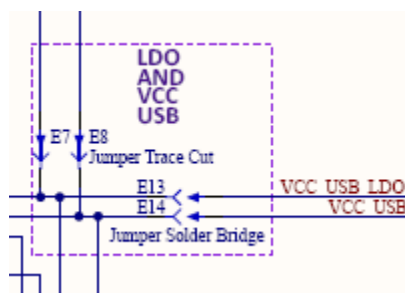

Figure 32.   VCC_USB_LDO Circuit

5.6.5.4 VCC_USB

By default, the Main MCU pin VCC_USB is connected to the +3V3 MCU supply voltage. Alternatively, this pin may be connected to MCU Pin Header J1. To do this, copper jumper E8 must be open, and copper jumper E14 must be closed.

5.6.5.5 Signal P409/CAN

By default, the Main MCU pin P409 is connected to a TSCAP-E capacitor. This pin may be connected to MCU Pin Header J1. To do this, copper jumper E12 must be closed. The TSCAP-E capacitor may be disconnected by making copper jumper E15 open.
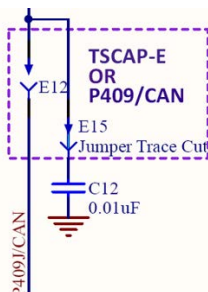

Figure 33.   P409/CAN Circuit

5.6.5.6 Signal P408/CMPIN1/CAN

By default, the Main MCU pin P408 is connected to both CAN and CMPIN1. P408/CAN is connected to J1, and P408/CMPIN1 is connected to J3. To disconnect P408/CAN from J1, copper jumper E41 must be open. To disconnect P408/CMPIN1 from J3, copper jumper E42 must be open.
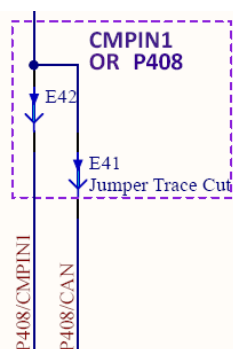

Figure 34.   P408/CMPIN1/CAN Circuit

5.6.5.7 Signal P102/SPI/ANSD1P

By default, the Main MCU pin P102 is connected to both SPI and ANSD1P. P102/SPI is connected to J1, and P102/ANSD1P is connected to J3. To disconnect P102/SPI from J1, copper jumper E43 must be open. To disconnect P102/ANSD1P from J3, copper jumper E44 must be open.
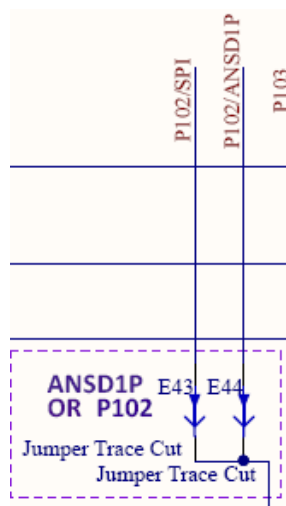

Figure 35.   P102/SPI/ANSD1P Circuit

6. Certifications

The EK-RA2A1 v1 meets the following certifications/standards. See page 3 of this User's Manual for the disclaimer and precautions.

6.1   EMC/EMI Standards

- FCC Notice (Class A)

  This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

  NOTE- This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
  — Reorient or relocate the receiving antenna.
  — Increase the separation between the equipment and receiver.
  — Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
  — Consult the dealer or an experienced radio/television technician for help.

- Innovation, Science and Economic Development Canada ICES-003 Compliance:
  CAN ICES-3 (A)/NMB-3(A)

- CE Class A (EMC)

  This product is herewith confirmed to comply with the requirmeents set out in the Council Directives on the Approximation of the laws of the Member States relating to electromagnetic Compatibility Directive 2004/108/EEC.
  Warning – This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be requried to take adequate measures to correct this interference.

- Taiwan: Chinese National Standard 13438, C6357 compliance, Class A limits

- Australia/New Zealand AS/NZS CISPR 32:2015, Class A

6.2   Material Selection, Waste, Recycling and Disposal Standards

- EU RoHS

- China SJ/T 113642014, 10-year environmental protection use period.

6.3   Safety Standards

- UL 94V-0

7. Design and Manufacturing Information

The design and manufacturing information about EK-RA2A1 v1 board are available in the "EK-RA2A1v1 Design Package" available on renesas.com/ra/ek-ra2a1.

- Design package file name: ek-ra2a1-v1-designpackage.zip
- Design package contents

File Type	Content	File/Folder Name
File (PDF)	Schematics	ek-ra2a1-v1-schematics
File (PDF)	Mechanical Drawing	ek-ra2a1-v1-mechdwg
File (PDF)	3D Drawing	ek-ra2a1-v1-3d
File (PDF)	BOM	ek-ra2a1-v1-bom
Folder	Manufacturing Files	Manufacturing Files
Folder	Design Files	Design Files - Altium

8. Website and Support

Visit the following URLs to learn about the kit and the RA family of microcontrollers, download tools and documentation, and get support.

EK-RA2A1 Resources   renesas.com/ra/ek-ra2a1
RA Product Information   renesas.com/ra
RA Product Support Forum   renesas.com/ra/forum
Renesas Support   renesas.com/support

Revision History

Rev.	Date	Description	
		Page	**Summary**
1.00	Oct.02.19	—	Initial release
1.01	Apr.09.20	—	Second release

EK-RA2A1 v1 – User's Manual

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