RL78/G1G Group

Renesas Starter Kit User's Manual

RENESAS MCU
RL78 Family / RL78/G1X Series

Renesas Electronics
www.renesas.com

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Disclaimer

By using this Renesas Starter Kit (RSK), the user accepts the following terms:

The RSK is not guaranteed to be error free, and the entire risk as to the results and performance of the RSK is assumed by the User. The RSK is provided by Renesas on an "as is" basis without warranty of any kind whether express or implied, including but not limited to the implied warranties of satisfactory quality, fitness for a particular purpose, title and non-infringement of intellectual property rights with regard to the RSK. Renesas expressly disclaims all such warranties. Renesas or its affiliates shall in no event be liable for any loss of profit, loss of data, loss of contract, loss of business, damage to reputation or goodwill, any economic loss, any reprogramming or recall costs (whether the foregoing losses are direct or indirect) nor shall Renesas or its affiliates be liable for any other direct or indirect special, incidental or consequential damages arising out of or in relation to the use of this RSK, even if Renesas or its affiliates have been advised of the possibility of such damages.

Precautions

The following precautions should be observed when operating any RSK product:

This Renesas Starter Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the RSK hardware functionality, and electrical characteristics. It is intended for users designing sample code on the RSK platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK product, but does not intend to be a guide to embedded programming or hardware design. Further details regarding setting up the RSK and development environment can found in the tutorial manual.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RL78/G1G Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK hardware.	RSKRL78G1G User's Manual	R20UT3022EG
Tutorial Manual	Provides a guide to setting up RSK environment, running sample code and debugging programs.	RSKRL78G1G Tutorial Manual	CS+: R20UT3019EG e^{2}studio: R20UT3023EG
Quick Start Guide	Provides simple instructions to setup the RSK and run the first sample.	RSKRL78G1G Quick Start Guide	CS+: R20UT3020EG e^{2}studio: R20UT3024EG
Code Generator Tutorial Manual	Provides a guide to code generation and importing into the IDE (Integrated Development Environment).	RSKRL78G1G Code Generator Tutorial Manual	CS+: R20UT3021EG e^{2}studio: R20UT3025EG
Schematics	Full detail circuit schematics of the RSK.	RSKRL78G1G Schematics	R20UT3017EG
Hardware Manual	Provides technical details of the RL78/G1G microcontroller.	RL78/G1G Group Hardware Manual	R01UH0499EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
BC	Battery Charging
bps	Bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DIP	Dual In-line Package
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
E1	Renesas On-chip Debugging Emulator
EEPROM	Electronically Erasable Programmable Read Only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
GPT	General PWM Timer
I^2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LIN	Local Interconnect Network
MCU	Micro-controller Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not applicable
n/c (NC)	Not connected
NMI	Non-maskable Interrupt
OTG	On The Go™
PC	Personal Computer
PDC	Parallel Data Capture Unit
PLL	Phase Locked Loop
Pmod™	This is a Digilent Pmod™ Compatible connector. Pmod™ is registered to Digilent Inc. Digilent-Pmod_Interface_Specification (Link valid at 14 Apr, 2014)
POE	Port Output Enable
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read Only Memory
RSK	Renesas Starter Kit
RTC	Realtime Clock
SAU	Serial Array Unit
SCI	Serial Communications Interface
SFR	Special Function Registers
SPI	Serial Peripheral Interface
SSI	Serial Sound Interface
TAU	Timer Array Unit
TFT	Thin Film Transistor
TPU	Timer Pulse Unit
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WDT	Watchdog timer

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Table of Contents

RENESAS

RSKRL78G1G

RENESAS STARTER KIT

R20UT3022EG0100
Rev. 1.00
Jan 15, 2015

1. Overview

1.1 Purpose

This RSK is an evaluation tool for Renesas microcontrollers. This manual describes the technical details of the RSK hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

1.2 Features

This RSK provides an evaluation of the following features:

- Renesas microcontroller programming
- User code debugging
- User circuitry such as switches, LEDs and a potentiometer
- Sample application
- Sample peripheral device initialisation code

The RSK board contains all the circuitry required for microcontroller operation.

1.3 Board specification

Board specification was shown in **Table 1-1** below.

Item	Specification
Microcontroller	Part No : R5F11EFAAFP
	Package : 44-pin LQFP
	On-Chip Memory : ROM 16KB, RAM 1.5KB
On-Board Memory	I²C EEPROM : 16Kbit
Input Clock	RL78/G1G Main : 20MHz
	RL78/G1C Main: 12MHz
Power Supply [*1]	DC Power Jack : 5 V Input
	Power IC: 5Vinput, 3.3V output
Debug Interface	E1 14-pin box header
Push Switch	Reset Switch x 1
	User Switch x 3
Potentiometer (for ADC)	Single-turn, 10kΩ
LED	Power indicator: green x 1
	User : green x 1, orange x 1, red x 2
USB to Serial Converter Interface	Connector : USB-MiniB
	Driver : RL78/G1C Microcontroller (Part No R5F10JBCANA)
Pmod™	PMOD1 : Angle type, 12-pin Connector
	PMOD2 : Straight type, 12-pin Connector
Application Board Interface [*2]	2.54mm pitch, 26-pin x 2 (JA1, JA2), 24-pin x 2 (JA5, JA6)

Table 1-1: Board Specifications

[*1]: Board can also supply 5V into RL78/G1G microcontroller without LDO regulator.
[*2]: The connector is not included to a product.

2. Power Supply

2.1   Requirements

This RSK is supplied with an E1 debugger. The debugger is able to power the RSK board with up to 200mA. When the RSK is connected to another system then that system should supply power to the RSK. This board has an optional centre positive supply connector using a barrel power jack.

Details of the external power supply requirements for the RSK, and configuration are shown in **Table 2-2** below. The default RSK power configuration is shown in **Bold, blue text.**

Connector	Supply voltage
PWR	5VDC Input

Table 2-1: PWR connector Requirements

J14 Setting *	Supply Source	Board_5V	Board_VDD UC_VDD
Pin1-2 shorted	PWR Connector/CON_5V/Unregulated_VDD /E1(5V)	5V	5V
Pin2-3 shorted (or **R116 Fitted**)	PWR Connector/CON_5V/Unregulated_VDD	5V	3.3V
	CON_3V3/**E1(3V3)**	**n/a**	**3.3V**
Open	DO NOT SET	DO NOT SET	DO NOT SET

Table 2-2: Main Power Supply Requirements

* By default, jumper J14 is not fitted to the RSK. R116 is fitted by default and becomes the same setting as 'J14 Pin2-3 shorted'.

The main power supply connected to PWR1 should supply a minimum of 5W to ensure full functionality.

2.2   Power-Up Behaviour

When the RSK is purchased, the RSK board has the 'Release' build of the example tutorial software pre-programmed into the Renesas microcontroller. Please consult the 'Renesas Starter Kit Code Generator Tutorial Manual' for further information of this example.

3.   Board Layout

3.1   Component Layout

Figure 3-1 below shows the top component layout of the board.
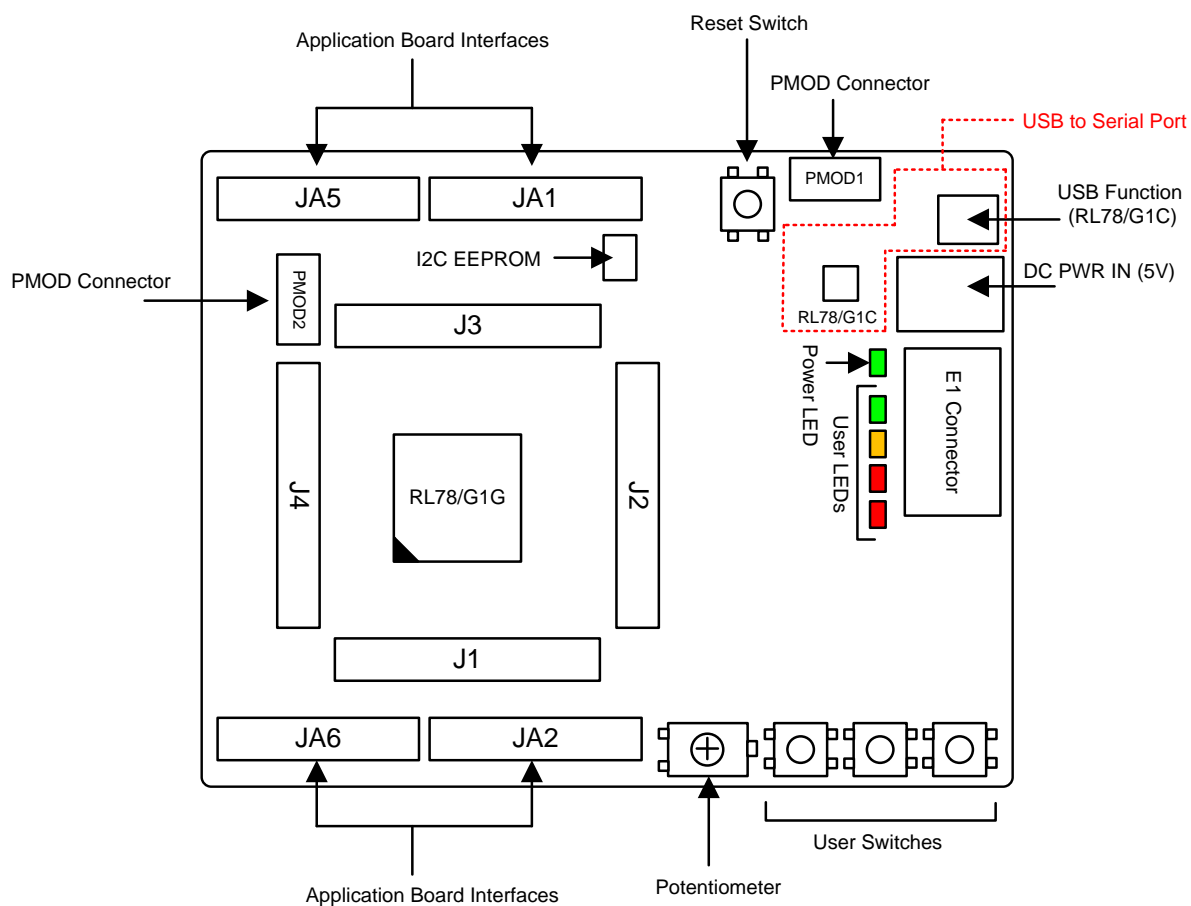
Figure 3-1: Board Layout

3.2   Board Dimensions

Figure 3-2 below gives the board dimensions and connector positions. All the through-hole connectors are on a common 0.1 inch grid for easy interfacing.
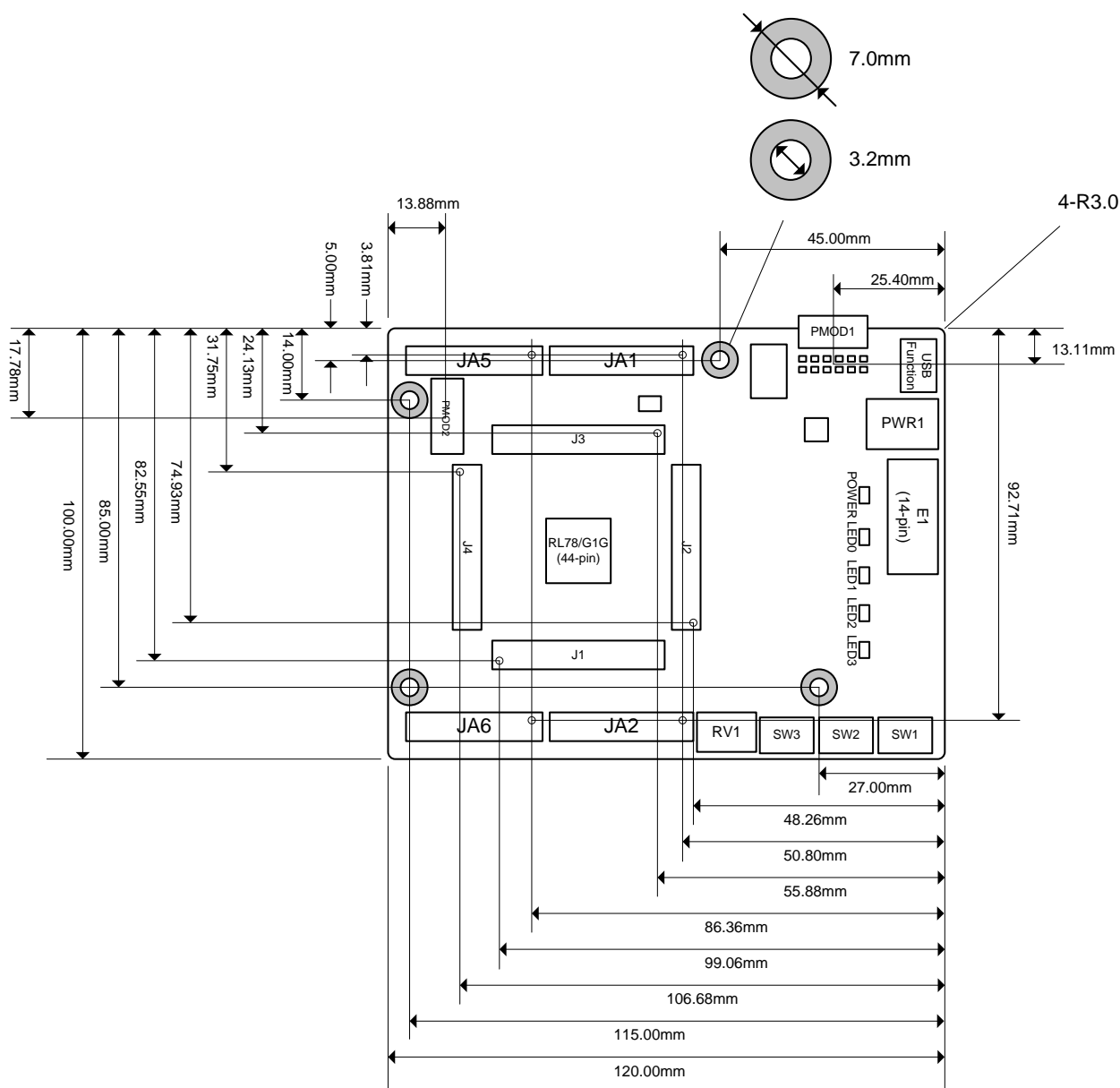
Figure 3-2: Board Dimensions

3.3   Component Placement

Figure 3-2 below shows placement of individual components on the top-side PCB – bottom-side component placement can be seen in **Figure 3-4**. Component types and values can be looked up using the board schematics.
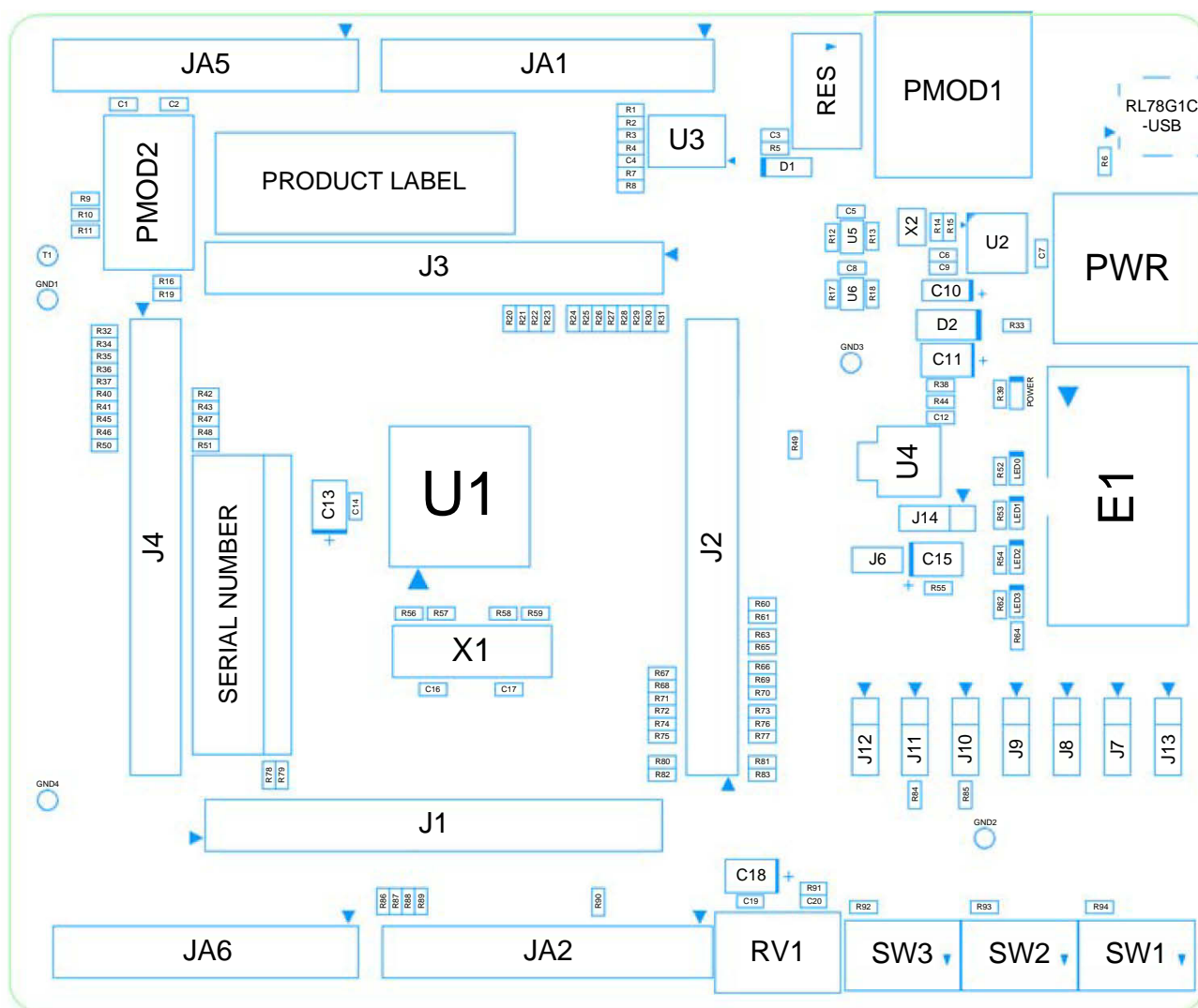
Figure 3-3: Top-Side Component Placement

Figure 3-4 below shows the component placement on the bottom-side of the RSK board.
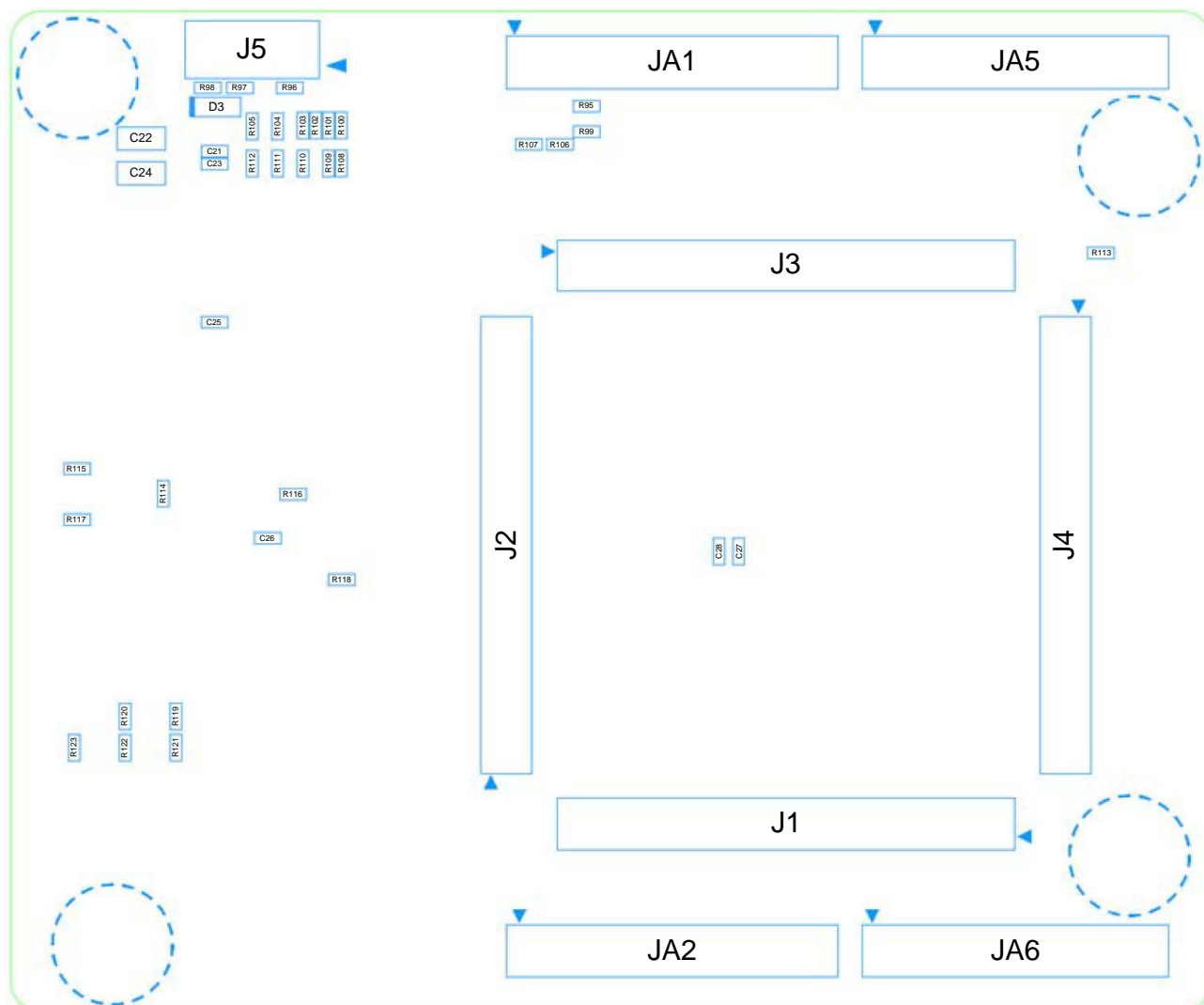
Figure 3-4: Bottom-Side Component Placement

4.   Connectivity

4.1   Internal RSK Connections

The diagram below shows the RSK board components and their connectivity to the MCU.
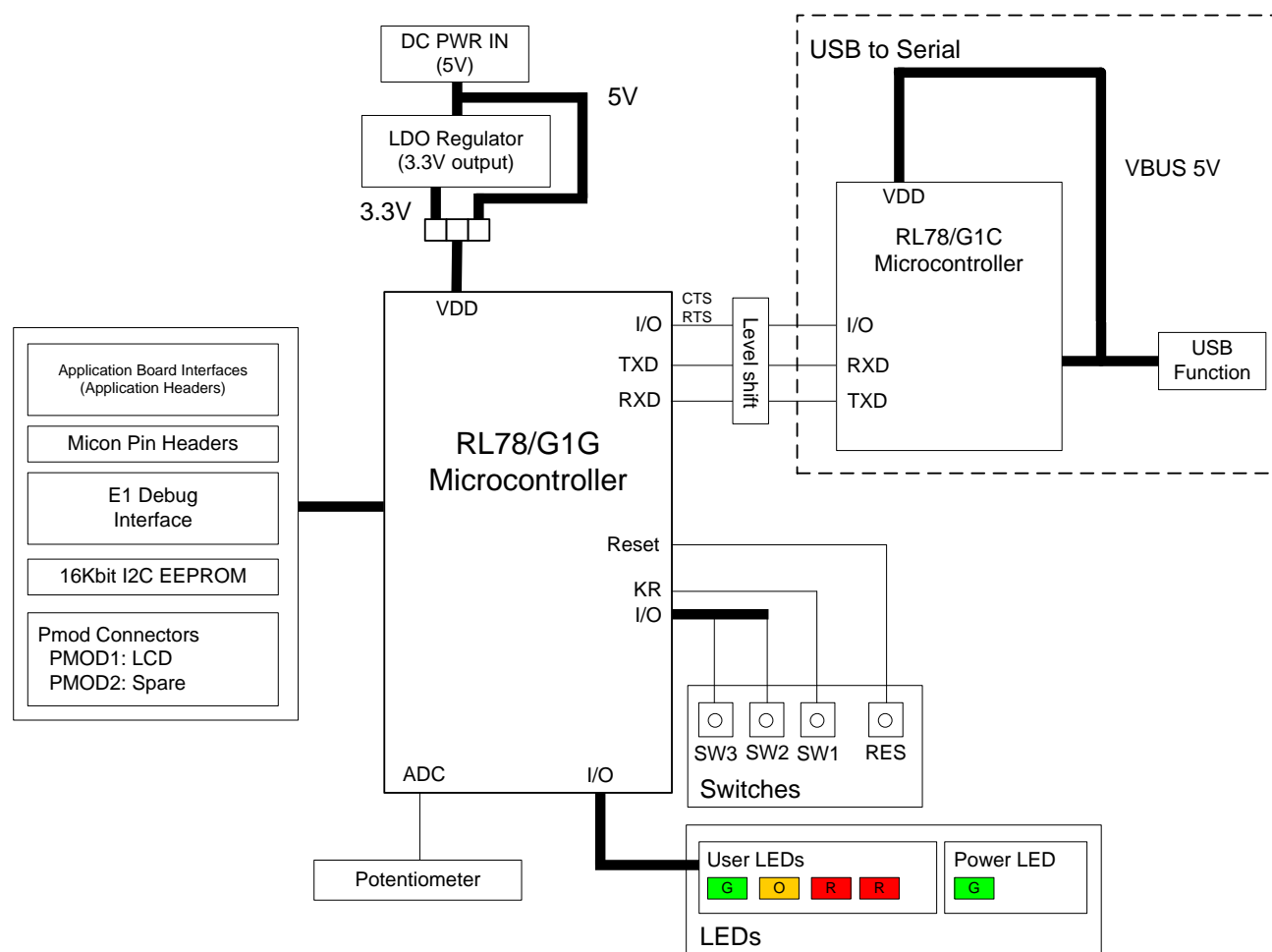
Figure 4-1: Internal RSK Block Diagram

4.2   Debugger Connections

The diagram below shows the connections between the RSK, E1 debugger and the host PC.
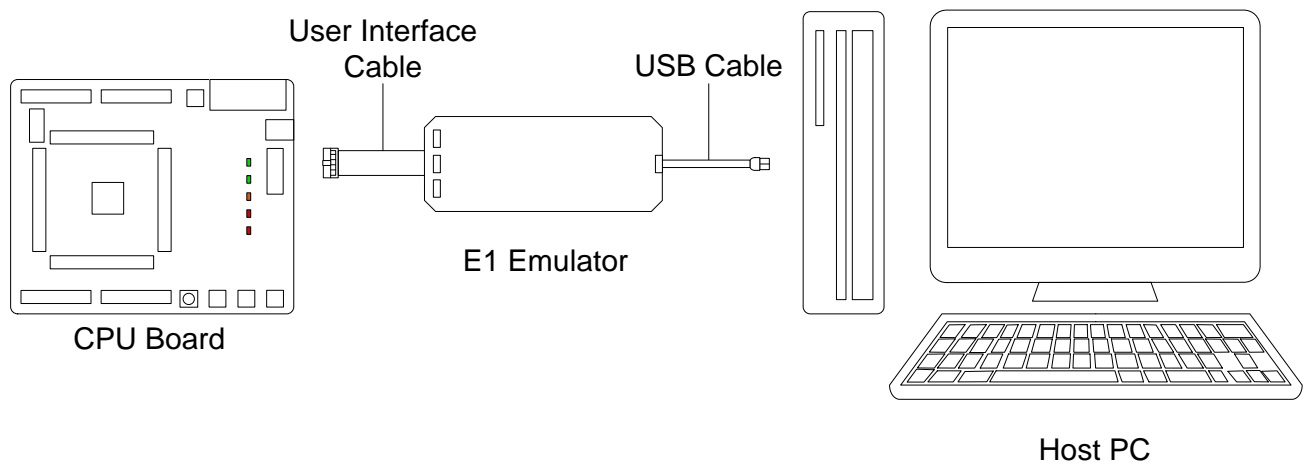
Figure 4-2: Debugger Connection Diagram

5.   User Circuitry

5.1   Reset Circuit

A reset control circuit is not fitted to the RSK, as the MCU is capable of voltage and power-on detection. Resets are handled internally, and the reset switch is connected directly to the RESET pin on the MCU.

5.2   Clock Circuit

A clock circuit is fitted to the RSK to generate the required clock signal to drive the MCU, and associated peripherals. Refer to the RL78/G1G Group Hardware Manual for details regarding the clock signal requirements, and the RSKRL78/G1G board schematics for information regarding the clock circuitry in use on the RSK. Details of the oscillators fitted to the board are listed in **Table 5-1** below.

Crystal	Function	Default Placement	Frequency	Device Package
X1	Main MCU crystal for RL78/G1G	Fitted	20MHz	Encapsulated, SMT
X2	Main MCU crystal for RL78/G1C	Fitted	12MHz	Encapsulated, SMT

Table 5-1: Oscillators

5.3   Switches

There are four switches located on the RSK board. The function of each switch and its connection is shown in **Table 5-2**. For further information regarding switch connectivity, refer to the RSK schematics.

Switch	Function	MCU Port	Pin
RES	When pressed, the microcontroller is reset	RESETn	3
SW1	Connects to a key return input for user controls	KR0(P70)	20
SW2	Connects to a general purpose I/O for user controls	P124	4
SW3	Connects to a general purpose I/O for user controls	P123	5

Table 5-2: Switch Connections

5.4   LEDs

There are five LEDs on the RSK. The function of each LED, its colour, and its connections are shown in **Table 5-3**.

LED	Colour	Function	MCU Port	Pin
POWER	Green	Indicates the power status	-	-
LED0	Green	User operated LED	P41	1
LED1	Orange	User operated LED	P63	15
LED2	Red	User operated LED	P72	18
LED3	Red	User operated LED	P73	17

Table 5-3: LED Connections

5.5   Potentiometer

A single-turn potentiometer is connected as a potential divider to analog input ANI0 (Port P20, Pin 41).

The potentiometer is fitted to offer an easy method of supplying a variable analog input to the microcontroller. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the device User's Manual: Hardware for further details.

5.6   Pmod™

A Pmod™ Compatible debug LCD module is supplied with the RSK, and should be connected to the PMOD1 header.

Care should be taken when installing the LCD module to ensure pins are not bent or damaged. The LCD module is vulnerable to electrostatic discharge (ESD); therefore appropriate ESD protection should be used.

The Digilent Pmod™ Compatible header uses a SPI interface. Some RSKs will be provided with a monochrome display, others will have a colour display. Code for the appropriate display will be included in the product software support. Connection information for the Digilent Pmod™ Compatible header is provided in **Table 5-4 and Table 5-5** below.

Please note that the connector numbering adheres to the Digilent Pmod™ standard and is different from all other connectors on the RSK designs. Details can be found in the Digilent Pmod™ Interface Specification Revision: November 20, 2011
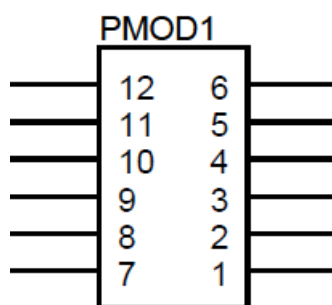
Figure 5-1: Digilent Pmod™ Compatible Header Pin Numbering

Digilent Pmod™ Compatible Header Connections (PMOD1)							
Pin	**Circuit Net Name**	**MCU**		**Pin**	**Circuit Net Name**	**MCU**	
		Port	**Pin**			**Port**	**Pin**
1	P62	P62	14	7	P-INTP4	P31	16
2	P-SO00_TxD0	P51	23	8	P71	P71	19
					P-INTP5	P16	25
3	P-SI00_RxD0	P50	22	9	P61	P61	13
4	P-SCK00	P30	21	10	P60	P60	12
5	GROUND	-	-	11	GROUND	-	-
6	Board_3V3	-	-	12	Board_3V3	-	-

Table 5-4: Pmod™1 Header Connections (PMOD1)

Digilent Pmod™ Compatible Header Connections (PMOD2)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	P17	P17	24	7	P-INTP4	P31	16
2	P-SO00_TxD0	P51	23	8	P27	P27	34
					P-INTP0	P137	6
3	P-SI00_RxD0	P50	22	9	P146	P146	32
4	P-SCK00	P30	21	10	P147	P147	33
5	GROUND	-	-	11	GROUND	-	-
6	Board_3V3	-	-	12	Board_3V3	-	-

Table 5-5: Pmod™2 Header Connections (PMOD2)

5.7   USB Serial Port

A USB serial port implemented in another Renesas low power microcontroller (RL78/G1C) is fitted on the RSK to the microcontroller UART1. Multiple options are provided to allow re-use of the serial interface.
Connections between the USB to Serial converter and the microcontroller are listed in **Table 5-6** below.

Serial Signal	Function	MCU	
		Port	Pin
A-SO00_TxD0 [1]	UART0 Transmit Signal	P51	23
A-SI00_RxD0 [1]	UART0 Receive Signal	P50	22
TxD1	UART1 Transmit Signal	P00	43
RxD1	UART1 Receive Signal	P01	42
RS232TX [1]	External RS232 Transmit Signal	-	-
RS232RX [1]	External RS232 Receive Signal	-	-
RL78G1C_CTS [2]	Clear To Send	P146	32
RL78G1C_RTS [2]	Request to Send	P147	33

Table 5-6: Serial Port Connections

[1]: This connection is a not available in the default RSK configuration - refer to §6 for the required modifications.

[2]: CTS & RTS control is not supported on this RSK.

When the RSK board is first connected to a PC running Windows with the USB/Serial connection, the PC will look for a driver. This driver is installed during the installation process, so the PC should be able to find it. The PC will report that it is installing for a driver and then report that a driver has been installed successfully, as shown in **Figure 5-2**. The exact messages may vary depending upon operating system.
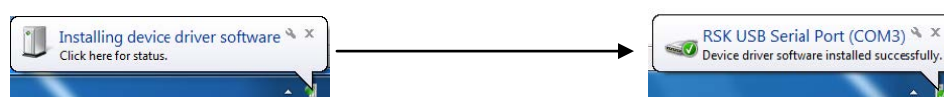
Figure 5-2: USB-Serial Windows Installation message

5.8   Simplified I^{2}C

The RL78/G1G features one Simplified I^{2}C interface modules. IIC00 is connected to a 16Kbit EEPROM (Electronically-Erasable Programmable Read Only Memory). Specific details of the EEPROM device and the connections can be found in the board schematics.

On board EEPROM only supports single device on bus. To allow external I^{2}C device, option links have to be modified – refer to §6 for further details.

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6.   Configuration

6.1   Modifying the RSK

This section lists the option links that are used to modify the way RSK operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers or by configuration DIP switches

A link resistor is a 0Ω surface mount resistor, which is used to short or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. **Bold, blue text** indicates the default configuration that the RSK is supplied with. Refer to the component placement diagram (§3) to locate the option links, jumpers and DIP switches.

> When removing soldered components, always ensure that the RSK is not exposed to a soldering iron for intervals greater than 5 seconds. This is to avoid damage to nearby components mounted on the board.

> When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MCU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to the RL78/G1G Group Hardware Manual and RSKRL78G1G schematics for further information.

6.2   Power Supply Configuration

Table 6-1 and Table 6-2 below details the function of the option links associated with power supply configuration.

Reference	Explanation	Fit	DNF	Related Ref.
Board_5V (PWR Connector)	Connects PWR to Board_5V	R33	-	U4.IN
	Disconnects PWR from Board_5V	-	R33	U4.IN
Board_5V (CON_5V)	Connects CON_5V to Board_5V	R38	-	U4.IN, JA1
	Disconnects CON_5V from Board_5V	-	R38	U4.IN, JA1.1
Board_5V (Unregulated_VDD)	Connects Unregulated_VDD to Board_5V	R44	-	JA6.23
	Disconnects Unregulated_VDD from Board_5V	-	R44	JA6.23
Board_VDD (U4)	Connects Regulator output to Board_VDD	R116	-	-
	Disconnects Regulator output from Board_VDD	-	R116	-
Board_VDD (CON_3V3)	Connects CON_3V3 to Board_VDD	R55	-	JA1.3
	Disconnects CON_3V3 from Board_VDD	-	R55	JA1.3
Board_VDD (Board_3V3)	Connects Board_3V3 to Board_VDD	R49	-	PMOD1, PMOD2
	Disconnects Board_3V3 from Board_VDD	-	R49	PMOD1, PMOD2
Board_VDD (UC_VDD)	Connects Board_VDD to UC_VDD	R118	-	U1(VDD)
	Disconnects Board_VDD from UC_VDD	-	R118	U1(VDD)

Table 6-1: Power Supply Option Links (1)

Reference	Jumper Position	Explanation	Related Ref.
J14 [*1]	Shorted Pin1-2	Connects 5V power rail to Board_VDD	-
	Shorted Pin2-3	Connects Regulator output to Board_VDD	R116
	All open	DO NOT SET	-
J6 [*2]	Shorted Pin1-2	Connects Board_VDD to UC_VDD	R118
	All open	Enables current probe for MCU current consumption.	-

Table 6-2: Power Supply Option Links (2)

[*1]: By default, jumper J14 is not fitted to the RSK. R116 is fitted by default and becomes the same setting as 'J14 Shorted Pin2-3'.

[*2]: By default, jumper J6 is not fitted to the RSK. R118 is fitted by default and becomes the same setting as 'J6 Shorted Pin1-2'.

6.3   Clock Configuration

Table 6-3 below details the function of the option links associated with clock configuration.

Reference	Explanation	Fit	DNF	Related Ref.
X1, CON_X1, CON_EXTAL	Connects crystal (X1) to RL78/G1G	R57, R58	R59, R56	U1(X1, X2)
	Connects CON_EXTAL to RL78/G1G.	R56	R57, R58	U1(EXTAL)

Table 6-3: Clock Option Links

Items shown in **bold** are the Fit / Do Not Fit (DNF) default configuration that the RSK is supplied with.

6.4   ADC & PGA & Comparator Configuration

Table 6-4 below details the function of the option links associated with ADC, PGA (Programmable Gain Amplifiers) and Comparator configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TI00_**TxD1**_CMP0P	43	P00	TI00	R47	R48, R51	JA2.21	-	-
			TxD1	**R48**	R47, **R51**	JA6.8	-	-
						U5.3	R122/J7.2-3	J7.1-2, R120
			CMP0P	R51	R47, R48	JA6.20	-	-
TO00_**RxD1**_PGA	42	P01	TO00	R45	R46, R50	JA2.19	-	-
			RxD1	**R46**	R45, R50	JA6.7	-	-
						U6.4	R121/J8.2-3	J8.1-2, R119
			PGA	R50	R45, R46	JA2.24	R88	R87
ANI0_AVREFP	41	P20	AVREFP	R42	R43	JA1.7	-	-
			ANI0	R43	R42	JA1.9	-	-
						RV1	R91	-
ANI1_AVREFM	40	P21	ANI1	R40	R41	JA1.10	-	-
			AVREFM	R41	R40	JA1.6	-	-
P27_**ANI7**	34	P27	P27	R34	R32	PMOD2.8	R35	R36
			ANI7	**R32**	**R34**	JA5.4	-	-

Table 6-4: ADC & PGA & Comparator Option Links

6.5   General I/O & LED Configuration

Table 6-5 below details the function of the option links associated with General I/O and LED configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P60_IO0	12	P60	P60	R81	R83	PMOD1.10	-	-
			IO0	R83	R81	JA1.15	-	-
P61_IO1	13	P61	P61	R82	R80	PMOD1.9	-	-
			IO1	R80	R82	JA1.16	-	-
P62_IO2_M1UD	14	P62	P62	R73	R76, R77	PMOD1.1	-	-
			IO2	R76	R73, R77	JA1.17	-	-
			M1UD	R77	R73, R76	JA2.11	-	-
LED1_IO3	15	P63	LED1	R75	R74	LED1	-	-
			IO3	R74	R75	JA1.18	-	-
SW1_IO4	20	P70	SW1	R60	R61	SW1	-	-
			IO4	R61	R60	JA1.19	-	-
P71_IO5	19	P71	P71	R68	R67	PMOD1.8	R24	R25
			IO5	R67	R68	JA1.20	-	-
LED2_IO6	18	P72	LED2	R63	R65	LED2	-	-
			IO6	R65	R63	JA1.21	-	-
LED3_IO7	17	P73	LED3	R72	R71	LED3	-	-
			IO7	R71	R72	JA1.22	-	-

Table 6-5: General I/O & LED Option Links

Items shown in **bold** are the Fit / Do Not Fit (DNF) default configuration that the RSK is supplied with.

6.6   I^{2}C & EEPROM Configuration

Table 6-6 and Table 6-7 below details the function of the option links associated with I^{2}C and EEPROM configuration.

Signal name	MCU Pin	MCU Port	MCU Peripheral Selection Signal	Fit	DNF	Destination Selection Interface /Function	Fit	DNF
SCL00_P-SCK00_A-SCK00_INTP3	21	P30	SCL00	J9.1-2	J10.Open	U3.6	R3	-
						JA1.26	-	R3
			P-SCK00	J9.2-3	J10.Open	PMOD1.4, PMOD2.4	-	-
			A-SCK00	J10.1-2	J9.Open	JA2.10	-	-
			INTP3	J10.2-3	J9.Open	JA1.23	-	-
SDA00_P-SI00_RxD0_A-SI00_RxD0_INTP1	22	P50	SDA00	J11.1-2	J12.Open	U3.5	R2	-
						JA1.25	-	R2
			INTP1	J11.2-3	J12.Open	JA2.7	-	-
			P-SI00_RxD0	J12.1-2	J11.Open	PMOD1.3, PMOD2.3	-	-
			A-SI00_RxD0	J12.2-3	J11.Open	JA2.8	-	-
						U6.4	J8.1-2	J8.2-3 /R121, R119

Table 6-6: I^{2}C & EEPROM Option Links (1)

Reference	MCU Peripheral Selection Function	Fit	DNF	Destination Selection Interface/Function
SDA00 (JA1_SDA00), SCL00 (JA1_SCL00),	Operates with Board_VDD	R7	R8	U3, JA1.25, JA1.26
	Operates with Board_5V	R8	R7	U3, JA1.25, JA1.26
SDA00, SCL00	Enable EEPROM Write Protection	R106	-	U3
	Disables EEPROM Write Protection	-	R106	U3

Table 6-7: I^{2}C & EEPROM Option Links (2)

Items shown in **bold** are the Fit / Do Not Fit (DNF) default configuration that the RSK is supplied with.

6.7 IRQ Configuration

Table 6-8 below details the function of the option links associated with the IRQ configuration.

| Signal name | MCU | | MCU Peripheral Selection | | | Destination Selection | | |
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P-INTP5_**A-INTP5**_TRDIOC0	25	P16	P-INTP5	R27	R28, R29	PMOD1.8	R25	R24
			A-INTP5	R29	R27, R28	JA2.23	-	-
			TRDIOC0	R28	R27, R29	JA6.13	-	-
SCL00_**P-SCK00**_A-SCK00_INTP3	21	P30	SCL00	J9.1-2	J10.Open	U3.6	R3	-
						JA1.26	-	R3
			P-SCK00	J9.2-3	J10.Open	PMOD1.4, PMOD2.4	-	-
			A-SCK00	J10.1-2	J9.Open	JA2.10	-	-
			INTP3	J10.2-3	J9.Open	JA1.23	-	-
P-INTP4_**A-INTP4**_TO03	16	P31	P-INTP4	R66	R69, R70	PMOD1.7	-	-
						PMOD2.7	R100	-
			A-INTP4	R69	R66, R70	JA2.9	-	-
			TO03	R70	R66, R69	JA2.20	-	-
SDA00_P-SI00_RxD0_A-SI00_RxD0_**INTP1**	22	P50	SDA00	J11.1-2	J12.Open	U3.5	R2	-
						JA1.25	-	R2
			INTP1	J11.2-3	J12.Open	JA2.7	-	-
			P-SI00_RxD0	J12.1-2	J11.Open	PMOD1.3, PMOD2.3	-	-
			A-SI00_RxD0	J12.2-3	J11.Open	JA2.8	-	-
						U6.4	J8.1-2	J8.2-3/R121, R119
P-INTP0_**A-INTP0**	6	P137	P-INTP0	R78	R79	PMOD2.8	R36	R35
			A-INTP0	R79	R78	JA2.24	R87	R88

Table 6-8: IRQ Option Links

6.8 Timer Configuration

Table 6-9 below details the function of the option links associated with Timer configuration.

| Signal name | MCU | | MCU Peripheral Selection | | | Destination Selection | | |
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TI00_**TxD1**_CMP0P	43	P00	TI00	R47	R48, R51	JA2.21	-	-
			TxD1	R48	R47, R51	JA6.8	-	-
						U5.3	R122/J7.2-3	J7.1-2, R120
			CMP0P	R51	R47, R48	JA6.20	-	-
TO00_**RxD1**_PGA	42	P01	TO00	R45	R46, R50	JA2.19	-	-
			RxD1	R46	R45, R50	JA6.7	-	-
						U6.4	R121/J8.2-3	J8.1-2, R119
			PGA	R50	R45, R46	JA2.24	R88	R87
P-INTP5_**A-INTP5**_TRDIOC0	25	P16	P-INTP5	R27	R28, R29	PMOD1.8	R25	R24
			A-INTP5	R29	R27, R28	JA2.23	-	-
			TRDIOC0	R28	R27, R29	JA6.13	-	-
P17_TI02	24	P17	P17	R31	R30	PMOD2.1	-	-
			TI02	R30	R31	JA2.22	-	-
P-INTP4_**A-INTP4**_TO03	16	P31	P-INTP4	R66	R69, R70	PMOD1.7	-	-
						PMOD2.7	R100	-
			A-INTP4	R69	R66, R70	JA2.9	-	-
			TO03	R70	R66, R69	JA2.20	-	-
P62_IO2_M1UD	14	P62	P62	R73	R76, R77	PMOD1.1	-	-
			IO2	R76	R73, R77	JA1.17	-	-
			M1UD	R77	R73, R76	JA2.11	-	-

Table 6-9: Timer Option Links

Items shown in **bold** are the Fit / Do Not Fit (DNF) default configuration that the RSK is supplied with.

6.9   PMOD1 Interface Configuration

Table 6-10 below details the function of the option links associated with PMOD1 Interface configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P-INTP5_A-INTP5_TRDIOC0	25	P16	P-INTP5	R27	R28, R29	PMOD1.8	R25	R24
			A-INTP5	R29	R27, R28	JA2.23	-	-
			TRDIOC0	R28	R27, R29	JA6.13	-	-
SCL00_P-SCK00_A-SCK00_INTP3	21	P30	SCL00	J9.1-2	J10.Open	U3.6	R3	-
						JA1.26	-	R3
			P-SCK00	J9.2-3	J10.Open	PMOD1.4, PMOD2.4	-	-
			A-SCK00	J10.1-2	J9.Open	JA2.10	-	-
			INTP3	J10.2-3	J9.Open	JA1.23	-	-
P-INTP4_A-INTP4_TO03	16	P31	P-INTP4	R66	R69, R70	PMOD1.7	-	-
						PMOD2.7	R100	-
			A-INTP4	R69	R66, R70	JA2.9	-	-
			TO03	R70	R66, R69	JA2.20	-	-
SDA00_P-SI00_RxD0_A-SI00_RxD0_INTP1	22	P50	SDA00	J11.1-2	J12.Open	U3.5	R2	-
						JA1.25	-	R2
			INTP1	J11.2-3	J12.Open	JA2.7	-	-
			P-SI00_RxD0	J12.1-2	J11.Open	PMOD1.3, PMOD2.3	-	-
			A-SI00_RxD0	J12.2-3	J11.Open	JA2.8	-	-
						U6.4	J8.1-2	J8.2-3/R121, R119
P-SO00_TxD0_A-SO00_TxD0	23	P51	A-SO00_TxD0	J13.1-2	J13.2-3, R123	JA2.6	-	-
						U5.3	J7.1-2	J7.2-3, R120, R122
			P-SO00_TxD0	J13.2-3/R123	J13.1-2	PMOD1.2, PMOD2.2	-	-
P60_IO0	12	P60	P60	R81	R83	PMOD1.10	-	-
			IO0	R83	R81	JA1.15	-	-
P61_IO1	13	P61	P61	R82	R80	PMOD1.9	-	-
			IO1	R80	R82	JA1.16	-	-
P62_IO2_M1UD	14	P62	P62	R73	R76, R77	PMOD1.1	-	-
			IO2	R76	R73, R77	JA1.17	-	-
			M1UD	R77	R73, R76	JA2.11	-	-
P71_IO5	19	P71	P71	R68	R67	PMOD1.8	R24	R25
			IO5	R67	R68	JA1.20	-	-

Table 6-10: PMOD1 Interface Option Links

Items shown in **bold** are the Fit / Do Not Fit (DNF) default configuration that the RSK is supplied with.

6.10   PMOD2 Interface Configuration

Table 6-11 below details the function of the option links associated with PMOD2 Interface configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P17_TI02	24	P17	P17	R31	R30	PMOD2.1	-	-
			TI02	R30	R31	JA2.22	-	-
P27_ANI7	34	P27	P27	R34	R32	PMOD2.8	R35	R36
			ANI7	R32	R34	JA5.4	-	-
SCL00_P-SCK00_A-SCK00_INTP3	21	P30	SCL00	J9.1-2	J10.Open	U3.6	R3	-
						JA1.26	-	R3
			P-SCK00	J9.2-3	J10.Open	PMOD1.4, PMOD2.4	-	-
			A-SCK00	J10.1-2	J9.Open	JA2.10	-	-
			INTP3	J10.2-3	J9.Open	JA1.23	-	-
P-INTP4_A-INTP4_TO03	16	P31	P-INTP4	R66	R69, R70	PMOD1.7	-	-
						PMOD2.7	R100	-
			A-INTP4	R69	R66, R70	JA2.9	-	-
			TO03	R70	R66, R69	JA2.20	-	-
SDA00_P-SI00_RxD0_A-SI00_RxD0_INTP1	22	P50	SDA00	J11.1-2	J12.Open	U3.5	R2	-
						JA1.25	-	R2
			INTP1	J11.2-3	J12.Open	JA2.7	-	-
			P-SI00_RxD0	J12.1-2	J11.Open	PMOD1.3, PMOD2.3	-	-
			A-SI00_RxD0	J12.2-3	J11.Open	JA2.8	-	-
						U6.4	J8.1-2	J8.2-3/R121, R119
P-SO00_TxD0_A-SO00_TxD0	23	P51	A-SO00_TxD0	J13.1-2	J13.2-3, R123	JA2.6	-	-
						U5.3	J7.1-2	J7.2-3, R120, R122
			P-SO00_TxD0	J13.2-3/R123	J13.1-2	PMOD1.2, PMOD2.2	-	-
P-INTP0_A-INTP0	6	P137	P-INTP0	R78	R79	PMOD2.8	R36	R35
			A-INTP0	R79	R78	JA2.24	R87	R88
RL78G1C_CTS_P146	32	P146	RL78G1C_CTS	R23	R22	U6.6	-	-
			P146	R22	R23	PMOD2.9	-	-
RL78G1C_RTS_P147	33	P147	RL78G1C_RTS	R21	R20	U5.1	-	-
			P147	R20	R21	PMOD2.10	-	-

Table 6-11: PMOD2 Interface Option Links

Items shown in **bold** are the Fit / Do Not Fit (DNF) default configuration that the RSK is supplied with.

6.11   Serial & USB to Serial Configuration

Table 6-12 below details the function of the option links associated with Serial and USB to Serial configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TI00_**TxD1**_CMP0P	43	P00	TI00	R47	R48, R51	JA2.21	-	-
			TxD1	**R48**	**R47, R51**	**JA6.8**	-	-
						U5.3	R122/J7.2-3	J7.1-2, R120
			CMP0P	R51	R47, R48	JA6.20	-	-
TO00_**RxD1**_PGA	42	P01	TO00	R45	R46, R50	JA2.19	-	-
			RxD1	**R46**	**R45, R50**	**JA6.7**	-	-
						U6.4	R121/J8.2-3	J8.1-2, R119
			PGA	R50	R45, R46	JA2.24	R88	R87
SCL00_**P-SCK00**_A-SCK00_INTP3	21	P30	SCL00	J9.1-2	**J10.Open**	U3.6	**R3**	-
						JA1.26	-	R3
			P-SCK00	**J9.2-3**	**J10.Open**	**PMOD1.4, PMOD2.4**	-	-
			A-SCK00	J10.1-2	J9.Open	JA2.10	-	-
			INTP3	J10.2-3	J9.Open	JA1.23	-	-
SDA00_P-SI00_RxD0_A-SI00_RxD0_**INTP1**	22	P50	SDA00	J11.1-2	**J12.Open**	U3.5	**R2**	-
						JA1.25	-	R2
			INTP1	**J11.2-3**	**J12.Open**	**JA2.7**	-	-
			P-SI00_RxD0	J12.1-2	J11.Open	PMOD1.3, PMOD2.3	-	-
			A-SI00_RxD0	J12.2-3	J11.Open	JA2.8	-	-
						U6.4	J8.1-2	J8.2-3/R121, **R119**
P-SO00_TxD0_A-SO00_TxD0	23	P51	A-SO00_TxD0	J13.1-2	J13.2-3, R123	JA2.6	-	-
						U5.3	J7.1-2	J7.2-3, **R120**, R122
			P-SO00_TxD0	**J13.2-3**/**R123**	J13.1-2	**PMOD1.2, PMOD2.2**	-	-
RL78G1C_CTS_**P146**	32	P146	RL78G1C_CTS	R23	R22	U6.6	-	-
			P146	**R22**	**R23**	**PMOD2.9**	-	-
RL78G1C_RTS_**P147**	33	P147	RL78G1C_RTS	R21	R20	U5.1	-	-
			P147	**R20**	**R21**	**PMOD2.10**	-	-
RS232TX	-	-	RS232TX	R120	**J7.Open**, R122	JA6.5	-	-
RS232RX	-	-	RS232RX	R119	**J8.Open**, R121	JA6.6	-	-

Table 6-12: Serial & USB to Serial Option Links

Items shown in **bold** are the Fit / Do Not Fit (DNF) default configuration that the RSK is supplied with.

7. Headers

7.1   Application Headers

This RSK is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MCU pins.

Table 7-1 below lists the connections of the application header, JA1.

Application Header JA1					
Pin	**Header Name**	**MCU Pin**	**Pin**	**Header Name**	**MCU Pin**
	Circuit Net Name			**Circuit Net Name**	
1	5V	-	2	0V	-
	CON_5V			GROUND	
3	3V3	-	4	0V	-
	CON_3V3			GROUND	
5	AVDD	NC	6	AVSS	40
	NC			AVREFM	
7	AVREF	41	8	ADTRG	NC
	AVREFP			NC	
9	ADC0	41	10	ADC1	40
	ANI0			ANI1	
11	ADC2	39	12	ADC3	38
	ANI2			ANI3	
13	DAC0	NC	14	DAC1	NC
	NC			NC	
15	IO_0	12	16	IO_1	13
	IO0			IO1	
17	IO_2	14	18	IO_3	15
	IO2			IO3	
19	IO_4	20	20	IO_5	19
	IO4			IO5	
21	IO_6	18	22	IO_7	17
	IO6			IO7	
23	IRQ3/IRQAEC/M2_HSIN0	21/NC/NC	24	IIC_EX	NC
	INTP3/NC/NC			NC	
25	IIC_SDA	22	26	IIC_SCL	21
	JA1_SDA00 (SDA00)			JA1_SCL00 (SCL00)	

Table 7-1: Application Header JA1 Connections

Table 7-2 below lists the connections of the application header, JA2.

Pin	Header Name Circuit Net Name	MCU Pin	Pin	Header Name Circuit Net Name	MCU Pin
	Application Header JA2				
1	RESET	3	2	EXTAL	7
	RESETn			CON_EXCLK	
3	NMI	NC	4	Vss1	-
	NC			GROUND	
5	WDT_OVF	NC	6	SCIaTX	23
	NC			A-SO00_TxD0	
7	IRQ0/WKUP/M1_HSIN0	22/NC/22	8	SCIaRX	22
	INTP1/NC/INTP1			A-SI00_RxD0	
9	IRQ1/M1_HSIN1	16/16	10	SCIaCK	21
	A-INTP4/A-INTP4			A-SCK00	
11	M1_UD	14	12	CTSRTS	NC
	M1UD			NC	
13	M1_UP	26	14	M1_UN	27
	TRDIOB0			TRDIOD0	
15	M1_VP	28	16	M1_VN	30
	TRDIOA1			TRDIOC1	
17	M1_WP	29	18	M1_WN	31
	TRDIOB1			TRDIOD1	
19	TimerOut	42	20	TimerOut	16
	TO00			TO03	
21	TimerIn	43	22	TimerIn	24
	TI00			TI02	
23	IRQ2/M1_EncZ/M1_HSIN2	25/NC/25	24	M1_POE	6/42
	A-INTP5/NC/A-INTP5			JA2_PIN24 (A-INTP0/PGA)	
25	M1_TRCCLK	NC	26	M1_TRDCLK	NC
	NC			NC	

Table 7-2: Application Header JA2 Connections

Table 7-3 below lists the connections of the application header, JA5.

Pin	Header Name / Circuit Net Name	MCU Pin	Pin	Header Name / Circuit Net Name	MCU Pin
	Application Header JA5				
1	ADC4 / ANI4	37	2	ADC5 / ANI5	36
3	ADC6 / ANI6	35	4	ADC7 / ANI7	34
5	CAN1TX / NC	NC	6	CAN1RX / NC	NC
7	CAN2TX / NC	NC	8	CAN2RX / NC	NC
9	IRQ4/M2_EncZ/M2_HSIN1 / NC/NC/NC	NC/NC/NC	10	IRQ5/M2_HSIN2 / NC/NC	NC/NC
11	M2_UD / NC	NC	12	M2_Uin / NC	NC
13	M2_Vin / NC	NC	14	M2_Win / NC	NC
15	M2_Toggle / NC	NC	16	M2_POE / NC	NC
17	M2_TRCCLK / NC	NC	18	M2_TRDCLK / NC	NC
19	M2_UP / NC	NC	20	M2_UN / NC	NC
21	M2_VP / NC	NC	22	M2_VN / NC	NC
23	M2_WP / NC	NC	24	M2_WN / NC	NC

Table 7-3: Application Header JA5 Connections

Table 7-4 below lists the connections of the application header, JA6.

Pin	Header Name	MCU Pin	Pin	Header Name	MCU Pin
	Circuit Net Name			Circuit Net Name	
1	DREQ	NC	2	DACK	NC
	NC			NC	
3	TEND	NC	4	STBYn	NC
	NC			NC	
5	RS232TX	NC	6	RS232RX	NC
	RS232TX			RS232RX	
7	SCIbRX	42	8	SCIbTX	43
	RxD1			TxD1	
9	SCIcTX	NC	10	SCIbCK	NC
	NC			NC	
11	SCIcCK	NC	12	SCIcRX	NC
	NC			NC	
13	M1_Toggle	25	14	M1_Uin	NC
	TRDIOC0			NC	
15	M1_Vin	NC	16	M1_Win	NC
	NC			NC	
17	Reserved	NC	18	Reserved	NC
	NC			NC	
19	Reserved	NC	20	CMP0P	43
	NC			CMP0P	
21	Reserved	NC	22	CMP1P	44
	NC			CMP1P	
23	Unregulated_VDD	-	24	Vss	-
	Unregulated_VDD			GROUND	

Table 7-4: Application Header JA6 Connections

7.2   Microcontroller Pin Headers

This RSK is fitted with MCU pin headers, which are used to access all the MCU's pins.
Table 7-5 below lists the connections of the microcontroller pin header, J1.

Microcontroller Pin Header J1					
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name	MCU Pin
1	LED0	1	2	TOOL0	2
3	RESETn	3	4	SW2	4
5	SW3	5	6	P-INTP0_A-INTP0	6
7	CON_EXCLK	7	8	CON_X1	8
9	NC	-	10	GROUND	10
11	UC_VDD	11	12	NC	NC
13	NC	NC	14	NC	NC
15	NC	NC	16	NC	NC
17	NC	NC	18	NC	NC
19	NC	NC	20	NC	NC
21	NC	NC	22	NC	NC
23	NC	NC	24	NC	NC
25	NC	NC	26	NC	NC
27	NC	NC	28	NC	NC
29	NC	NC	30	NC	NC
31	NC	NC	32	NC	NC
33	NC	NC	34	NC	NC
35	NC	NC	36	NC	NC

Table 7-5: Microcontroller Pin Header, J1

Table 7-6 below lists the connections of the microcontroller pin header, J2.

Microcontroller Pin Header J2					
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name	MCU Pin
1	P60_IO0	12	2	P61_IO1	13
3	P62_IO2_M1UD	14	4	LED1_IO3	15
5	P-INTP4_A-INTP4_TO03	16	6	LED3_IO7	17
7	LED2_IO6	18	8	P71_IO5	19
9	SW1_IO4	20	10	SCL00_P-SCK00_A-SCK00_INTP3	21
11	SDA00_P-SI00_RxD0_A-SI00_RxD0_INTP1	22	12	NC	NC
13	NC	NC	14	NC	NC
15	NC	NC	16	NC	NC
17	NC	NC	18	NC	NC
19	NC	NC	20	NC	NC
21	NC	NC	22	NC	NC
23	NC	NC	24	NC	NC
25	NC	NC	26	NC	NC
27	NC	NC	28	NC	NC
29	NC	NC	30	NC	NC
31	NC	NC	32	NC	NC
33	NC	NC	34	NC	NC
35	NC	NC	36	NC	NC

Table 7-6: Microcontroller Pin Header, J2

Table 7-7 below lists the connections of the microcontroller pin header, J3.

Microcontroller Pin Header J3					
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name	MCU Pin
1	P-SO00_TxD0_A-SO00_TxD0	23	2	P17_TI02	24
3	P-INTP5_A-INTP5_TRDIOC0	25	4	TRDIOB0	26
5	TRDIOD0	27	6	TRDIOA1	28
7	TRDIOB1	29	8	TRDIOC1	30
9	TRDIOD1	31	10	RL78G1C_CTS_P146	32
11	RL78G1C_RTS_P147	33	12	NC	NC
13	NC	NC	14	NC	NC
15	NC	NC	16	NC	NC
17	NC	NC	18	NC	NC
19	NC	NC	20	NC	NC
21	NC	NC	22	NC	NC
23	NC	NC	24	NC	NC
25	NC	NC	26	NC	NC
27	NC	NC	28	NC	NC
29	NC	NC	30	NC	NC
31	NC	NC	32	NC	NC
33	NC	NC	34	NC	NC
35	NC	NC	36	NC	NC

Table 7-7: Microcontroller Pin Header, J3

Table 7-8 below lists the connections of the microcontroller pin header, J4.

Microcontroller Pin Header J4					
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name	MCU Pin
1	P27_ANI7	34	2	ANI6	35
3	ANI5	36	4	ANI4	37
5	ANI3	38	6	ANI2	39
7	ANI1_AVREFM	40	8	ANI0_AVREFP	41
9	TO00_RxD1_PGA	42	10	TI00_TxD1_CMP0P	43
11	CMP1P	44	12	NC	NC
13	NC	NC	14	NC	NC
15	NC	NC	16	NC	NC
17	NC	NC	18	NC	NC
19	NC	NC	20	NC	NC
21	NC	NC	22	NC	NC
23	NC	NC	24	NC	NC
25	NC	NC	26	NC	NC
27	NC	NC	28	NC	NC
29	NC	NC	30	NC	NC
31	NC	NC	32	NC	NC
33	NC	NC	34	NC	NC
35	NC	NC	36	NC	NC

Table 7-8: Microcontroller Pin Header, J4

8.   Code Development

8.1   Overview

For all code debugging using Renesas software tools, the RSK board must be connected to a PC via an E1/E20 debugger. An E1 debugger is supplied with this RSK product.

For further information regarding the debugging capabilities of the E1/E20 debuggers, refer to E1/E20 Emulator Additional Document for User's Manual (R20UT1994EJ).

8.2   Compiler Restrictions

The compiler supplied with this RSK will build a maximum of 64k code and data. To use the compiler with programs greater than this size you need to purchase a compiler license from your Renesas supplier.

8.3   Mode Support

The RL78/G1G microcontroller only supports single-chip operating mode.

8.4   Debugging Support

The E1 emulator (as supplied with this RSK) supports hardware break points, software break points and basic trace functionality. For further details, refer to the E1/E20 Emulator User's Manual (R20UT0398EJ).

8.5   Address Space

For the MCU address space details, refer to the 'Memory Space' section of RL78/G1G Group Hardware Manual.

9. Additional Information

Technical Support
For information about the RL78/G1G Group microcontrollers refer to the RL78/G1G Group Hardware Manual.

For information about the RL78 assembly language, refer to the RL78 Family Software Manual.

Technical Contact Details

Please refer to the contact details listed in section 9 of the "Quick Start Guide"

General information on Renesas Microcontrollers can be found on the Renesas website at:
http://www.renesas.com/

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