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# RL78/L1C Group

Renesas Starter Kit User's Manual For CubeSuite+

RENESAS MCU RL78 Family / L1X Series

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This Renesas Starter Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever
  possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

# How to Use This Manual

### 1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the RSK hardware functionality, and electrical characteristics. It is intended for users designing sample code on the RSK platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK product, but does not intend to be a guide to embedded programming or hardware design. Further details regarding setting up the RSK and development environment can found in the tutorial manual.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RL78/L1C Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK hardware.	RSKRL78L1C User's Manual	R20UT2203EG
Tutorial	Provides a guide to setting up RSK environment, running sample code and debugging programs.	RSKRL78L1C Tutorial Manual	R20UT2204EG
Quick Start Guide	Provides simple instructions to setup the RSK and run the first sample.	RSKRL78L1C Quick Start Guide	R20UT2205EG
Code Generator Tutorial	Provides a guide to code generation and importing into the CubeSuite+ IDE.	RSKRL78L1C Code Generator Tutorial Manual	R20UT2887EG
Schematics	Full detail circuit schematics of the RSK.	RSKRL78L1C Schematics	R20UT2202EG
Hardware Manual	Provides technical details of the RL78/L1C microcontroller.	RL78/L1C Group Hardware Manual	R01UH0409EJ

# 2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
E1	On-chip Debugger
ESD	Electrostatic Discharge
IIC	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
EMC	Electromagnetic Compatibility
LCD	Liquid Crystal Display
LED	Light Emitting Diode
EMC	Electromagnetic Compatibility
MCU	Micro-controller Unit
n/a or NA	Not applicable
n/c or NC	Not connected
PC	Personal Computer
RSK	Renesas Starter Kit
SAU	Serial Array Unit
TAU	Timer Array Unit
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

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# RENESAS

### RSKRL78L1C

**RENESAS STARTER KIT** 

### 1.1 Purpose

This RSK is an evaluation tool for Renesas microcontrollers. This manual describes the technical details of the RSK hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

### 1.2 Features

This RSK provides an evaluation of the following features:

- Renesas microcontroller programming
- User code debugging
- User circuitry such as switches, LEDs and a potentiometer
- Sample application
- Sample peripheral device initialisation code

The RSK board contains all the circuitry required for microcontroller operation.



# 2. Power Supply

### 2.1 Requirements

This RSK is supplied with an E1 debugger. The debugger is able to power the RSK board with up to 200mA. When the RSK is connected to another system then that system should supply power to the RSK. This board has an optional centre positive supply connector using a 2.0mm barrel power jack.

Details of the external power supply requirements for the RSK, and configuration are shown in **Table 2-1** below. The default RSK power configuration is shown in **bold**, **blue text**.

J6 Setting	J7 Setting	J8 Setting	Supply Type	Board_VDD
Pin2-3 shorted	Pin2-3 shorted	All open	PWR, VBUS, CON_5V	3.3V
Pin1-2 shorted	Pin1-2 shorted	Don't care	E1(3.3V), CON_3V3	3.3V
Pin2-3 shorted	Pin2-3 shorted	Pin1-2 shorted	PWR, VBUS, CON_5V	1.8V
Pin2-3 shorted	Pin2-3 shorted	Pin2-3 shorted	PWR, VBUS, CON_5V	1.62V
All open	All open	All open	DO NOT SET	

#### Table 2-1: Main Power Supply Requirements

The main power supply connected to PWR1 should supply a minimum of 5W to ensure full functionality.

### 2.2 Power-Up Behaviour

When the RSK is purchased, the RSK board has the 'Release' or stand-alone code from the example tutorial software pre-programmed into the Renesas microcontroller. On powering up the board the LCD panel will show 'RL78' in the bottom left and will respond to SW3 switch presses by performing an A/D conversion and displaying the result in the main part of the LCD panel.



# 3. Board Layout

### 3.1 Component Layout

Figure 3-1 below shows the top component layout of the board.

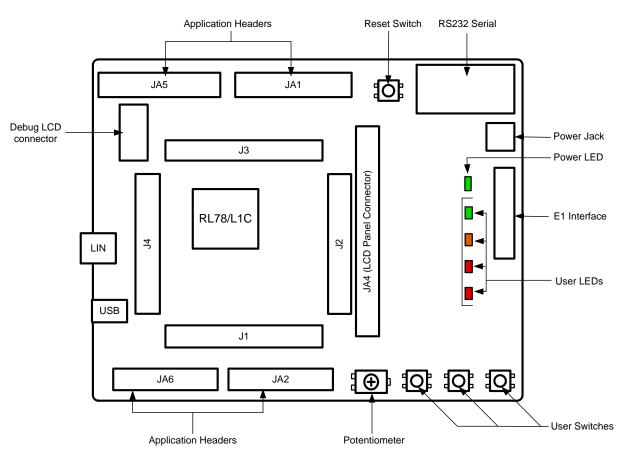


Figure 3-1: Board Layout



### 3.2 Board Dimensions

**Figure 3-2** below gives the board dimensions and connector positions. All the through-hole connectors are on a common 0.1 inch grid for easy interfacing.

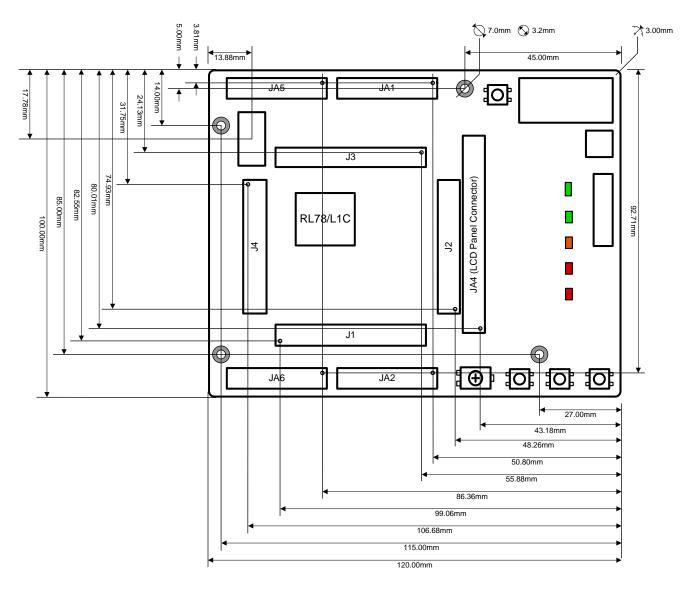


Figure 3-2: Board Dimensions



### 3.3 Component Placement

**Figure 3-3** below shows placement of individual components on the top-side PCB. Component types and values can be looked up using the board schematics.

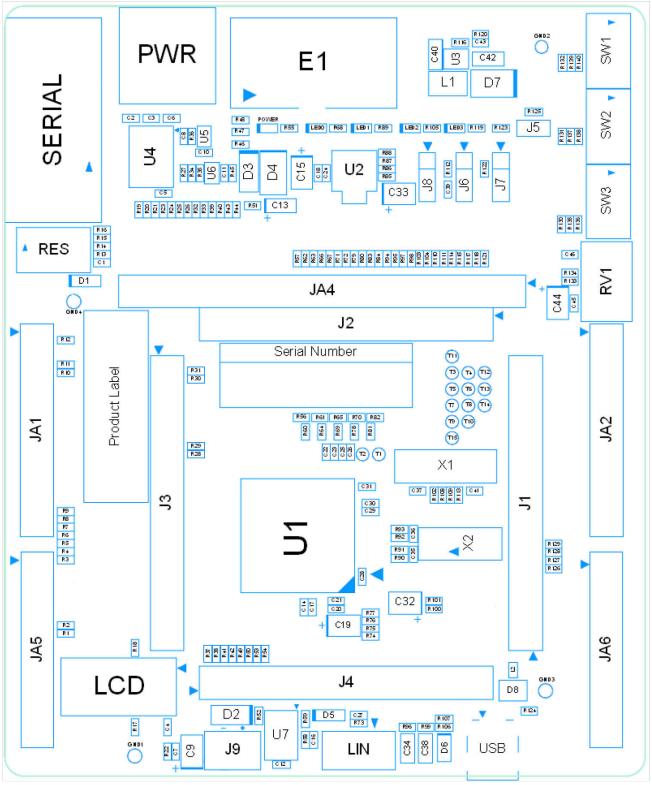


Figure 3-3: Top-Side Component Placement



# 4. Connectivity

### 4.1 Internal RSK Connections

The diagram below shows the RSK board components and their connectivity to the MCU.

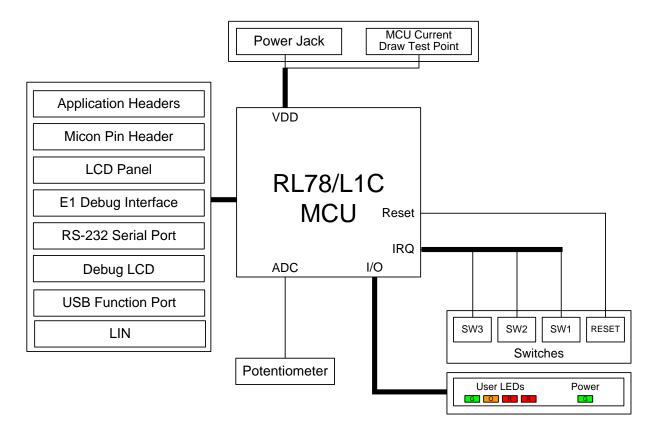
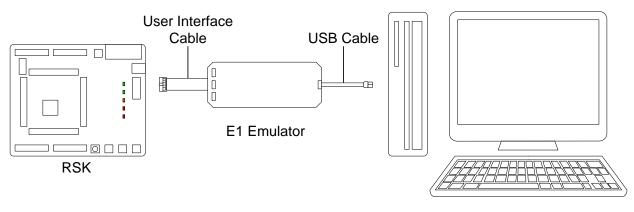


Figure 4-1: Internal RSK Block Diagram



## 4.2 Debugger Connections

The diagram below shows the connections between the RSK, E1 debugger and the host PC.



Host PC

Figure 4-2: Debugger Connection Diagram



# 5. User Circuitry

### 5.1 Reset Circuit

A reset control circuit is not fitted to the RSK, as the MCU is capable of voltage and power-on detection. Resets are handled internally, and the reset switch is connected directly to the RESET pin on the MCU (pin 13).

### 5.2 Clock Circuit

A clock circuit is fitted to the RSK to generate the required clock signal to drive the MCU, and associated peripherals. Refer to the RL78/L1C Group Hardware Manual for details regarding the clock signal requirements, and the RSKRL78L1C board schematics for information regarding the clock circuitry in use on the RSK. Details of the oscillators fitted to the board are listed in **Table 5-1** below.

Crystal	Function	Default Placement	Frequency	Device Package
X1	Main MCU oscillator.	Fitted	12MHz	Encapsulated, SMT
X2	Sub MCU oscillator	Fitted	32.768kHz	Encapsulated, SMT

### 5.3 Switches

There are four switches located on the RSK board. The function of each switch and its connection is shown in **Table 5-2**. For further information regarding switch connectivity, refer to the RSK schematics.

Switch Function	Eurotion	MCU		
	Port	Pin		
RES	When pressed, the microcontroller is reset.	RESETn	13	
SW1	Connects to an IRQ input for user controls.	INTP0 (P137)	16	
SW2	Connects to an IRQ input for user controls.	INTP1 (P03)	66	
SW3	Connects to an IRQ input for user controls.	INTP2 (P04)	65	

#### Table 5-2: Switch Connections



### 5.4 LEDs

There are five LEDs on the RSK. The function of each LED, its colour, and its connections are shown in **Table 5-3**.

LED Co	Colour	Function	MCU		
	Colour	Function	Port	Pin	
POWER	Green	Indicates the power status	NC	-	
LED0	Green	User operated LED.	P05	64	
LED1	Orange	User operated LED.	P07	62	
LED2	Red	User operated LED.	P41	11	
LED3	Red	User operated LED.	P42	10	

#### Table 5-3: LED Connections

### 5.5 Potentiometer

A single-turn potentiometer is connected as a potential divider to analog input ANI0, pin 4. The potentiometer can be used to create a voltage between Board\_VDD and ground.

The potentiometer is fitted to offer an easy method of supplying a variable analog input to the microcontroller. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the RL78/L1C Group Hardware Manual for further details.



### 5.6 LCD Panel

A versatile LCD display panel is supplied with the RSK, and should be connected to the JA4 header. The panel is directly driven by circuitry inside the MCU. Connection information for the LCD panel is provided in table **Table 5-4** below.

	LCD Panel Header (JA4)							
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name	MCU Pin			
1	VL4	VL4, Pin 28	2	VL3	VL3, Pin 29			
3	VL2	VL2, Pin 27	4	VL1	VL1, Pin 26			
5	Ground	-	6	Ground	-			
7	COM0	COM0, Pin 61	8	COM1	COM1, Pin 60			
9	COM2	COM2, Pin 59	10	COM3	COM3, Pin 58			
11	SEG0	SEG0, Pin 57	12	SEG1	SEG1, Pin 56			
13	SEG2	SEG2, Pin 55	14	SEG3	SEG3, Pin 54			
15	SEG4	SEG4, Pin 53	16	SEG5	SEG5, Pin 52			
17	SEG6	SEG6, Pin 51	18	SEG7	SEG7, Pin 50			
19	SEG8	SEG8, Pin 49	20	SEG9	SEG9, Pin 48			
21	SEG10	SEG10, Pin 47	22	SEG11	SEG11, Pin 46			
23	SEG12	SEG12, Pin 45	24	SEG13	SEG13, Pin 44			
25	SEG14	SEG14, Pin 43	26	SEG15	SEG15, Pin 42			
27	SEG16	SEG16, Pin 41	28	SEG17	SEG17, Pin 40			
29	SEG18	SEG18, Pin 39	30	SEG19	SEG19, Pin38			
31	SEG20	SEG20, Pin 37	32	SEG21	SEG21, Pin 36			
33	SEG22	SEG22, Pin 35	34	SEG23	SEG23, Pin 34			
35	SEG24	SEG24, Pin 33	36	SEG25	SEG25, Pin 32			
37	SEG26	SEG26, Pin 31	38	SEG27	SEG27, Pin 30			
39	SEG32	SEG32, Pin 85	40	SEG33	SEG33, Pin 84			
41	SEG34	SEG34, Pin 83	42	SEG35	SEG35, Pin 82			
43	SEG40	SEG40, Pin 77	44	SEG41	SEG41, Pin 76			
45	SEG42	SEG42, Pin 75	46	SEG43	SEG43, Pin 74			
47	DLCDD4_SEG44	SEG44, Pin 73	48	DLCDD5_SEG45	SEG45, Pin 72			
49	DLCDD6_SEG46	SEG46, Pin 71	50	DLCDD7_SEG47	SEG47, Pin 70			

Table 5-4: LCD Header Connections



### 5.7 Debug LCD Module

A debug LCD header is fitted to the RSK; however the two-line debug LCD is not supplied with this kit. It is not possible to use the debug LCD and the LCD panel at the same time, and they should not both be fitted to the RSK.

Care should be taken when installing the LCD module to ensure pins are not bent or damaged. The LCD module is vulnerable to electrostatic discharge (ESD); therefore appropriate ESD protection should be used.

The debug LCD module uses a 4-bit interface to reduce pin allocation. Connection information for the debug LCD module is provided in **Table 5-5** below.

Debug LCD Header							
Pin Circuit Net Nam	Circuit Net Name	MCU	CU	J	Circuit Net Name	MCU	
Pin	Circuit Net Name	Port	Pin	- Pin	Circuit Net Name	Port	Pin
1	GROUND	-	-	2	Board_5V	-	-
3	No Connection	-	-	4	DLCDRS	P44	8
5	R/W (pulled to ground)	-	-	6	DLCDE (pulled to ground)	P130	5
7	No Connection	-	-	8	No Connection	-	-
9	No Connection	-	-	10	No Connection	-	-
11	DLCDD4_SEG44	P14	73	12	DLCDD5_SEG45	P15	72
13	DLCDD6_SEG46	P16	71	14	DLCDD7_SEG47	P17	70

 Table 5-5: LCD Header Connections

### 5.8 RS232 Serial Port

An RS232 serial port is fitted to the RSK and connected via a level shifter to the microcontroller Serial Array Unit (SAU). Connections between the RS232 header and the microcontroller are listed in **Table 5-6** below.

Signal Name	Function	MCU		RS232 Connector
Signal Name	Function	Signal	Pin	Pin
SO10_TXD1	SAU UART1 Transmit Signal.	TXD1	67	Pin 2
SI10_RXD1	SAU UART1 Receive Signal	RXD1	68	Pin 3
SO00_TXD0	SAU UART0 Transmit Signal.	TXD0	79	Pin 2*
SI00_RXD0	SAU UART0 Receive Signal	RXD0	80	Pin 3*
SO30_TXD3	SAU UART3 Transmit Signal.	TXD3	32	Pin 2*
SI30_RXD3	SAU UART3 Receive Signal.	RXD3	33	Pin 3*
RS232TX	External SCI Transmit Signal.	n/a	-	Pin 2*
RS232RX	External SCI Receive Signal.	n/a	-	Pin 3*

### Table 5-6: Serial Port Connections

\* This connection is a not available in the default RSK configuration - refer to §6.2 for the required modifications.



### 5.9 Local Interconnect Network (LIN)

A LIN transceiver IC is fitted to the RSK, and connected to the LIN MCU peripheral. For further details regarding the LIN protocol and supported modes of operation, please refer to the RL78/L1C hardware manual. Connections between the LIN connector and the microcontroller are listed in **Table 5-7** below.

LIN Signal	Function		CU
LIN Signal	Function	Port	Pin
LINTXD	LIN Transmit Signal	P26	79
LINRXD	LIN Receive Signal	P25	80
LINNSLP	LIN Transceiver Device Sleep Control	P24	81

Table 5-7: LIN Connections

### 5.10 USB Function

A USB 2.0 function controller is contained within the MCU. Connections between the USB connector and the microcontroller are listed in **Table 5-8** below.

USB Signal	Function	MCU		
	Function	Port	Pin	
UVBUS	Cable monitor pin.	UVBUS	93	
UDP	Positive differential data signal.	UDP	95	
UDM	Negative differential data signal.	UDM	94	

Table 5-8: USB Connections



# 6. Configuration

### 6.1 Modifying the RSK

This section lists the option links that are used to modify the way RSK operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers.

Table 6-1 below shows the RSKRL78L1C default configuration with respect to the peripheral functionality. **Bold, blue text** indicates the default configuration that the RSK is supplied with. It is noted that certain peripheral functions are disabled by default, as shown in Table 6.1 in the column entitled **Secondary Function**. It is possible to activate these disabled peripherals, but at the expense of the default peripheral functions as shown in the Table. Refer to the sections cited in the Table in order to perform any required modifications.

The following sub-sections contain Tables illustrating which link resistors need to added/removed to enable/disable specific functions. A single horizontal line in the Table traces an individual signal path from the MCU on the left of the Table, through any intermediate connections, to any header connections on the right side of the Table. Each line in the Table thereby shows how the MCU signal can be configured for each of its multiplexed functions. Default RSK functional configurations are shown in **bold**, **blue text**.

A link resistor is a  $0\Omega$  surface mount resistor, which is used to short or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. Refer to the component placement diagram (§3.3) to locate the option links and jumpers.

When removing soldered components, always ensure that the RSK is not exposed to a soldering iron for intervals greater than 5 seconds. This is to avoid damage to nearby components mounted on the board.

When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MCU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to the RL78/L1C Group Hardware Manual and RSKRL78L1C schematics for further information.

Primary Function	See §	Secondary Function	See §	Tertiary Function	See §
RS232 with UART1	6.2	RS232 with UART0/3	6.2	E1 Debugger	6.3
LIN	6.2	Serial comms with SAU00	6.2	N/A	
	6.10				
LCD Panel	6.4	UART3/INTP6/IO	6.4	N/A	
LED1, LED2, LED3	6.5	TAU0	6.5	N/A	
IIC	6.6	N/A		N/A	
On board Crystals	6.8	External clocks supplied	6.8	N/A	

Table 6-1: RSK Default Configuration by Function



### 6.2 RS232 Serial Port Configuration

Table 6-2 below details the function of the option links associated with the serial port configuration.

Signal Name	MC	U	Exc	lusive fur	nction		Heade	r connec	tion
	Port	Pin	Signal	IC Pin	ΕĬ	Remove	Header Pin	Ť	Remove
SHDn	_	_	SHD GND	U4.20	R34	-	-	-	-
311011	-	_	n/c	-	-	R34	-	-	-
SO10_TXD1	P02	67	RS232 out to TXD1 SO10_TXD1	U4.13 -	R26 R20	R23 R24 R25 R19	JA6.8	Direct	Direct
SI10_RXD1	P01	68	RS232 in to RXD1 SI10_RXD1	U4.15 -	R44 R33	R39 R40 R43 R32	JA6.7	Direct	Direct
			LINTXD	U7.4	R38	R41	LIN.2	-	-
			SO00_TXD0	-	-	-	JA2.6	R41	R38
LINTXD_SO00_TXD0	P26	79	RS232 out to SO00_TXD0	U4.13	R41 R23 <b>R20</b>	R38 R24 R25 R26 R19	-	-	-
			LINRXD	U7.1	R53	<b>R50</b>	LIN.2	-	-
LINRXD_SI00_RXD0	P25	80	SI00_RXD0 RS232 in to SI00_RXD0	- U4.15	- R50 R40 <b>R33</b>	- R53 <b>R39</b> R43 R44 <b>R32</b>	JA2.8 -	R50 -	R53 -
			LINNSLP	U7.2	R42	R49	-	-	-
LINNSLP_SCK00	P24	81	SCK00	-	-	-	JA2.10	R49	R42
			<b>SEG25</b> SO30_TXD3	-	-	-	JA4.36 JA6.9	<b>R118</b> R121	R121 R118
SEG25_SO30_TXD3 P35	32	RS232 out to SO30_TXD3	U4.13	R121 R25 <b>R20</b>	R118 <b>R23</b> R24 R26 <b>R19</b>	-	-	-	
			SEG24	-	-	-	JA4.35	R115	R117
			SI30_RXD3	-	-	-	JA6.12	R117	R115
SEG24_SI30_RXD3 P34	P34	33	RS232 in to SI30_RXD3	U4.15	R39 R117 <b>R33</b>	R115 <b>R40</b> R43 R44 <b>R32</b>	-	-	-
	Daa		SEG23	-	-	-	JA4.34	R111	R114
SEG23_SCK30	P33	34	SCK30	-	-	-	JA6.11	R114	R111
L	•	Table	6-2: RS232 Se		Ontion I	inko		•	

Table 6-2: RS232 Serial Port Option Links



Signal Name	MC	U	Exc	Exclusive function				Header connection		
	Port	Pin	Signal	IC Pin	ĿĬ	Remove	Header Pin	Ξ	Remove	
RS232TX	-	-	RS232 out to RS232TXD	U4.13	R24 <b>R20</b>	R23 R25 R26 R19	JA6.5	-	-	
RS232RX	-	-	RS232 in to RS232RX	U4.15	R43 <b>R33</b>	<b>R39</b> <b>R40</b> R44 <b>R32</b>	JA6.6	-	-	

Table 6-2: RS232 Serial Port Option Links (continuation)

### 6.3 E1 Debugger Interface

**Table 6-3** below details the function of the option links associated with E1 Debugger configuration. The default configuration is for E1 debug/programming, but it is possible to enable Flash programming via the COM port.

Signal Name	MC	U	Exclusi	Exclusive function					ection		
	Port	MCU Pin	Signal	IC Pin	Fit	Remove	Header Pin	Fit	Remove		
RESETn		13	T_RESETn to RESETn	-	-	-	E1.6	R14	-		
RESETT	<b>KESEIN</b> - 13	13	13	n/c	-	-	-	-	-	R14	
RESETn		10	R2IN to RESETn	U5.4	R36	-	-	-	-		
RESEIII	- 13	- 13	- 13	- 13	n/c	-	-	R36	-	-	-
TOOL0	P40	10	T1OUT to TOOL0	U4.13	R19	R20	-	-	-		
	12	RS232 as UART (§6.2)	-	R20	R19	-	-	-			
TOOL0	D40	10	R1IN to TOOL0	U4.15	R32	R33	-	-	-		
TOOLU	P40	40 12	RS232 as UART (§6.2)	-	R33	R32	-	-	-		

Table 6-3: E1 Debugger Interface Option Links



## 6.4 LCD Panel Configuration

Signal Name	M	CU		Header c	onnection	
	Port	Pin	Signal	Header Pin	Fit	Remove
SEG20 REMOOUT	P30	37	SEG20	JA4.31	R104	R110
		0.	REMOOUT	JA2.19	R110	R104
SEG23 SCK30	P33	34	SEG23	JA4.34	R111	R114
02020_00000	1.00	01	SCK30	JA6.11	R114	R111
SEG24 SI30 RXD3	P34	33	SEG24	JA4.35	R115	R117
	104	00	SI30_RXD3	JA6.12	R117	R115
SEG25 SO30 TXD3	P35	32	SEG25	JA4.36	R118	R121
02023_0030_1703	F 33	32	SO30_TXD3	JA6.9	R121	R118
SEG4 INTP6	P50	53	SEG4	JA4.15	R30	R31
3234_11176	F 30	55	INTP6	JA5.9	R31	R30
IO0 SEG12	P70	45	IO0	JA1.15	R57	R62
100_32012			SEG12	JA4.23	R62	R57
IO1 SEG13	P71	44	IO1	JA1.16	R63	R66
101_32013		44	SEG13	JA4.24	R66	R63
IO2 SEG14	P72	10	102	JA1.17	R67	R71
102_32014	F1Z	43	SEG14	JA4.25	R71	R67
IO3 SEG15	P73	42	IO3	JA1.18	R72	R79
103_32013	F13	42	SEG15	JA4.26	R79	R72
IO4 SEG16	P74	41	IO4	JA1.19	R80	R83
104_36010	F/4	41	SEG16	JA4.27	R83	R80
IO5 SEG17	P75	40	IO5	JA1.20	R84	R94
105_32017	F73	40	SEG17	JA4.28	R94	R84
IO6 SEG18	P76	39	IO6	JA1.21	R98	R103
100_36010	F/0	39	SEG18	JA4.29	R103	R98
IO7 SEG19	P77	38	107	JA1.22	R95	R97
107_32019	F//	30	SEG19	JA4.30	R97	R95

 Table 6-4 below details the function of the option links associated with the LCD Panel header.

Table 6-4: LCD Panel Option Links

### 6.5 LED/Timer Pin Configuration

**Table 6-5** below details the function of the option links associated with LED pin configuration.

Signal Name	M	CU	Header connection				
	Port	Pin	Signal	Header Pin	Fit	Remove	
	DOZ	60	LED1	-	R29	R28	
LED1_TO06	P07	62	TO06	JA2.20	R28	R29	
	P41	11	LED2	-	R129	R128	
LED2_TI07	P41	11	TI07	JA2.22	R128	R129	
	P42	10	LED3	-	R127	R126	
LED3_TI05	P42		TI05	JA2.21	R126	R127	

Table 6-5: LED/Timer Pin Option Links
---------------------------------------

### 6.6 **IIC Pin Configuration**

Table 6-6 below details the function of the option links associated with IIC pin configuration.

Signal Name	MCU		Header connection			
	Port	Pin	Signal	Header Pin	Fit	Remove
			Board_VDD	-	R5	R6
IIC Pull up	-		Board_5V	-	R6	R5

Table 6-6: IIC Option Links

### 6.7 Power Supply Configuration

**Table 6-7** below details the function of the option links associated with power supply configuration.

Signal	Exclusive function		Heade	Header connection			
Name	Function	IC Pin	Header Pin	Fit	Remove		
Board 5V	Supply power through PWR connector	U2.IN	-	R48	-		
Board_5V	Do not supply power through PWR connector	02.IN	-	-	R48		
Board 51/	Supply power through VBUS connection		-	R51 R107	-		
Board_5V	Do not supply power through VBUS connection	U2.IN	-	-	R51 R107		
Board_5V	Connected to CON_5V	U2.IN	JA1.1	R47	-		
Board_5V	Not connected to CON_5V	02.11	-	-	R47		
Board_5V	Connected to Unregulated_VDD	U2.IN	JA6.23	R46	-		
Board_5V	Not connected to Unregulated_VDD	02.11	-	-	R46		
Board 5V	Board_5V hardwired to U3 regulator output <sup>1</sup>	U3.1	-	R122	-		
Board_5V	Board_5V not hardwired to U3 regulator output <sup>1</sup>	03.1	-	-	R122		
Board_VDD	Supply power through CON_3V3	-	JA1.3	R12	-		
	Do not supply power through CON_3V3	-	-	-	R12		
Board_VDD	Board_VDD hardwired to U3 regulator input <sup>1</sup>	U3.VIN	-	R112	-		
	Board_VDD not hardwired to U3 regulator input <sup>1</sup>	-	-	-	R112		
	Bypass current probe (J5) for MCU	U1.21	J1.21	R125	-		
Board_VDD		U1.90	J4.15				
Noto	Enable current probe(J5) for MCU	-	-	-	R125		

Note:

1. Alternatively, use J6 and J7 as detailed in **Table 2-1** in §2.1.

Table 6-7: Power Supply Option Links



## 6.8 Clock Circuit Configuration

MCU		Header connection					
Port	Pin	Connection	Header Pin	Fit	Remove		
D101	10	On board X1.2	-	R102	R108		
PIZI	18	External CON_X1	J1.18	R108	R102		
D100	D100	17	On board X1.1	-	R113	R109	
PIZZ	17	External CON_X2	J1.17, JA2.2	R109	R113		
D102	15	On board X2.4	-	R92	R93		
P123	15	External CON_XT1	J1.15	R93	R92		
D104	14	On board X2.1	-	R91	R90		
F124	14	External CON_XT2	J1.14	R90	R91		
		Port         Pin           P121         18           P122         17           P123         15	PortPinConnectionP12118On board X1.2P12217External CON_X1P12217On board X1.1External CON_X2On board X2.4P12315On board X2.4P12414On board X2.1	Port         Pin         Connection         Header Pin           P121         18         On board X1.2         -           P121         18         External CON_X1         J1.18           P122         17         On board X1.1         -           External CON_X2         J1.17, JA2.2            P123         15         On board X2.4         -           P124         14         On board X2.1         -	Port         Pin         Connection         Header Pin         Fit           P121         18         On board X1.2         -         R102           External CON_X1         J1.18         R108           P122         17         On board X1.1         -         R113           P123         15         On board X2.4         -         R92           P124         14         On board X2.1         -         R93		

**Table 6-8** below details the function of the option links associated with clock circuit.

Table 6-8: Clock Circuit Option Links

### 6.9 ADC Configuration

**Table 6-9** below details the function of the option links associated with the ADC circuit.

Signal Name	М	CU	Header connection						
	Port	Pin	Signal	Header Pin	Fit	Remove			
		00	UC_VDD	-	R75	R74			
AVDD -	98	CON_AVDD	JA1.5	R74	R75				
	AVSS -		GROUND	-	R76	R77			
AVSS		-	-	99	CON_AVSS	JA1.6	R77	R76	
					R11	R10			
ADPOT AVREFP	P150	4	ADPOT	-	R101	R100			
ADPUI_AVREFP	P 150	4	AVPREF	JA1.7	R100	R101			
ADPOT			RV1 Supply Board_VDD	-	R134	R133			
ADPUT	-	-	RV1 Supply CON_AVDD	JA1.5	R133	R134			
AVREFM	P151	3	JA1.6 connected to CON_AVSS	JA1.6	R11	R10			
AVREFIN	FISI	3	JA1.6 connected to AVREFM	JA1.6	R10	R11			

Table 6-9: ADC Option Links

### 6.10 LIN Configuration

Table 6-10 below details the function of the option links associated with the LIN Transceiver.

Signal	Exclusive function		Head	er connec	ction
Name	Name In L L Name		Header Pin	Ĭ	Remove
	LIN line pulled up for master operation <sup>1</sup>	117.6		R58 R73	-
LIN	LIN line pulled down for slave operation <sup>1</sup>	U7.6	LIN.2		R58 R73

Note:

1. Remove one of these links before connecting 2 RSKs together.

Table 6-10: LIN Option Links`

# 7. Headers

### 7.1 Application Headers

This RSK is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MCU pins.

Note that JA4 has been omitted from this list as it is the LCD panel connector, and connections are described in §5.6

Application Header JA1					
Pin	Header Name	MCU Pin	Pin	Header Name	MCU Pin
Pin	Circuit Net Name		Pin	Circuit Net Name	
1	5V		2	0V	
1	CON_5V		2	GROUND	
3	3V3		4	0V	
3	CON_3V3	] -	4	GROUND	
5	AVDD	- 98*	6	AVSS	99*
5	CON_AVDD	- 90	0	JA1_PIN6	
7	AVREF	4*	8	ADTRG	NC
/	AVREFP	- 4	0	NC	
9	ADC0	- 2	10	ADC1	1
9	ANI2		10	ANI3	
11	ADC2	- 100	00 12	ADC3	97
11	ANI4			ANI5	- 97
13	DAC0	7	14	DAC1	6
13	ANO0	] /	14	ANO1	0
15	IO_0	45*	16	IO_1	44*
15	100	- 45	16	IO1	44
17	IO_2	- 43*	18	IO_3	42*
17	102	43	10	103	42
19	104	- 41*	20	IO_5	40*
19	IO_4	- 41	20	105	40
21	IO6	- 39*	22	IO_7	38*
21	IO_6	- 39	22	107	
23	IRQ3/IRQAEC/M2_HSIN0	63/NC/NC	24	IIC_EX	NC
23	INTP5		24	NC	
25	IIC_SDA	- 23	26	IIC_SCL	22
20	JA1_SDAA0	_ 23	26	JA1_SCLA0	

Table 7-1 below lists the connections of the application header, JA1.

Table 7-1: Application Header JA1 Connections

Application Header JA2				JA2		
Pin	Header Name	MOULDIN	Pin	Header Name	MOLLBin	
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name	MCU Pin	
1	RESET	- 13	2	EXTAL	17*	
1	RESETn	- 13	2	CON_X2	- 17	
3	NMI	NC	4	Vss1		
3	NC		4	GROUND		
5	WDT_OVF	NC	6	SCIaTX	79*	
5	NC		0	SO00_TXD0	- 79	
7	IRQ0/WKUP/M1_HSIN0	16/NC/NC	8	SCIaRX	80*	
1	INTP0	TO/INC/INC	0	SI00_RXD0	- 00	
•	IRQ1/M1_HSIN1	66/NC	10	SCIaCK	81*	
9	INTP1	- 66/NC	10	SCK00	- 81	
11	M1_UD	– NC	12	CTSRTS	NC	
11	NC		12	NC		
13	M1_UP	NC		14	M1_UN	NC
13	NC		14	NC		
15	M1_VP	NC	16	M1_VN	NC	
15	NC		10	NC		
17	M1_WP	NC	18	M1_WN	NC	
17	NC		10	NC		
19	TimerOut	37*	20	TimerOut	62*	
19	REMOOUT	- 37	20	NC	- 02	
21	TimerIn	- 10*	22	TimerIn	11*	
21	TI05		~~	NC		
23	IRQ2/M1_EncZ/M1_HSIN2	65/NC/NC	24	M1_POE	NC	
23	INTP2		24	NC		
25	M1_TRCCLK	NC	26	M1_TRDCLK	NC	
20	NC		20	NC		

Table 7-2 below lists the connections of the application header, JA2.

Table 7-2: Application Header JA2 Connections



	Application Header JA5					
Pin	Header Name	MCU Din	Pin	Header Name	MCU Pin	
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name		
	ADC4			ADC5		
1	ANI16	- 89	2	ANI17	88	
_	ADC6	07		ADC7		
3	ANI18	- 87	4	ANI19	- 86	
-	CAN1TX	NO	0	CAN1RX	NO	
5	NC	- NC	6	NC	- NC	
7	CAN2TX	NO		CAN2RX	N	
7	NC	- NC	8	NC	– NC	
	IRQ4/M2_EncZ/M2_HSN1	- 53*/NC/NC	4.0	IRQ5/M2_HSIN2	0/010	
9	INTP6		10	INTP7	9/NC	
	M2_UD	- NC		M2_Uin		
11	NC		12	NC	- NC	
40	M2_Vin			M2_Win	NIC	
13	NC	- NC	14	NC	- NC	
45	M2_UD	NO	10	M2_POE	NIC	
15	NC	- NC	16	NC	- NC	
47	M2_TRCCLK			40	M2_TRDCLK	NIC
17	NC	- NC	18	NC	- NC	
19	M2_UP	NC	20	M2_UN		
19	NC	- NC	20	NC	- NC	
24	M2_VP	NG	20	M2_VN	NC	
21	NC	- NC	22	NC	- NC	
00	M2_WP		0.1	M2_WIN		
23	NC	- NC	24	NC	— NC	

Table 7-3 below lists the connections of the application header, JA5.

Table 7-3: Application Header JA5 Connections



	Application Header JA6						
Pin	Header Name	MCU Pin	Pin	Header Name			
Pin	Circuit Net Name		Pin	Circuit Net Name	MCU Pin		
4	DREQ	NIC	0	DACK	NIC		
1	NC	- NC	2	NC	- NC		
0	TEND	NO		STBYn	NIC		
3	NC	- NC	4	NC	- NC		
~	RS232TX	NC	0	RS232RX	NC		
5	RS232TX		6	RS232RX	- NC		
7	SCIbRX	69	0	SCIbTX	67		
7	SI10_RXD1	- 68	8	SO10_TXD1	- 67		
0	SCIcTX	32*	2.2*	10	SCIbCK	60	
9	SO30_TXD3		10	SCK10	- 69		
11	SCIcCK	34*	12	SCIcRX	33*		
11	SCK30	34**	12	SI30_RXD3	33"		
13	M1_Toggle	NC	Toggle	oggle NC 14	14	M1_Uin	NC
13	NC		14	NC			
15	M1_Vin	NC	NC	16	M1_Win	NC	
15	NC		10	NC			
17	EXT_USB_VBUS	NC	18	Reserved	NC		
17	NC		10	NC			
19	EXT_USB_BATT	NC	20	Reserved	NC		
19	NC		20	NC			
21	EXT_USB_CHG	NC	22	Reserved	NC		
21	NC		~~~	NC			
23	Unregulated_VDD		24	Vss			
23	Unregulated_VDD		24	GROUND			

Table 7-4 below lists the connections of the application header, JA6.

Table 7-4: Application Header JA6 Connections



### 7.2 Microcontroller Pin Headers

This RSK is fitted with MCU pin headers, which are used to access all the MCU's pins.

	Microcontroller Pin Header J1				
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name	MCU Pin
1	ANI3	1	2	ANI2	2
3	AVREFM	3	4	ADPOT_AVREFP	4
5	DLCDE	5	6	ANO1	6
7	ANO0	7	8	DLCDRS	8
9	INTP7	9	10	LED3_TIO5	10
11	LED2_TIO7	11	12	TOOL0	12
13	RESETn	13	14	CON_XT2	14*
15	CON_XT1	15*	16	INTP0	16
17	CON_X2	17*	18	CON_X1	18*
19	NC	-	20	GROUND	-
21	UC_VDD	21, 90	22	SCLA0	22
23	SDAA0	23	24	CAPH	24
25	CAPL	25	26	NC	-
27	NC	-	28	NC	-
29	NC	-	30	NC	-
31	NC	-	32	NC	-
33	NC	-	34	NC	-
35	NC	-	36	NC	-

**Table 7-5** below lists the connections of the microcontroller pin header, J1.

#### Table 7-5: Microcontroller Pin Header, J1

\* Note: Not a default connection to an MCU pin- requires modification of zero ohm links - refer to schematic.

Table 7-6 below lists the connections of the microcontroller pin header, J2.

	Microcontroller Pin Header J2				
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name	MCU Pin
1	VL1	26	2	VL2	27
3	VL4	28	4	VL3	29
5	SEG27	30	6	SEG26	31
7	SEG25_SO30_TXD3	32	8	SEG24_SI30_RXD3	33
9	SEG23_SCK30	34	10	SEG22	35
11	SEG21	36	12	SEG20_REMOOUT	37
13	IO7_SEG19	38	14	IO6_SEG18	39
15	IO5_SEG17	40	16	IO4_SEG16	41
17	IO3_SEG15	42	18	IO2_SEG14	43
19	IO1_SEG13	44	20	IO0_SEG12	45
21	SEG11	46	22	SEG10	47
23	SEG9	48	24	SEG8	49
25	SEG7	50	26	NC	-
27	NC	-	28	NC	-
29	NC	-	30	NC	-
31	NC	-	32	NC	-
33	NC	-	34	NC	-
35	NC	-	36	NC	-

Table 7-6: Microcontroller Pin Header, J2

	Microcontroller Pin Header J3				
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name	MCU Pin
1	SEG6	51	2	SEG5	52
3	SEG4_INTP6	53	4	SEG3	54
5	SEG2	55	6	SEG1	56
7	SEG0	57	8	COM3	58
9	COM2	59	10	COM1	60
11	COM0	61	12	LED1_TO06	62
13	INTP5	63	14	LED0	64
15	INTP2	65	16	INTP1	66
17	SO10_TXD1	67	18	SI10_RXD1	68
19	SCK10	69	20	DLCDD7_SEG47	70
21	DLCDD6_SEG46	71	22	DLCDD5_SEG45	72
23	DLCDD4_SEG44	73	24	SEG43	74
25	SEG42	75	26	NC	-
27	NC	-	28	NC	-
29	NC	-	30	NC	-
31	NC	-	32	NC	-
33	NC	-	34	NC	-
35	NC	-	36	NC	-

Table 7-7 below lists the connections of the microcontroller pin header, J3.

#### Table 7-7: Microcontroller Pin Header, J3

Table 7-8 below lists the connections of the microcontroller pin header, J4.

	Microcontroller Pin Header J4				
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name	MCU Pin
1	SEG41	76	2	SEG40	77
3	P27	78	4	LINTXD_SO00_TXD0	79
5	LINRXD_SI00_RXD0	80	6	LINNSLP_SCK00	81
7	SEG35	82	8	SEG34	83
9	SEG33	84	10	SEG32	85
11	ANI19	86	12	ANI18	87
13	ANI17	88	14	ANI16	89
15	UC_VDD	21, 90	16	GROUND	-
17	NC	-	18	UVBUS	93
19	NC	-	20	NC	-
21	P156	96	22	ANI5	97
23	CON_AVDD	98*	24	CON_AVSS	99*
25	ANI4	100	26	NC	-
27	NC	-	28	NC	-
29	NC	-	30	NC	-
31	NC	-	32	NC	-
33	NC	-	34	NC	-
35	NC	-	36	NC	-

### Table 7-8: Microcontroller Pin Header, J4



# 8. Code Development

### 8.1 Overview

For all code debugging using Renesas software tools, the RSK board must be connected to a PC via an E1/E20 debugger. An E1 debugger is supplied with this RSK product.

For further information regarding the debugging capabilities of the E1/E20 debuggers, refer to E1/E20 Emulator Additional Document for User's Manual (R20UT1994EJ).

### 8.2 Compiler Restrictions

The compiler supplied with this RSK will build a maximum of 64k code and data. To use the compiler with programs greater than this size you need to purchase a compiler license from your Renesas supplier.

### 8.3 Mode Support

The RL78/L1C microcontroller only supports single-chip operating mode.

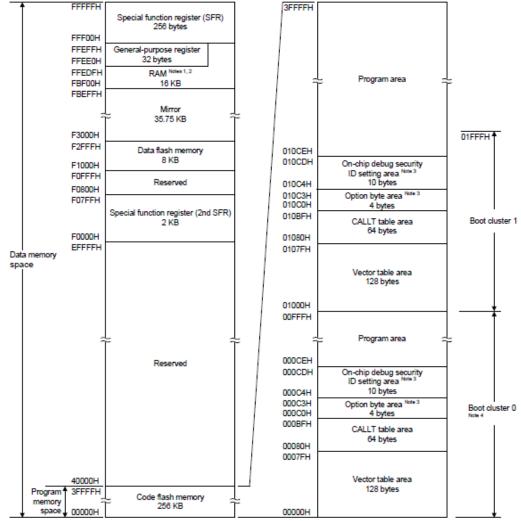
### 8.4 Debugging Support

The E1 emulator (as supplied with this RSK) supports hardware break points, software break points and basic trace functionality. For further details, refer to the E1/E20 Emulator User's Manual (R20UT0398EJ).



### 8.5 Address Space

**Figure 8-1** below details the address space of the MCU. This diagram is taken from the Hardware Manual Rev.1.00. The MCU fitted to the RSK has 256KB of ROM. For further details, refer to the RL78/L1C Group Hardware Manual.



- Note 1. Do not allocate RAM addresses which are used as a stack area, a data buffer, a branch destination of vector interrupt processing, and a DTC transfer destination/transfer source to the area FFE20H to FFEDFH when performing selfprogramming and rewriting the data flash memory. Since the area FBF00H to FC309H is used for each library, this area cannot be used.
- Note 2. Instructions can be executed from the RAM area excluding the general-purpose register area.
- Note 3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

Note 4. Writing boot cluster 0 can be prohibited depending on the setting of security (see 30.7 Security Settings).

Caution 1. While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed and the RAM area + 10 bytes when instructions are fetched from RAM areas, respectively. Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see 27.3.3 RAM parity error detection function.

Caution 2. The internal RAM area in the following products cannot be used as the stack memory when using the on-chip debugging trace function.

R5F110xJ, R5F111xJ (x = M, P): FC300H to FC6FFH

#### Figure 8-1: MCU Address Space Diagram

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# 9. Additional Information

#### **Technical Support**

For details on how to use CubeSuite+, refer to the manual available on the DVD or from the web site.

For information about the RL78/L1C series microcontrollers refer to the RL78/L1C Group Hardware Manual.

For information about the RL78 assembly language, refer to the RL78 Series Software Manual.

#### **Technical Contact Details**

#### Please refer to the contact details listed in section 9 of the "Quick Start Guide"

General information on Renesas Microcontrollers can be found on the Renesas website at: <u>http://www.renesas.com/</u>

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**REVISION HISTORY** 

## RSK RL78L1C User's Manual

Rev.	Date		Description
		Page	Summary
1.00	Jan 16, 2014		First Edition issued
1.01	Mar 19, 2014 —		[2. List of Abbreviations and Acronyms] was updated.
		15, 17	Table format of Table 5-3, 5-5, 5-6 were updated.
		16	Header pin information of Table 5-4 was fixed. (Header Pin.38: SEG25 to SEG27)
		20	Exclusive function of Table 6-2 was fixed. (R25: standard font to bold font, R26: bold font to standard font)
		23	Table 6-7 was fixed.         (VBUS connection information was fixed)         (Unregulated_VCC was renamed)         (Notice was added to U3 regulator input)         (U1.90 was added to U1.21)
		25 to 28	Table format of Table 7-1 to 7-4 were updated.         (Both Header Name and Circuit Net Name are indicated)
		29	Table 7-5 was fixed. (ADPOT_AVPREF was renamed) (Header Pin.20: 20 to -) (Header Pin.21: 90 was added)
		30	All Circuit Net Name information of Table 7-8 was fixed.
		32	Figure 8-1 was updated.
1.02	Apr 04, 2014	17	Table 5-6 was fixed. (SO03_TXD3 to SO30_TXD3) (SI03_RXD3 to SI30_RXD3)
		21	Table 6-3 was fixed.         (Option Links were corrected for TOOL0 of last line)
		23	Table 6-7 was fixed.         (IC Pin and Header Pin were corrected for Board_VDD related to U3 regulator input)

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