

ICL3221EEVAL1Z

User's Manual: Evaluation Board

Industrial Analog and Power

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ICL3221EEVAL1Z

Evaluation Board

The ICL3221EEVAL1Z board enables the evaluation of the [ICL3221E](#) single-channel RS-232 transceiver.

Key Features

- 15kV ESD-protected
- 1μA powerdown
- 250kbps transceiver with manual and automatic powerdown features
- Invalid receive signal indicator
- The receiver is controlled by a separate enable pin

Specifications

This board has been configured and optimized for the following operating conditions:

- Up to 250kbps data rate
- $V_{CC} = 3.0V$ to $5.5V$

Ordering Information

Part Number	Description
ICL3221EEVAL1Z	ICL3221EIVZ evaluation board

Related Literature

For a full list of related documents, visit our website:

- [ICL3221E](#) device page

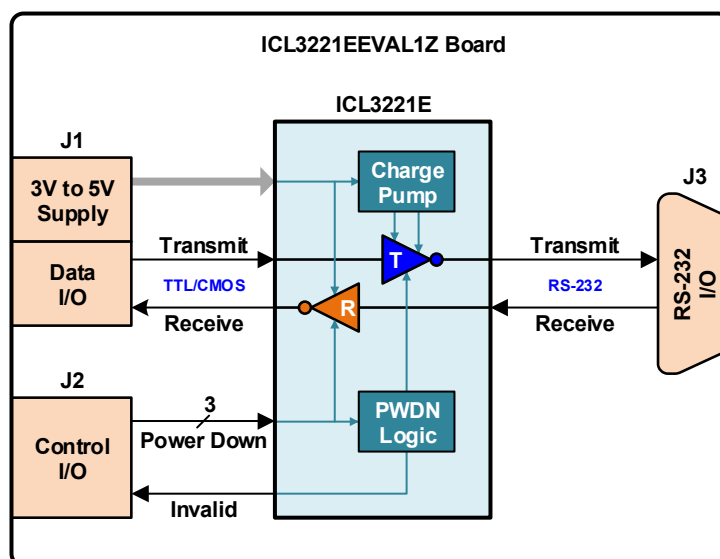


Figure 1. ICL3221EEVAL1Z Board Block Diagram

1. Functional Description

The ICL3221E is a single-channel, 250kbps RS-232 transceiver that operates from a single supply of $V_{CC} = 3.0V$ to $5.5V$. The transmitter converts TTL/CMOS levels to RS-232 voltages of $> \pm 5.0V$ and the receiver converts the RS-232 voltages back to TTL/CMOS levels.

To drive positive and negative output voltages, the transmitter is powered by a charge pump that converts the V_{CC} supply into a positive output voltage of $V^+ > 5.5V$ and a negative output voltage of $V^- < -5.5V$. The receiver is directly powered by V_{CC} .

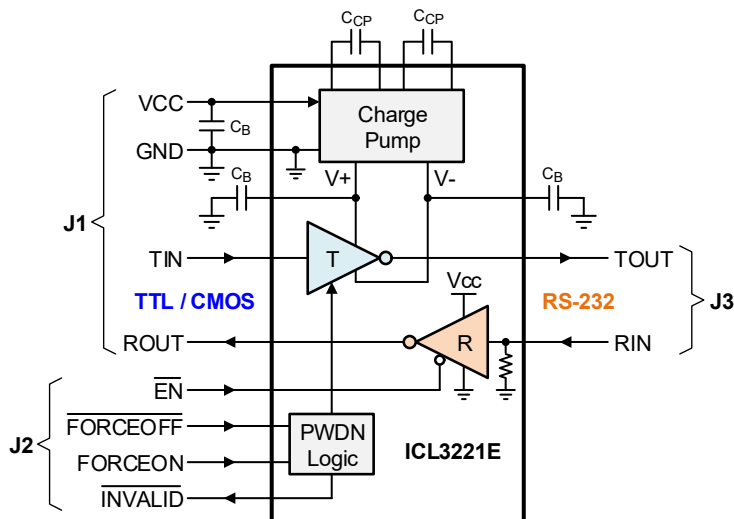


Figure 2. Functional Block Diagram of ICL3221E

The ICL3221E features an auto power-down function that disables the transmitter if there is no valid RS-232 signal at the receiver input; at the same time, the INVALID output turns low. When a valid RS-232 signal is detected, the transmitter is automatically enabled, and the INVALID output turns high.

Auto power-down does not affect the receiver. To power down the receiver, the EN input must be driven high. Auto power-down can be enabled or disabled. When disabled, the transmitter can still be powered down per software, which is commonly referred to as manual power-down. Table 1 lists the necessary logic states of the auto power-down inputs, FORCEON and FORCEOFF, for automatic or manual power-down.

To enable auto power-down, make FORCEOFF = High, and FORCEON = Low. To disable auto power-down, make FORCEON = High. In this case, use FORCEOFF as a manual shutdown input.

Table 1. Power-Down Truth Table

Valid Receiver Input Signal Present?	<u>FORCEOFF</u> Input	<u>FORCEON</u> Input	Transmitter Output	<u>INVALID</u> Output	Operating Mode	
Yes	H	L	Active	H	Auto Power-Down enabled	Normal Operation
Yes	H	L	Active	H		
No	H	L	High-Z	L		Powered Down
No	H	L	High-Z	L		
No	H	H	Active	L	Auto Power-Down disabled	Normal Operation
No	H	H	Active	L		
Yes	L	X	High-Z	H		Manual Power-Down
No	L	X	High-Z	L		

2. PCB Layout Guide Lines

Most applications use a single capacitor value of 0.1μF for the charge pump capacitors and the bypass capacitors of the V_{CC}, V₊, and V₋ supplies. Connect these capacitors as close as possible to the IC.

2.1 ICL3221EEVAL1Z Evaluation Board

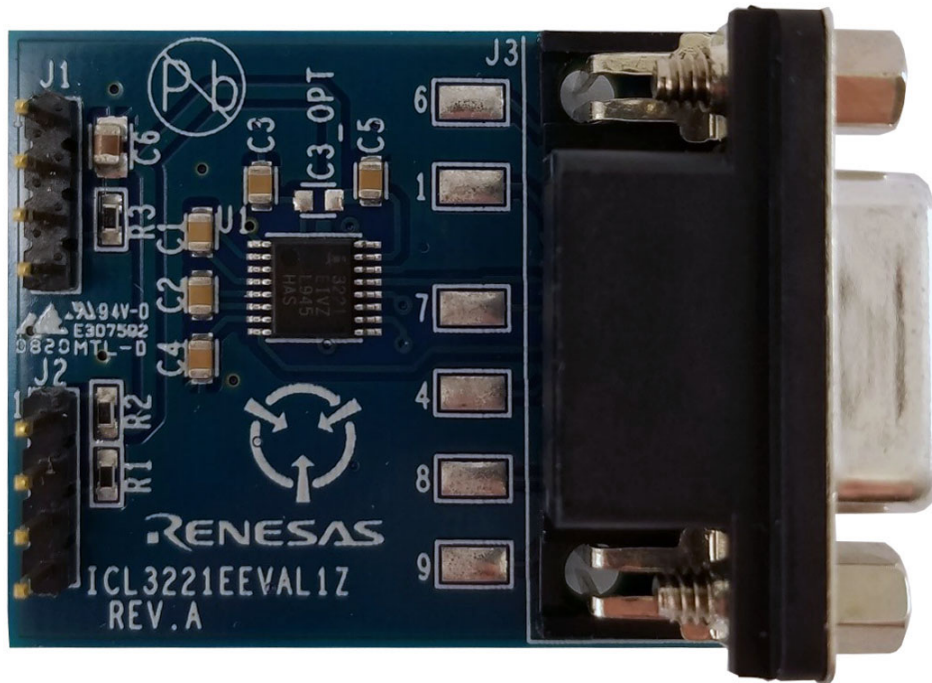


Figure 3. Top Side

2.2 ICL3221EEVAL1Z Circuit Schematic

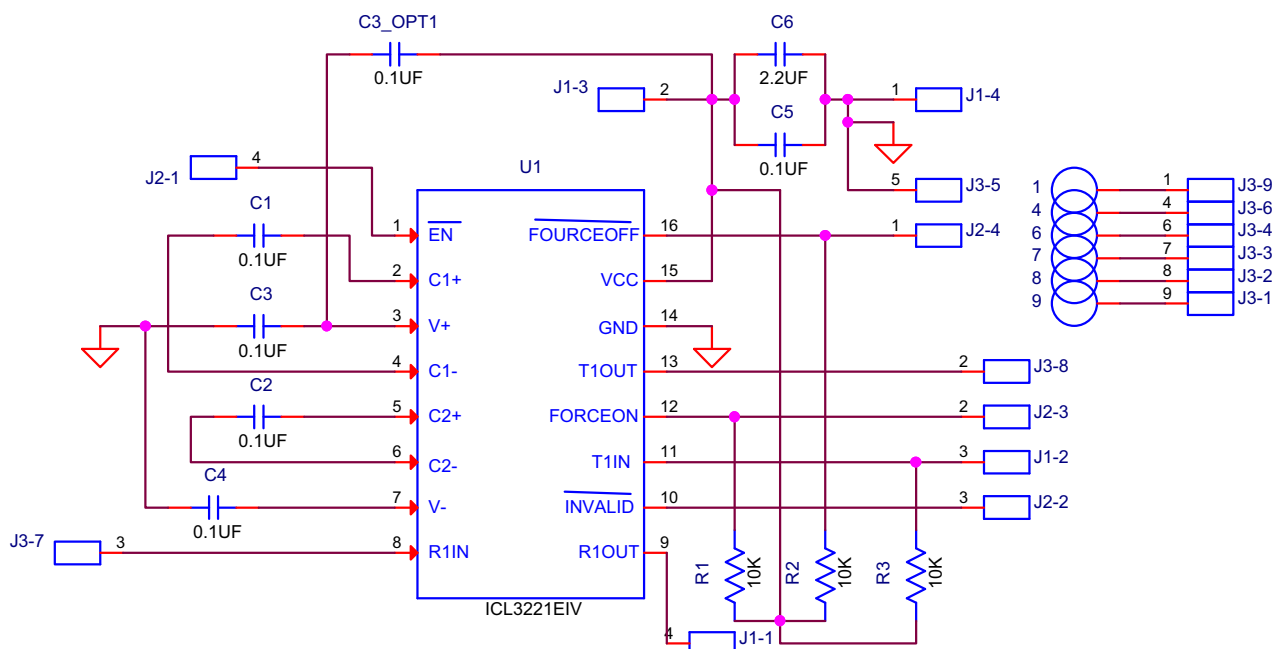


Figure 4. ICL3221EEVAL1Z Schematic

2.3 Bill of Materials

Part Number	Qty	Reference Designator	Description	Manufacturer
ICL3221EEVAL1ZREVAPCB	1		PWB-PCB, ICL3221EEVAL1Z, REVA, ROHS	Imagineering Inc
C2012X7R1C225K-T	1	C6	CAP, SMD, 0805, 2.2μF, 16V, 10%, X7R, ROHS	TDK
CC0603KRX7R8BB104	5	C1, C2, C3, C4, C5	CAP, SMD, 0603, 0.1μF, 25V, 10%, X7R, ROHS	Yageo
H1045-DNP	0	C3_OPT	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS	
68000-236HLF-1X4	2	J1, J2	CONN-HEADER, 1x4, BRKAWY 1x36, 2.54mm, ROHS	Berg/FCI
A-DF09A/KG-T2S	1	J3	CONN-D-SUB, RECEPTACLE, TH, 9POS, DUAL ROW, R/A, ROHS	Assmann WSW Components
ICL3221EIVZ	1	U1	IC-RS-232 TRANSMITTER/RECEIVER, 16P, TSSOP, ROHS	Renesas Electronics
CR0603-10W-1002FT	3	R1, R2, R3	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	Venkel
3X5-STATIC-BAG	1	Place assy in bag	BAG, STATIC, 3x5, ZIP LOC	Renesas Common Stock
DNP	0	1, 4, 6, 7, 8, 9 (5015)	DO NOT POPULATE OR PURCHASE	
LABEL-DATE CODE	1	AFFIX TO BACK OF PCB	LABEL-DATE CODE_LINE 1: YRWK/REV#, LINE 2: BOM NAME	Renesas Electronics America

2.4 Board Layout

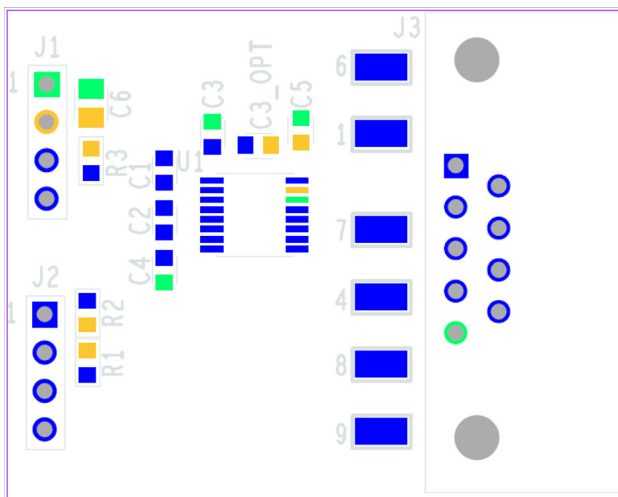


Figure 5. Silkscreen Top

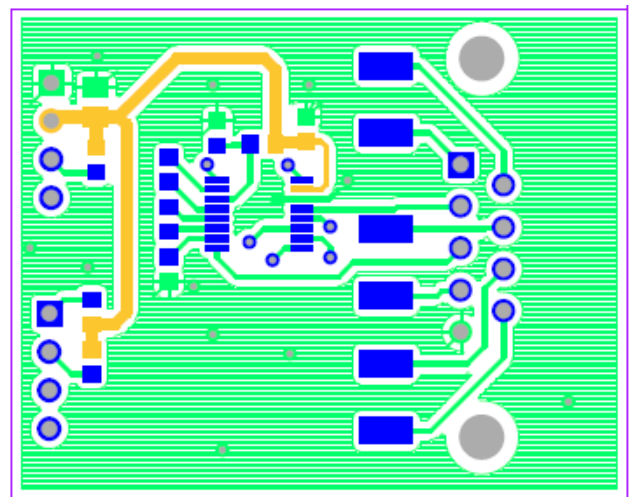


Figure 6. Top Layer

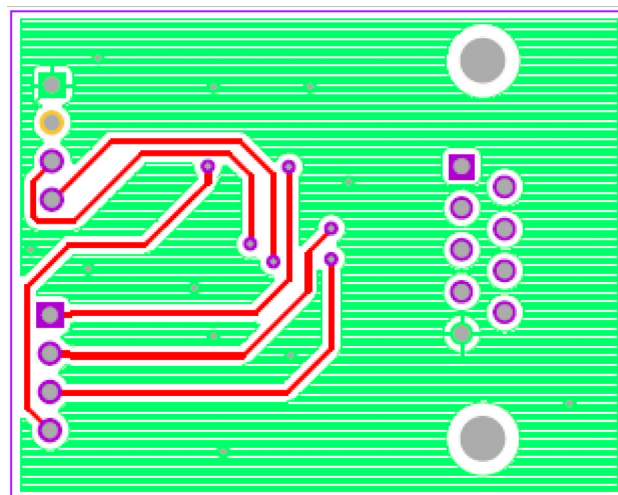


Figure 7. Bottom Layer

3. Typical Performance Curves

The RS-232 signal waveforms in [Figure 8](#) were measured with the measurement setup in [Figure 9](#).

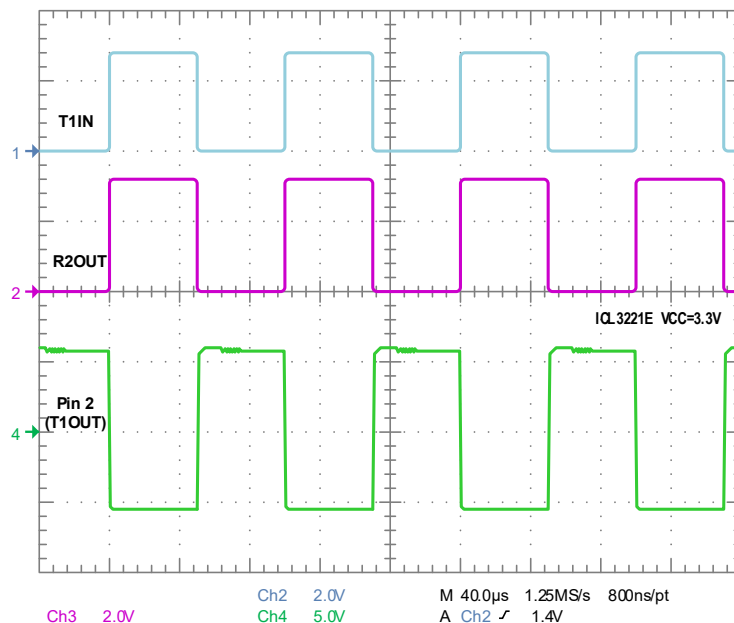


Figure 8. RS-232 Signal Waveforms

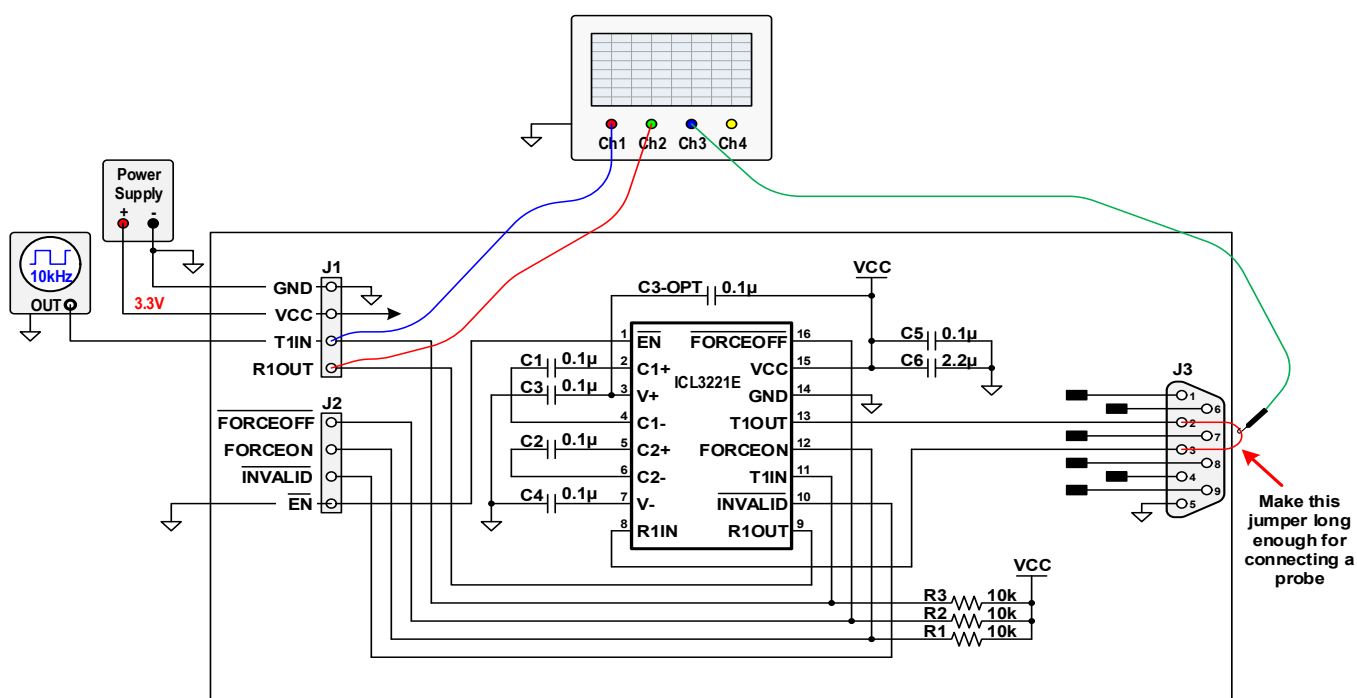


Figure 9. Measurement Setup

4. Revision History

Rev.	Date	Description
1.00	Apr.10.20	Initial release

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