ISL9122AIIN-EVZ, ISL9122AIRN-EVZ

Evaluation Boards

The ISL9122AIIN-EVZ and ISL9122AIRN-EVZ platform allows quick evaluation of the high-performance features of the ISL9122A buck-boost regulator. The ISL9122A is a highly integrated non-inverting buck-boost switching regulator that accepts input voltages both above or below the regulated output voltage. It features an extremely low quiescent current consumption, excellent efficiency and an I^2C interface that allows you to access its internal registers, for output voltage and operation mode control.

Key Features

- Small, compact design
- I^2C interface for programmable V_{OUT}, slew rate and various operation modes (Forced Bypass, Auto-PFM, Forced PWM)
- Connectors, test points, and jumpers for easy probing

Specifications

The boards are designed to operate at the following operating conditions:

- Input voltage rating from 1.8V to 5.5V
- Programmable output voltage range of 1.8V to 5.375V and selectable transition slew rate through I^2C interface
- Up to 500mA output current (V_{IN} = 3.6V, V_{OUT} = 3.3V)
- Operating temperature range: -40°C to +85°C

Ordering Information

Part Number	Description
ISL9122AIIN-EVZ	Evaluation board for ISL9122AIINZ
ISL9122AIRN-EVZ	Evaluation board for ISL9122AIRNZ

Related Literature

For a full list of related documents, visit our website:

- ISL9122A device page

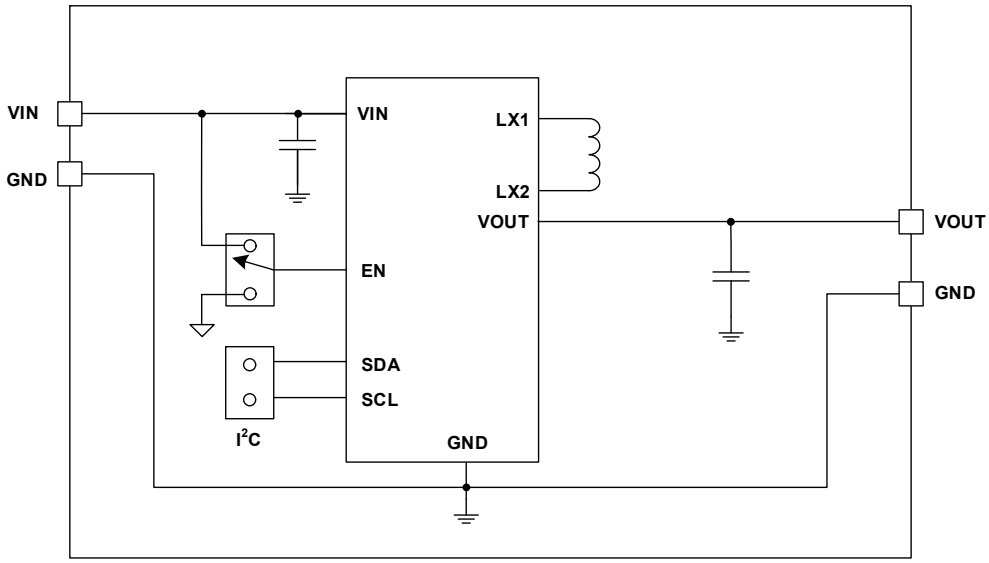

Figure 1. ISL9122AIIN-EVZ, ISL9122AIRN-EVZ Block Diagram

1. Functional Description

The ISL9122AIIN-EVZ and ISL9122AIRN-EVZ evaluation boards provide a simple platform to evaluate the feature-rich ISL9122A buck-boost regulator. Both boards have a 3.3V output after start-up and an output voltage that can be programmed by I^2C. Each evaluation board is optimized to best perform with the ISL9122A IC series. The input power and load connections are provided through multi-pin connectors for high-current operations.

The evaluation boards are shown in Figure 4 and Figure 5. Table 1 lists the test points and jumpers for the boards. The ISL9122A internal registers can be accessed by I^2C through the onboard jumper header J5, and its mode control register configures the part into the various operation modes. See the Evaluation Software Installation and Use to configure the board output voltage and operation modes.

Table 1. Description of Test Points and Jumpers

Test Points	Description
J1	Header for connecting input power
J2	Header for connecting external load
J4	Header for the EN pin J4 = GND disables the part output; J4 = V_{IN} enables the part output
J5	Header for connecting I^2C interface
J1 S+/S-	V_{IN} Kelvin connection for efficiency measurements
J2 S+/S-	V_{OUT} Kelvin connection for efficiency measurements
TP1	Through Hole Mount PCB test point for LX1 (Input side of power inductor)
TP2	Through Hole Mount PCB test point for LX2 (Output side of power inductor)
TP3	Through Hole Mount PCB test point for VOUT
TP4	Single Turret Terminal test point for VIN
TP5	Single Turret Terminal test point for VOUT
TP6	Single Turret Terminal test point for GND
TP7	Single Turret Terminal test point for GND

The following are included in this manual:

- ISL9122 Evaluation Software Window
- ISL9122AIIN-EVZ Circuit Schematic
- ISL9122AIIN-EVZ Board Layout
- ISL9122AIIN-EVZ Bill of Materials
- ISL9122AIRN-EVZ Circuit Schematic
- ISL9122AIRN-EVZ Board Layout
- ISL9122AIRN-EVZ Bill of Materials

1.1 Operating Range

The V_{IN} range of the boards is 1.8V to 5.5V while the adjustable V_{OUT} range is 1.8V to 5.375V. The I_{OUT} range of the boards is 0 to 500mA. The operating ambient temperature range is -40°C to +85°C.

1.2 Quick Start Guide

For both evaluation boards, the default output voltage is set at 3.3V. Use the following procedures to configure and power-up the board for proper operation. During the power-on process, the expected waveforms are shown in Figure 2.

1. Connect the power supply to J1, with voltage setting between 1.8V and 5.5V.
2. Connect the electronic load to J2.
3. Place the scope probes on VOUT test point and other test points of interest.
4. Ensure that the EN pin jumper (J4) is pulled up to V_{IN}.
5. Turn on the power supply. At the end of soft start sequence, ISL9122A is operating in Regulation mode by default with V_{OUT} = 3.3V.
6. Monitor the output voltage start-up sequence on the scope. The waveforms should look similar to those shown in Figure 2.
7. Turn on the electronic load.
8. Measure the output voltage with the voltmeter. The voltage should regulate within the datasheet specification limits.
9. To determine efficiency, measure input and output voltages at the Kelvin sense test points (S+ and S-), which are part of J1 and J2 headers. The bench power supply can be connected to the VIN and GND headers on J1. The electronic load can be connected to the VOUT and GND headers on J2. Measure the input and output currents. Calculate the efficiency based on these measurements.

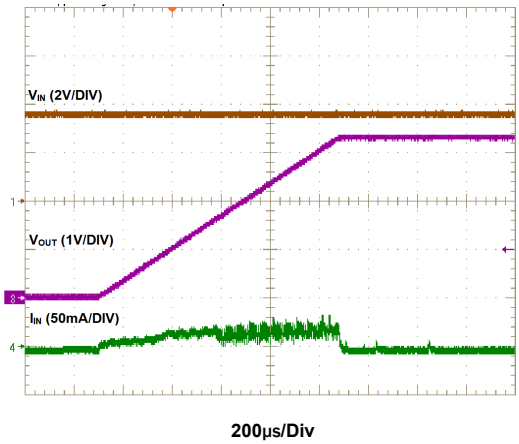

Figure 2. ISL9122A Start-Up with V_{IN} = 3.6V and V_{OUT} = 3.3V

1.3 Evaluation Software Installation and Use

1. The ISL9122 evaluation software is available for download from the Renesas website. Save the file and install the evaluation software by double clicking on the file name. Follow the instructions that appear on-screen to install the application.
2. Attach the USB - I^2C interface dongle to the computer using the supplied USB cable.
3. Attach the USB - I^2C interface dongle to the 20-pin header J5 on the ISL9122A evaluation board.
4. Following the Quick Start Guide, connect the power supply, DC load, and other test equipment to the evaluation board; next, apply power.
5. Launch the ISL9122 evaluation software. The installer adds a shortcut in the **Start** menu (Start > Intersil > ISL9122 > ISL9122 Evaluation Software Customer).
   Select **ISL9122 Evaluation Software Customer** to launch the evaluation software.
6. When launched, the ISL9122 evaluation software detects the USB - I^2C interface, and the **CONNECT** button turns green (see Figure 3). If a connection is not established, this button is brown. Select this button once to

force a manual connection; the button should turn green. If the button remains brown, please check the cable connections, change to another USB port on computer, or try reinstalling the ISL9122 GUI software.

7. Set the 7-bit I^2C address to 0x18, which matches with ISL9122A I^2C address. Selecting **READ ALL** reads from all registers simultaneously and populates all the register panels. Using **WRITE ALL** overwrites all the writable registers with the values specified or modified in the GUI.
8. The ISL9122A has five control registers. See Table 2 through Table 6 for detailed register descriptions.
9. Register **RO_REG1** (Address: 0x02) provides chip identification information. See Table 2 for its register contents. The **Get IC INFO_RO_REG1** button reads from this read-only register.
10. To change the output voltage, you can use the **VSET Control** slider in the **VSET** register (Address: 0x11) panel and perform a Write REG operation. The output voltage ramps up at the slew rate specified in the **DVSRATE** setting of **CONV_CFG** register. If the modified output voltage is lower than the initial value, its ramp down rate depends on the applied load and output capacitance. The **Read REG** button provides the contents of the register, so adjust the slider accordingly. Use Table 4 to decode the VSET content required for the desired output voltage.
11. Register **INTFLG_REG** (Address: 0x03) contains the fault flags. The background color changes from green to red: when (1) a fault occurs from the list in Table 3, and (2) this register is read using either the **Check Fault** button or the **READ ALL** button. Each bit is set by a fault event and cleared when read. When the bit is cleared after reading, the background color changes from red back to green.
12. Register **CONV_CFG** (Address: 0x12) contains crucial converter configuration bits. Table 5 describes its register contents. Selecting the **Write** (or **Read)** button writes (or reads) the entire **CONV_CFG** register in one go.
13. Use **EN_AND** bit to disable the converter through I^2C by toggling the **Soft Start EN_AND** button from **Soft Start enabled** to **Soft Start inhibit**.
14. Selecting the **Soft DSCHG enabled** button presents a soft discharge resistor on the output pin, when the converter is disabled through I^2C using the EN_AND bit. By default, the **Soft DSCHG disabled** button is selected.
15. Use the **DVSRATE** drop-down list to modify the dynamic voltage scaling rate for voltage ramp up, when output voltage is modified using the **VSET** register.
16. Use the **FMODE** drop-down list to select one of the forced operating modes: **Normal** (Auto-PFM, default), **Forced PWM** and **Forced Bypass**.
17. Use the **CTRL Type** drop-down list to select the control mode between **Type I** and **Type II** error amplifier.
18. Register **INTFLG_MASK** (Address: 0x13) contains additional features influencing the part behavior. Selecting the **Write** (or **Read**) button writes (or reads) the entire **INTFLG_MASK** register in one go.
19. As mentioned in Table 6, use **OC_FAULT** drop-down to select the overcurrent handling mechanism for the part. By default, the part is set to **Hiccup mode** during overcurrent, but this setting can be changed to **Shutdown mode** or **Current Limit mode** using this register.
20. Use the **EN_OR** drop-down list to enable a push-button ON functionality for the EN pin. By default, this feature is disabled.

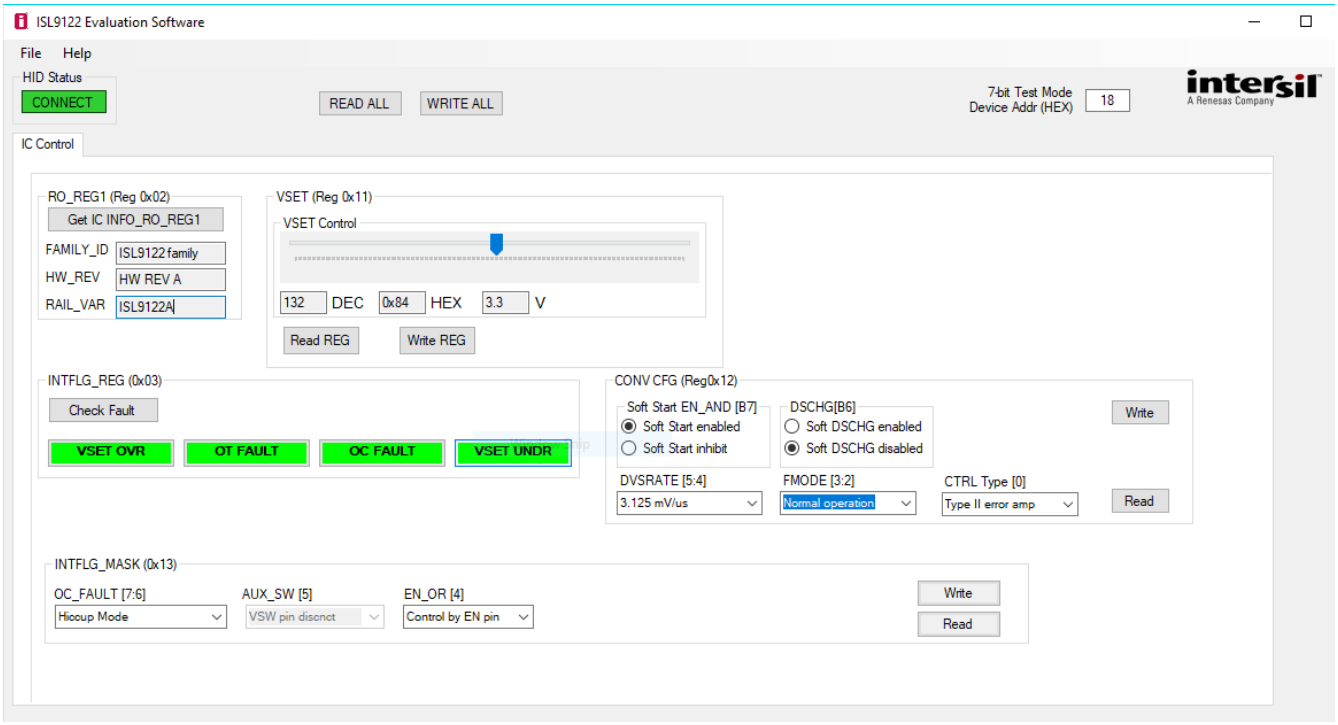

Figure 3. ISL9122 Evaluation Software Window

Table 2. Register Address 0x02: RO_REG1

Bit	Name	Type	Reset	Description
7:6	FAMILY_ID[1:0]	R	0x0	Chip family identifier 0x0 = ISL9122 stand-alone converter family
5:3	HW_REV[2:0]	R	0x3	Chip revision level 0x3 = Hardware revision D
2:0	RAIL_VAR[2:0]	R	0x0	Converter variant identifier 0x0 = High voltage input Buck-Boost (ISL9122A)

Table 3. Register Address 0X03: INTFLG_REG

Bit	Name	Type	Reset	Description
3	INT3	R	0x0	Voltage setting under range
2	INT2	R	0x0	Voltage setting over range
1	INT1	R	0x0	Over-temperature
0	INT0	R	0x0	Overcurrent

Table 4. Register Address 0x11: VSET

Bit	Name	Type	Reset	Description
7:0	VSET[7:0]	R/W	000	Output voltage setting V_{OUT} = VSET*0.025V Minimum limit = 1.8V Maximum limit = 5.375V

Table 5. Register Address 0X12: CONV_CFG

Bit	Name	Type	Reset	Description
7	EN_AND	R/W	0x1	Enable bit. ANDed with the enable input 0x0 = EN pin going high wakes up the I^2C, but does not start the converter. The converter is started by writing 1 to this bit using I^2C while the EN pin is high 0x1 = EN pin going high wakes up the I^2C and starts the converter **Note:** EN pin low always disables the converter and I^2C
6	DISCH	R/W	0x0	0x0 = No discharge resistor is present when converter is disabled over I^2C 0x1 = Discharge resistor is present when converter is disabled over I^2C
5:4	DVSRATE[1:0]	R/W	0x0	Dynamic Voltage Scaling slew rate applied when the output voltage setting is changed 0x0 = 3.125mV/µs 0x1 = 6.25mV/µs 0x2 = 0.78125mV/µs 0x3 = 1.5625mV/µs
3:2	FMODE[1:0]	R/W	0x0	Forced operating modes 0x0 = Normal operation with automatic mode transitions 0x1 = RESERVED. **DO NOT USE** this combination 0x2 = Forced PWM mode with no PFM operation 0x3 = Forced Bypass. Disables switching. If the Forced Bypass mode is selected and the part is disabled over I^2C (CONV_CFG[7] = EN_AND = 0), the converter remains in Forced Bypass
1	CONV_RSVD	R/W	0x0	Reserved
0	TYPE1	R/W	0x1	0x0 = Type I error amplifier for best transient response with voltage positioning 0x1 = Type II error amplifier for best steady state voltage accuracy. **DO NOT USE** Type II error amplifier if overcurrent fault handling is disabled (INTFLG_MASK[7] = OC_FAULT_MODE = 0x2 or 0x3)

Table 6. Register Address 0X13: INTFLG_MASK

Bit	Name	Type	Reset	Description
7:6	OC_FAULT_MODE	R/W	0x0	Overcurrent fault handling modes 0x0 = Hiccup mode with 100ms wait 0x1 = Shutdown mode. Requires restart over I^2C or EN pin 0x2 = Current limit with no fault action taken. USE ONLY with Type I error amplifier (CONV_CFG[0] = TYPE1 = 0x0) 0x3 = Reserved. USE ONLY with Type I error amplifier (CONV_CFG[0] = TYPE1 = 0x0)
5	EN_OR	R/W	0x0	Enable override bit for I^2C control of converter. Implements push-button ON operation; the button pulls EN high and the part starts. If EN_OR is set from OTP or over I^2C, the part remains enabled when the button is released 0x0 = Controlled by the EN pin 0x1 = Held in enable state - EN pin is ignored

2. PCB Layout Guidelines

The ISL9122AIIN-EVZ and ISL9122AIRN-EVZ PCB layouts have been optimized for electrical and thermal performance.

- The input and output capacitors should be positioned as close to the IC as possible.
- The ground connections of the input and output capacitors should be kept as short as possible, and should be on the component layer to avoid problems that are caused by high-switching currents flowing through PCB vias.

2.1 ISL9122AIIN-EVZ Evaluation Board

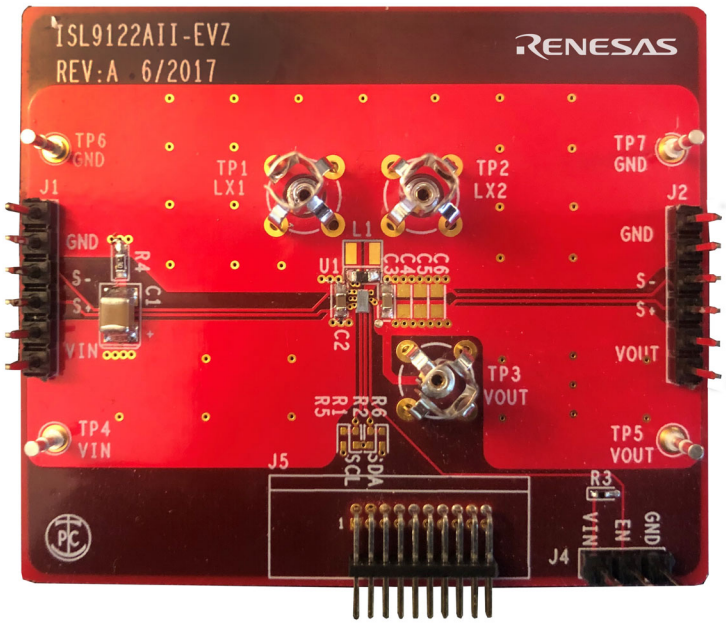

Figure 4. ISL9122AIIN-EVZ Evaluation Board (Top)

2.2 ISL9122AIRN-EVZ Evaluation Board

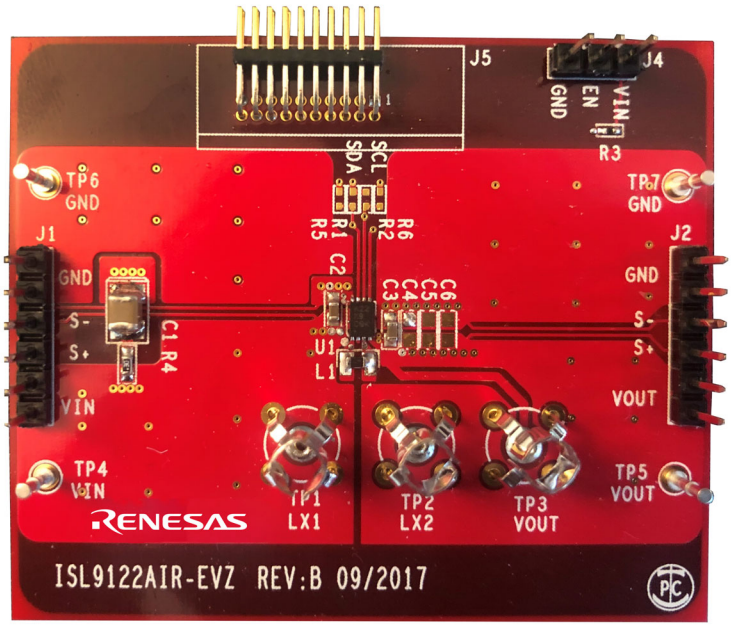

Figure 5. ISL9122AIRN-EVZ Evaluation Board (Top)

2.3 ISL9122AIIN-EVZ Circuit Schematic

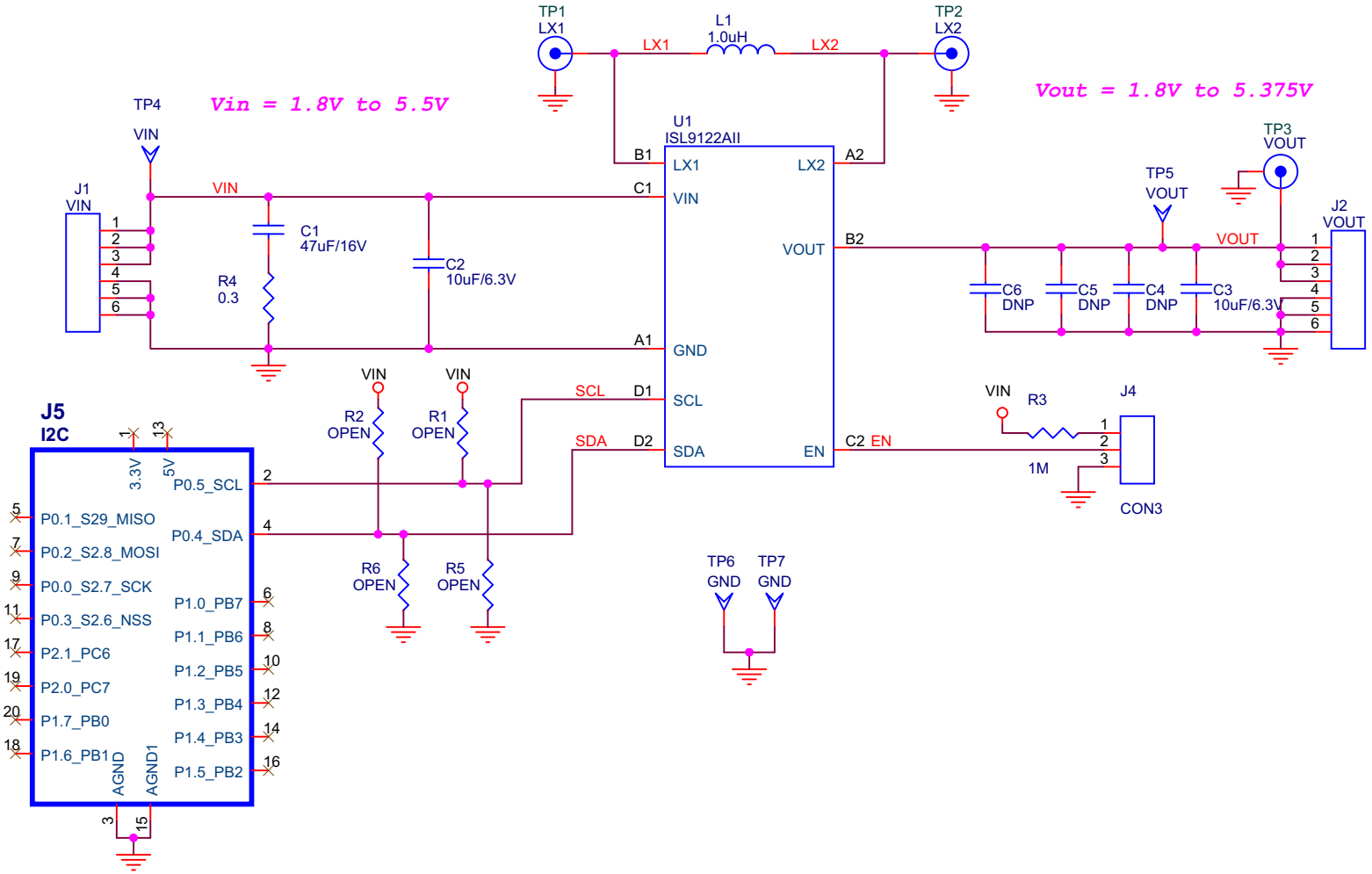

Figure 6. ISL9122AIIN-EVZ Circuit Schematic

2.4 ISL9122AIRN-EVZ Circuit Schematic

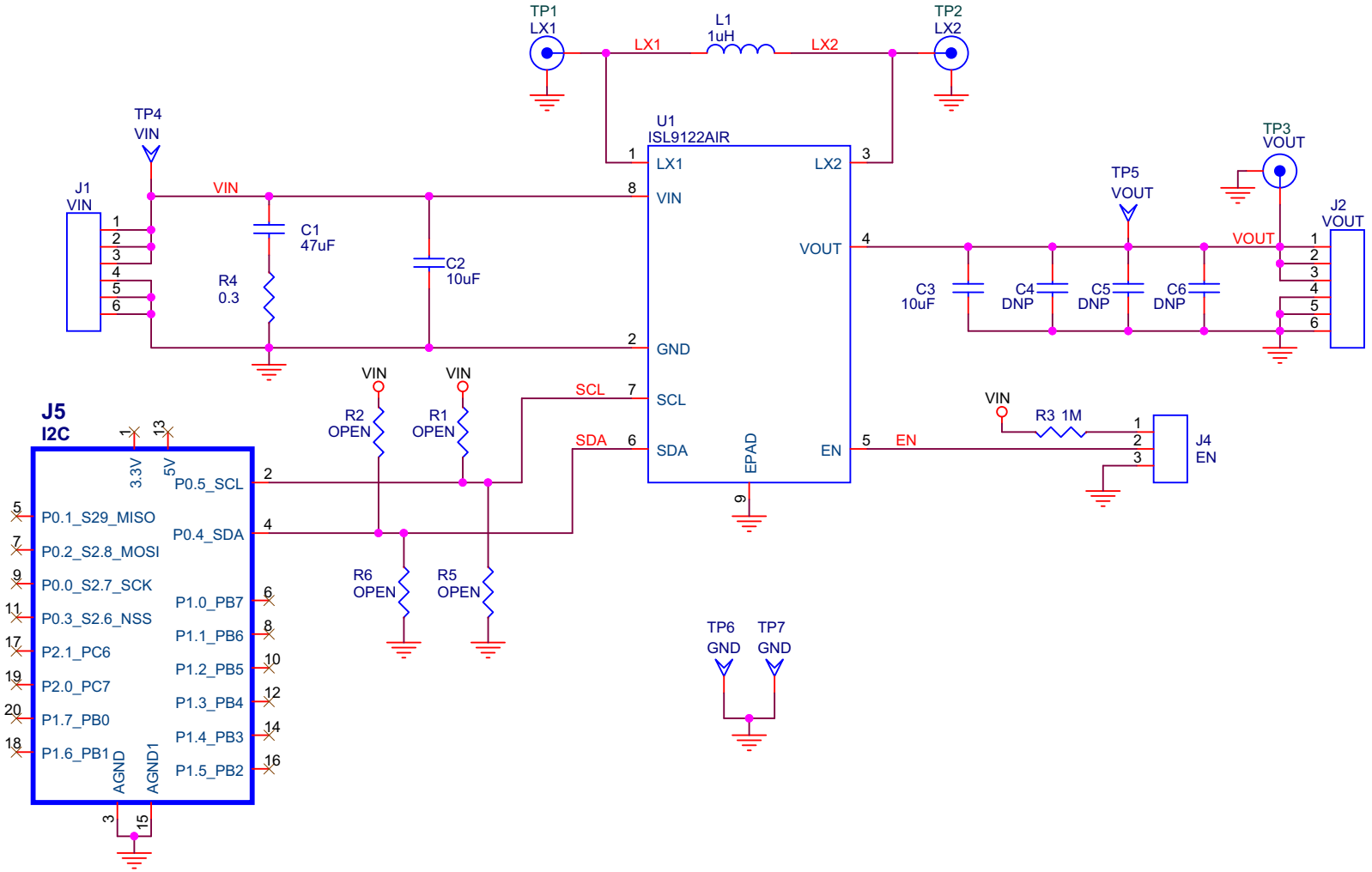

Figure 7. ISL9122AIRN-EVZ Circuit Schematic

2.5 ISL9122AIIN-EVZ Bill of Materials

Qty	Reference Designator	Part	PCB Footprint	Description	Manufacturer Part Number	Manufacturer
1	C1	47µF/16V	C_1210	CAP CER, X5R, SMD, ROHS, -55°C ~ 85°C	GRM32ER61C476ME15	Murata
2	C2, C3	10µF/6.3V	C_0402	CAP CER, X5R, SMD, ROHS, -55°C ~ 85°C	GRM188R60J106ME84D	Murata
1	J1	VIN	con-1x6	BERGSTIK II 0.100" SR STRAIGHT	68000-236	FCI
1	J2	VOUT	con-1x6	BERGSTIK II 0.100" SR STRAIGHT	68000-236	FCI
1	J4	EN	CON-1X3	BERGSTIK II 0.100" SR STRAIGHT	68000-236	FCI
1	J5	I2C	usb_apple	CONN HDR 1.27MM R/A AU 20POS	M50-3901042	Harwin Inc
1	L1	1µH	FERRITE_0603	FIXED IND 1µH 1.7A 128MΩ SMD	DFE18SAN1R0MG0L	Murata
2	R1, R2	OPEN	R_0402	RES SMD 1% 1/10W 0603	OPEN	Any
1	R3	1M	R_0402	RES SMD 1% 1/10W 0603	ANY	Any
1	R4	0.3	R_0603	RES SMD 1% 1/10W 0603	ANY	Any
1	TP1	LX1	tek131-5031-00-pc	PCB Test Point, Through Hole Mount, 1.72 mm	131-5031-00	Mouser
1	TP2	LX2	tek131-5031-00-pc	PCB Test Point, Through Hole Mount, 1.72 mm	131-5031-00	Mouser
1	TP3	VOUT	tek131-5031-00-pc	PCB Test Point, Through Hole Mount, 1.72 mm	131-5031-00	Mouser
1	TP4	VIN	TP_PC	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	TP5	VOUT	TP_PC	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
2	TP6, TP7	GND	TP_PC	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	U1	ISL9122AIINZ-T	wlcsp8_39x71_157		ISL9122AII	Renesas Electronics America
1	J4	Shunt installed between 1-2	2.54 mm	Headers & Wire Housings Mini Jumper GF 6.0MM Close	151-8010-E	Kobiconn

2.6 ISL9122AIRN-EVZ Bill of Materials

Qty	Reference Designator	Part	PCB Footprint	Description	Manufacturer Part Number	Manufacturer
1	C1	47µF/16V	C_1210	CAP CER, X5R, SMD, RoHS, -55°C ~ 85°C	GRM32ER61C476ME15	Murata
2	C2, C3	10µF/6.3V	C_0603	CAP CER, X5R, SMD, RoHS, -55°C ~ 85°C	GRM188R60J106ME84D	Murata
3	C4, C5, C6	DNP	C_0603		open	Murata
1	J1	VIN	con-1x6	BERGSTIK II 0.100" SR STRAIGHT	68000-236	FCI
1	J2	VOUT	con-1x6	BERGSTIK II 0.100" SR STRAIGHT	68000-236	FCI
1	J4	EN	CON-1X3	BERGSTIK II 0.100" SR STRAIGHT	68000-236	FCI
1	J5	I2C	usb_conn_20	CONN HDR 1.27MM R/A AU 20POS	M50-3901042	Harwin Inc
1	L1	1µH	FERRITE_0603	FIXED IND 1µH 950MA 200MΩ SMD	DFE18SAN1R0MG0L	Murata
4	R1, R2, R5, R6	OPEN	R_0402	RES SMD 1% 1/10W 0603	OPEN	Any
1	R3	1M	R_0402	RES SMD 1% 1/10W 0603	ANY	Any
1	R4	0.3	R_0603	RES SMD 1% 1/10W 0603	ANY	Any
1	TP1	LX1	tek131-5031-00-pc	PCB Test Point, Through Hole Mount, 1.72 mm	131-5031-00	Mouser
1	TP2	LX2	tek131-5031-00-pc	PCB Test Point, Through Hole Mount, 1.72 mm	131-5031-00	Mouser
1	TP3	VOUT	tek131-5031-00-pc	PCB Test Point, Through Hole Mount, 1.72 mm	131-5031-00	Mouser
1	TP4	VIN	TP_PC	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	TP5	VOUT	TP_PC	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
2	TP6, TP7	GND	TP_PC	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	U1	ISL9122AIRNZ-T	8 Lead Dual Flat No Lead Plactic Package	dfn8_79x118_197		Renesas Electronics America
1	J4	Shunt installed between 1-2	2.54 mm	Headers & Wire Housings Mini Jumper GF 6.0MM Close	151-8010-E	Kobiconn

2.7 ISL9122AIIN-EVZ Board Layout

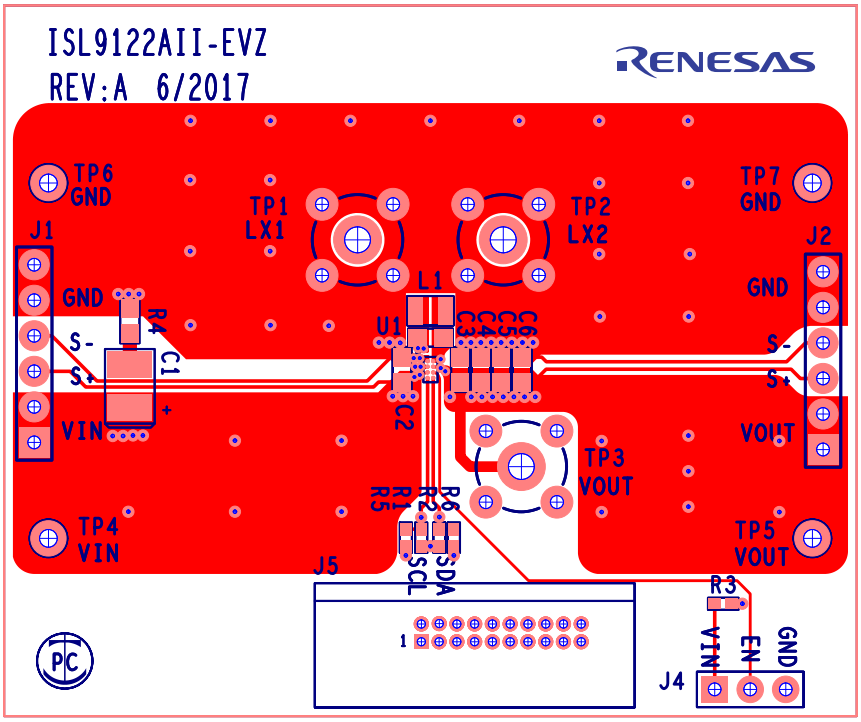

Figure 8. Top Layer Silk Screen

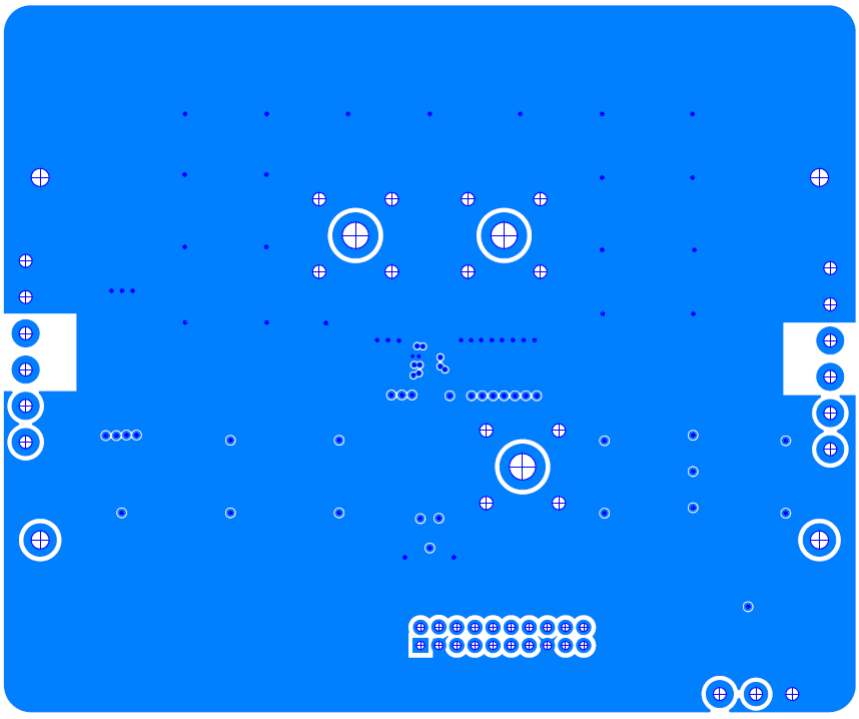

Figure 9. Inner Layer 2

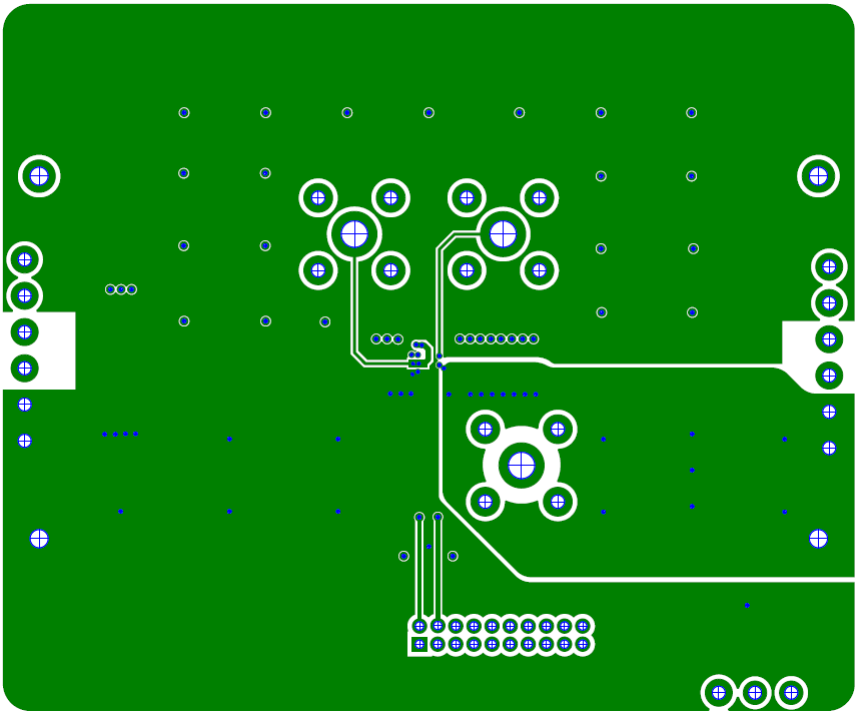

Figure 10. Inner Layer 3

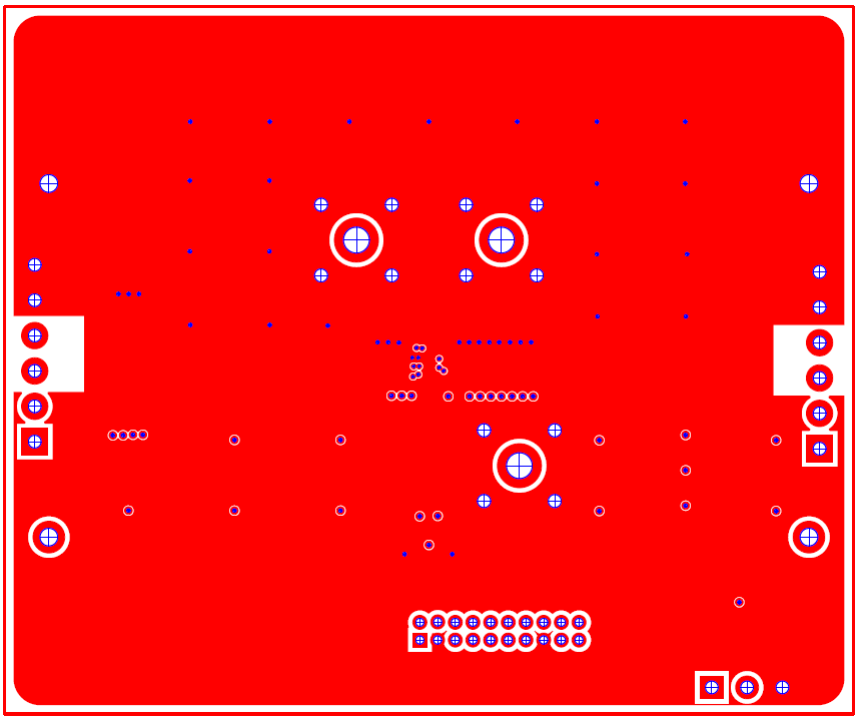

Figure 11. Bottom Layer Silk Screen

2.8 ISL9122AIRN-EVZ Board Layout

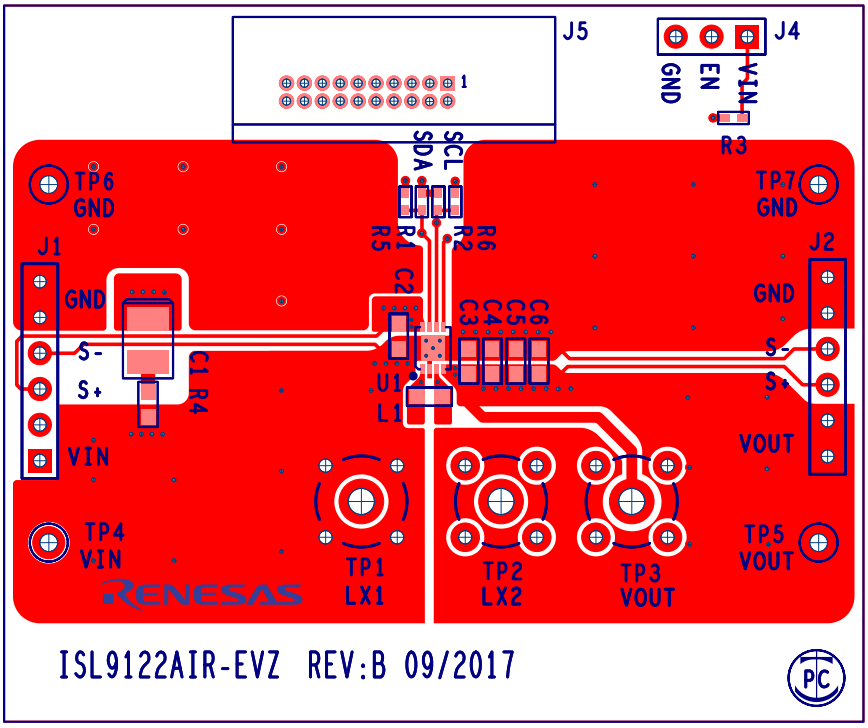

Figure 12. Top Layer Silk Screen

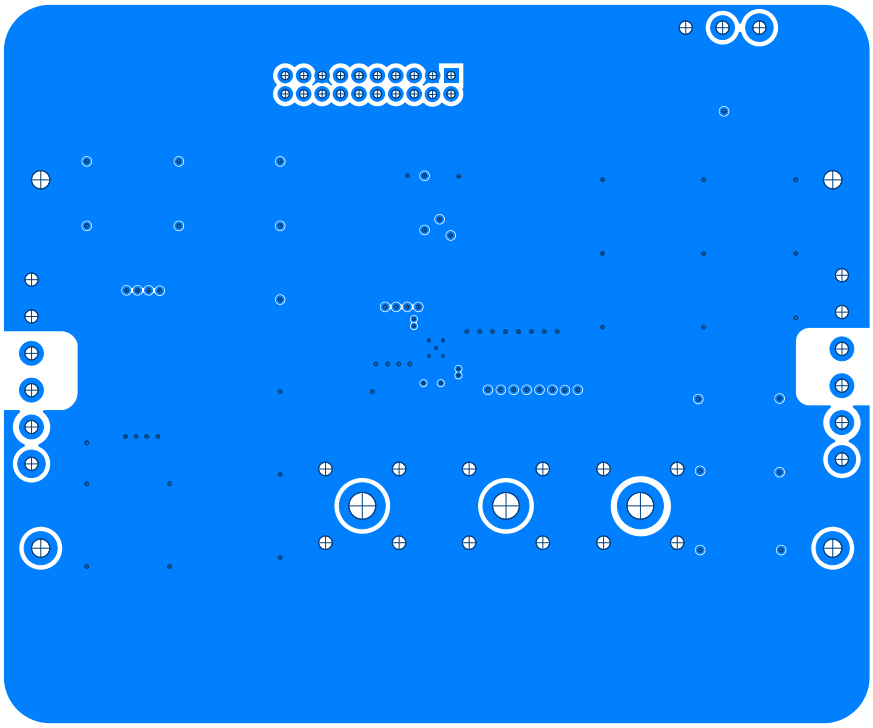

Figure 13. Inner Layer 2

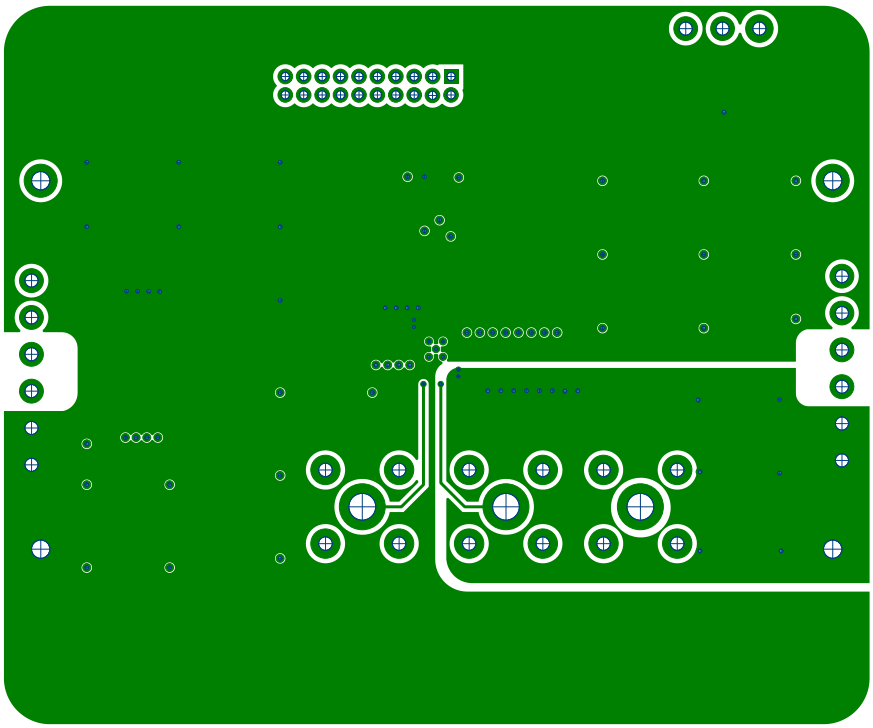

Figure 14. Inner Layer 3

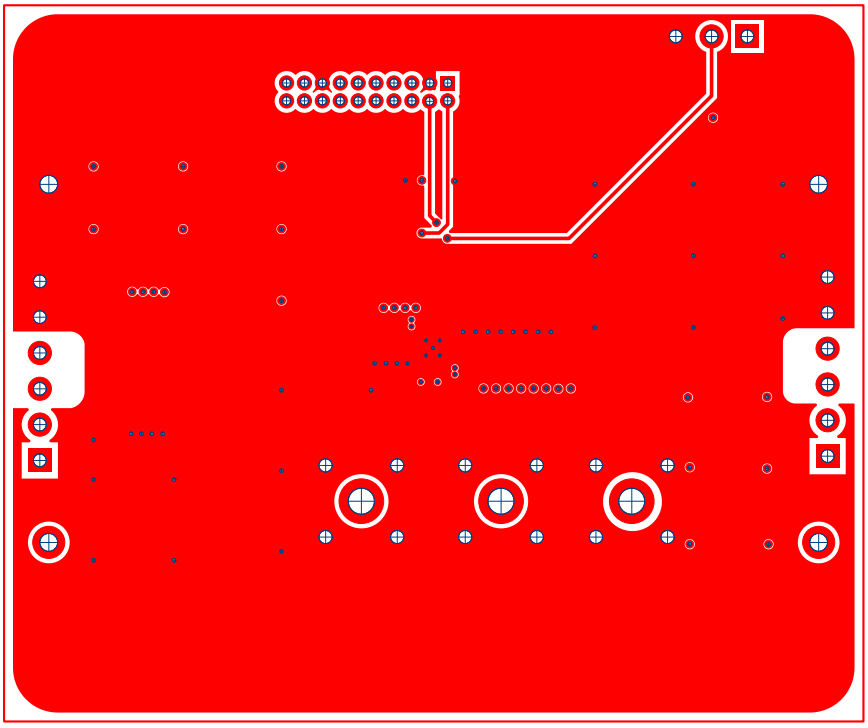

Figure 15. Bottom Layer Silk Screen

3. Revision History

Rev.	Date	Description
1.01	Oct.1.20	Updated Ordering Information table. Updated BOMs
1.00	Aug.18.20	Initial release

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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