

# R1RP0408D Series

R10DS0288EJ0100

Rev.1.00

Nov.18.19

## 4M High Speed SRAM (512-kword × 8-bit)

### Description

The R1RP0408D Series is a 4-Mbit high speed static RAM organized 512-k word × 8-bit. It has realized high speed access time by employing CMOS process (6-transistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in 400-mil 36-pin plastic SOJ.

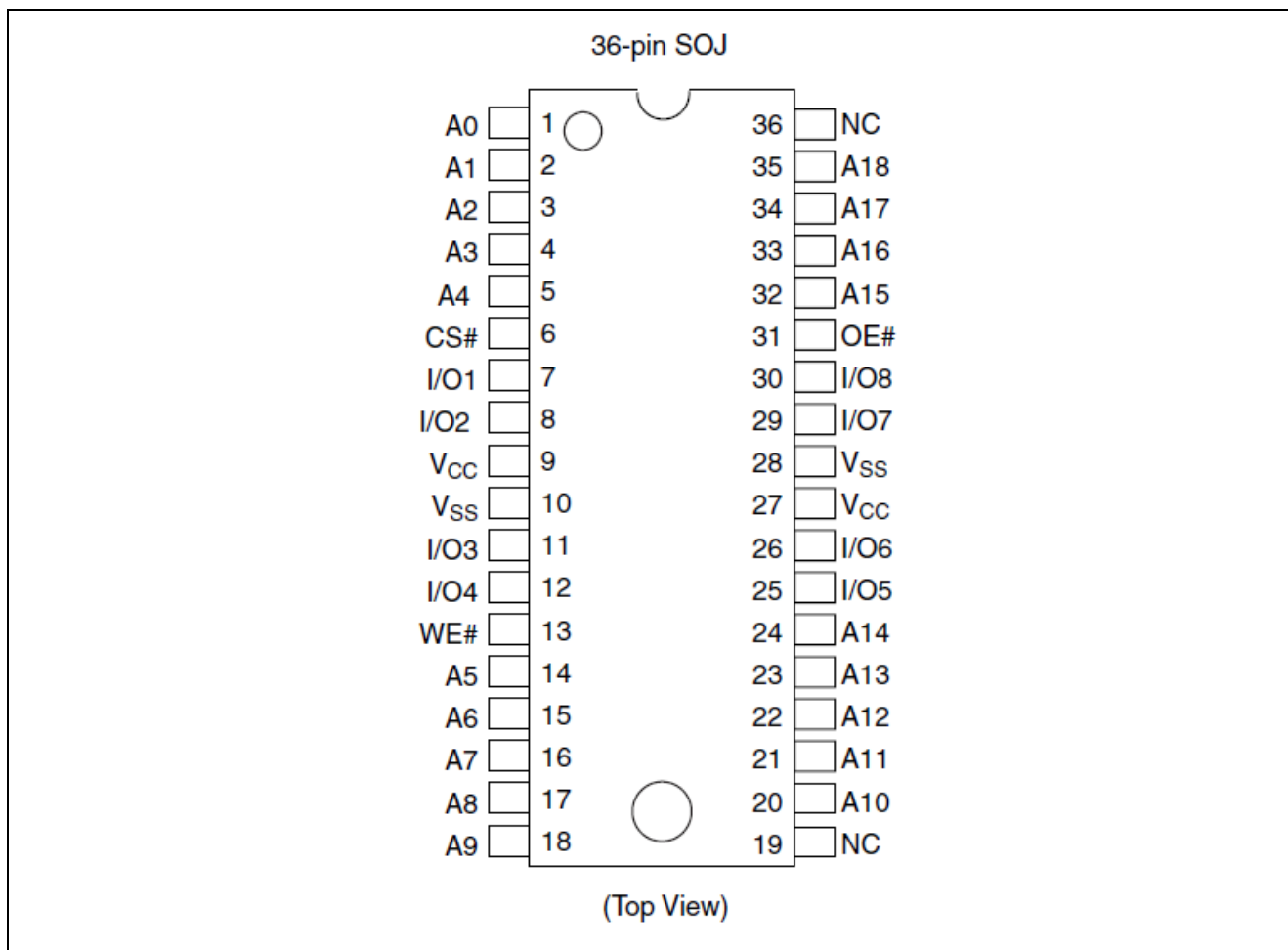
### Features

- Single 5.0V supply: 5.0V ± 10%
- Access time: 12ns (max)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  - All inputs and outputs
- Operating current: 130mA (max)
- TTL standby current: 40mA (max)
- CMOS standby current : 5mA (max)
  - : 1.0mA (max) (L-version)
- Data retention current : 0.5mA (max) (L-version)
- Data retention voltage : 2.0V (min) (L-version)
- Center V<sub>CC</sub> and V<sub>SS</sub> type pin out

### Ordering Information

Type No.	Access time	Version	Package
R1RP0408DGE-2PR	12ns	Normal	400-mil 36-pin plastic SOJ
R1RP0408DGE-2LR	12ns	L-Version	

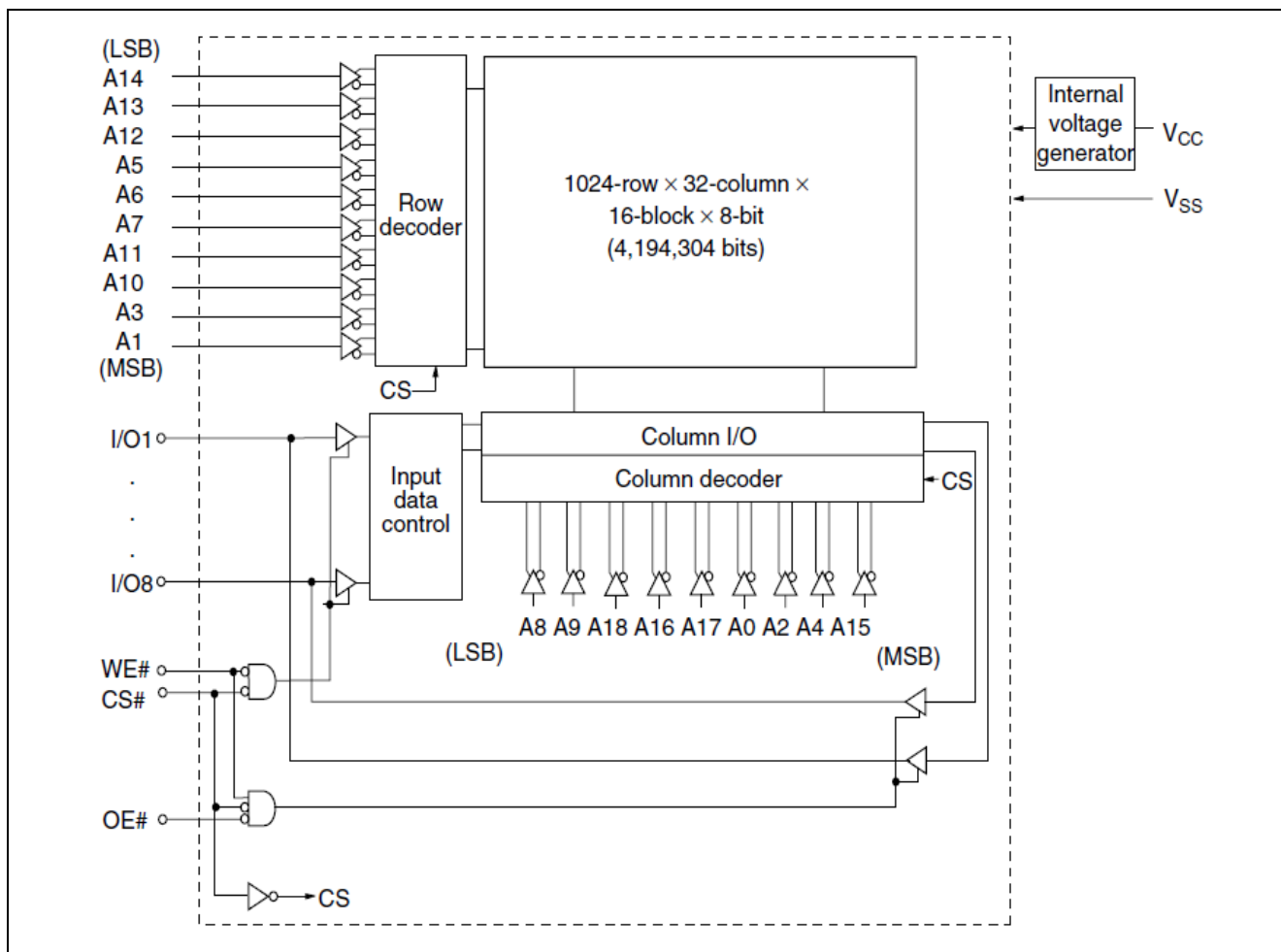
## Pin Arrangement



## Pin Description

Pin name	Function
A0 to A18	Address input
I/O1 to I/O8	Data input/output
CS#	Chip select
OE#	Output enable
WE#	Write enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NC	No connection

## Block Diagram



## Operation Table

CS#	OE#	WE#	Mode	V <sub>CC</sub> current	I/O	Ref. cycle
H	×	×	Standby	I <sub>SB</sub> , I <sub>SB1</sub>	High-Z	—
L	H	H	Output disable	I <sub>CC</sub>	High-Z	—
L	L	H	Read	I <sub>CC</sub>	D <sub>OUT</sub>	Read cycle (1) to (3)
L	H	L	Write	I <sub>CC</sub>	D <sub>IN</sub>	Write cycle (1)
L	L	L	Write	I <sub>CC</sub>	D <sub>IN</sub>	Write cycle (2)

Note: H: V<sub>IH</sub>, L: V<sub>IL</sub>, ×: V<sub>IH</sub> or V<sub>IL</sub>

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V <sub>SS</sub>	V <sub>CC</sub>	−0.5 to +7.0	V
Voltage on any pin relative to V <sub>SS</sub>	V <sub>T</sub>	−0.5* <sup>1</sup> to V <sub>CC</sub> + 0.5* <sup>2</sup>	V
Power dissipation	P <sub>T</sub>	1.0	W
Operating temperature	T <sub>opr</sub>	0 to +70	°C
Storage temperature	T <sub>stg</sub>	−55 to +125	°C
Storage temperature under bias	T <sub>bias</sub>	−10 to +85	°C

Notes: 1. V<sub>T</sub> (min) = −2.0V for pulse width (under shoot) ≤ 6ns.

2. V<sub>T</sub> (max) = V<sub>CC</sub> + 2.0V for pulse width (over shoot) ≤ 6ns.

## Recommended DC Operating Conditions

(T<sub>a</sub> = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub> * <sup>3</sup>	4.5	5.0	5.5	V
	V <sub>SS</sub> * <sup>4</sup>	0	0	0	V
Input voltage	V <sub>IH</sub>	2.0	—	V <sub>CC</sub> + 0.5* <sup>2</sup>	V
	V <sub>IL</sub>	−0.5* <sup>1</sup>	—	0.8	V

Notes: 1. V<sub>IL</sub> (min) = −2.0V for pulse width (under shoot) ≤ 6ns.

2. V<sub>IH</sub> (max) = V<sub>CC</sub> + 2.0V for pulse width (over shoot) ≤ 6ns.

3. The supply voltage with all V<sub>CC</sub> pins must be on the same level.

4. The supply voltage with all V<sub>SS</sub> pins must be on the same level.

## DC Characteristics

(Ta = 0 to +70°C, V<sub>CC</sub> = 5.0V ± 10%, V<sub>SS</sub> = 0V)

Parameter	Symbol	Min	Max	Unit	Test conditions
Input leakage current	I <sub>LI</sub>	—	2	μA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>	—	2	μA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Operating power supply current	I <sub>CC</sub>	—	130	mA	Min cycle CS# = V <sub>IL</sub> , I <sub>OUT</sub> = 0mA Other inputs = V <sub>IH</sub> /V <sub>IL</sub>
Standby power supply current	I <sub>SB</sub>	—	40	mA	Min cycle, CS# = V <sub>IH</sub> , Other inputs = V <sub>IH</sub> /V <sub>IL</sub>
	I <sub>SB1</sub>	—	5	mA	f = 0MHz V <sub>CC</sub> ≥ CS# ≥ V <sub>CC</sub> - 0.2V,
		—*1	1.0*1	mA	(1) 0V ≤ V <sub>IN</sub> ≤ 0.2V or (2) V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V
Output voltage	V <sub>OL</sub>	—	0.4	V	I <sub>OL</sub> = 8mA
	V <sub>OH</sub>	2.4	—	V	I <sub>OH</sub> = -4mA

Note: 1. This characteristics is guaranteed only for L-version.

## Capacitance

(Ta = +25°C, f = 1.0MHz)

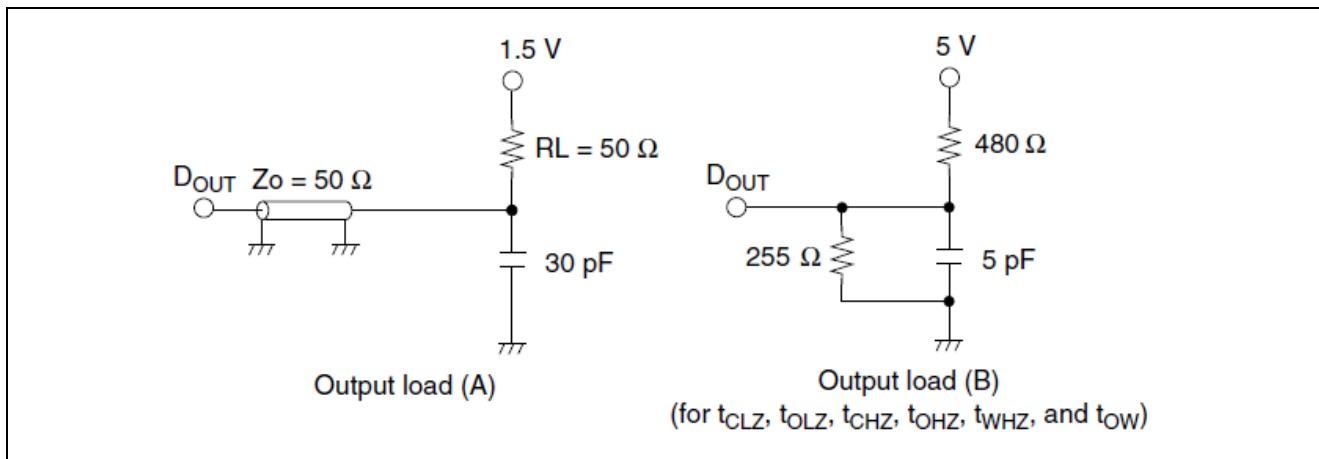
Parameter	Symbol	Min	Max	Unit	Test conditions
Input capacitance*1	C <sub>IN</sub>	—	6	pF	V <sub>IN</sub> = 0V
Input/output capacitance*1	C <sub>I/O</sub>	—	8	pF	V <sub>I/O</sub> = 0V

Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics

**Test Conditions** ( $T_a = 0$  to  $+70^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$ , unless otherwise noted.)

- Input pulse levels: 3.0V/0.0V
- Input rise and fall time: 3ns
- Input and output timing reference levels: 1.5V
- Output load: See figures (Including scope and jig)



## Read Cycle

Parameter	Symbol	R1RP0408D		Unit	Notes
		Min	Max		
Read cycle time	$t_{RC}$	12	—	ns	
Address access time	$t_{AA}$	—	12	ns	
Chip select access time	$t_{ACS}$	—	12	ns	
Output enable to output valid	$t_{OE}$	—	6	ns	
Output hold from address change	$t_{OH}$	3	—	ns	
Chip select to output in low-Z	$t_{CLZ}$	3	—	ns	1
Output enable to output in low-Z	$t_{OLZ}$	0	—	ns	1
Chip deselect to output in high-Z	$t_{CHZ}$	—	6	ns	1
Output disable to output in high-Z	$t_{OHZ}$	—	6	ns	1

**Write Cycle**

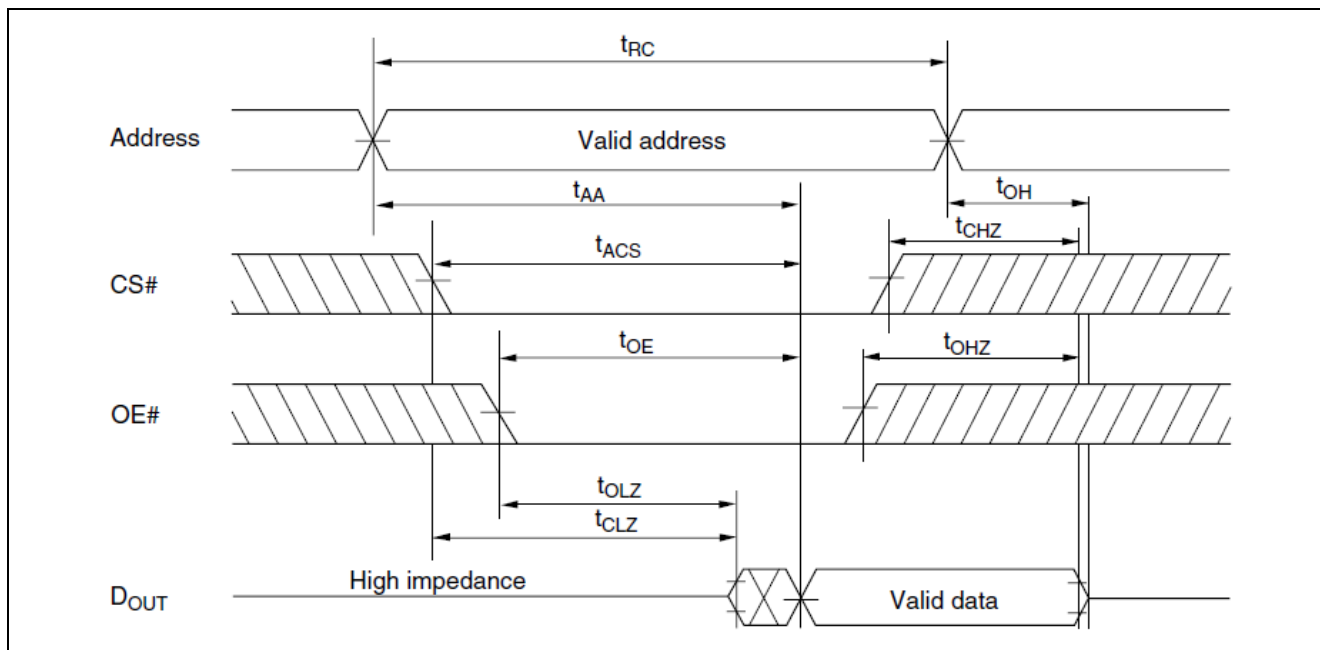
Parameter	Symbol	R1RP0408D		Unit	Notes
		Min	Max		
Write cycle time	t <sub>WC</sub>	12	—	ns	
Address valid to end of write	t <sub>AW</sub>	8	—	ns	
Chip select to end of write	t <sub>CW</sub>	8	—	ns	9
Write pulse width	t <sub>WP</sub>	8	—	ns	8
Address setup time	t <sub>AS</sub>	0	—	ns	6
Write recovery time	t <sub>WR</sub>	0	—	ns	7
Data to write time overlap	t <sub>DW</sub>	6	—	ns	
Data hold from write time	t <sub>DH</sub>	0	—	ns	
Write disable to output in low-Z	t <sub>OW</sub>	3	—	ns	1
Output disable to output in high-Z	t <sub>OZH</sub>	—	6	ns	1
Write enable to output in high-Z	t <sub>WHZ</sub>	—	6	ns	1

Notes: 1. Transition is measured  $\pm 200\text{mV}$  from steady voltage with output load (B). This parameter is sampled and not 100% tested.

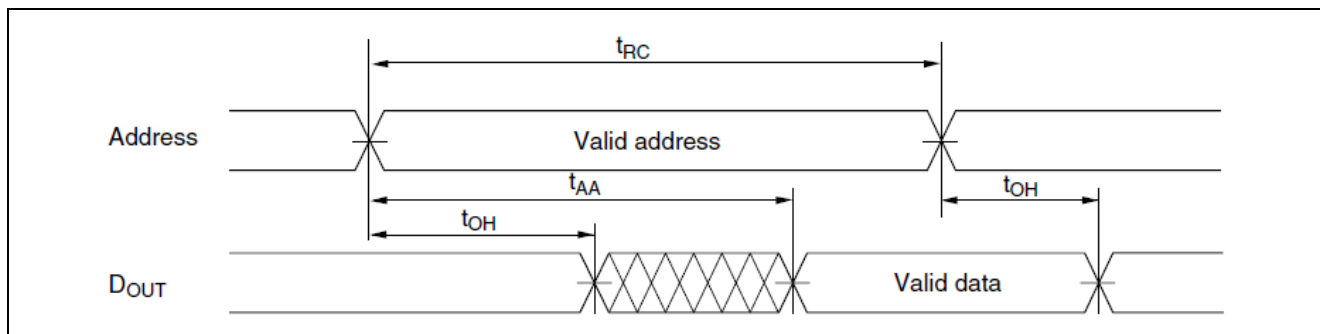
2. Address should be valid prior to or coincident with CS# transition low.
3. WE# and/or CS# must be high during address transition time.
4. If CS# and OE# are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
5. If the CS# low transition occurs simultaneously with the WE# low transition or after the WE# transition, output remains a high impedance state.
6. t<sub>AS</sub> is measured from the latest address transition to the later of CS# or WE# going low.
7. t<sub>WR</sub> is measured from the earlier of CS# or WE# going high to the first address transition.
8. A write occurs during the overlap of a low CS# and a low WE#. A write begins at the latest transition among CS# going low and WE# going low. A write ends at the earliest transition among CS# going high and WE# going high. t<sub>WP</sub> is measured from the beginning of write to the end of write.
9. t<sub>CW</sub> is measured from the later of CS# going low to the end of write.

## Timing Waveforms

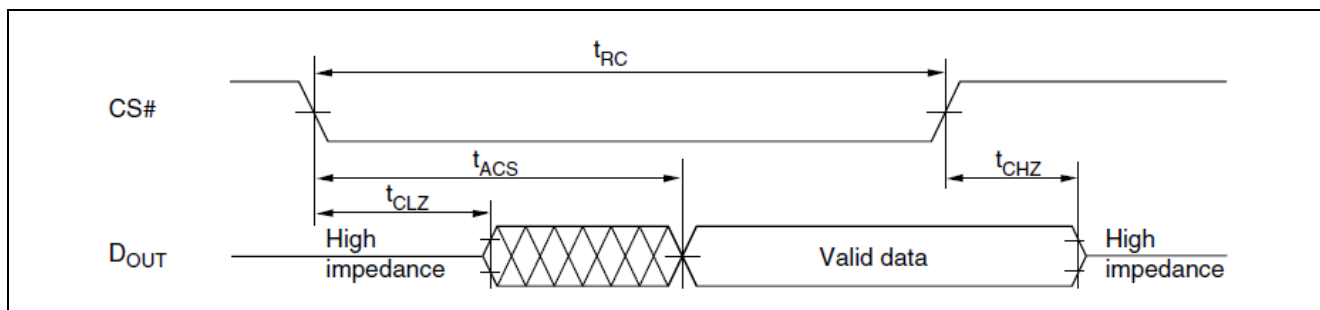
Read Timing Waveform (1) ( $WE\# = V_{IH}$ )



Read Timing Waveform (2) ( $WE\# = V_{IH}$ ,  $LB\# = V_{IL}$ ,  $UB\# = V_{IL}$ )

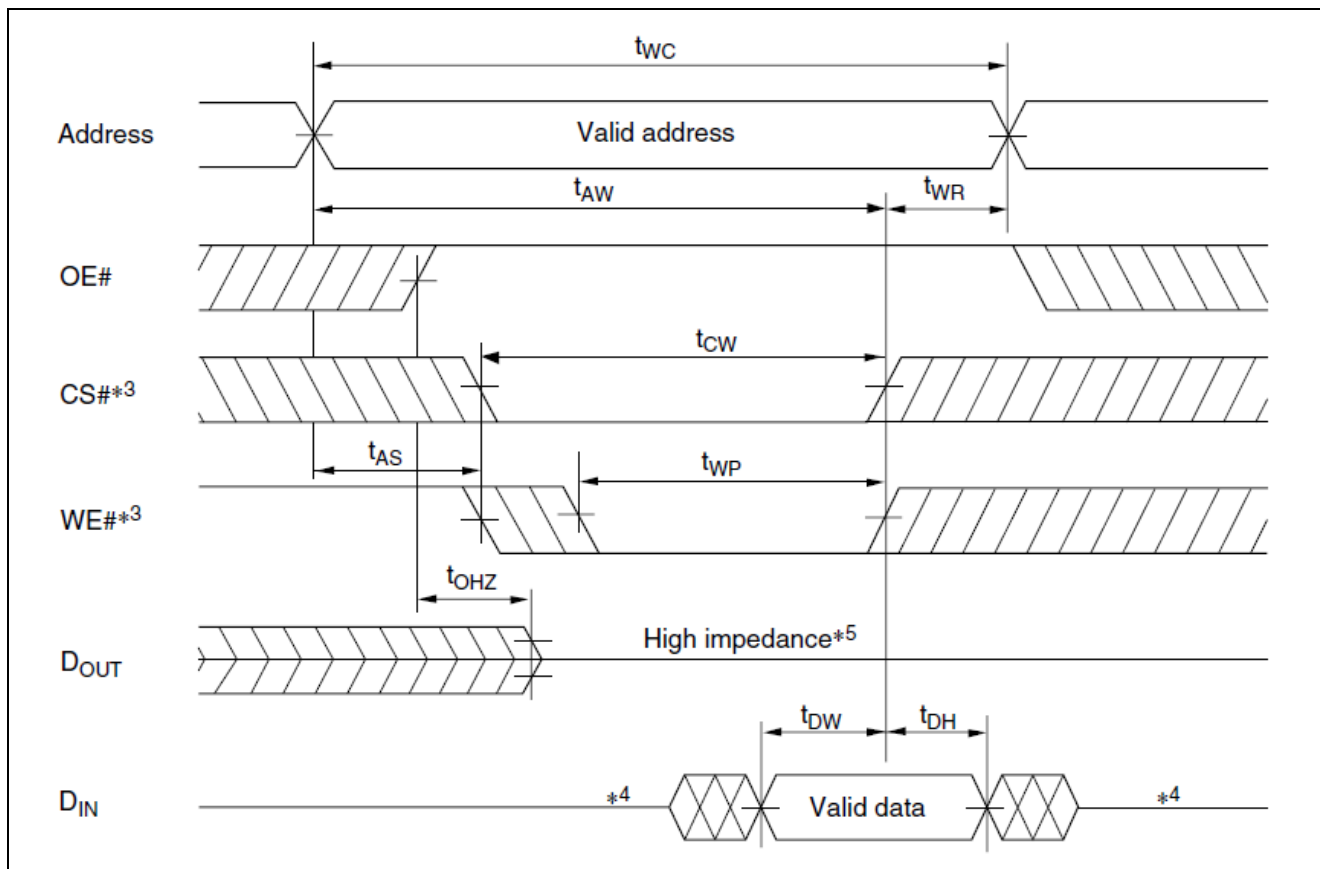


Read Timing Waveform (3) ( $WE\# = V_{IH}$ ,  $CS\# = V_{IL}$ ,  $OE\# = V_{IL}$ )\*2

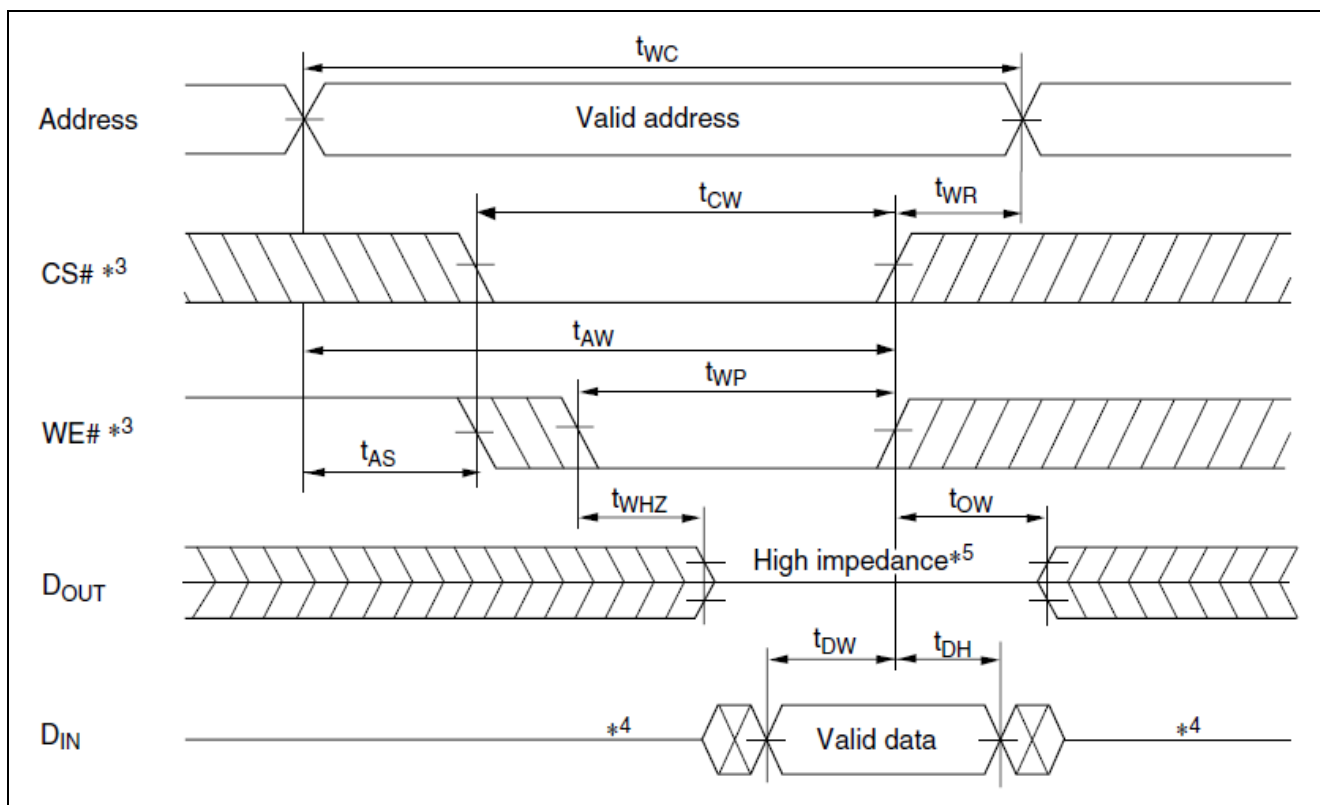




## Write Timing Waveform (1) (WE# Controlled)



## Write Timing Waveform (2) (CS# Controlled)



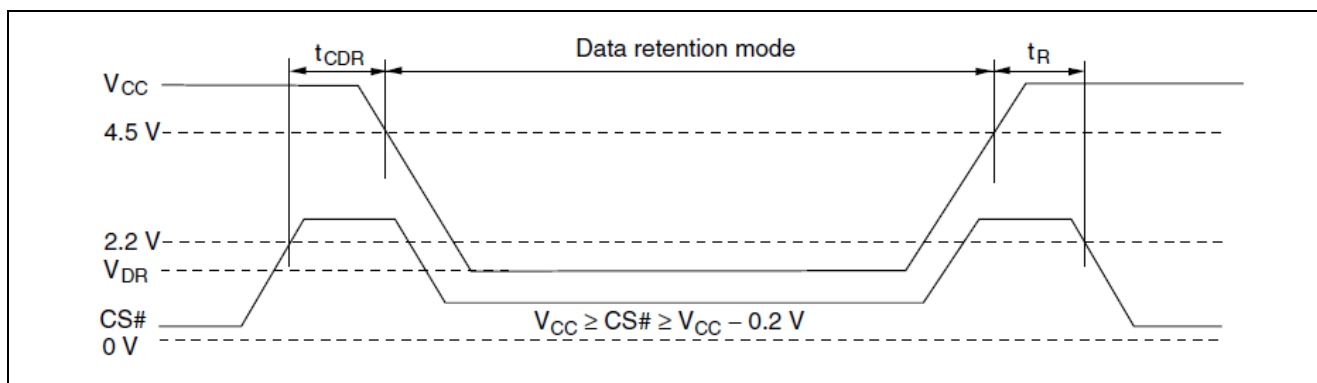
## Low $V_{CC}$ Data Retention Characteristics

(Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Max	Unit	Test conditions
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	V	$V_{CC} \geq CS\# \geq V_{CC} - 0.2V$ , (1) $0V \leq V_{IN} \leq 0.2V$ or (2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2V$
Data retention current	$I_{CCDR}$	—	500	$\mu A$	$V_{CC} = 3V$ $V_{CC} \geq CS\# \geq V_{CC} - 0.2V$ , (1) $0V \leq V_{IN} \leq 0.2V$ or (2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2V$
Chip deselect to data retention time	$t_{CDR}$	0	—	ns	See retention waveform
Operation recovery time	$t_R$	5	—	ms	

### Low $V_{CC}$ Data Retention Timing Waveform



**Revision History**

Rev.	Date	Description	
		Page	Summary
1.00	Nov.18.19	-	First Edition issued

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

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