

# R1LP0408D Series

4Mb Advanced LPSRAM (512-kword × 8-bit)

R10DS0274EJ0200

Rev.2.00

2019.10.29

## Description

The R1LP0408D Series is a family of 4-Mbit static RAMs organized 512-kword × 8-bit, fabricated by Renesas's high-performance CMOS and TFT technologies. The R1LP0408D Series has realized higher density, higher performance and low power consumption. The R1LP0408D Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 32-pin SOP and 32-pin TSOP.

## Features

- Single 5V supply: 4.5V to 5.5V
- Access time: 55ns (max.)
- Power dissipation:
  - Standby: 4μW (typ.)
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Battery backup operation

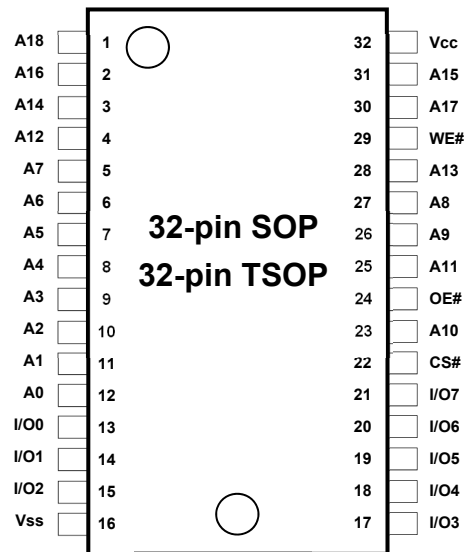
## Ordering Information

Orderable part name	Access time	Temperature range	Package	Shipping container
R1LP0408DSP-5SI#B*	55 ns	-40 ~ +85°C	525-mil 32-pin plastic SOP	Tube (Magazine)
R1LP0408DSP-5SI#S*				Embossed tape
R1LP0408DSB-5SI#B*			400-mil 32-pin plastic TSOP (II)	Tray
R1LP0408DSB-5SI#S*				Embossed tape

Note 1. \* = Revision code for Assembly site change, etc. (\* = 0, 1, etc.)



## Pin Arrangement

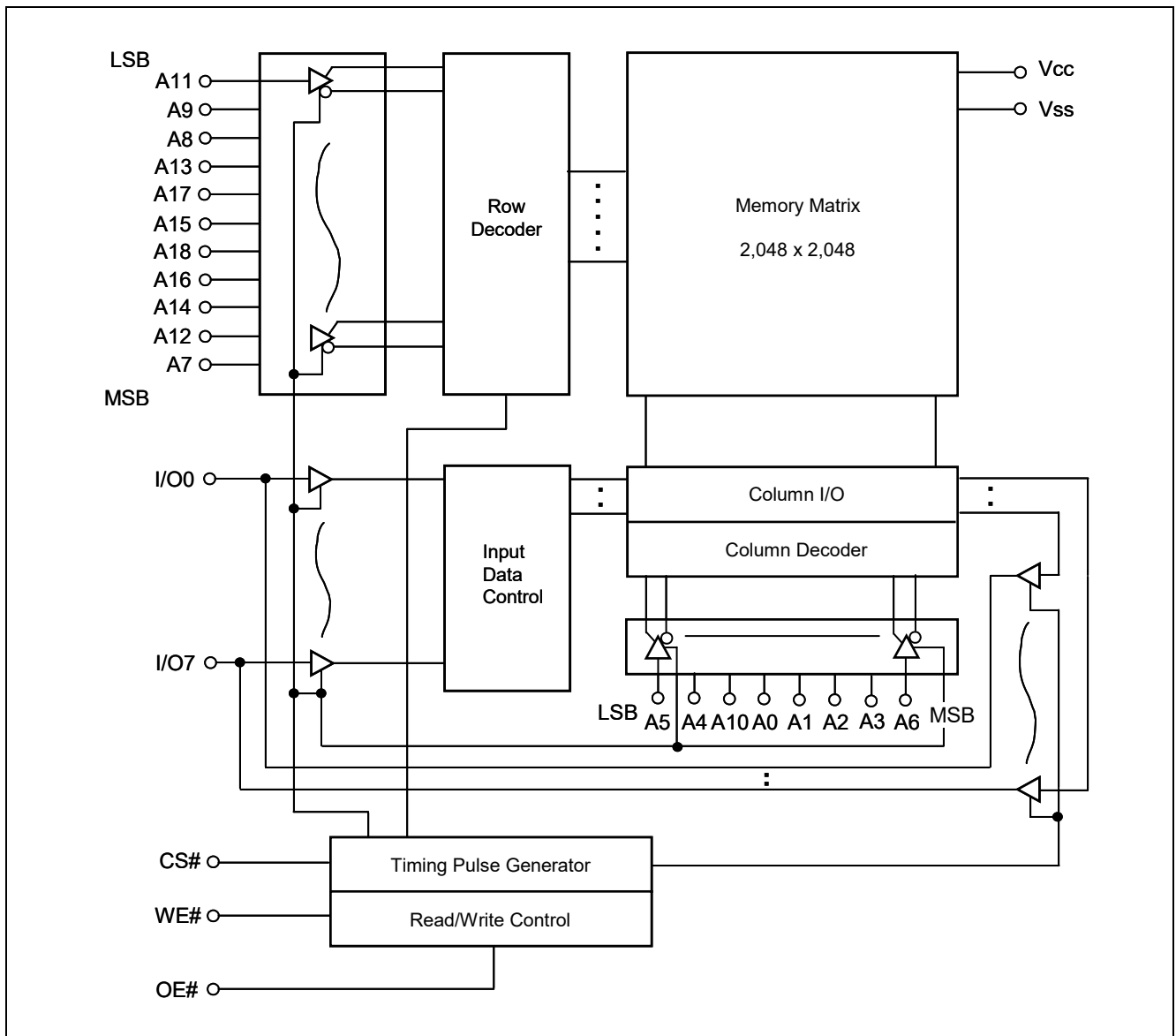


## Pin Description

Pin name	Function
Vcc	Power supply
Vss	Ground
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CS#	Chip select
WE#	Write enable
OE#	Output enable



## Block Diagram





## Operation Table

WE#	CS#	OE#	Mode	Vcc current	I/O0 to I/O7	Ref. cycle
x	H	x	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
H	L	H	Output disable	$I_{CC}$	High-Z	—
H	L	L	Read	$I_{CC}$	Dout	Read cycle
L	L	H	Write	$I_{CC}$	Din	Write cycle (1)
L	L	L	Write	$I_{CC}$	Din	Write cycle (2)

Note 1. H:  $V_{IH}$  L:  $V_{IL}$  x:  $V_{IH}$  or  $V_{IL}$

## Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to Vss	$V_{CC}$	-0.5 to +7.0	V
Terminal voltage on any pin relative to Vss	$V_T$	$-0.5^{*1}$ to $V_{CC}+0.3^{*2}$	V
Power dissipation	$P_T$	0.7	W
Operation temperature	$T_{opr}$	-40 to +85	°C
Storage temperature range	$T_{stg}$	-65 to 150	°C
Storage temperature range under bias	$T_{bias}$	-40 to +85	°C

Note 1. -3.0V for pulse  $\leq 30$ ns (full width at half maximum)

2. Maximum voltage is +7.0V.



## DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	
	V <sub>SS</sub>	0	0	0	V	
Input high voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> +0.3	V	
Input low voltage	V <sub>IL</sub>	-0.3	—	0.8	V	1
Ambient temperature range	T <sub>a</sub>	-40	—	+85	°C	

Note 1. -3.0V for pulse ≤ 30ns (full width at half maximum)

## DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Input leakage current	I <sub>LI</sub>	—	—	1	μA	Vin = Vss to Vcc	
Output leakage current	I <sub>LO</sub>	—	—	1	μA	CS# =V <sub>IH</sub> or OE# =V <sub>IH</sub> , V <sub>I/O</sub> =Vss to Vcc	
Operating current	I <sub>CC</sub>	—	5* <sup>1</sup>	10	mA	CS# =V <sub>IL</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	
Average operating current	I <sub>CC1</sub>	—	15* <sup>1</sup>	25	mA	Min. cycle, duty =100%, I <sub>I/O</sub> = 0mA, CS# =V <sub>IL</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub>	
	I <sub>CC2</sub>	—	3* <sup>1</sup>	5	mA	Cycle =1μs, duty =100%, I <sub>I/O</sub> = 0mA, CS# ≤ 0.2V, V <sub>IH</sub> ≥ Vcc-0.2V, V <sub>IL</sub> ≤ 0.2V	
Standby current	I <sub>SB</sub>	—	0.1* <sup>1</sup>	0.5	mA	CS# =V <sub>IH</sub> , Others = Vss to Vcc	
Standby current	I <sub>SB1</sub>	—	0.8* <sup>1</sup>	2.5	μA	~+25°C	Vin = Vss to Vcc, CS# ≥ Vcc-0.2V
		—	1* <sup>2</sup>	3	μA	~+40°C	
		—	—	8	μA	~+70°C	
		—	—	10	μA	~+85°C	
Output high voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -1mA	
	V <sub>OH2</sub>	Vcc-0.5	—	—	V	I <sub>OH</sub> = -0.1mA	
Output low voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 2.1mA	

Note 1. Typical parameter indicates the value for the center of distribution at 5.0V (T<sub>a</sub>=25°C), and not 100% tested.

2. Typical parameter indicates the value for the center of distribution at 5.0V (T<sub>a</sub>=40°C), and not 100% tested.

## Capacitance

(V<sub>CC</sub> = 4.5V ~ 5.5V, f = 1MHz, T<sub>a</sub> = -40 ~ +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C <sub>in</sub>	—	—	8	pF	V <sub>in</sub> = 0V	1
Input / output capacitance	C <sub>I/O</sub>	—	—	10	pF	V <sub>I/O</sub> = 0V	1

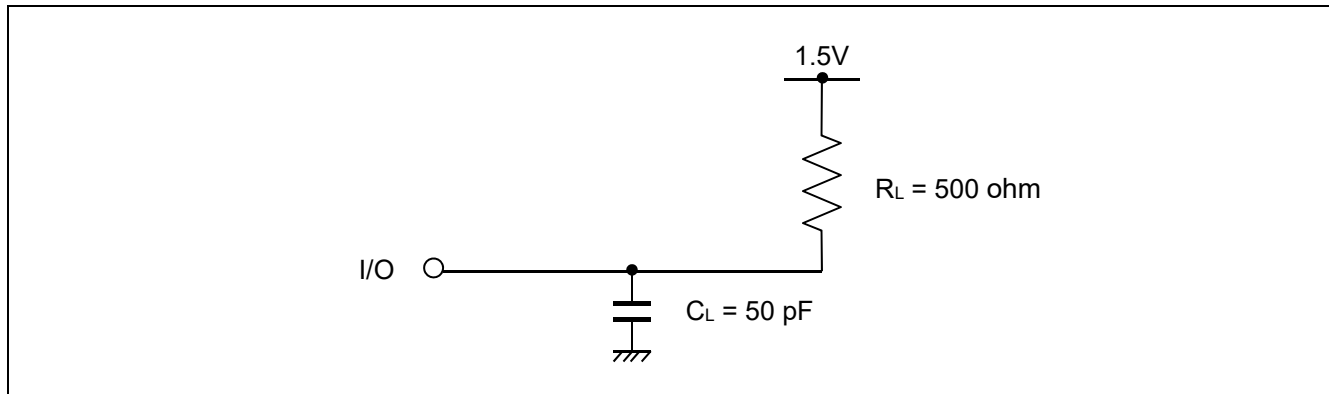
Note 1. This parameter is sampled and not 100% tested.



## AC Characteristics

Test Conditions ( $V_{CC} = 4.5V \sim 5.5V$ ,  $T_a = -40 \sim +85^{\circ}C$ )

- Input pulse levels:  $V_{IL} = 0.4V$ ,  $V_{IH} = 2.4V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.5V
- Output load: See figures (Including scope and jig)





**Read Cycle**

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	$t_{RC}$	55	—	ns	
Address access time	$t_{AA}$	—	55	ns	
Chip select access time	$t_{ACS}$	—	55	ns	
Output enable to output valid	$t_{OE}$	—	25	ns	
Chip select to output in low-Z	$t_{CLZ}$	10	—	ns	2
Output enable to output in low-Z	$t_{OLZ}$	5	—	ns	2
Chip deselect to output in high-Z	$t_{CHZ}$	0	20	ns	1,2
Output disable to output in high-Z	$t_{OHZ}$	0	20	ns	1,2
Output hold from address change	$t_{OH}$	10	—	ns	

**Write Cycle**

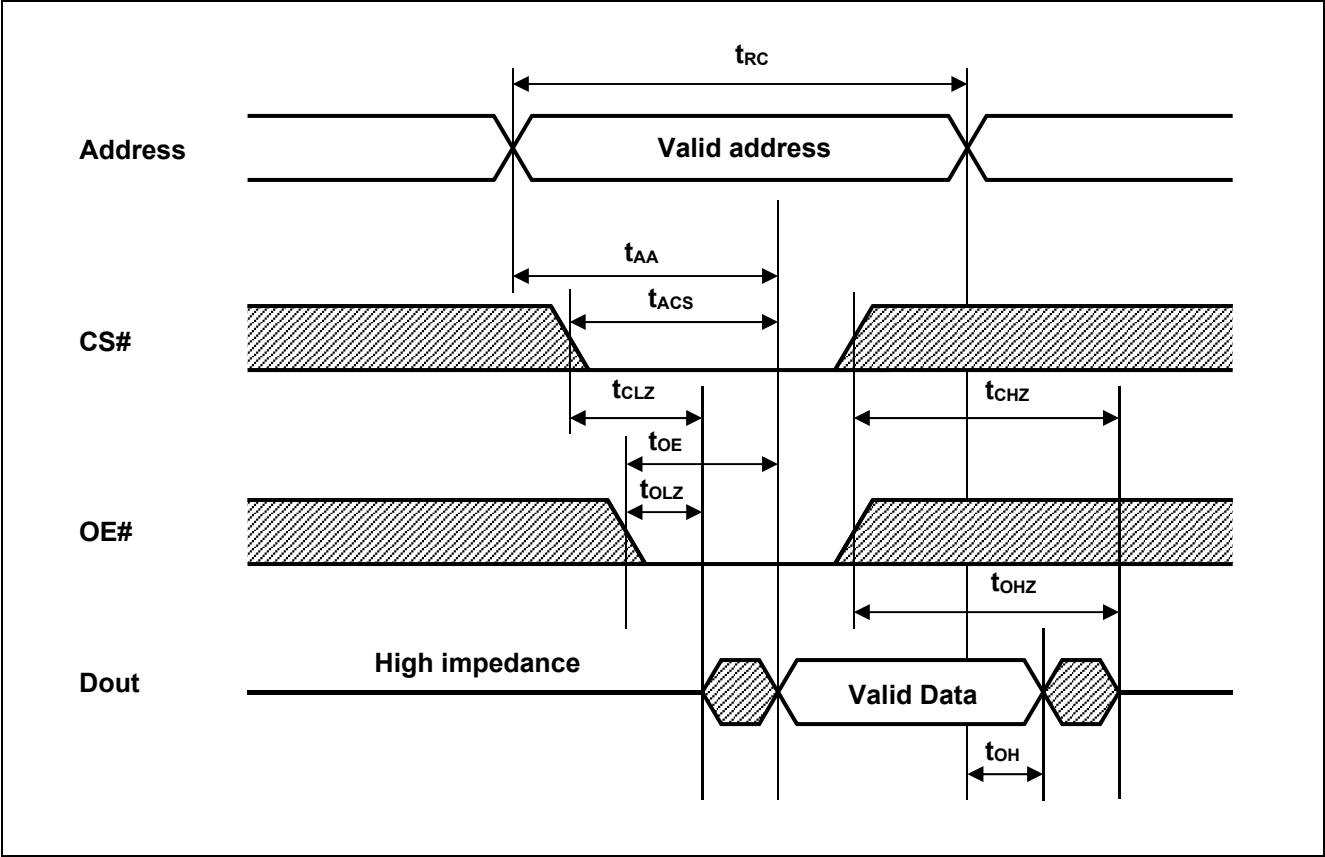
Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	$t_{WC}$	55	—	ns	
Chip select to end of write	$t_{CW}$	50	—	ns	4
Address setup time	$t_{AS}$	0	—	ns	5
Address valid to end of write	$t_{AW}$	50	—	ns	
Write pulse width	$t_{WP}$	40	—	ns	3,12
Write recovery time	$t_{WR}$	0	—	ns	6
Write to output in high-Z	$t_{WHZ}$	0	20	ns	1,2,7
Data to write time overlap	$t_{DW}$	25	—	ns	
Data hold from write time	$t_{DH}$	0	—	ns	
Output enable from end of write	$t_{OW}$	5	—	ns	2
Output disable to output in high-Z	$t_{OHZ}$	0	20	ns	1,2,7

- Note
1.  $t_{CHZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  2. This parameter is sampled and not 100% tested.
  3. A write occurs during the overlap ( $t_{WP}$ ) of a low CS# and a low WE#.  
A write begins at the later transition of CS# going low or WE# going low.  
A write ends at the earlier transition of CS# going high or WE# going high.  
 $t_{WP}$  is measured from the beginning of write to the end of write.
  4.  $t_{CW}$  is measured from CS# going low to end of write.
  5.  $t_{AS}$  is measured the address valid to the beginning of write.
  6.  $t_{WR}$  is measured from the earlier of WE# or CS# going high to the end of write cycle.
  7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
  8. If the CS# low transition occurs simultaneously with the WE# low transition or after the WE# transition, the output remain in a high impedance state.
  9. Dout is the same phase of the write data of this write cycle.
  10. Dout is the read data of next address.
  11. If CS# is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
  12. In the write cycle with OE# low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.  
$$t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$$



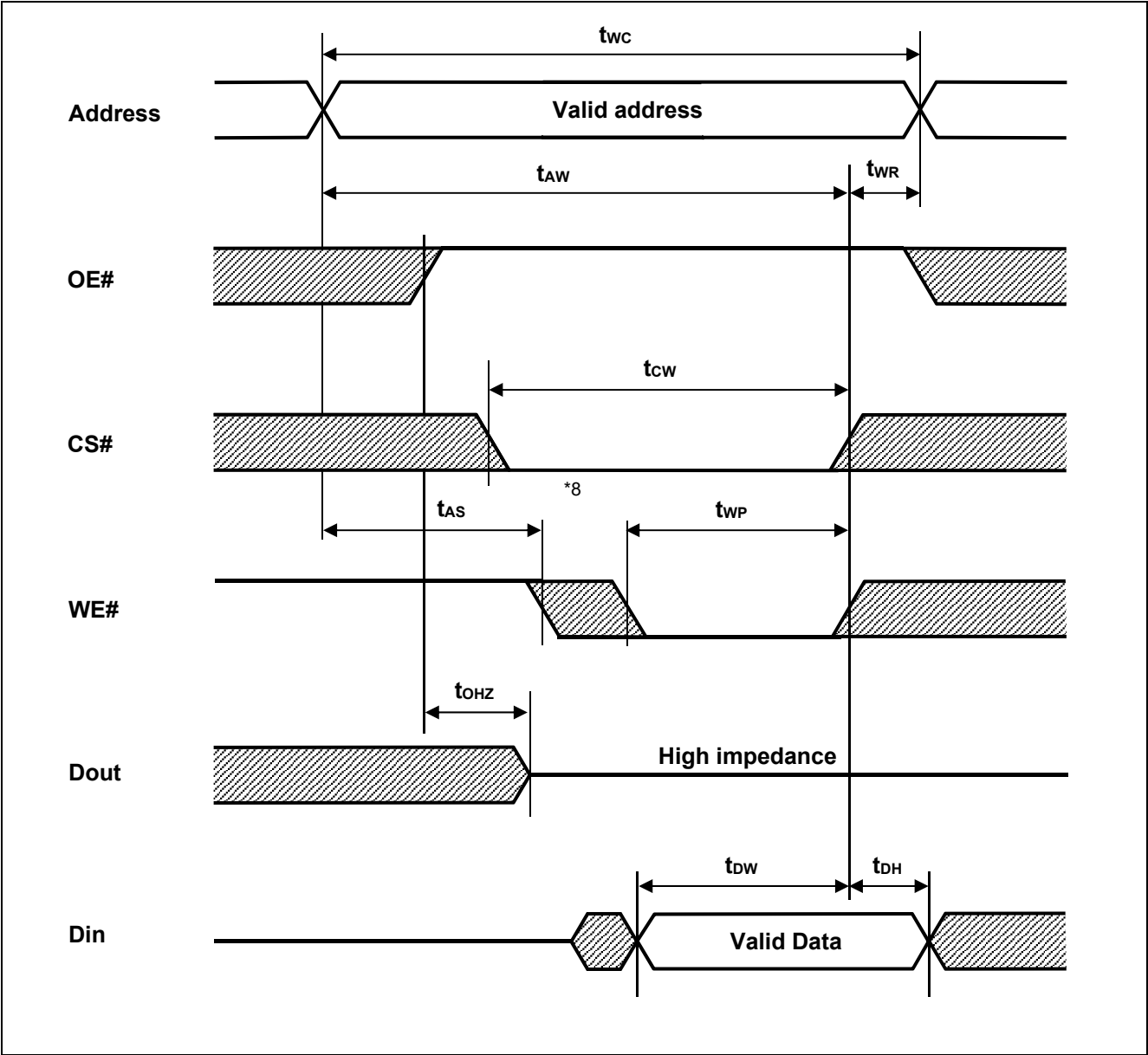
# Timing Waveforms

Read Cycle (WE# = V<sub>IH</sub>)



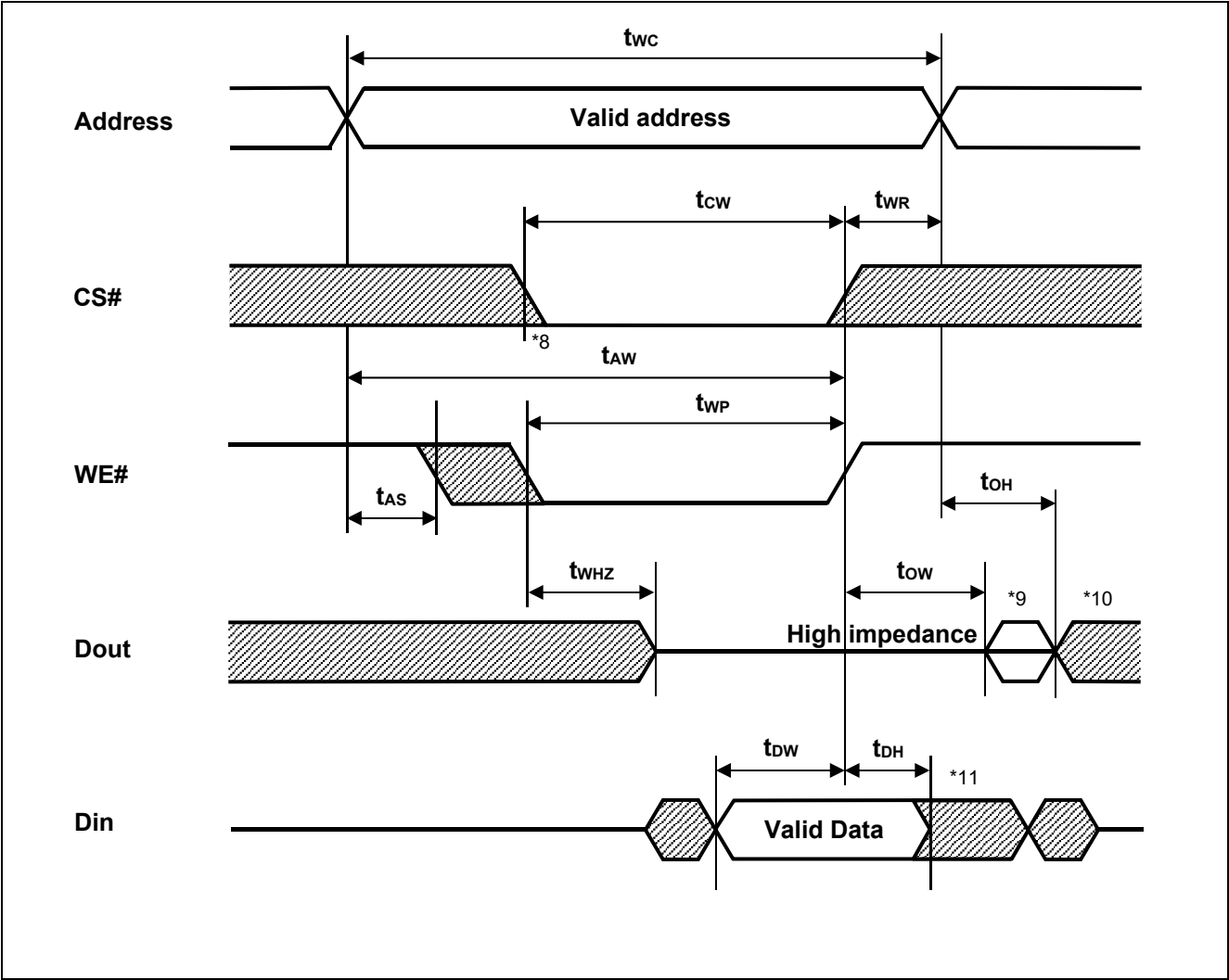


Write Cycle (1) (OE# CLOCK)





Write Cycle (2) (OE# Low Fixed)





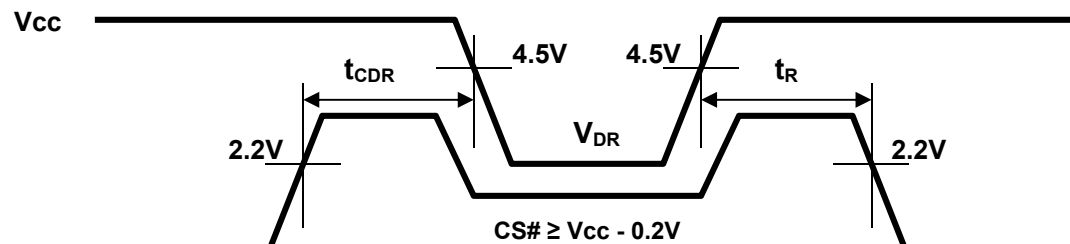
## Low Vcc Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions <sup>*3</sup>	
V <sub>CC</sub> for data retention	V <sub>DR</sub>	2.0	—	5.5	V	Vin ≥ 0V, CS# ≥ V <sub>CC</sub> -0.2V	
Data retention current	I <sub>CCDR</sub>	—	0.8 <sup>*1</sup>	2.5	μA	~+25°C	V <sub>CC</sub> =3.0V, Vin ≥ 0V, CS# ≥ V <sub>CC</sub> -0.2V
		—	1 <sup>*2</sup>	3	μA	~+40°C	
		—	—	8	μA	~+70°C	
		—	—	10	μA	~+85°C	
Chip deselect time to data retention	t <sub>CDR</sub>	0	—	—	ns	See retention waveform.	
Operation recovery time	t <sub>R</sub>	5	—	—	ms		

- Note
1. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25°C), and not 100% tested.
  2. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=40°C), and not 100% tested.
  3. CS# controls address buffer, WE# buffer, OE# buffer and Din buffer. If data retention mode, V<sub>in</sub> levels (address, WE#, OE#, I/O) can be in the high impedance state.

## Low Vcc Data Retention Timing Waveforms

### CS# Controlled





Revision History	R1LP0408D Series Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	2017.1.27	—	First Edition issued
2.00	2019.10.29	p.1	Revised orderable part name information.



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