R1LP0108E Series

1Mb Advanced LPSRAM (128k word x 8bit)

Description

The R1LP0108E Series is a family of low voltage 1-Mbit static RAMs organized as 131,072-word by 8-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies. The R1LP0108E Series has realized higher density, higher performance and low power consumption. The R1LP0108E Series is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives. It has been packaged in 32-pin SOP, 32-pin TSOP and 32-pin sTSOP.
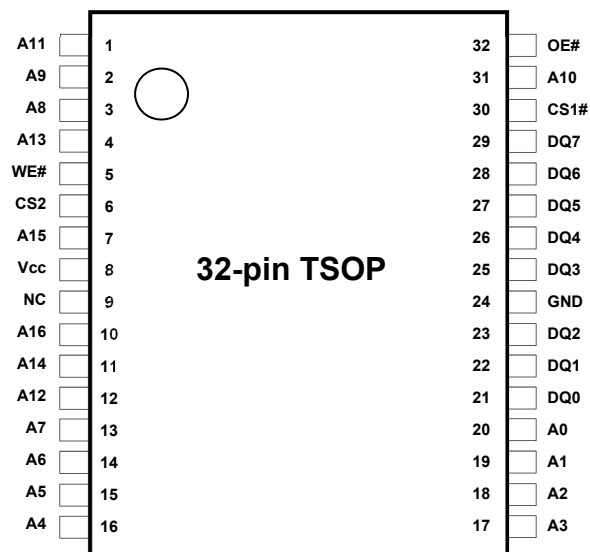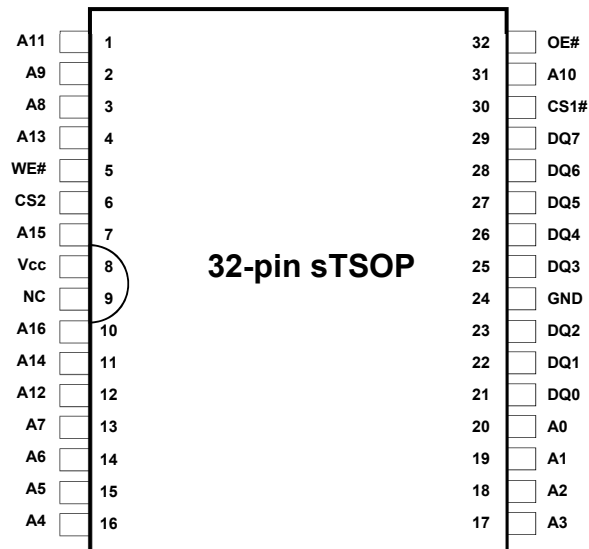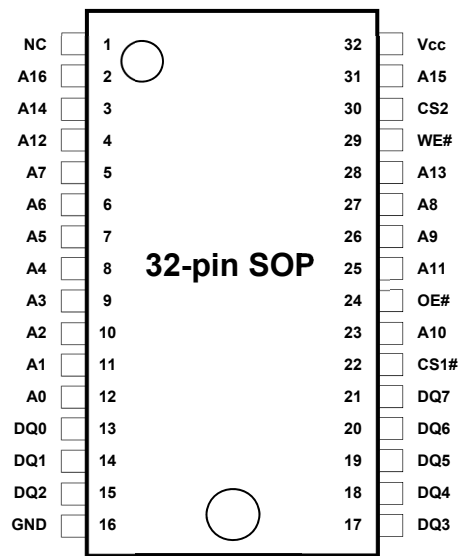
Features

- Single 4.5V~5.5V power supply
- Small stand-by current: 0.6µA (5.0V, typical)
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion by CS1# and CS2
- Common Data I/O
- Three-state outputs: OR-tie Capability
- OE# prevents data contention on the I/O bus

Ordering Information

Orderable part name	Access time	Temperature range	Package	Shipping container
R1LP0108ESN-5SI#B∗	55 ns	-40 ~ +85°C	525-mil 32-pin plastic SOP	Tube (Magazine)
R1LP0108ESN-5SI#S∗				Embossed tape
R1LP0108ESA-5SI#B∗			8mm×13.4mm 32-pin plastic sTSOP	Tray
R1LP0108ESA-5SI#S∗				Embossed tape
R1LP0108ESF-5SI#B∗			8mm×20mm 32-pin plastic TSOP	Tray
R1LP0108ESF-5SI#S∗				Embossed tape

Note 1.   ∗ = Revision code for Assembly site change, etc. (∗ = 0, 1, etc.)

Pin Arrangement

32-pin SOP

Pin	Signal		Pin	Signal
1	NC		32	Vcc
2	A16		31	A15
3	A14		30	CS2
4	A12		29	WE#
5	A7		28	A13
6	A6		27	A8
7	A5		26	A9
8	A4		25	A11
9	A3		24	OE#
10	A2		23	A10
11	A1		22	CS1#
12	A0		21	DQ7
13	DQ0		20	DQ6
14	DQ1		19	DQ5
15	DQ2		18	DQ4
16	GND		17	DQ3

32-pin sTSOP

Pin	Signal		Pin	Signal
1	A11		32	OE#
2	A9		31	A10
3	A8		30	CS1#
4	A13		29	DQ7
5	WE#		28	DQ6
6	CS2		27	DQ5
7	A15		26	DQ4
8	Vcc		25	DQ3
9	NC		24	GND
10	A16		23	DQ2
11	A14		22	DQ1
12	A12		21	DQ0
13	A7		20	A0
14	A6		19	A1
15	A5		18	A2
16	A4		17	A3

32-pin TSOP

Pin	Signal		Pin	Signal
1	A11		32	OE#
2	A9		31	A10
3	A8		30	CS1#
4	A13		29	DQ7
5	WE#		28	DQ6
6	CS2		27	DQ5
7	A15		26	DQ4
8	Vcc		25	DQ3
9	NC		24	GND
10	A16		23	DQ2
11	A14		22	DQ1
12	A12		21	DQ0
13	A7		20	A0
14	A6		19	A1
15	A5		18	A2
16	A4		17	A3

Pin Description

Pin name	Function
Vcc	Power supply
Vss (GND)	Ground
A0 to A16	Address input
DQ0 to DQ7	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
WE#	Write enable
OE#	Output enable
NC	Non connection

Block Diagram
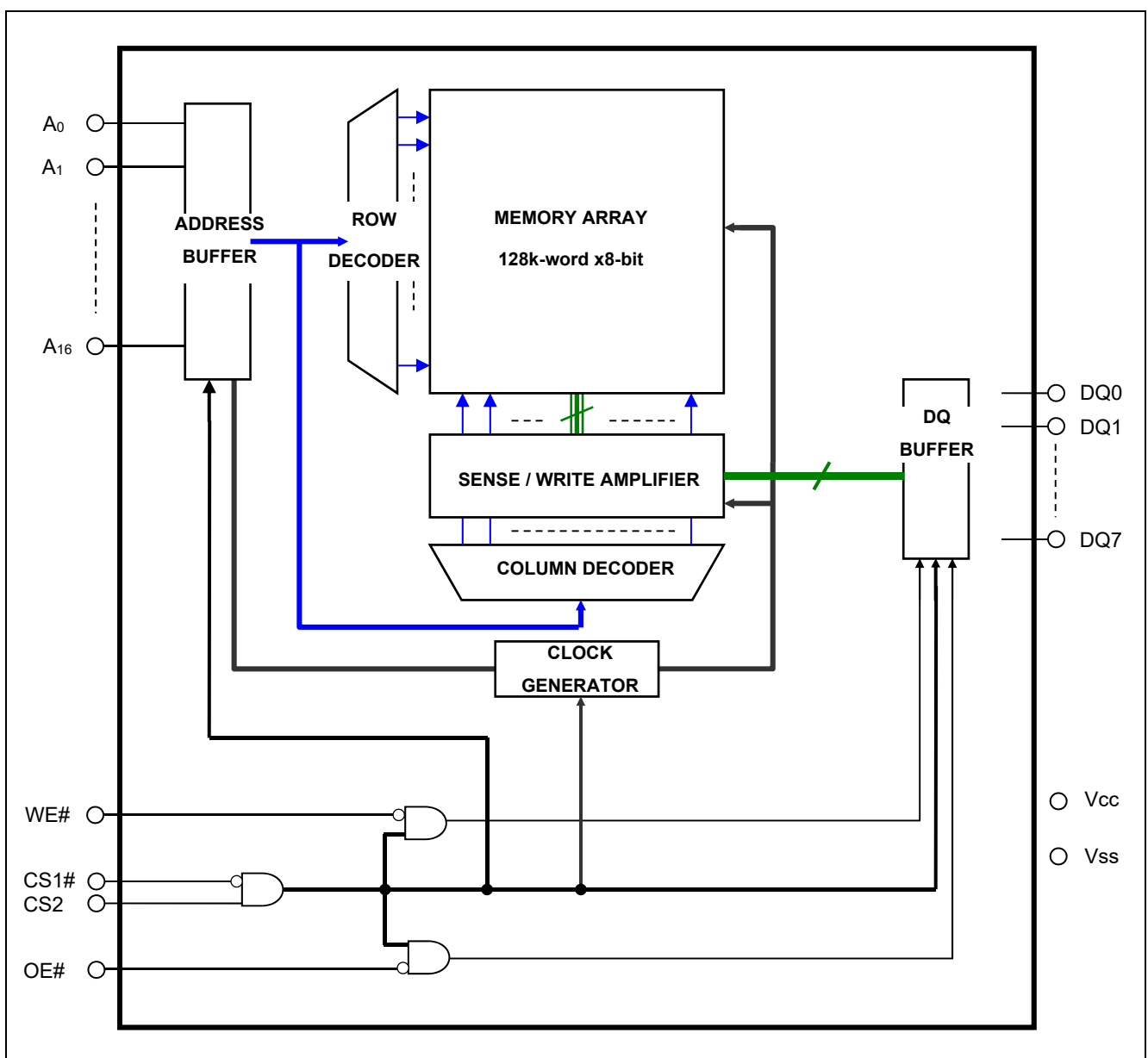
Operation Table

CS1#	CS2	WE#	OE#	DQ0~7	Operation
X	L	X	X	High-Z	Stand-by
H	X	X	X	High-Z	Stand-by
L	H	L	X	Din	Write
L	H	H	L	Dout	Read
L	H	H	H	High-Z	Output disable

Note 1.   H: V_{IH} L:V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum

Parameter	Symbol	Value	unit
Power supply voltage relative to Vss	Vcc	-0.3 to +7.0	V
Terminal voltage on any pin relative to Vss	V_T	-0.3[*1] to Vcc+0.3[*2]	V
Power dissipation	P_T	0.7	W
Operation temperature	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to 150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Note   1.   −3.0V for pulse ≤ 30ns (full width at half maximum)

2.   Maximum voltage is +7.0V.

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DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	Vcc	4.5	5.0	5.5	V	
	Vss	0	0	0	V	
Input high voltage	V_{IH}	2.2	-	Vcc+0.3	V	
Input low voltage	V_{IL}	-0.3	-	0.8	V	1
Ambient temperature range	Ta	-40	-	+85	°C	

Note   1.   –3.0V for pulse ≤ 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Input leakage current	$|I_{LI}|$	-	-	1	μA	Vin = Vss to Vcc
Output leakage current	$|I_{LO}|$	-	-	1	μA	CS1# =V_{IH} or CS2 =V_{IL} or OE# =V_{IH}, VI/O =Vss to Vcc
Average operating current	I_{CC1}	-	25	35	mA	Min. cycle, duty =100%, II/O = 0mA, CS1# =V_{IL}, CS2 =V_{IH}, Others = V_{IH}/V_{IL}
	I_{CC2}	-	2	5	mA	Cycle =1μs, duty =100%, II/O = 0mA, CS1# ≤ 0.2V, CS2 ≥ Vcc-0.2V, V_{IH} ≥ Vcc-0.2V, V_{IL} ≤ 0.2V
Standby current	I_{SB}	-	-	3	mA	"CS2 =V_{IL}" or "CS2 = V_{IH} and CS1# =V_{IH}", Others = Vss to Vcc
Standby current	I_{SB1}	-	0.6[*1]	2	μA	~+25°C · Vin = Vss to Vcc,
		-	-	3	μA	~+40°C · (1) CS2 ≤ 0.2V or
		-	-	8	μA	~+70°C · (2) CS1# ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V
		-	-	10	μA	~+85°C
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -1mA
	V_{OH2}	Vcc - 0.5	-	-	V	I_{OH} = -0.1mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA

Note   1.   Typical parameter indicates the value for the center of distribution at 5.0V (Ta= 25ºC), and not 100% tested.

Capacitance

(Vcc = 4.5V ~ 5.5V, f = 1MHz, Ta = -40 ~ +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	-	-	8	pF	Vin =0V	1
Input / output capacitance	C I/O	-	-	10	pF	VI/O =0V	1

Note   1.   This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc = 4.5V ~ 5.5V, Ta = -40 ~ +85°C)

- Input pulse levels: VIL = 0.6V, VIH = 2.4V
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.5V
- Output load: See figures (Including scope and jig)
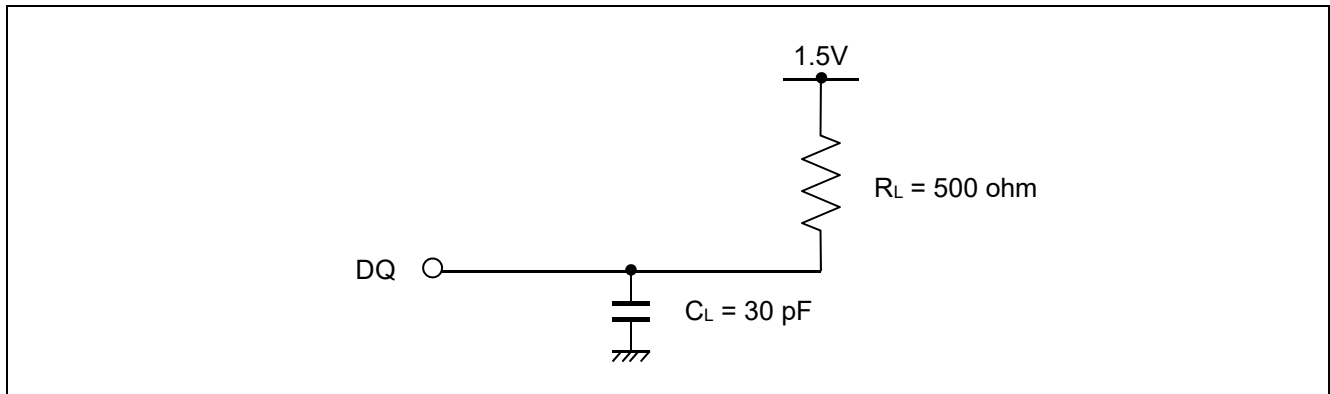
Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	t_{RC}	55	-	ns	
Address access time	t_{AA}	-	55	ns	
Chip select access time	t_{ACS1}	-	55	ns	
	t_{ACS2}	-	55	ns	
Output enable to output valid	t_{OE}	-	30	ns	
Output hold from address change	t_{OH}	5	-	ns	
Chip select to output in low-Z	t_{CLZ1}	5	-	ns	2,3
	t_{CLZ2}	5	-	ns	2,3
Output enable to output in low-Z	t_{OLZ}	5	-	ns	2,3
Chip deselect to output in high-Z	t_{CHZ1}	0	20	ns	1,2,3
	t_{CHZ2}	0	20	ns	1,2,3
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1,2,3

Write Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	t_{WC}	55	-	ns	
Address valid to end of write	t_{AW}	50	-	ns	
Chip select to end of write	t_{CW}	50	-	ns	5
Write pulse width	t_{WP}	45	-	ns	4
Address setup time	t_{AS}	0	-	ns	6
Write recovery time	t_{WR}	0	-	ns	7
Data to write time overlap	t_{DW}	25	-	ns	
Data hold from write time	t_{DH}	0	-	ns	
Output enable from end of write	t_{OW}	5	-	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1,2
Write to output in high-Z	t_{WHZ}	0	20	ns	1,2

Note
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE#.
   A write begins at the latest transition among CS1# going low, CS2 going high and WE# going low.
   A write ends at the earliest transition among CS1# going high, CS2 going low and WE# going high.
   t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of CS1# going low or CS2 going high to end of write.
6. t_{AS} is measured the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.
8. Don't apply inverted phase signal externally when DQ pin is output mode.
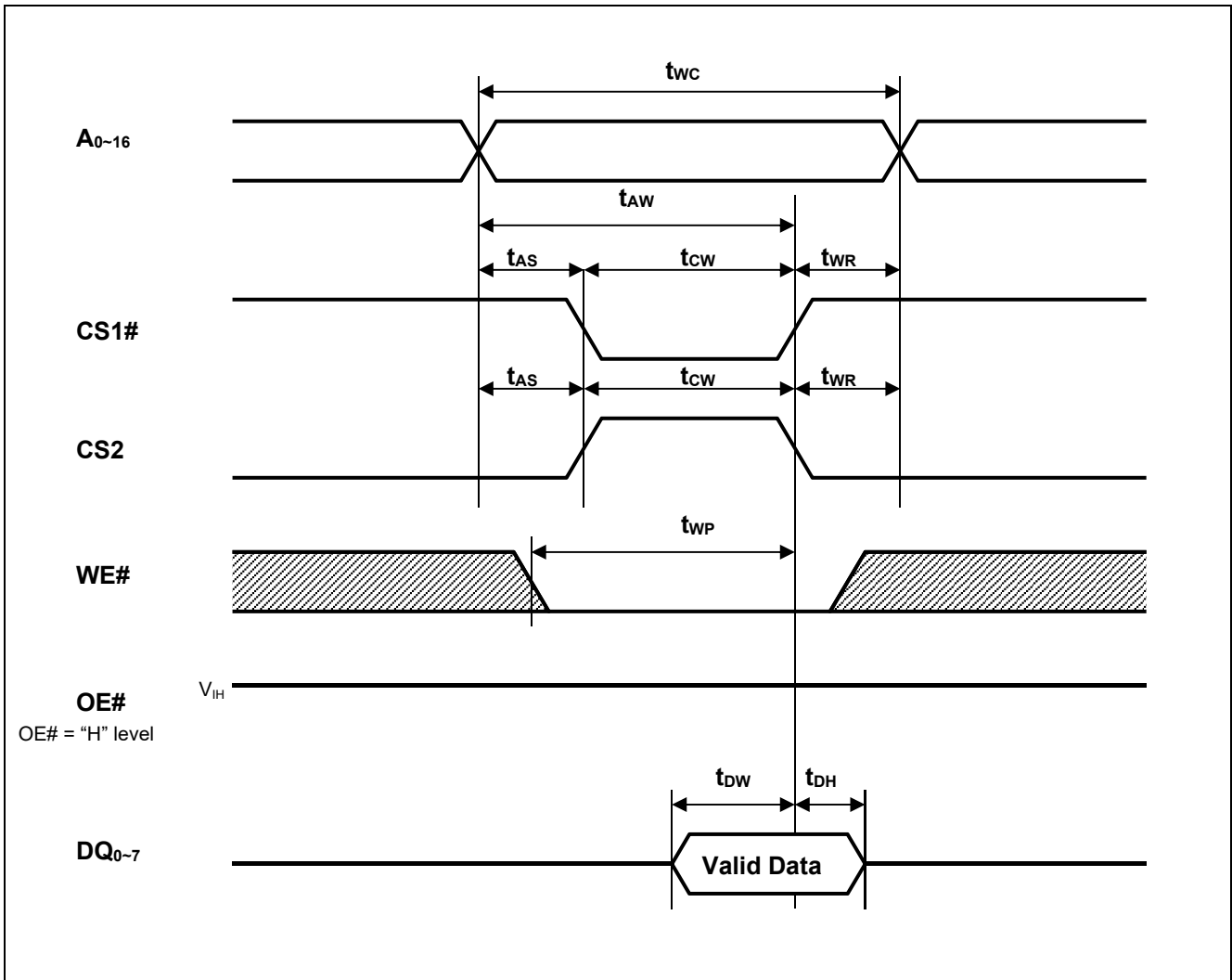
Timing Waveforms

Read Cycle
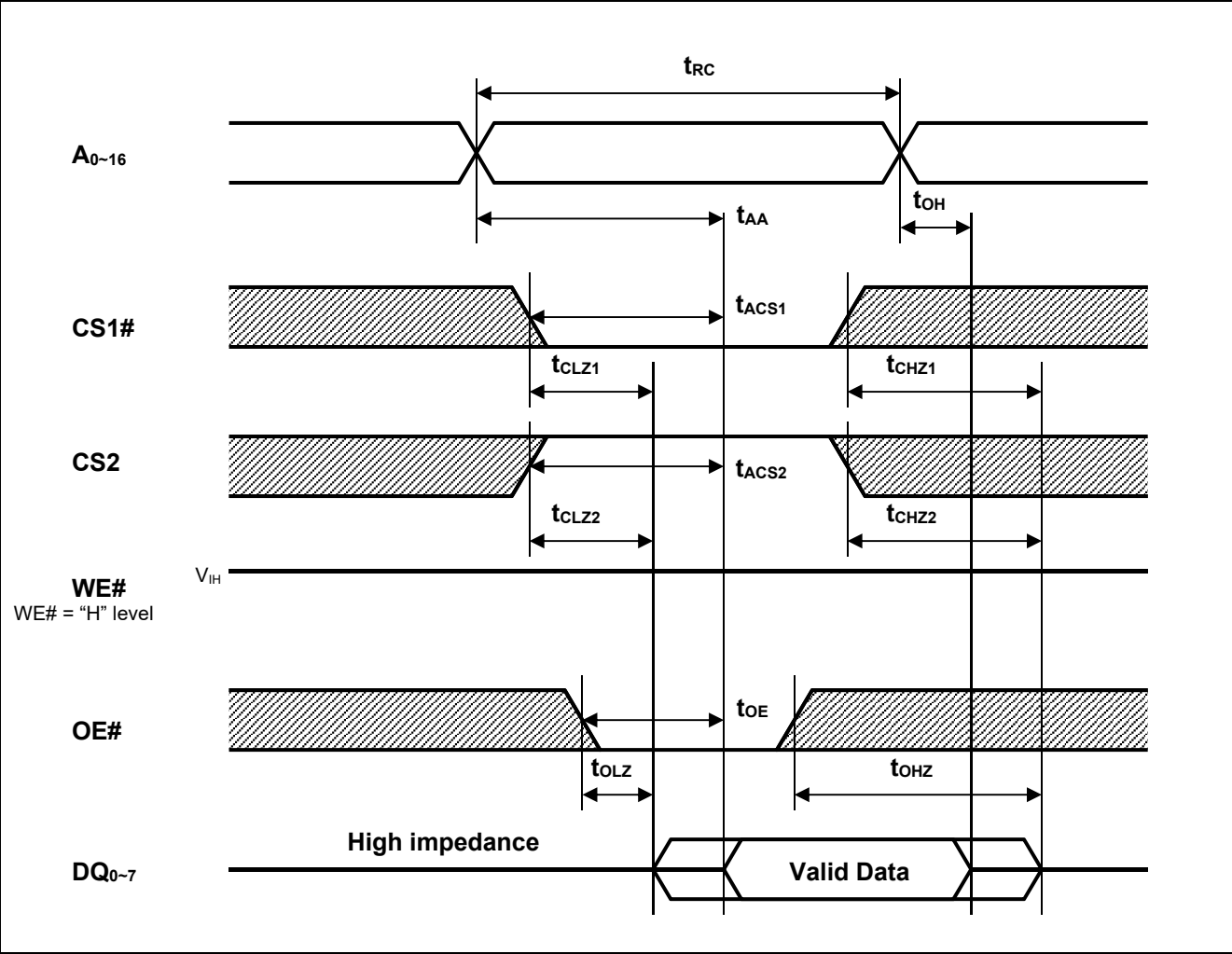
Write Cycle (1) (WE# CLOCK)
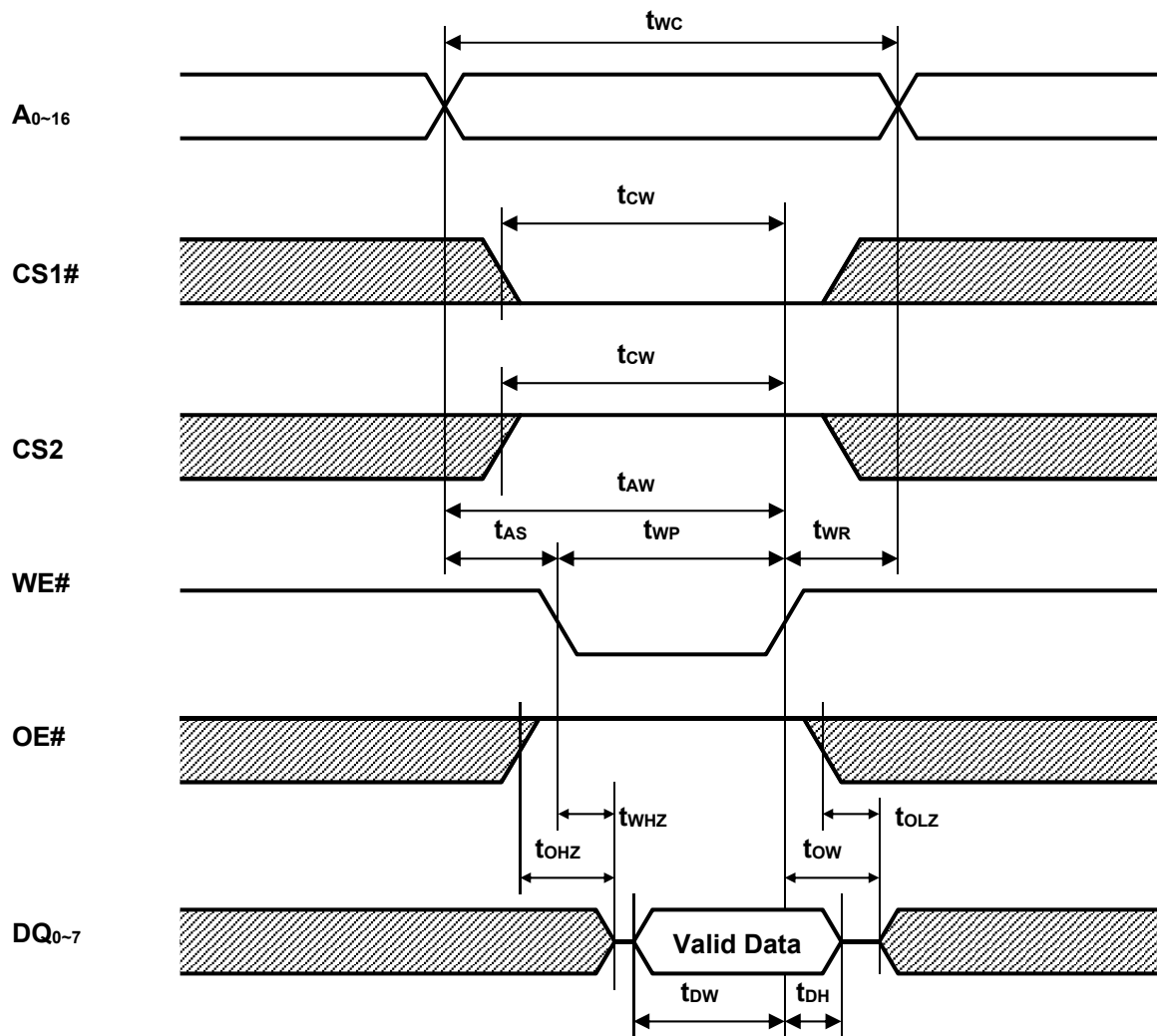
Write Cycle (2) (CS1#, CS2 CLOCK)

Low Vcc Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions[2]	
V_{CC} for data retention	V_{DR}	2.0	-	5.5	V	Vin ≥ 0V, (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V	
Data retention current	I_{CCDR}	-	0.6[1]	2	μA	~+25°C	Vcc=3.0V, Vin ≥ 0V, (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V
		-	-	3	μA	~+40°C	
		-	-	8	μA	~+70°C	
		-	-	10	μA	~+85°C	
Chip deselect time to data retention	t_{CDR}	0	-	-	ns	See retention waveform.	
Operation recovery time	t_R	5	-	-	ms		

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (Ta= 25ºC), and not 100% tested.

2. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, WE#, CS1#, OE#, DQ) can be in the high impedance state.

If CS1# controls data retention mode, CS2 must be CS2 ≥ Vcc-0.2V or 0V ≤ CS2 ≤ 0.2V. The other input levels (address, WE# ,OE#, DQ) can be in the high impedance state.

Low Vcc Data Retention Timing Waveforms
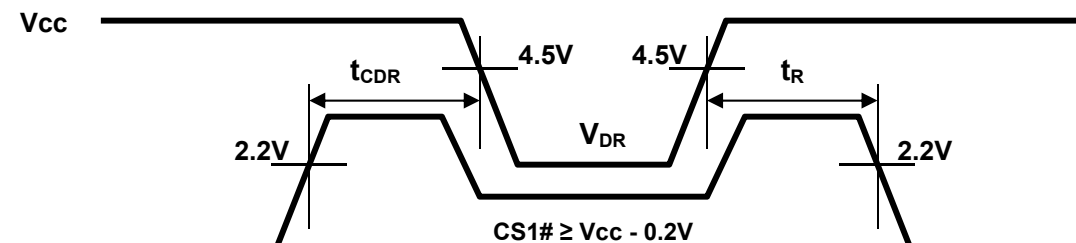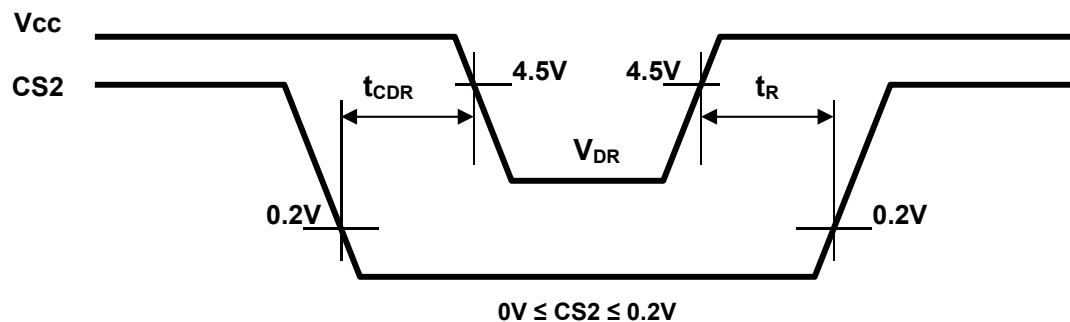
Revision History			R1LP0108E Series Data Sheet

			Description	
Rev.	Date	Page	Summary	
1.00	2017.1.27	-	First Edition issued	
2.00	2019.10.29	p.1	Revised orderable part name information.	

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