

RMLV0816BGSD - 4S2

8Mb Advanced LPSRAM (512k word × 16bit / 1024k word × 8bit)

R10DS0253EJ0201

Rev.2.01

2020.02.20

Description

The RMLV0816BGSD is a family of 8-Mbit static RAMs organized 524,288-word × 16-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMLV0816BGSD has realized higher density, higher performance and low power consumption. The RMLV0816BGSD offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 52pin μ TSOP (II).

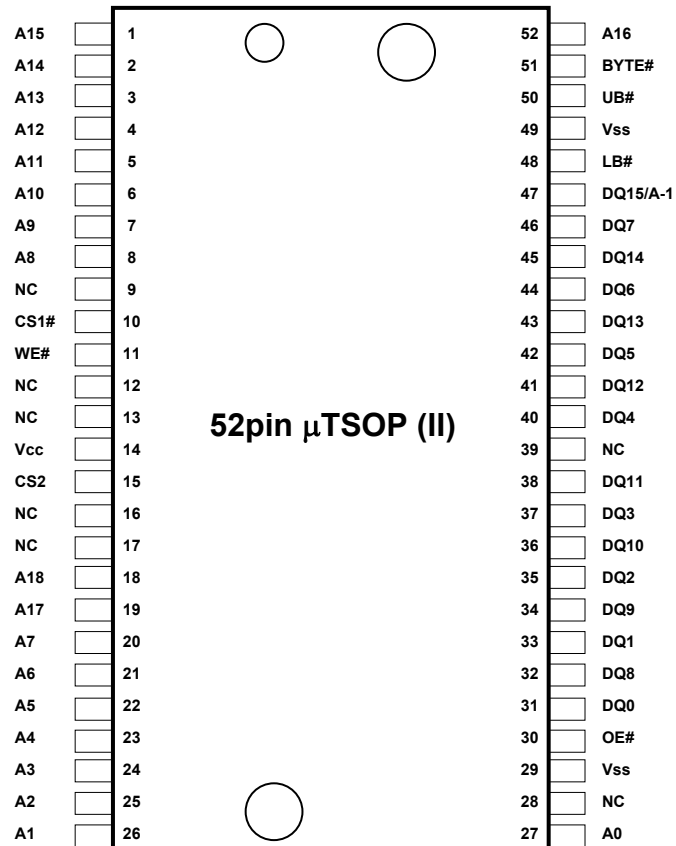
Features

- Single 3V supply: 2.4V to 3.6V
- Access time:
 - Power supply voltage from 2.7V to 3.6V: 45ns (max.)
 - Power supply voltage from 2.4V to 2.7V: 55ns (max.)
- Current consumption:
 - Standby: 0.45 μ A (typ.)
- Equal access and cycle times
- Common data input and output
 - Three state output
- Directly TTL compatible
 - All inputs and outputs
- Battery backup operation

Part Name Information

Part Name	Power supply	Access time	Temperature Range	Package
RMLV0816BGSD-4S2	2.7V to 3.6V	45 ns	-40 ~ +85°C	10.79mm × 10.49mm 52pin plastic μ TSOP (II)
	2.4V to 2.7V	55 ns		

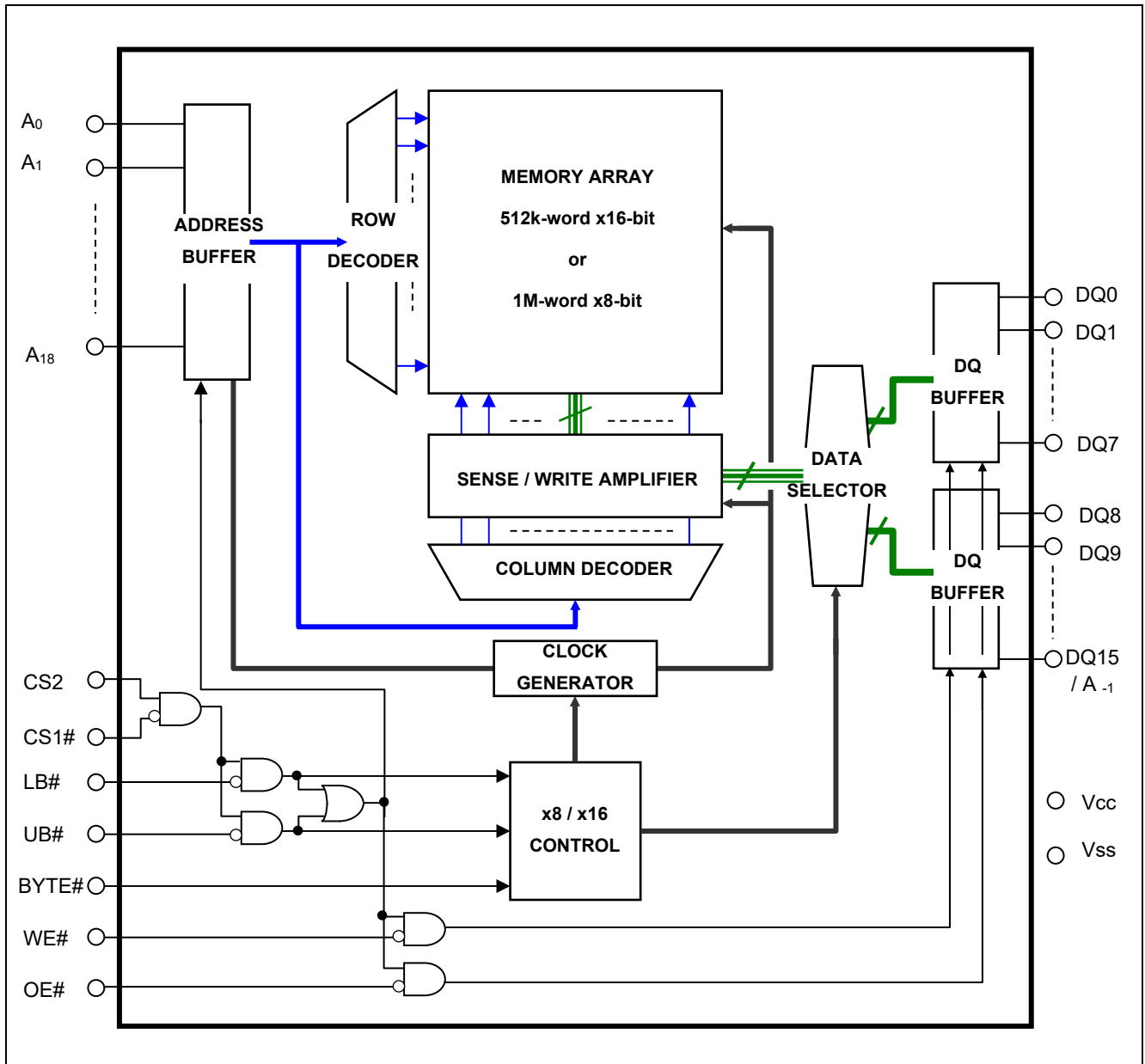
Pin Arrangement



Pin Description

Pin name	Function
V _{CC}	Power supply
V _{SS}	Ground
A0 to A18	Address input (word mode)
A-1 to A18	Address input (byte mode)
DQ0 to DQ15	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
OE#	Output enable
WE#	Write enable
LB#	Lower byte select
UB#	Upper byte select
BYTE#	Byte control mode enable
NC	No connection

Block Diagram



Operation Table

CS1#	CS2	BYTE#	UB#	LB#	WE#	OE#	DQ0~7	DQ8~14	DQ15	Operation
H	X	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	L	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	X	H	H	H	X	X	High-Z	High-Z	High-Z	Stand-by
L	H	H	H	L	L	X	Din	High-Z	High-Z	Write in lower byte
L	H	H	H	L	H	L	Dout	High-Z	High-Z	Read in lower byte
L	H	H	H	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	H	L	X	High-Z	Din	Din	Write in upper byte
L	H	H	L	H	H	L	High-Z	Dout	Dout	Read in upper byte
L	H	H	L	H	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	L	L	X	Din	Din	Din	Word write
L	H	H	L	L	H	L	Dout	Dout	Dout	Word read
L	H	H	L	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	L	X	X	L	X	Din	High-Z	A-1	Byte write
L	H	L	X	X	H	L	Dout	High-Z	A-1	Byte read
L	H	L	X	X	H	H	High-Z	High-Z	A-1	Output disable

Note 1. H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5 ² to $V_{CC}+0.3$ ³	V
Power dissipation	P_T	0.7	W
Operation temperature	T_{opr}	-40 to +85	°C
Storage temperature range	T_{stg}	-65 to +150	°C
Storage temperature range under bias	T_{bias}	-40 to +85	°C

Note 2. -3.0V for pulse ≤ 30 ns (full width at half maximum)

3. Maximum voltage is +4.6V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Supply voltage	V_{CC}	2.4	3.0	3.6	V		
	V_{SS}	0	0	0	V		
Input high voltage	V_{IH}	2.0	—	$V_{CC}+0.2$	V	$V_{CC}=2.4$ V to 2.7V	
		2.2	—	$V_{CC}+0.2$	V	$V_{CC}=2.7$ V to 3.6V	
Input low voltage	V_{IL}	-0.2	—	0.4	V	$V_{CC}=2.4$ V to 2.7V	4
		-0.2	—	0.6	V	$V_{CC}=2.7$ V to 3.6V	4
Ambient temperature range	T_a	-40	—	+85	°C		

Note 4. -3.0V for pulse ≤ 30 ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Input leakage current	I _{LI}	—	—	1	μA	Vin = V _{SS} to V _{CC}	
Output leakage current	I _{LO}	—	—	1	μA	BYTE# ≥ V _{CC} -0.2V or BYTE# ≤ 0.2V CS1# = V _{IH} or CS2 = V _{IL} or OE# = V _{IH} or WE# = V _{IL} or LB# = UB# = V _{IH} , V _{I/O} = V _{SS} to V _{CC}	
Average operating current	I _{CC1}	—	20* ⁵	25	mA	Cycle = 55ns, duty =100%, I _{I/O} = 0mA, BYTE# ≥ V _{CC} -0.2V or BYTE# ≤ 0.2V CS1# = V _{IL} , CS2 = V _{IH} , Others = V _{IH} /V _{IL}	
		—	25* ⁵	30	mA	Cycle = 45ns, duty =100%, I _{I/O} = 0mA, BYTE# ≥ V _{CC} -0.2V or BYTE# ≤ 0.2V CS1# = V _{IL} , CS2 = V _{IH} , Others = V _{IH} /V _{IL}	
	I _{CC2}	—	1.5* ⁵	3	mA	Cycle = 1μs, duty =100%, I _{I/O} = 0mA, BYTE# ≥ V _{CC} -0.2V or BYTE# ≤ 0.2V CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V, V _{IH} ≥ V _{CC} -0.2V, V _{IL} ≤ 0.2V	
Standby current	I _{SB}	—	—	0.3	mA	BYTE# ≥ V _{CC} -0.2V or BYTE# ≤ 0.2V CS2 = V _{IL} , Others = V _{SS} to V _{CC}	
Standby current	I _{SB1}	—	0.45* ⁵	2	μA	~+25°C	Vin = V _{SS} to V _{CC} , BYTE# ≥ V _{CC} -0.2V or BYTE# ≤ 0.2V (1) CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V or (3) LB# = UB# ≥ V _{CC} -0.2V, CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V
		—	0.6* ⁶	4	μA	~+40°C	
		—	—	7	μA	~+70°C	
		—	—	10	μA	~+85°C	
Output high voltage	V _{OH}	2.4	—	—	V	BYTE# ≥ V _{CC} -0.2V or BYTE# ≤ 0.2V I _{OH} = -1mA V _{CC} ≥2.7V	
	V _{OH2}	2.0	—	—	V	BYTE# ≥ V _{CC} -0.2V or BYTE# ≤ 0.2V I _{OH} = -0.1mA	
Output low voltage	V _{OL}	—	—	0.4	V	BYTE# ≥ V _{CC} -0.2V or BYTE# ≤ 0.2V I _{OL} = 2mA V _{CC} ≥2.7V	
	V _{OL2}	—	—	0.4	V	BYTE# ≥ V _{CC} -0.2V or BYTE# ≤ 0.2V I _{OL} = 0.1mA	

Note 5. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a = 25^\circ C$), and not 100% tested.

Note 6. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a = 40^\circ C$), and not 100% tested.

Capacitance

($T_a = 25^\circ C$, $f = 1MHz$)

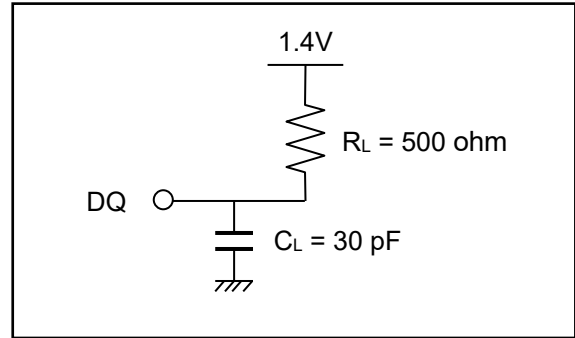
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C_{in}	—	—	8	pF	$V_{in} = 0V$	7
Input / output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O} = 0V$	7

Note 7. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions ($V_{CC} = 2.4V \sim 3.6V$, $T_a = -40 \sim +85^{\circ}C$)

- Input pulse levels:
 $V_{IL} = 0.4V$, $V_{IH} = 2.4V$ ($V_{CC}=2.7V$ to $3.6V$)
 $V_{IL} = 0.4V$, $V_{IH} = 2.2V$ ($V_{CC}=2.4V$ to $2.7V$)
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	Vcc=2.7V to 3.6V		Vcc=2.4V to 2.7V		Unit	Note
		Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	45	—	55	—	ns	
Address access time	t_{AA}	—	45	—	55	ns	
Chip select access time	t_{ACS1}	—	45	—	55	ns	
	t_{ACS2}	—	45	—	55	ns	
Output enable to output valid	t_{OE}	—	22	—	30	ns	
Output hold from address change	t_{OH}	10	—	10	—	ns	
LB#, UB# access time	t_{BA}	—	45	—	55	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	10	—	ns	8,9
	t_{CLZ2}	10	—	10	—	ns	8,9
LB#, UB# enable to low-Z	t_{BLZ}	5	—	5	—	ns	8,9
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	8,9
Chip deselect to output in high-Z	t_{CHZ1}	0	18	0	20	ns	8,9,10
	t_{CHZ2}	0	18	0	20	ns	8,9,10
LB#, UB# disable to high-Z	t_{BHZ}	0	18	0	20	ns	8,9,10
Output disable to output in high-Z	t_{OHZ}	0	18	0	20	ns	8,9,10

Note 8. This parameter is sampled and not 100% tested.

9. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

10. t_{CHZ1} , t_{CHZ2} , t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

Write Cycle

Parameter	Symbol	Vcc=2.7V to 3.6V		Vcc=2.4V to 2.7V		Unit	Note
		Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	45	—	55	—	ns	
Address valid to write end	t_{AW}	35	—	50	—	ns	
Chip select to write end	t_{CW}	35	—	50	—	ns	
Write pulse width	t_{WP}	35	—	40	—	ns	11
LB#,UB# valid to write end	t_{BW}	35	—	50	—	ns	
Address setup time to write start	t_{AS}	0	—	0	—	ns	
Write recovery time from write end	t_{WR}	0	—	0	—	ns	
Data to write time overlap	t_{DW}	25	—	25	—	ns	
Data hold from write end	t_{DH}	0	—	0	—	ns	
Output enable from write end	t_{OW}	5	—	5	—	ns	12
Output disable to output in high-Z	t_{OHZ}	0	18	0	20	ns	12,13
Write to output in high-Z	t_{WHZ}	0	18	0	20	ns	12,13

Note 11. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

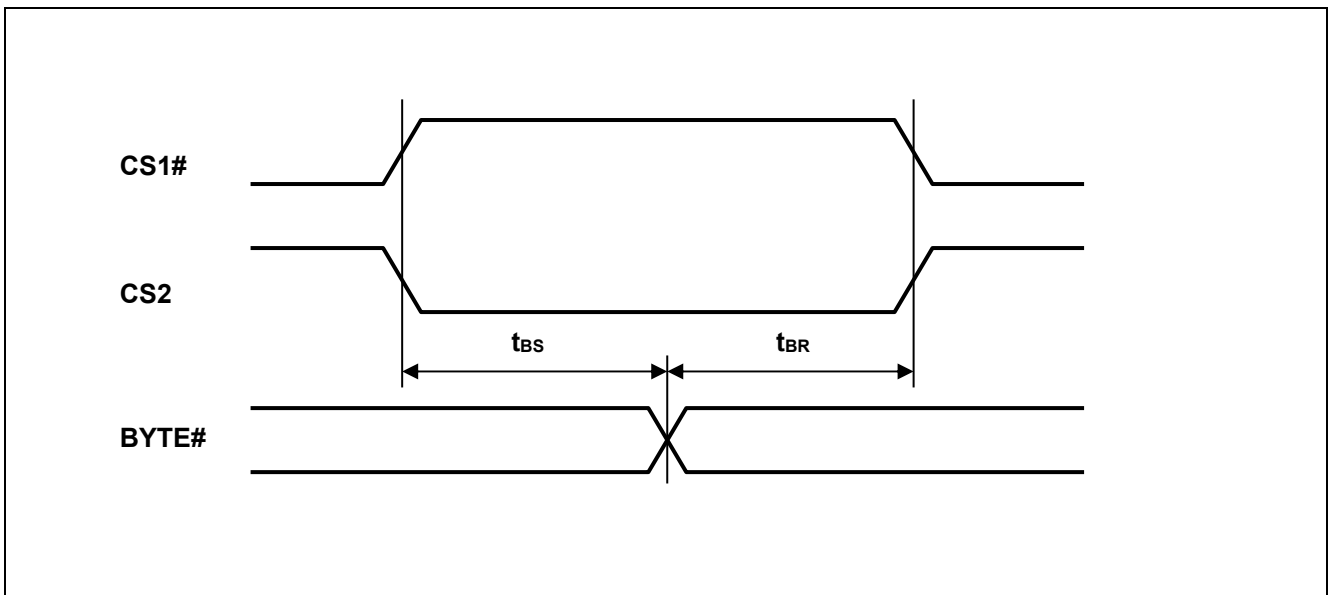
12. This parameter is sampled and not 100% tested.

13. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

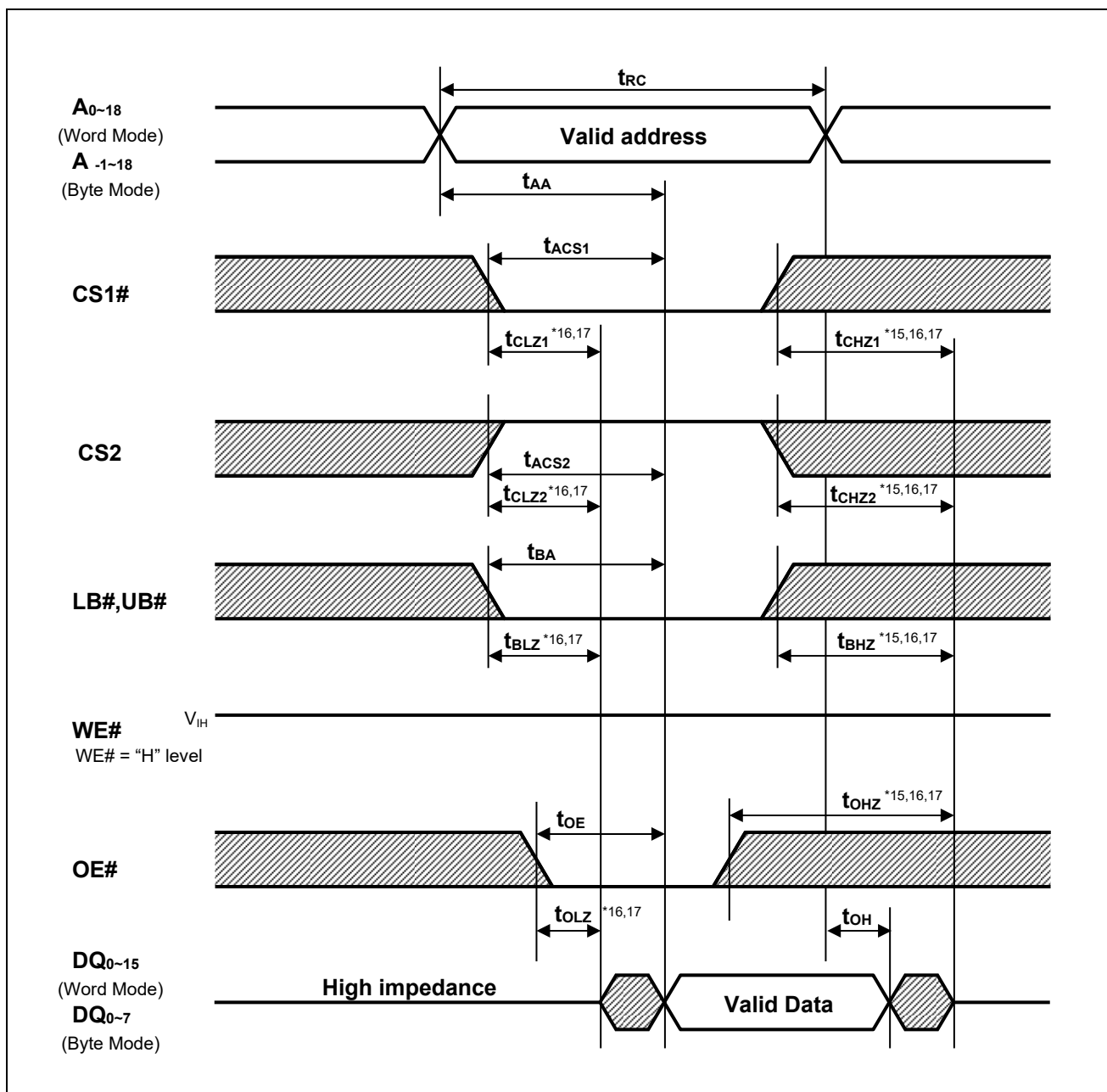
BYTE# Timing Conditions

Parameter	Symbol	Vcc=2.7V to 3.6V		Vcc=2.4V to 2.7V		Unit	Note
		Min.	Max.	Min.	Max.		
Byte setup time	t_{BS}	5	—	5	—	ms	
Byte recovery time	t_{BR}	5	—	5	—	ms	

BYTE# Timing Waveforms



Timing Waveforms

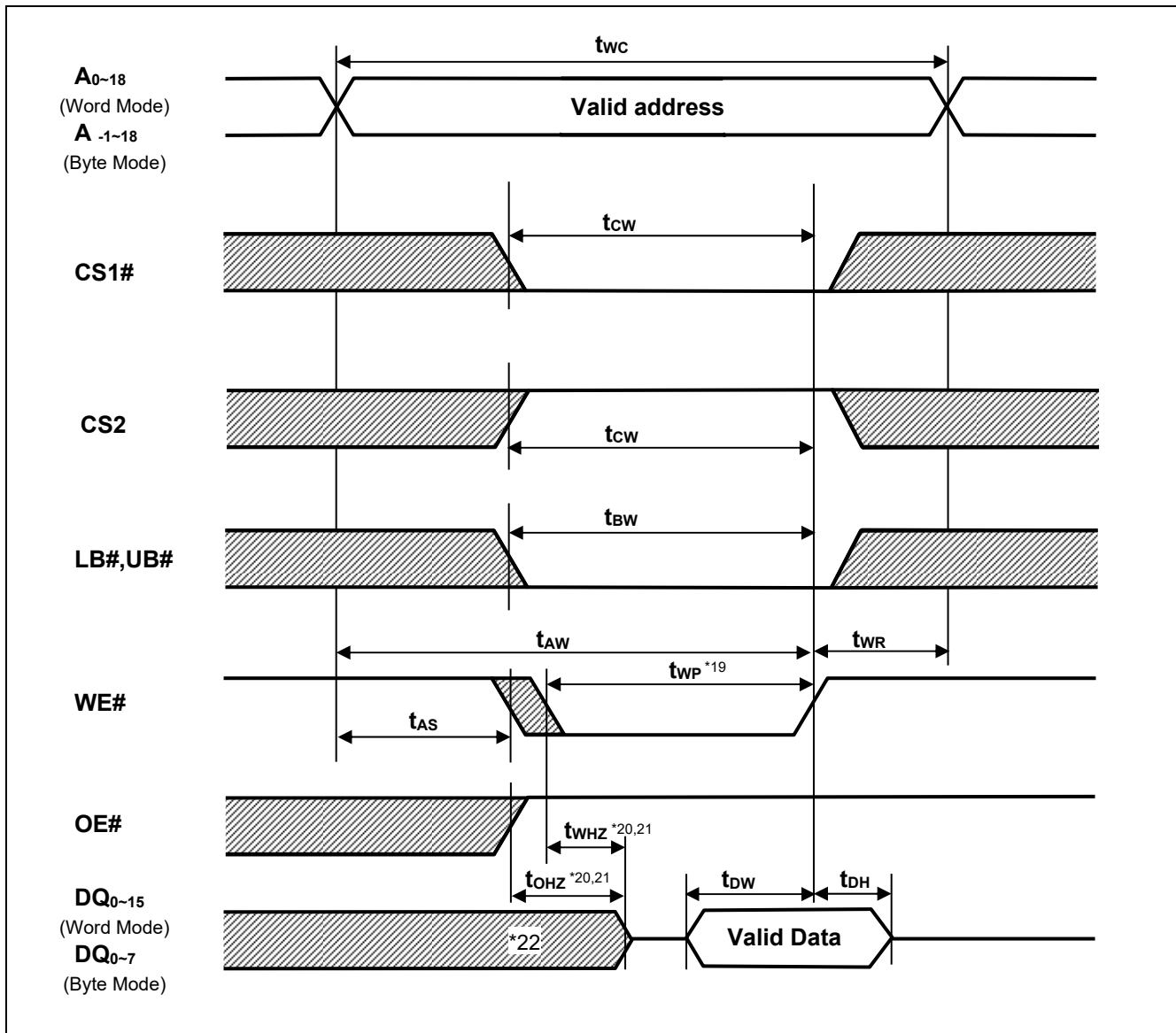
Read Cycle^{*14}

Note 14. BYTE# $\geq V_{CC} - 0.2V$ or BYTE# $\leq 0.2V$

15. t_{CHZ1} , t_{CHZ2} , t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

16. This parameter is sampled and not 100% tested

17. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

Write Cycle (1)^{*18} (WE# CLOCK, OE#="H" while writing)

Note 18. $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$

19. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

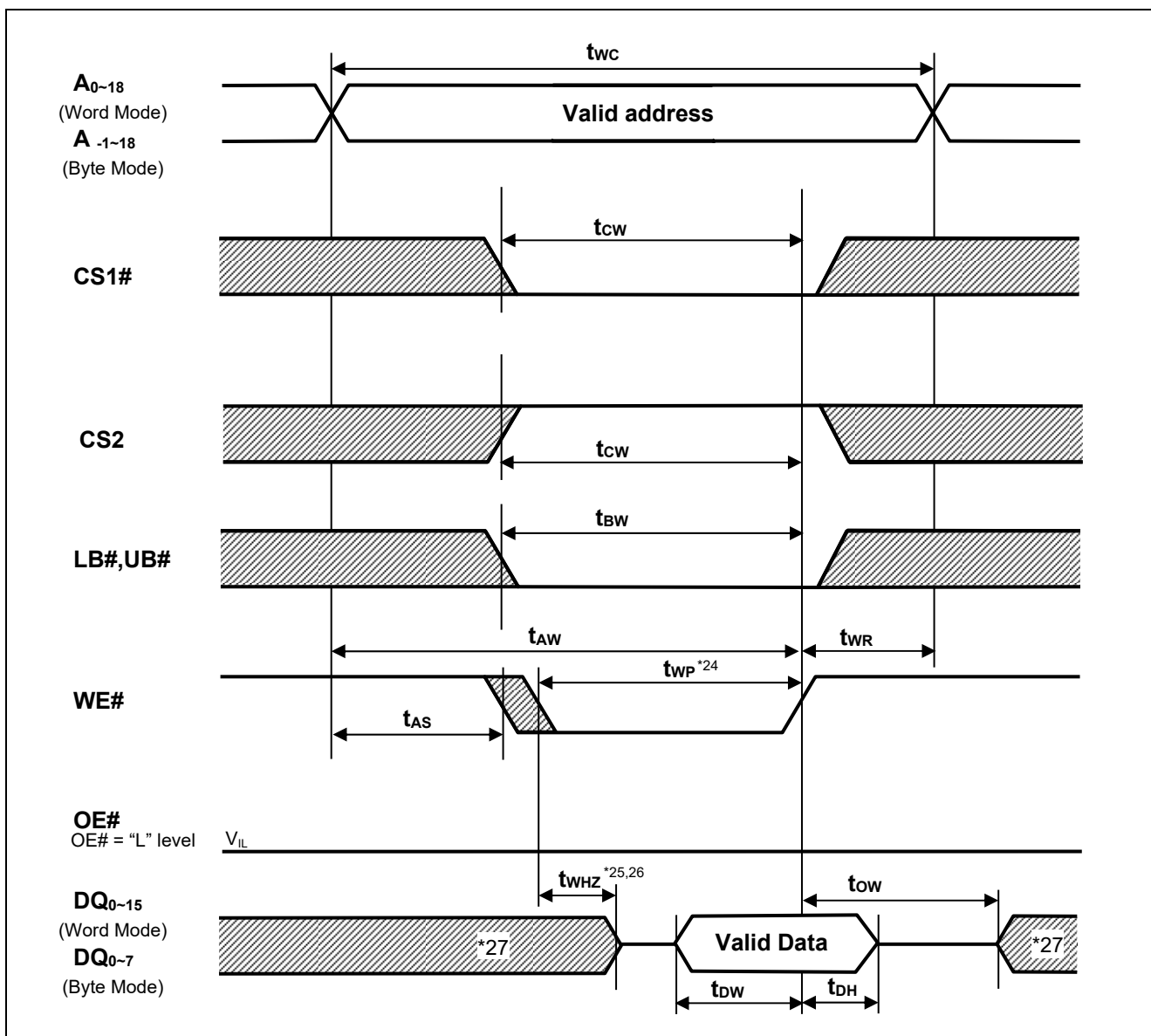
A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

20. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

21. This parameter is sampled and not 100% tested

22. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (2)^{*23} (WE# CLOCK, OE# Low Fixed)

Note 23. $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$

24. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

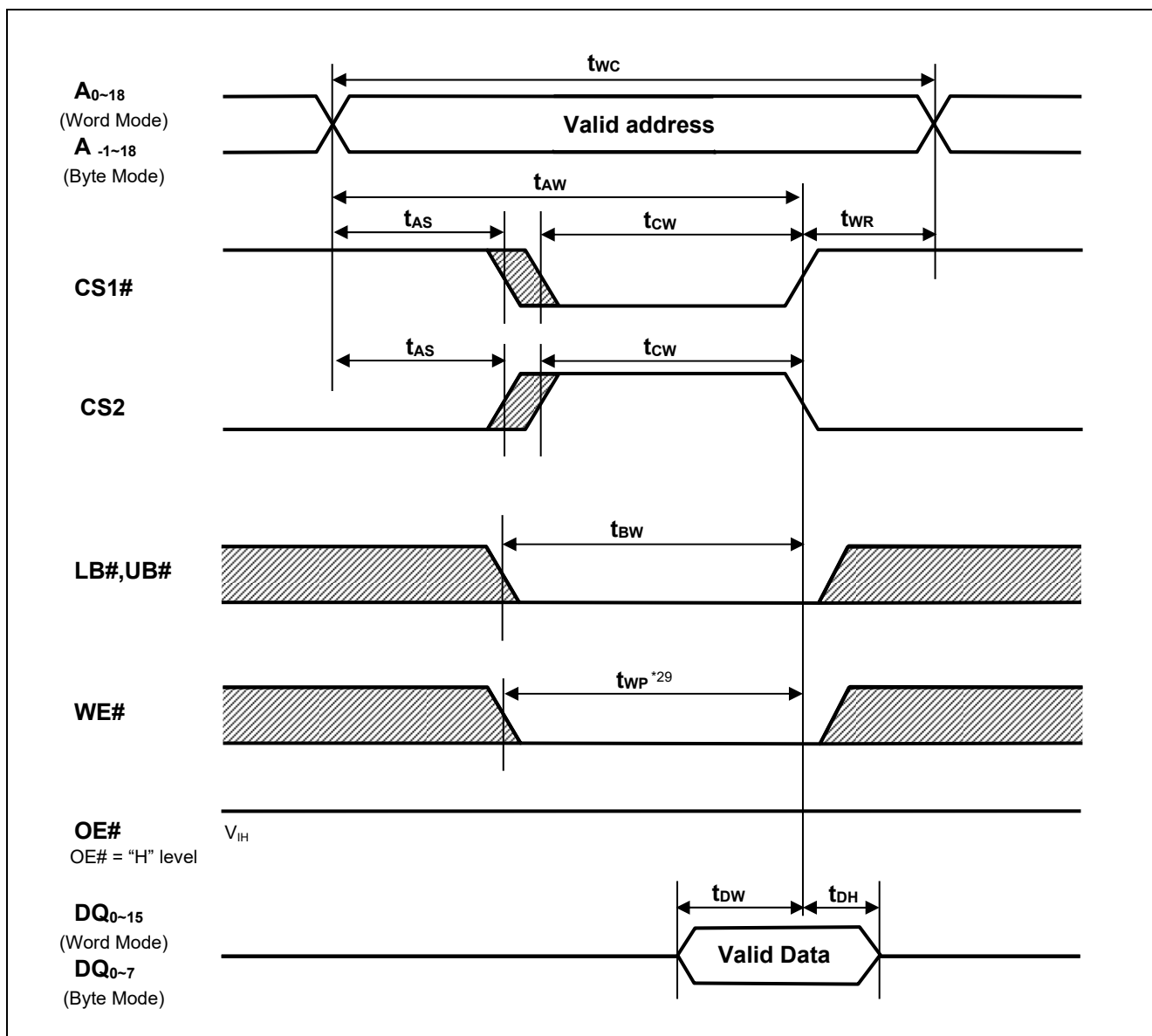
A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

25. t_{WHZ} is defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

26. This parameter is sampled and not 100% tested.

27. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (3)^{*28} (CS1#, CS2 CLOCK)

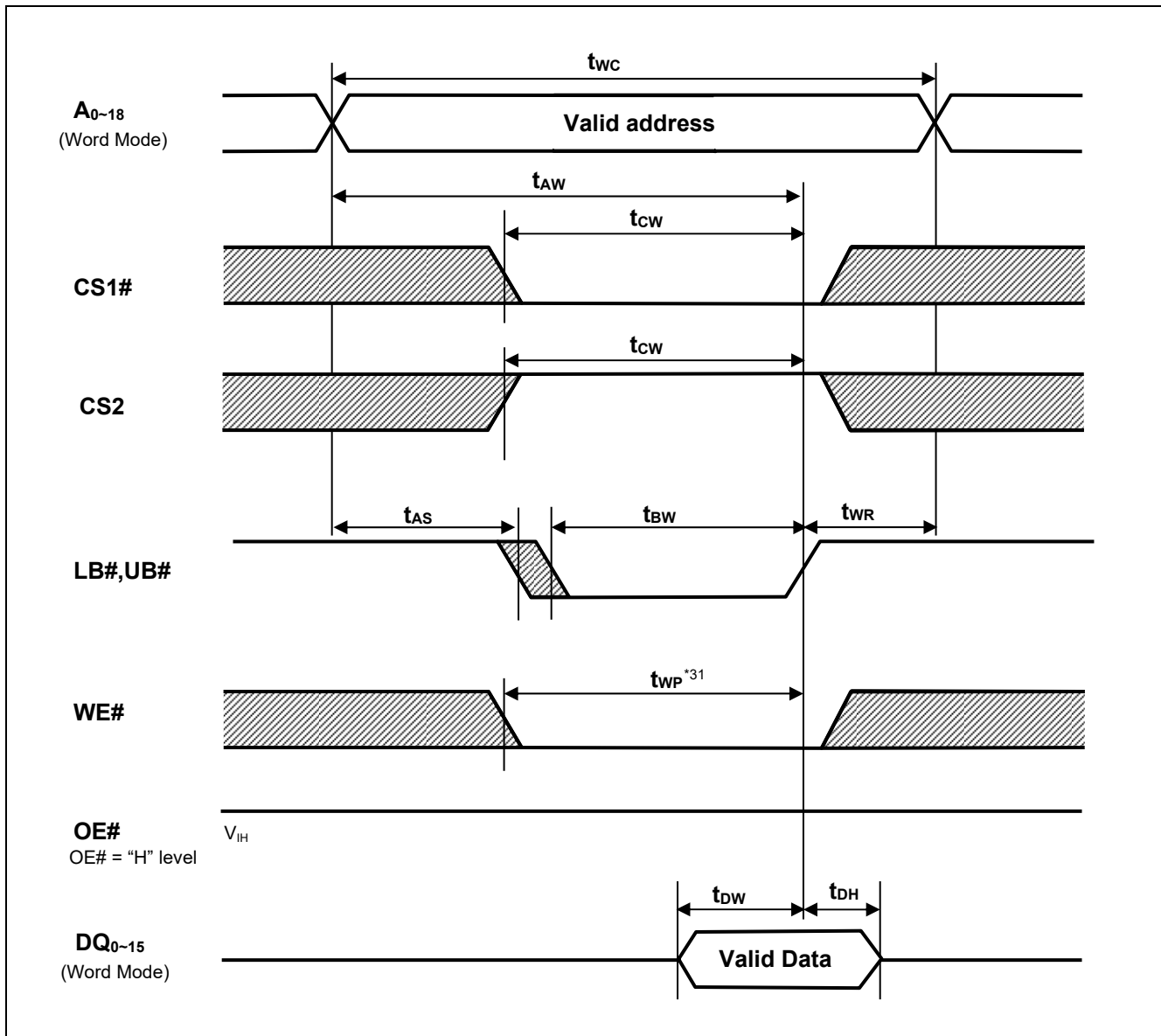
Note 28. $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$

29. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Write Cycle (4)^{*30} (LB#, UB# CLOCK, Word Mode)

Note 30. BYTE# $\geq V_{CC} - 0.2V$

31. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Low V_{CC} Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions ^{*34}	
V _{CC} for data retention	V _{DR}	1.5	—	3.6	V	Vin ≥ 0V, BYTE# ≥ Vcc -0.2V or BYTE# ≤ 0.2V (1) CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V or (3) LB# = UB# ≥ V _{CC} -0.2V, CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V	
Data retention current	I _{CCDR}	—	0.45 ^{*32}	2	μA	~+25°C	V _{CC} = 3.0V, Vin ≥ 0V, BYTE# ≥ Vcc -0.2V or BYTE# ≤ 0.2V (1) CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V or (3) LB# = UB# ≥ V _{CC} -0.2V, CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V
		—	0.6 ^{*33}	4	μA	~+40°C	
		—	—	7	μA	~+70°C	
		—	—	10	μA	~+85°C	
Chip deselect time to data retention	t _{CDR}	0	—	—	ns	See retention waveform.	
Operation recovery time	t _R	5	—	—	ms		

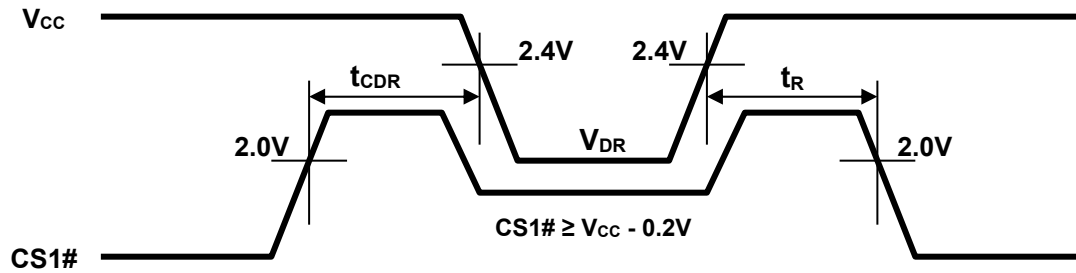
Note 32. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a = 25^{\circ}C$), and not 100% tested.

33. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a = 40^{\circ}C$), and not 100% tested.

34. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB# buffer, UB# buffer and DQ buffer. If CS2 controls data retention mode, V_{in} levels (address, WE#, CS1#, OE#, LB#, UB#, DQ) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$. The other inputs levels (address, WE#, OE#, LB#, UB#, DQ) can be in the high-impedance state.

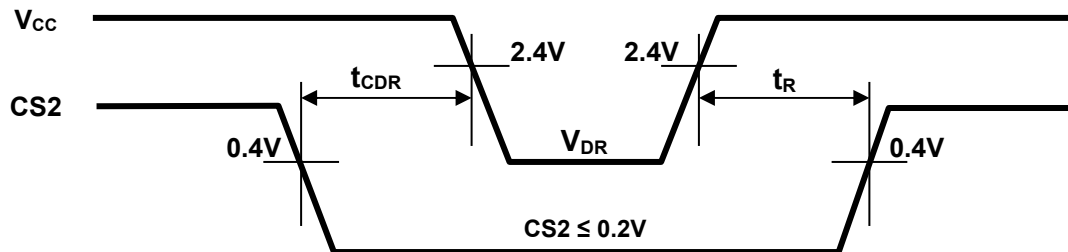
Low Vcc Data Retention Timing Waveforms (CS1# controlled)*35

CS1# Controlled



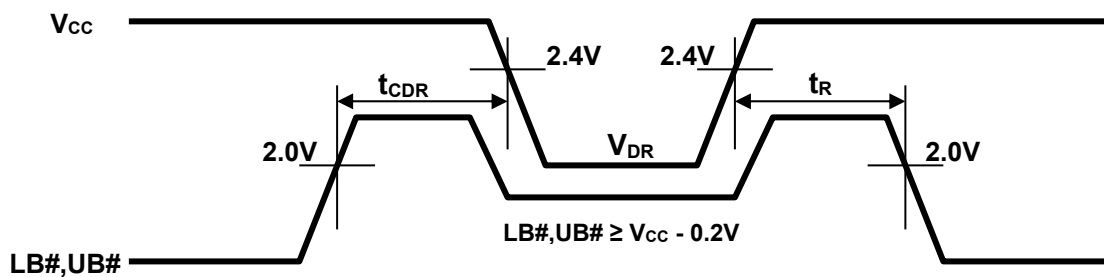
Low Vcc Data Retention Timing Waveforms (CS2 controlled)*35

CS2 Controlled



Low Vcc Data Retention Timing Waveforms (LB#,UB# controlled, Word Mode)*36

LB#,UB# Controlled



Note 35. $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$

36. $BYTE\# \geq V_{CC} - 0.2V$

Revision History	RMLV0816BGSD Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	2014.11.28	—	First Edition issued
2.00	2015.06.26	P.1, 5 P.5 P.13	Standby current I_{SB1} : 25°C 0.6μA ->0.45μA (typ.), 40°C 2μA ->0.6μA (typ.) Average operating current I_{CC2} : 25°C 2mA ->1.5mA (typ.) Data retention current I_{CCDR} : 25°C 0.6μA ->0.45μA (typ.), 40°C 2μA ->0.6μA (typ.)
2.01	2020.02.20	Last page	Updated the Notice to the latest version

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