

NP60N06VLK

60 V - 60 A - N-channel Power MOS FET

R07DS1339EJ0200 Rev.2.00

May 24, 2018

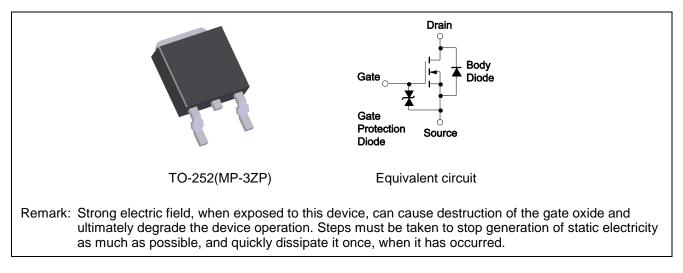
## Description

NP60N06VLK is N-channel MOS Field Effect Transistor designed for high current switching applications.

## Features

- Super low on-state resistance
- ----  $R_{DS(on)1} = 7.9 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 30 \text{ A}$ )
- Low  $C_{iss}$ :  $C_{iss} = 2400 \text{ pF TYP}$ . ( $V_{DS} = 25 \text{ V}$ )
- Designed for automotive application and AEC-Q101 qualified

### Outline



### **Ordering Information**

Part No.	Lead Plating	Packing		Package	
NP60N06VLK-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-252(MP-3ZP)	
NP60N06VLK-E2-AY *1			Taping (E2 type)	10-252(1017-527)	

Note: \*1. Pb-free (This product does not contain Pb in the external electrode)

## **Absolute Maximum Ratings** (T<sub>A</sub> = 25°C)

ltem	Symbol	Ratings	Unit
Drain to Source Voltage ( $V_{GS} = 0 V$ )	V <sub>DSS</sub>	60	V
Gate to Source Voltage ( $V_{DS} = 0 V$ )	V <sub>GSS</sub>	±20	V
Drain Current (DC) ( $T_c = 25^{\circ}C$ )	I <sub>D(DC)</sub>	±60	A
Drain Current (pulse) *1*3	I <sub>D(pulse)</sub>	±240	A
Total Power Dissipation ( $T_C = 25^{\circ}C$ )	P <sub>T1</sub>	105	W
Total Power Dissipation ( $T_A = 25^{\circ}C$ )	P <sub>T2</sub>	1.2	W
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	-55 to +175	°C
Repetitive Avalanche Current *2*3	I <sub>AR</sub>	25	A
Repetitive Avalanche Energy *2*3	E <sub>AR</sub>	63	mJ

## **Thermal Resistance**

Channel to Case Thermal Resistance	Rth(ch-C) *3	1.43	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A) *3	125	°C/W

Notes: \*1.  $T_C$  = 25°C, PW  $\leq$  10  $\mu s,$  Duty Cycle  $\leq$  1%

- \*2. R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20 V  $\rightarrow$  0 V
- \*3. Not subject of production test. Verified by design/characterization.



Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μΑ	$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$
Gate Leakage Current	I <sub>GSS</sub>			±10	μΑ	$V_{GS} = \pm 20 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	1.5	2.1	2.5	V	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$
Forward Transfer Admittance *1	y <sub>fs</sub>	33	54		S	$V_{DS} = 5 V, I_D = 30 A$
Drain to Source On-state	R <sub>DS(on)1</sub>		6.1	7.9	mΩ	$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}$
Resistance *1	R <sub>DS(on)2</sub>		7.4	12.0	mΩ	$V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$
Input Capacitance *2	Ciss		2400	3600	pF	$V_{DS} = 25 V,$
Output Capacitance *2	Coss		230	350	pF	$V_{GS} = 0 V,$
Reverse Transfer Capacitance *2	C <sub>rss</sub>		80	150	pF	f = 1 MHz
Turn-on Delay Time *2	t <sub>d(on)</sub>		18	40	ns	$V_{DD} = 30 \text{ V}, I_D = 30 \text{ A},$
Rise Time *2	tr		6	20	ns	Vgs = 10 V,
Turn-off Delay Time *2	t <sub>d(off)</sub>		45	90	ns	R <sub>G</sub> = 0 Ω
Fall Time *2	t <sub>f</sub>		3	10	ns	_
Total Gate Charge *2	Q <sub>G</sub>		37	56	nC	$V_{DD} = 48 V,$
Gate to Source Charge	Q <sub>GS</sub>		9		nC	V <sub>GS</sub> = 10 V,
Gate to Drain Charge	Q <sub>GD</sub>		8		nC	I <sub>D</sub> = 60 A
Body Diode Forward Voltage *1	VF(S-D)		0.9	1.5	V	IF = 60 A, VGS = 0 V
Reverse Recovery Time	t <sub>rr</sub>		32		ns	$I_F = 60 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Qrr		30		nC	di/dt = 100 A/µs

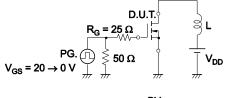
## **Electrical Characteristics** (T<sub>A</sub> = 25°C)

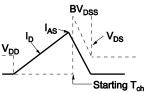
Note: \*1. Pulsed test

Note: \*2. Not subject of production test. Verified by design/characterization.

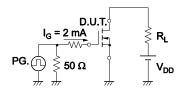
### TEST CIRCUIT 1 AVALANCHE CAPABILITY

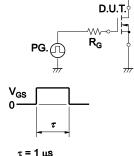
### TEST CIRCUIT 2 SWITCHING TIME



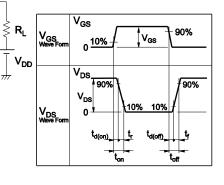


### **TEST CIRCUIT 3 GATE CHARGE**



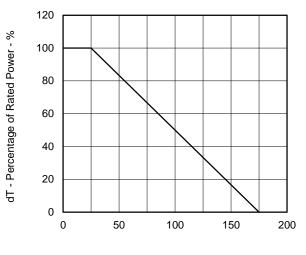






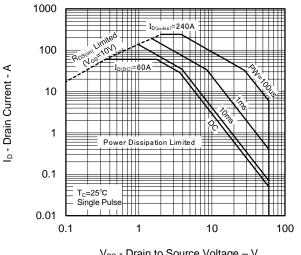
## **Typical Characteristics** (T<sub>A</sub> = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

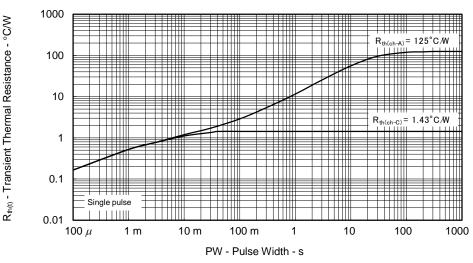


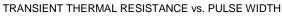
 $T_{C}$  - Case Temperature -  $^{\circ}C$ 





 $V_{DS}$  - Drain to Source Voltage – V





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TOTAL POWER DISSIPATION vs.

100

T<sub>c</sub> - Case Temperature - °C

150

200

120

100

80

60

40

20

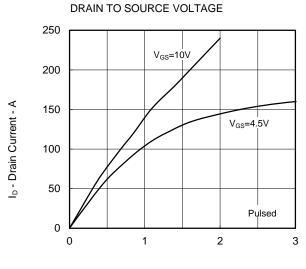
0

0

50

 $P_t - Total Power Dissipation - W$ 

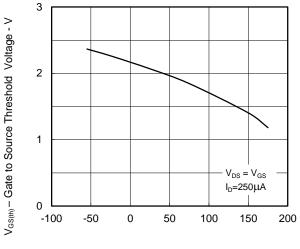
CASE TEMPERATURE



DRAIN CURRENT vs.

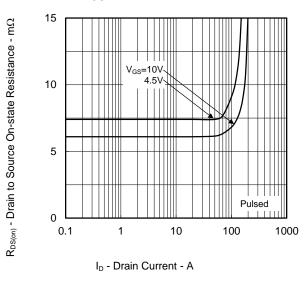


GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

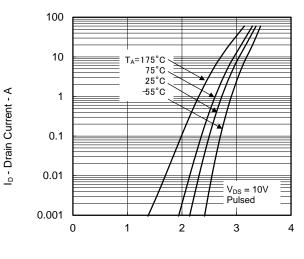


T<sub>ch</sub> - Channel Temperature - °C

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

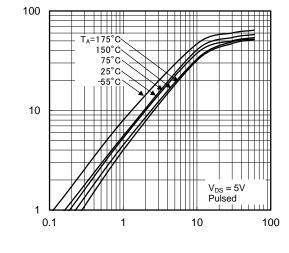


FORWARD TRANSFER CHARACTERISTICS

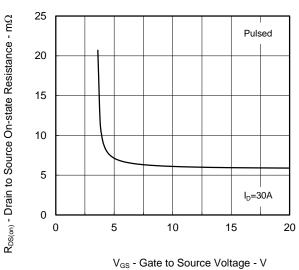


V<sub>GS</sub> - Gate to Source Voltage - V

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



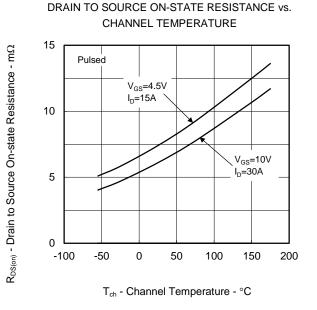
I<sub>D</sub> - Drain Current - A



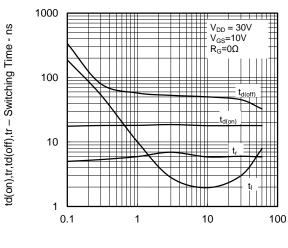
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



 $\mid y_{fs} \mid$  - Forward Transfer Admittance - S

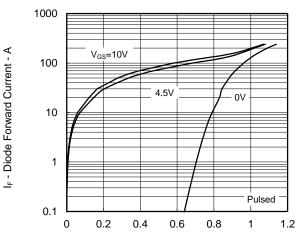


#### SWITCHING CHARACTERISTICS



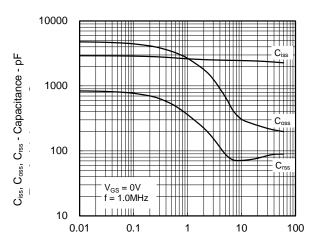
I<sub>D</sub> - Drain Current - A

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



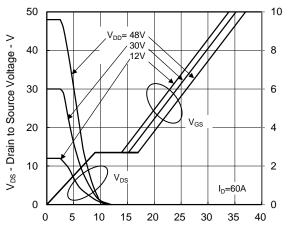
 $V_{\text{F(S-D)}}$  - Source to Drain Voltage - V

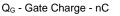
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



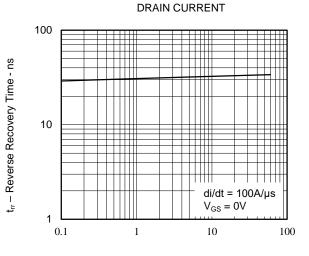








REVERSE RECOVERY TIME vs.

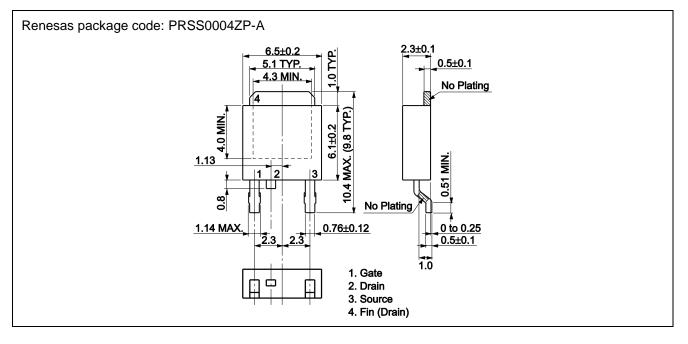


IF - Drain Current - A



## Package Drawings (Unit: mm)

## TO-252 (MP-3ZP) (Mass: 1.48 g TYP.)





**Revision History** 

## NP60N06VLK Data Sheet

		Description			
Rev.	Date	Page	Summary		
1.00	Apr. 8, 2016	—	First Edition Issued		
2.00	May 24 ,2018	2	Note 3 was added		
		3	Note 2 was added		

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