

NP30N06QDK

60 V – 30 A – Dual N-channel Power MOS FET

Application: Automotive

R07DS1332EJ0200

Rev.2.00

May 24, 2018

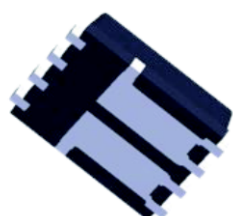
Description

NP29N06QDK is a dual N-channel MOS Field Effect Transistor designed for high current switching applications.

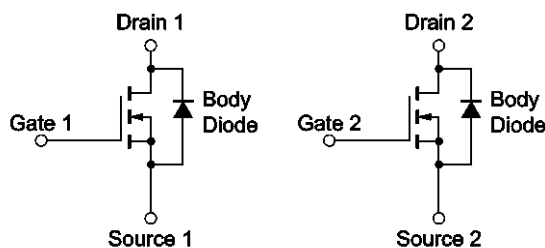
Features

- Super low on-state resistance
 - $R_{DS(on)1} = 14 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$)
 - $R_{DS(on)2} = 21 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 4.5 \text{ V}$, $I_D = 7.5 \text{ A}$)
- Low C_{iss} : $C_{iss} = 1500 \text{ pF TYP.}$ ($V_{DS} = 25 \text{ V}$)
- Designed for automotive application and AEC-Q101 qualified
- Small size package 8-pin HSON dual

Outline



8-pin HSON dual



Equivalent circuit

Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Ordering Information

Part No.	Lead Plating	Packing		Package
NP30N06QDK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON dual
NP30N06QDK-E2-AY *1			Taping (E2 type)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0\text{ V}$)	V_{DSS}	60	V
Gate to Source Voltage ($V_{DS} = 0\text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$) *4	$I_{D(DC)}$	± 30	A
Drain Current (pulse) *1, 4, 5	$I_{D(pulse)}$	± 120	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$) *4	P_{T1}	59	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$) *2, 4	P_{T2}	1.0	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55\text{ to }+175$	$^\circ\text{C}$
Repetitive Avalanche Current *3, 5	I_{AR}	19	A
Repetitive Avalanche Energy *3, 5	E_{AR}	35	mJ

Thermal Resistance

Channel to Case Thermal Resistance $R_{th(ch-C)}^{*5}$ 2.54 $^\circ\text{C/W}$

Channel to Ambient Thermal Resistance *2 $R_{th(ch-A)}^{*5}$ 150 $^\circ\text{C/W}$

Notes: *1. $T_C = 25^\circ\text{C}$, $PW \leq 10\text{ }\mu\text{s}$, Duty Cycle $\leq 1\%$

*2. Mounted on glass epoxy substrate of $40\text{ mm} \times 40\text{ mm} \times 1.6\text{ mm}$ with 4% copper area ($35\text{ }\mu\text{m}$)

*3. $R_G = 25\text{ }\Omega$, $V_{GS} = 20\text{ V} \rightarrow 0\text{ V}$

*4. One channel operation

*5. Not subject of production test. Verified by design/characterization.

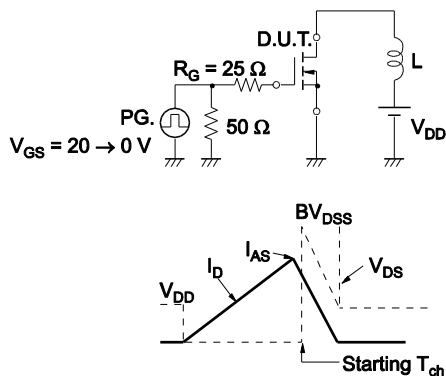
Electrical Characteristics (T_A = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μA	V _{DS} = 60 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}			±100	nA	V _{GS} = ±20 V, V _{DS} = 0 V
Gate to Source Threshold Voltage	V _{GS(th)}	1.5	2.1	2.5	V	V _{DS} = V _{GS} , I _D = 250 μA
Forward Transfer Admittance *1	y _{fs}	13	25		S	V _{DS} = 5 V, I _D = 15 A
Drain to Source On-state Resistance *1	R _{DS(on)1}		11.5	14	mΩ	V _{GS} = 10 V, I _D = 15 A
	R _{DS(on)2}		16.5	21	mΩ	V _{GS} = 4.5 V, I _D = 7.5 A
Input Capacitance *2	C _{iss}		1500	2250	pF	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz
Output Capacitance *2	C _{oss}		160	240	pF	
Reverse Transfer Capacitance *2	C _{rss}		50	90	pF	
Turn-on Delay Time *2	t _{d(on)}		15	30	ns	V _{DD} = 30 V, I _D = 15 A, V _{GS} = 10 V, R _G = 0 Ω
Rise Time *2	t _r		5	13	ns	
Turn-off Delay Time *2	t _{d(off)}		50	100	ns	
Fall Time *2	t _f		3	8	ns	
Total Gate Charge *2	Q _G		25	38	nC	V _{DD} = 48 V, V _{GS} = 10 V, I _D = 30 A
Gate to Source Charge	Q _{GS}		5		nC	
Gate to Drain Charge	Q _{GD}		4		nC	
Body Diode Forward Voltage *1	V _{F(S-D)}		0.9	1.5	V	I _F = 30 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		25		ns	I _F = 30 A, V _{GS} = 0 V, di/dt = 100 A/μs
Reverse Recovery Charge	Q _{rr}		26		nC	

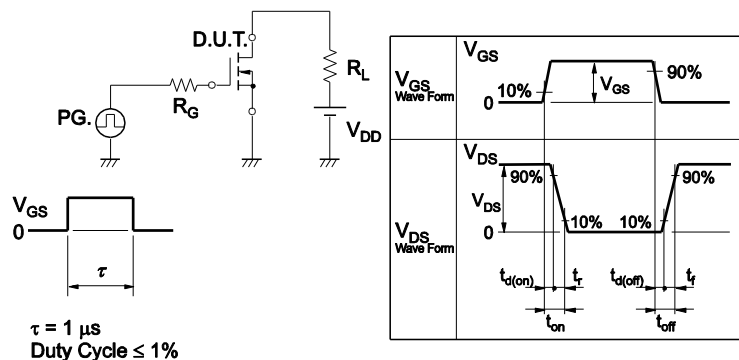
Note: *1. Pulsed test

Note: *2. Not subject of production test. Verified by design/characterization.

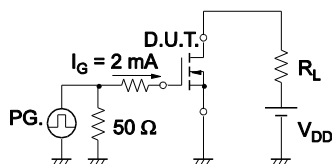
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

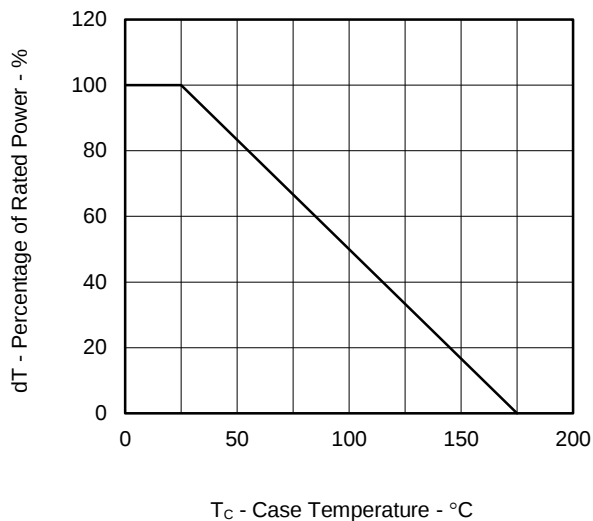


TEST CIRCUIT 3 GATE CHARGE

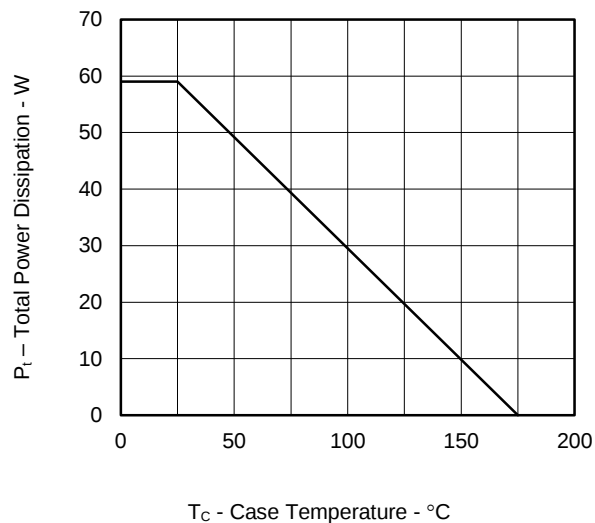


Typical Characteristics ($T_A = 25^\circ\text{C}$)

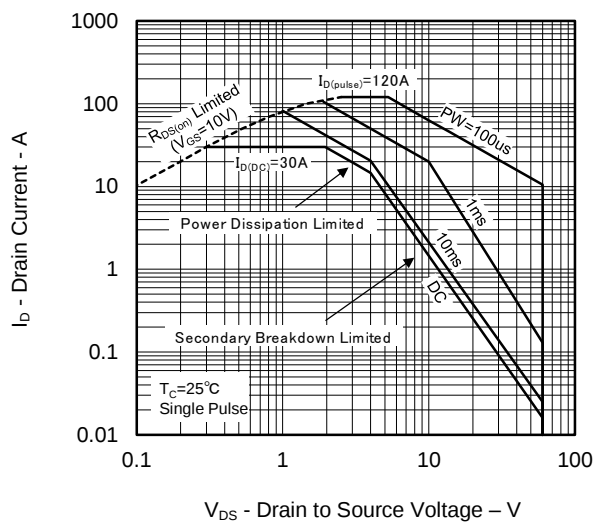
DERATING FACTOR OF FORWARD BIAS SAFE
OPERATING AREA



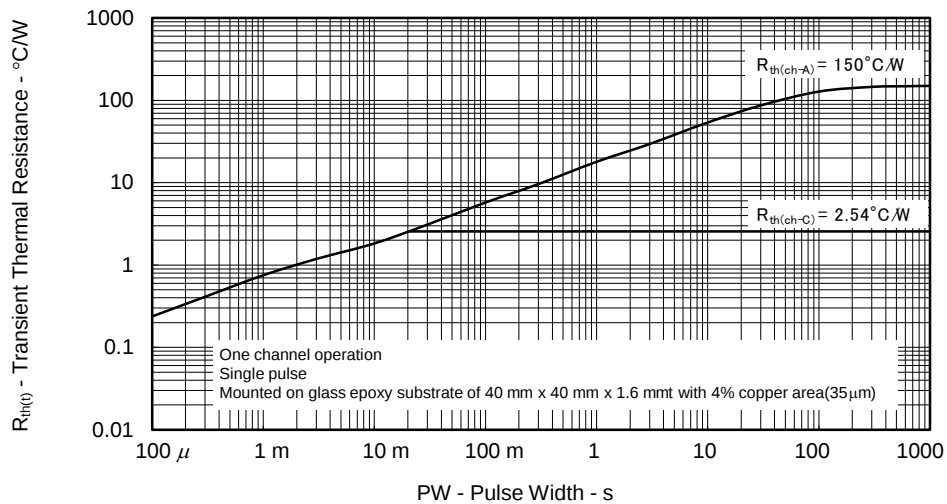
TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE

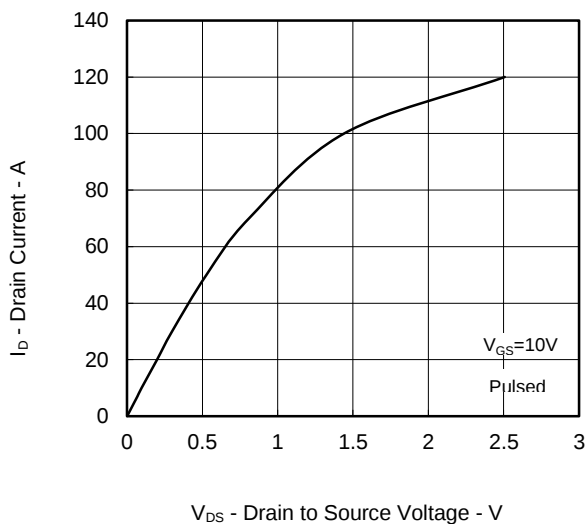


FORWARD BIAS SAFE OPERATING AREA

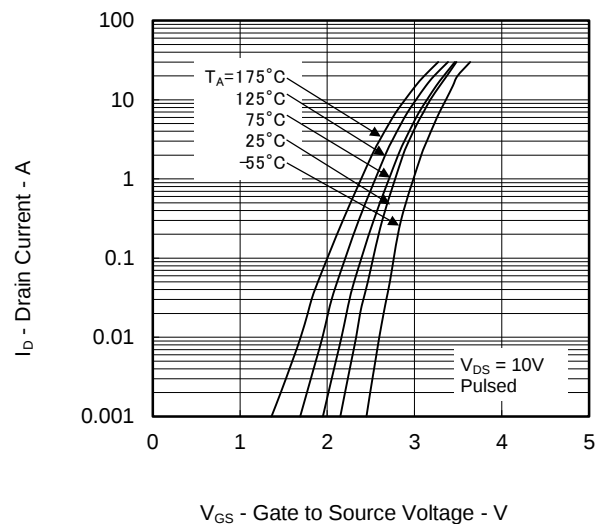
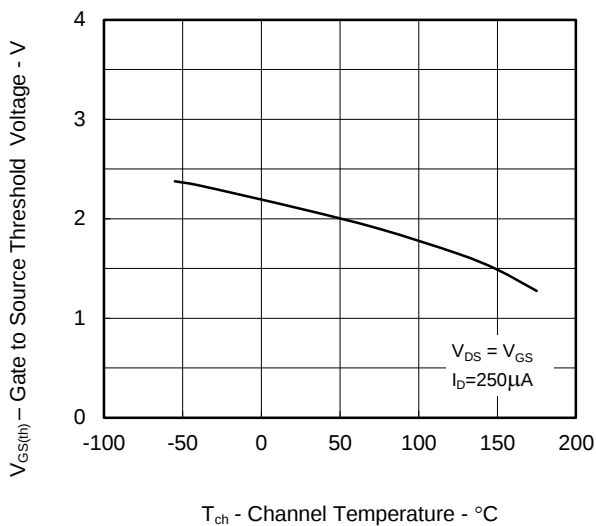
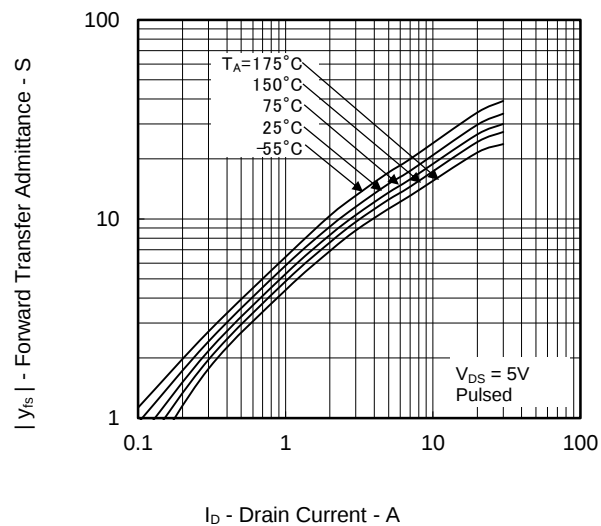
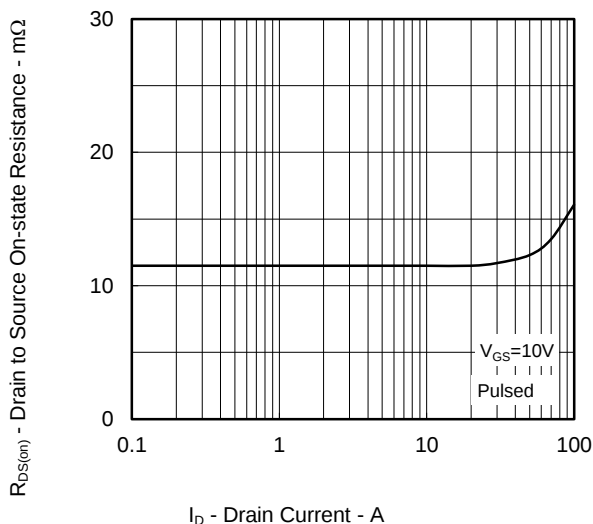
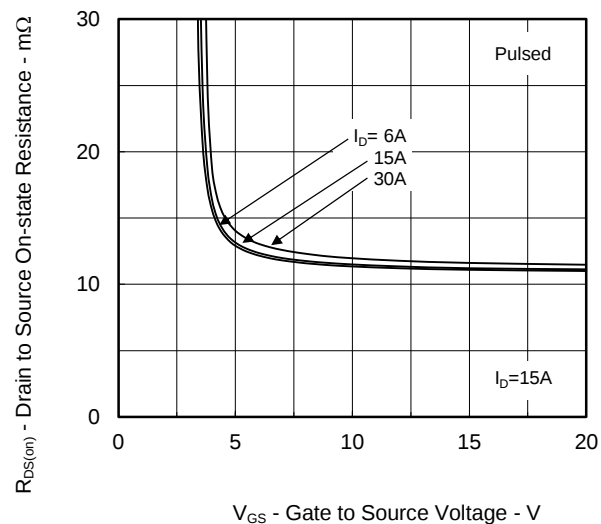


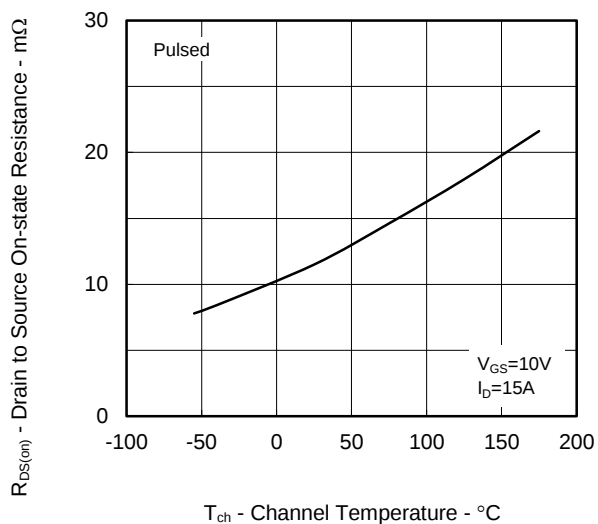
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



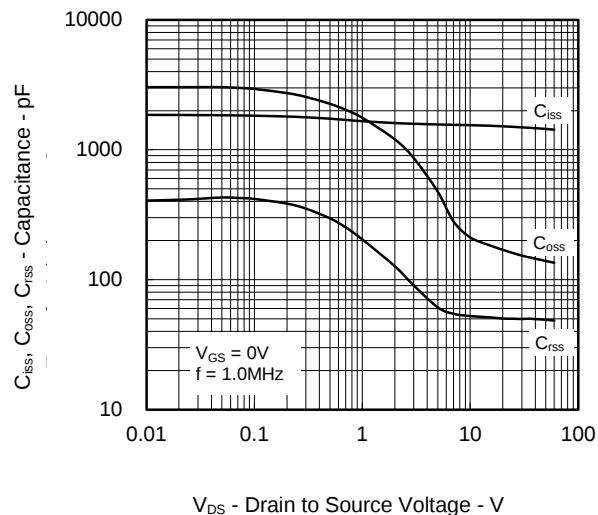
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

FORWARD TRANSFER CHARACTERISTICS

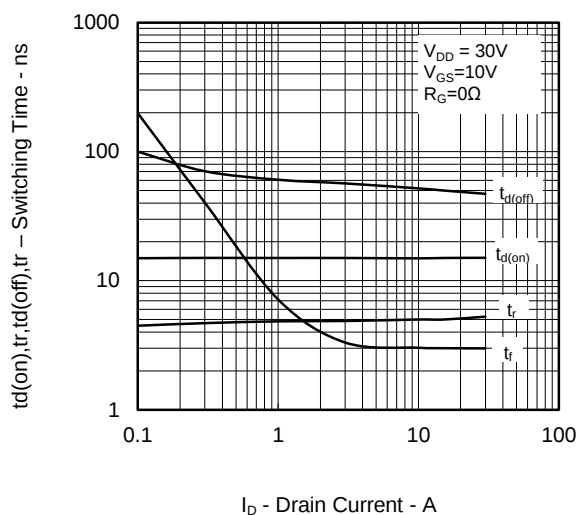
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATUREFORWARD TRANSFER ADMITTANCE vs. DRAIN
CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE

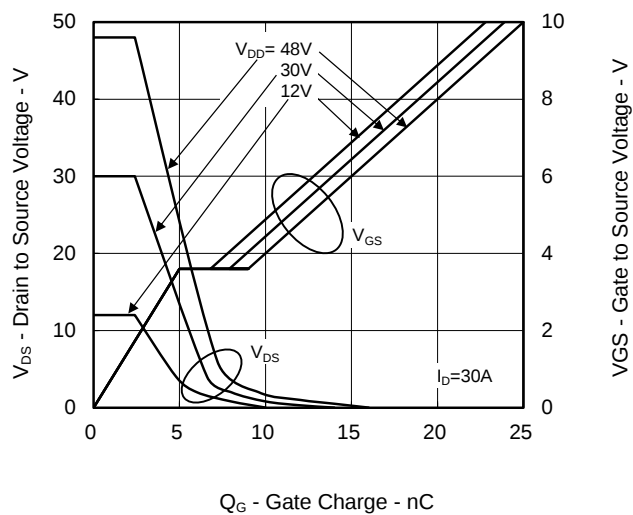
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



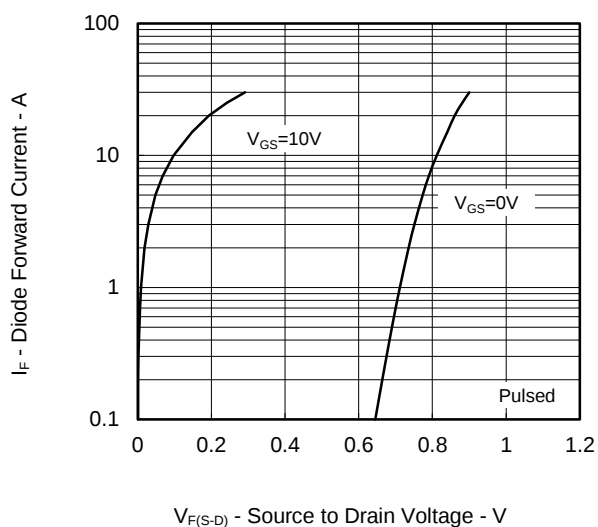
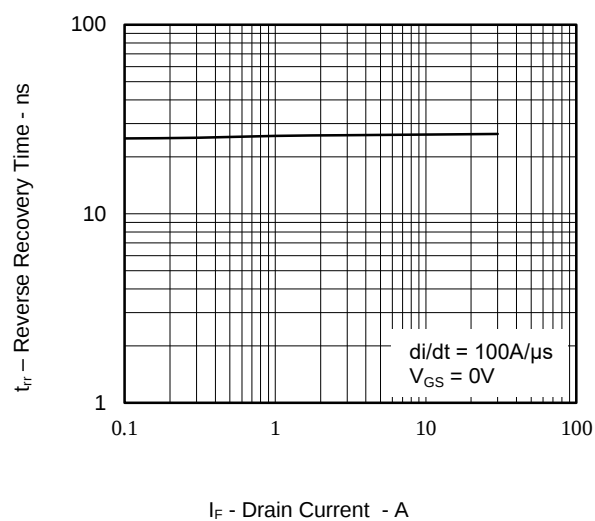
SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS

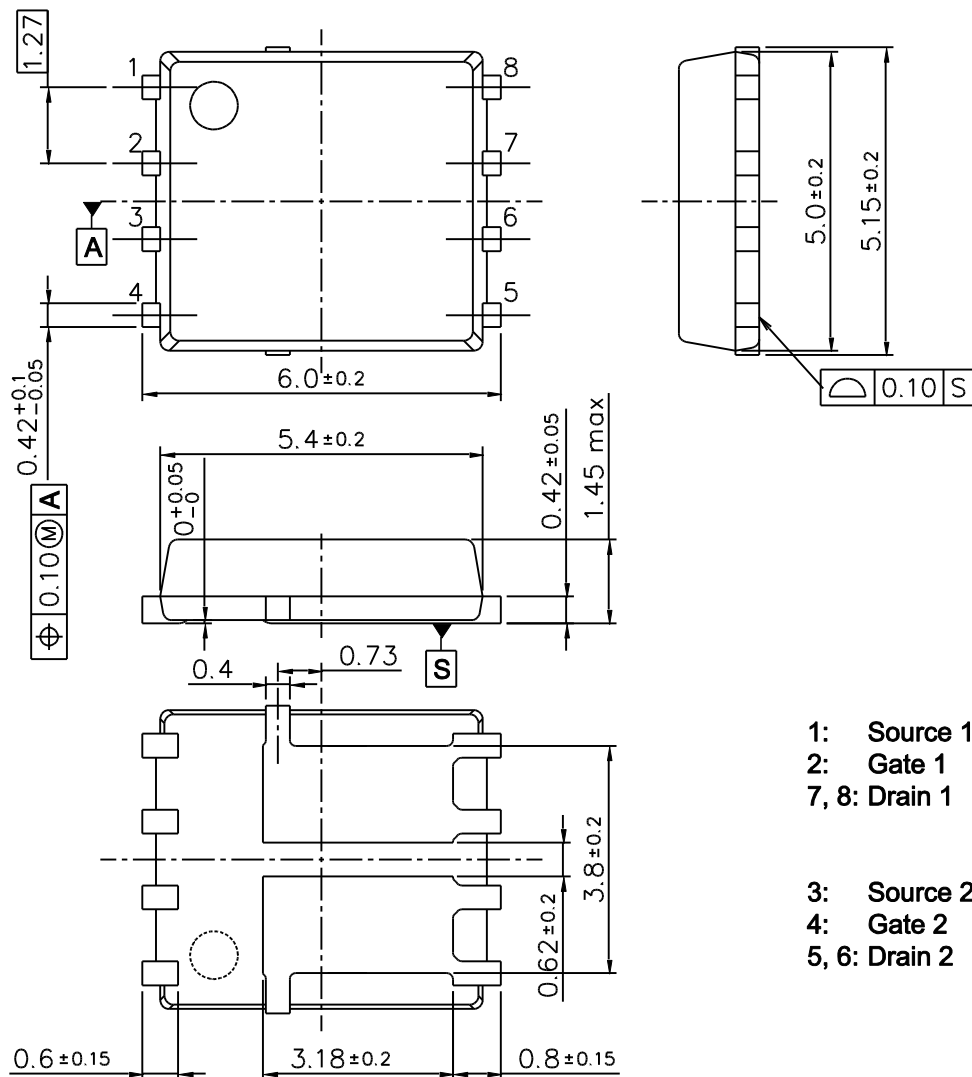


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

REVERSE RECOVERY TIME vs.
DRAIN CURRENT

Package Drawings (Unit: mm)**8-pin HSON Dual (Mass: 0.12 g TYP.)**

Renesas package code: PLSN0008DA-A



Revision History	NP30N06QDK Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Mar 28, 2016	—	First Edition Issued
2.00	May 24 ,2018	2	Note 5 was added
		3	Note 2 was added

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