NP60N04VLK

40 V – 60 A – N-channel Power MOS FET
Application: Automotive

R07DS1246EJ0200
Rev.2.00
May 24, 2018

Description

The NP60N04VLK is N-channel MOS Field Effect Transistors designed for high current switching applications.

Features

- Super low on-state resistance
  $R_{DS(on)}$ = 3.9 mΩ MAX. (V_{GS} = 10 V, I_D = 30 A)
- Low C_{iss}: C_{iss} = 2450 pF TYP. (V_{DS} = 25 V)
- Logic level drive type
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Packing		Package
NP60N04VLK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	TO-252 (MP-3ZP)
NP60N04VLK-E2-AY *1			Taping (E2 type)	

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±60	A
Drain Current (pulse) *1*3	$I_{D(pulse)}$	±240	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	105	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Repetitive Avalanche Current *2*3	I_{AR}	28	A
Repetitive Avalanche Energy *2*3	E_{AR}	78	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$ *3	1.43	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$ *3	125	°C/W

Notes: *1 T_C = 25°C, $P_W \leq$ 10 μs, Duty Cycle ≤ 1%
*2 R_G = 25 Ω, V_{GS} = 20 V → 0 V
*3 Not subject of production test. Verified by design/characterization.

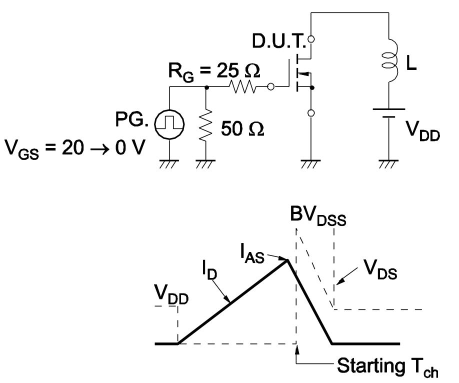
Electrical Characteristics (T_A = 25°C)

Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	±10	μA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	1.5	1.8	2.5	V	V_{DS} = V_{GS}, I_D = 250 μA
Forward Transfer Admittance *1	| y_{fs} |	30	61	—	S	V_{DS} = 5 V, I_D = 30 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$	—	3.2	3.9	mΩ	V_{GS} = 10 V, I_D = 30 A
	$R_{DS(on)2}$	—	4.3	8.6	mΩ	V_{GS} = 4.5 V, I_D = 15 A
Input Capacitance *2	C_{iss}	—	2450	3680	pF	V_{DS} = 25 V
Output Capacitance *2	C_{oss}	—	340	510	pF	V_{GS} = 0 V
Reverse Transfer Capacitance *2	C_{rss}	—	140	260	pF	f = 1 MHz
Turn-on Delay Time *2	$t_{d(on)}$	—	14	31	ns	V_{DD} = 20 V, I_D = 30 A
Rise Time *2	t_r	—	6	15	ns	V_{GS} = 10 V
Turn-off Delay Time *2	$t_{d(off)}$	—	49	98	ns	R_G = 0 Ω
Fall Time *2	t_f	—	6	15	ns	
Total Gate Charge *2	Q_G	—	42	63	nC	V_{DD} = 32 V
Gate to Source Charge	Q_{GS}	—	11	—	nC	V_{GS} = 10 V
Gate to Drain Charge	Q_{GD}	—	6	—	nC	I_D = 60 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$	—	0.9	1.5	V	I_F = 60 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	—	36	—	ns	I_F = 60 A, V_{GS} = 0 V
Reverse Recovery Charge	Q_{rr}	—	44	—	nC	di/dt = 100 A/μs

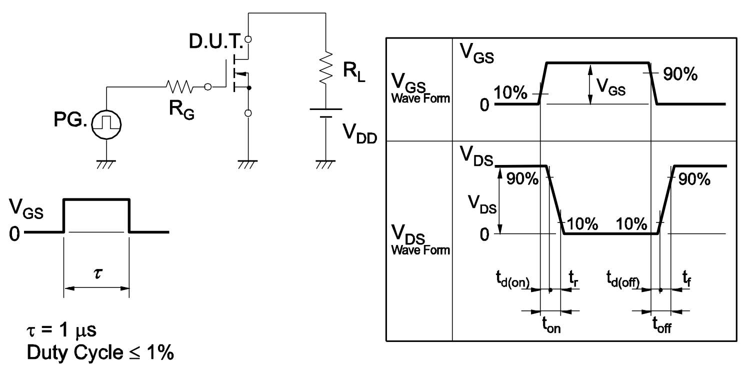
Note: *1 Pulsed test

Note: *2 Not subject of production test. Verified by design/characterization.

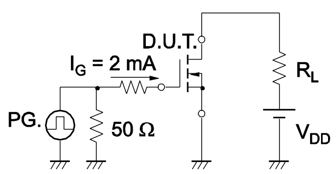
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

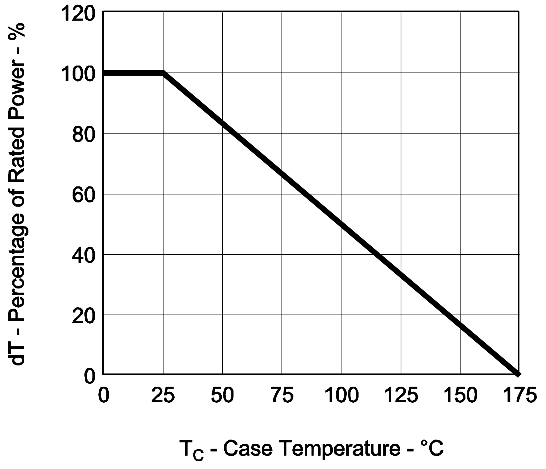


TEST CIRCUIT 3 GATE CHARGE

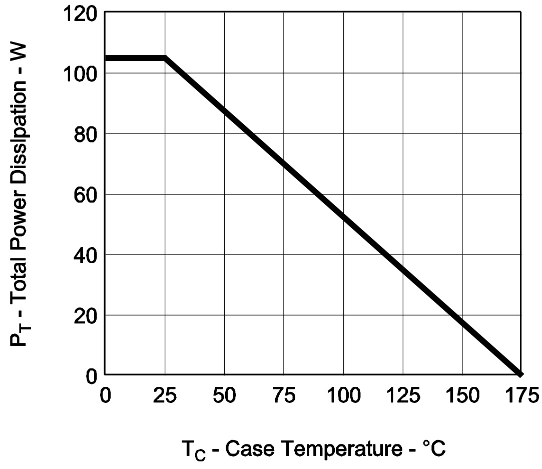


Typical Characteristics (T_A = 25°C)

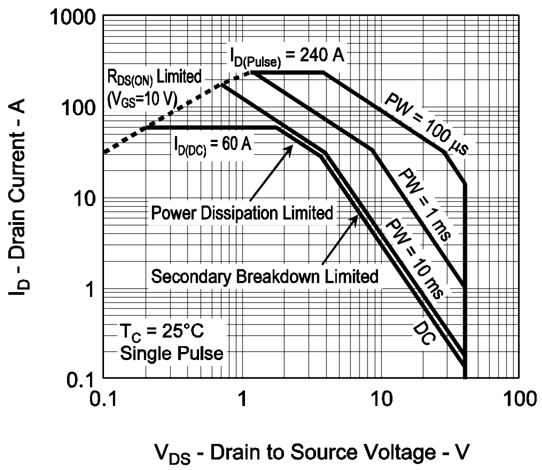
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



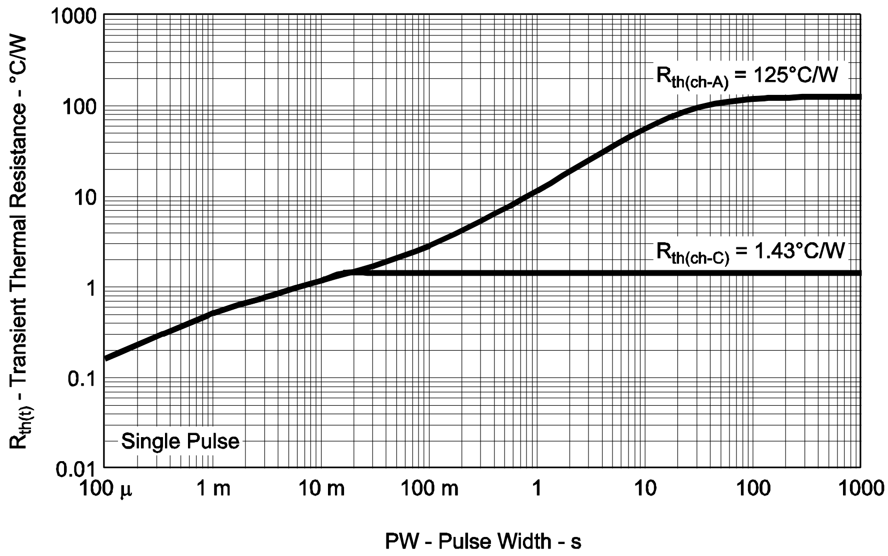
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



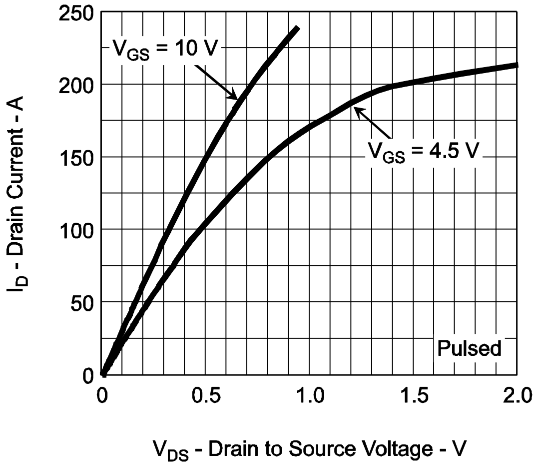
FORWARD BIAS SAFE OPERATING AREA



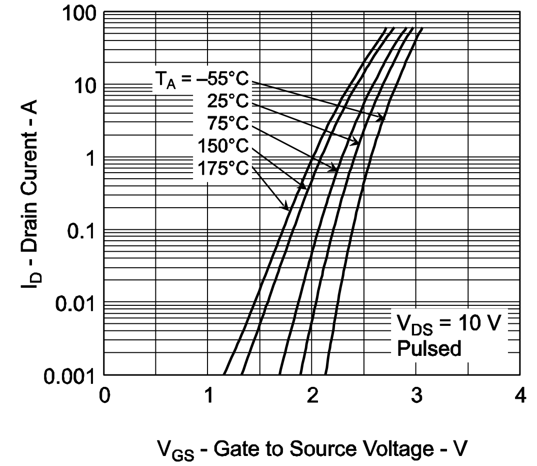
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



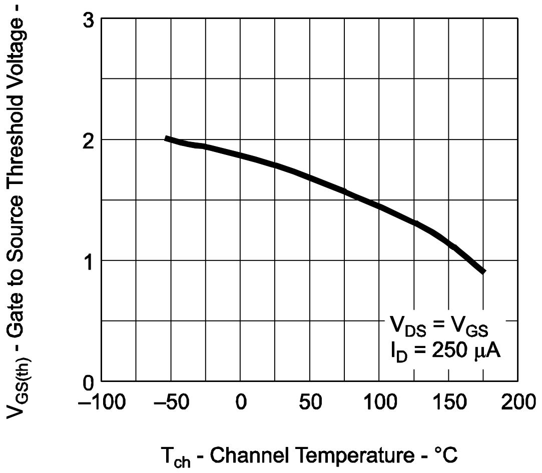
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



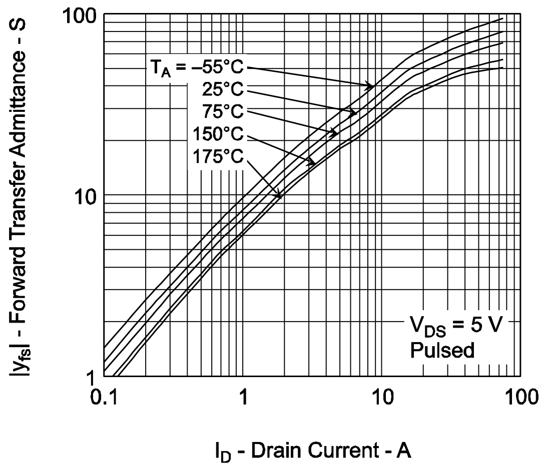
FORWARD TRANSFER CHARACTERISTICS



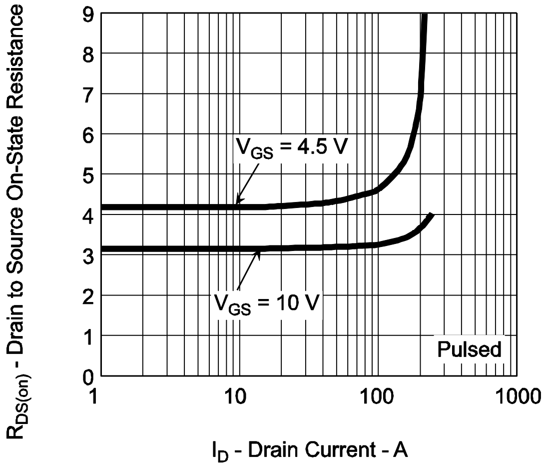
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



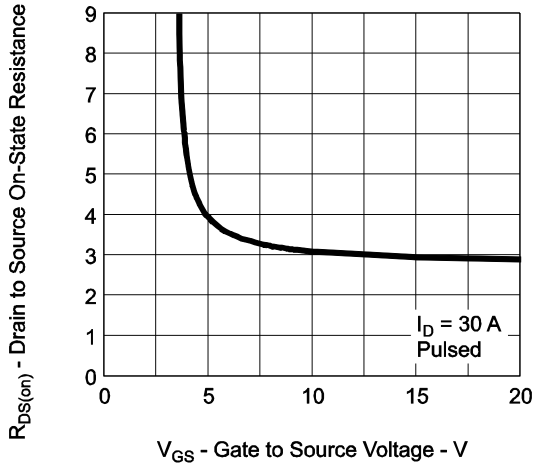
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



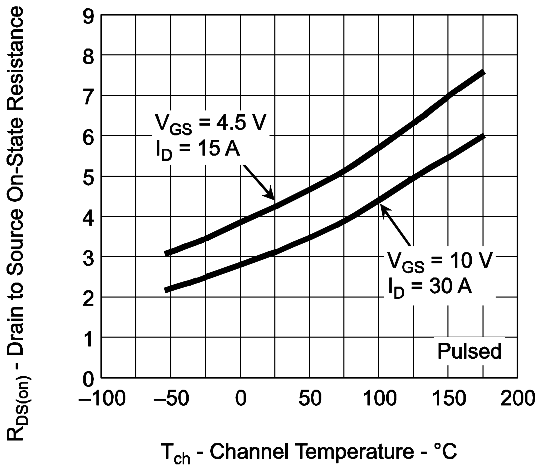
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



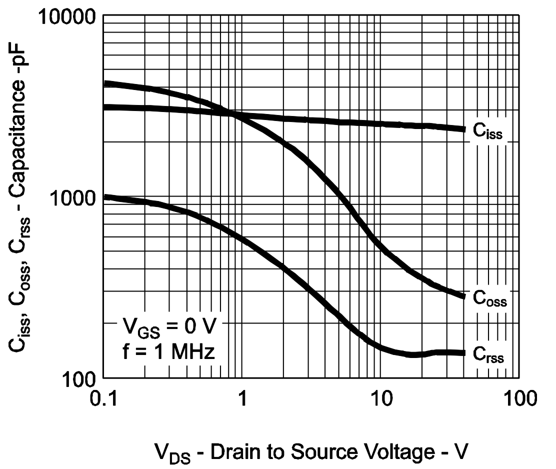
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



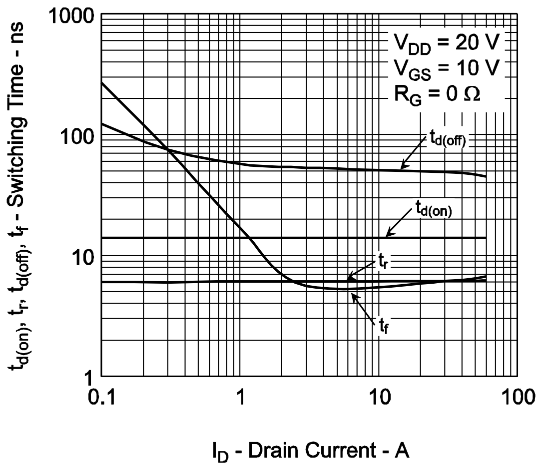
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



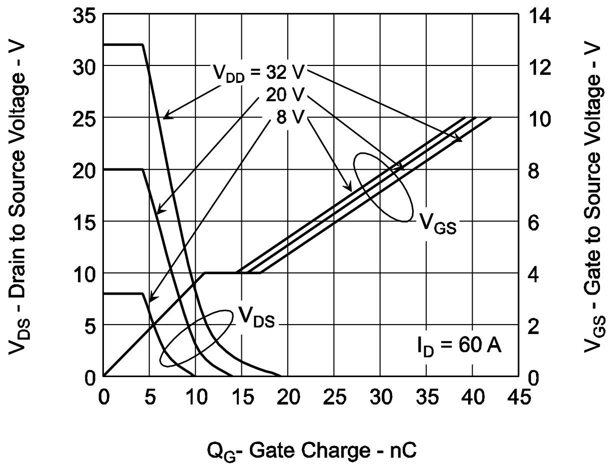
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



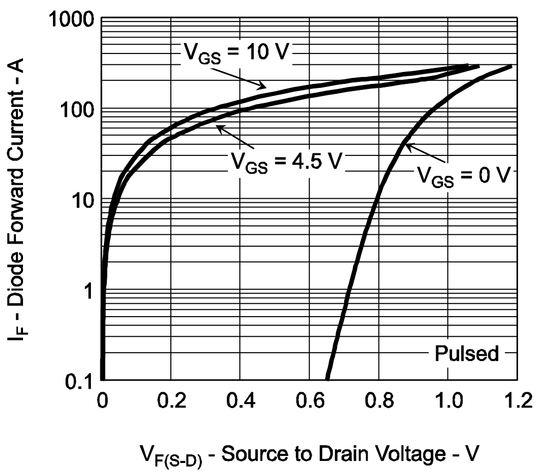
SWITCHING CHARACTERISTICS



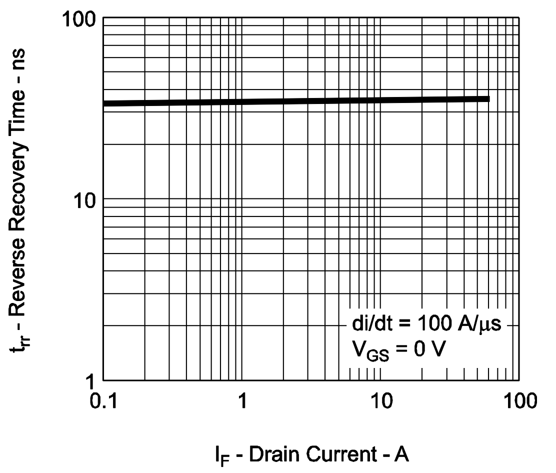
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



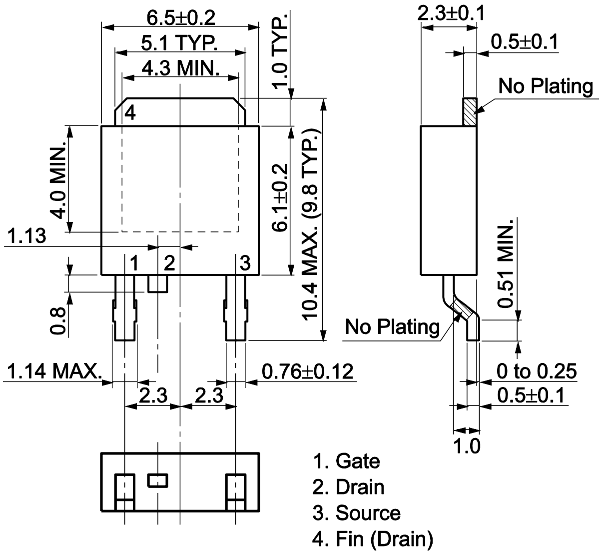
REVERSE RECOVERY TIME vs. DRAIN CURRENT



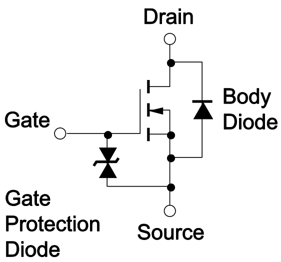
Package Drawing (Unit: mm)

TO-252 (MP-3ZP) (Mass: 0.3g TYP.)

Renesas Code: PRSS0004ZP-A



Equivalent Circuit



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	NP60N04VLK Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Feb 12, 2015	—	First Edition Issued
2.00	May 24 ,2018	1	Note 3 was added
		2	Note 2 was added

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