

NP75N04YUK

May 24, 2018

Data Sheet

Description

The NP75N04YUK is N-channel MOS Field Effect Transistors designed for high current switching applications.

Features

- Super low on-state resistance
 - $R_{DS(on)} = 3.3 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 38 \text{ A})$
- Non logic level drive type
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Pac	Package	
NP75N04YUK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP75N04YUK-E2-AY *1			Taping (E2 type)	

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit	
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	40	V	
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V	
Drain Current (DC) ($T_c = 25^{\circ}C$)	I _{D(DC)}	±75	A	
Drain Current (pulse) *1, 4	I _{D(pulse)}	±300	A	
Total Power Dissipation ($T_c = 25^{\circ}C$)	P _{T1}	138	W	
Total Power Dissipation ($T_A = 25^{\circ}C$) *2	P _{T2}	1.0	W	
Channel Temperature	T _{ch}	175	°C	
Storage Temperature	T _{stg}	–55 to +175	°C	
Repetitive Avalanche Current *3, 4	I _{AR}	35	A	
Repetitive Avalanche Energy *3, 4	E _{AR}	123	mJ	

Thermal Resistance

Channel to Case Thermal Resistance	Rth(ch-C)*4	1.09	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A) *4	150	°C/W

Notes: *1 T_C = 25°C, $P_W \leq$ 10 $\mu s,$ Duty Cycle \leq 1%

- *2 Mounted on glass epoxy substrate of 40 mm \times 40 mm \times 1.6 mmt with 4% Copper area (35 $\mu m)$
- *3 R_G = 25 Ω , V_{GS} = 20 V \rightarrow 0 V
- *4. Not subject of production test. Verified by design/characterization.



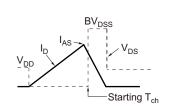
Electrical Characteristics (T_A = 25°C)

ltem	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions	
Zero Gate Voltage Drain Current	I _{DSS}			1	μA	V _{DS} = 40 V, V _{GS} = 0 V	
Gate Leakage Current	I _{GSS}			±100	nA	V_{GS} = ±20 V, V_{DS} = 0 V	
Gate to Source Threshold Voltage	V _{GS(th)}	2.0	3.0	4.0	V	V_{DS} = V_{GS} , I_D = 250 μ A	
Forward Transfer Admittance *1	y _{fs}	31	62	—	S	V _{DS} = 5 V, I _D = 38 A	
Drain to Source On-state Resistance *1	R _{DS(on)}	_	2.6	3.3	mΩ	V_{GS} = 10 V, I_{D} = 38 A	
Input Capacitance *2	Ciss	_	3400	5100	pF	V _{DS} = 25 V	
Output Capacitance *2	Coss	_	480	720	pF	V _{GS} = 0 V	
Reverse Transfer Capacitance *2	Crss	_	180	330	pF	f = 1 MHz	
Turn-on Delay Time *2	t _{d(on)}	_	24	48	ns	V_{DD} = 20 V, I_{D} = 38 A	
Rise Time *2	tr	_	10	25	ns	V _{GS} = 10 V	
Turn-off Delay Time *2	t _{d(off)}	_	60	120	ns	$R_G = 0 \Omega$	
Fall Time *2	t _f	_	7	17	ns	1	
Total Gate Charge *2	Q_{G}	_	58	87	nC	V _{DD} = 32 V	
Gate to Source Charge	Q_{GS}	_	16	—	nC	V _{GS} = 10 V	
Gate to Drain Charge	Q _{GD}		15	_	nC	I _D = 75 A	
Body Diode Forward Voltage *1	V _{F(S-D)}		0.9	1.5	V	I _F = 75 A, V _{GS} = 0 V	
Reverse Recovery Time	trr		42		ns	I _F = 75 A, V _{GS} = 0 V	
Reverse Recovery Charge	Qrr		51	_	nC	di/dt = 100 A/μs	

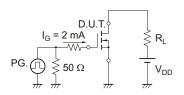
Note: *1 Pulsed test

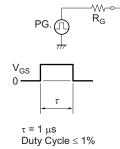
Note: *2 Not subject of production test. Verified by design/characterization.

TEST CIRCUIT 1 AVALANCHE CAPABILITY



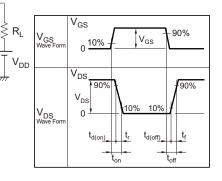
TEST CIRCUIT 3 GATE CHARGE





TEST CIRCUIT 2 SWITCHING TIME

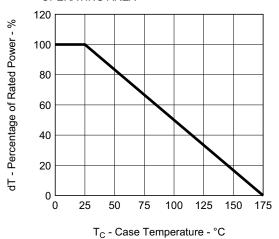
D.U.T.

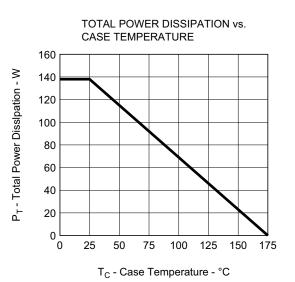




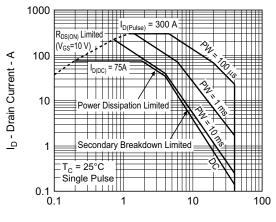
Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

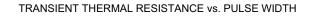


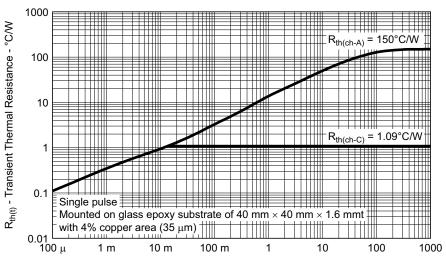


FORWARD BIAS SAFE OPERATING AREA



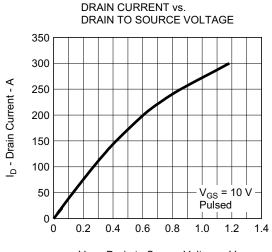




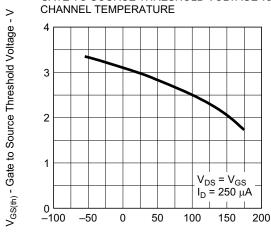


PW - Pulse Width - s

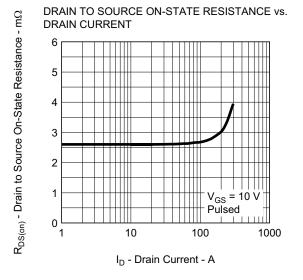




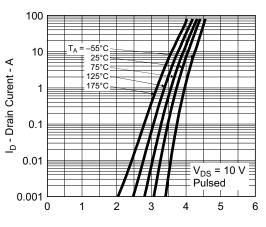
V_{DS} - Drain to Source Voltage - V



T_{ch} - Channel Temperature - °C

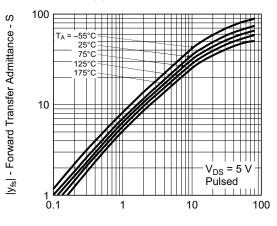


FORWARD TRANSFER CHARACTERISTICS

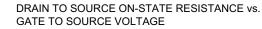


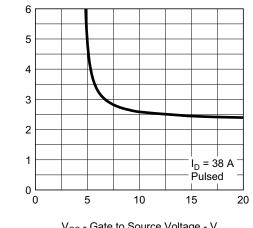


FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



I_D - Drain Current - A



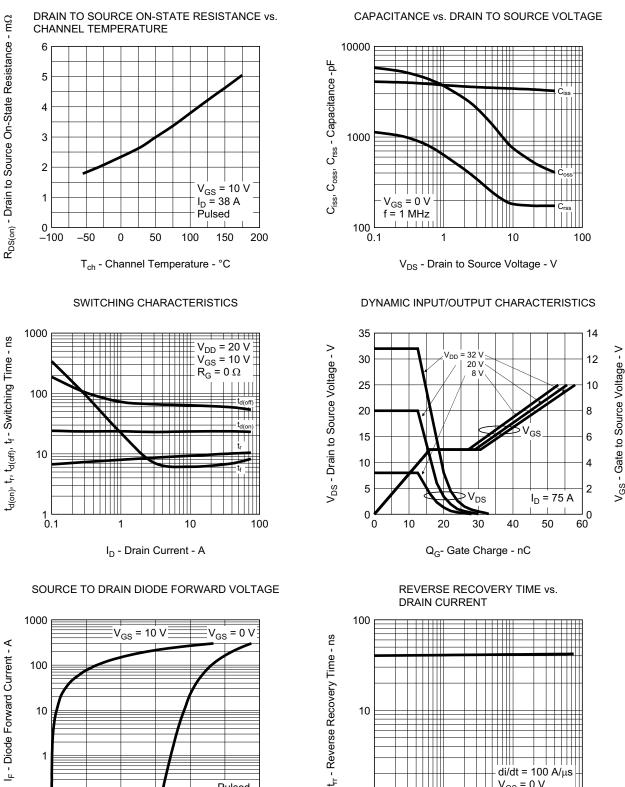


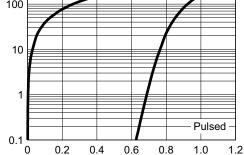
V_{GS} - Gate to Source Voltage - V

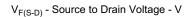
GATE TO SOURCE THRESHOLD VOLTAGE vs.

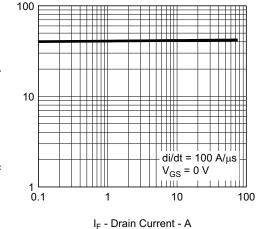
 $R_{DS(on)}$ - Drain to Source On-State Resistance - $m\Omega$

NP75N04YUK





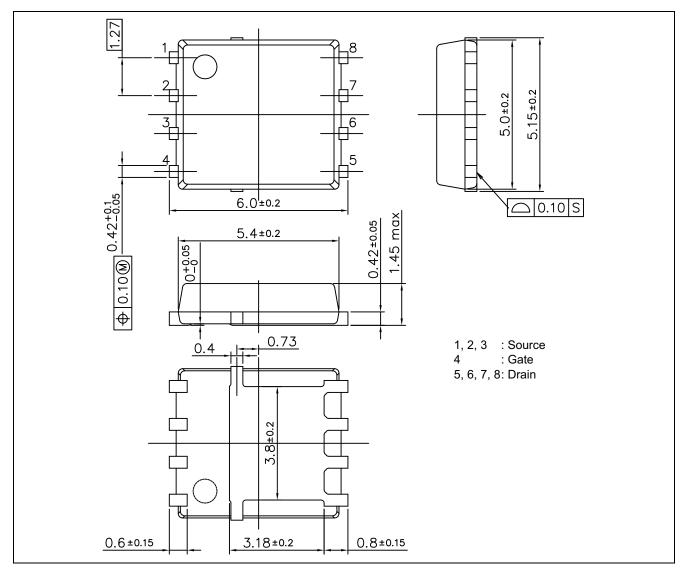




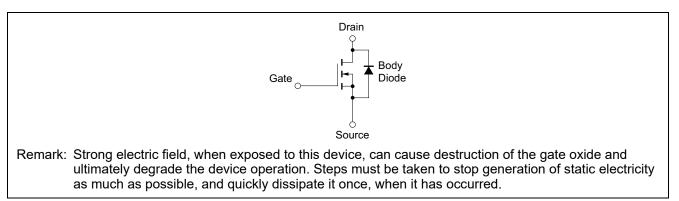


Package Drawing (Unit: mm)

8-pin HSON (Mass: 0.128 g TYP.)



Equivalent Circuit





Revision History

NP75N04YUK Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Feb 08, 2013	—	First Edition Issued	
2.00	May 24 ,2018	1	Note 4 was added	
		2	Note 2 was added	

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