

NP100N055PUK

MOS FIELD EFFECT TRANSISTOR

R07DS0589EJ0200 Rev.2.00 May 24, 2018

Description

The NP100N055PUK is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance $R_{DS(on)} = 3.25 \text{ m}\Omega \text{ MAX. } (V_{GS} = 10 \text{ V}, I_D = 50 \text{ A})$
- Low C_{iss} : $C_{iss} = 4900 \text{ pF TYP.} (V_{DS} = 25 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Pac	Package	
NP100N055PUK-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-263 (MP-25ZP)
NP100N055PUK-E2-AY *1			Taping (E2 type)	

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	55	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±100	Α
Drain Current (pulse) *1, 3	I _{D(pulse)}	±400	Α
Total Power Dissipation (T _C = 25°C)	P _{T1}	176	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.8	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	–55 to 175	°C
Repetitive Avalanche Current *2, 3	I _{AR}	38	Α
Repetitive Avalanche Energy *2,3	Ear	144	mJ

Thermal Resistance

Channel to Case Thermal Resistance $R_{th(ch-C)^*3}$ 0.85 °C/W Channel to Ambient Thermal Resistance $R_{th(ch-A)^*3}$ 83.3 °C/W

Notes: *1 T_C = 25°C, $P_W \le 10~\mu s$, Duty Cycle $\le 1\%$

*2 R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V

*3 Not subject of production test. Verified by design/characterization.

Electrical Characteristics (T_A = 25°C)

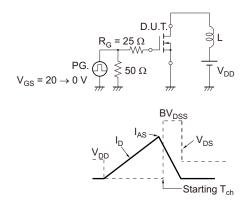
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions	
Zero Gate Voltage Drain Current	I _{DSS}	_	_	1	μΑ	V _{DS} = 55 V, V _{GS} = 0 V	
Gate Leakage Current	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
Forward Transfer Admittance *1	y fs	40	80	_	S	$V_{DS} = 5 \text{ V}, I_{D} = 50 \text{ A}$	
Drain to Source On-state Resistance *1	R _{DS(on)}	_	2.70	3.25	mΩ	$V_{GS} = 10 \text{ V}, I_{D} = 50 \text{ A}$	
Input Capacitance *2	C _{iss}	_	4900	7350	pF	V _{DS} = 25 V	
Output Capacitance *2	Coss	_	500	750	pF	$V_{GS} = 0 V$	
Reverse Transfer Capacitance *2	C _{rss}	_	180	330	pF	f = 1 MHz	
Turn-on Delay Time *2	t _{d(on)}	_	28	70	ns	$V_{DD} = 28 \text{ V}, I_{D} = 50 \text{ A}$	
Rise Time *2	t _r	_	12	30	ns	V _{GS} = 10 V	
Turn-off Delay Time *2	t _{d(off)}	_	70	140	ns	$R_G = 0 \Omega$	
Fall Time *2	t _f	_	7	20	ns		
Total Gate Charge *2	Q_{G}	_	80	120	nC	V _{DD} = 44 V	
Gate to Source Charge	Q _{GS}	_	21	_	nC	V _{GS} = 10 V	
Gate to Drain Charge	Q _{GD}	_	20	_	nC	I _D = 100 A	
Body Diode Forward Voltage *1	V _{F(S-D)}		0.9	1.5	V	I _F = 100 A, V _{GS} = 0 V	
Reverse Recovery Time	t _{rr}		52	_	ns	I _F = 100 A, V _{GS} = 0 V	
Reverse Recovery Charge	Qrr	_	95	_	nC	di/dt = 100 A/μs	

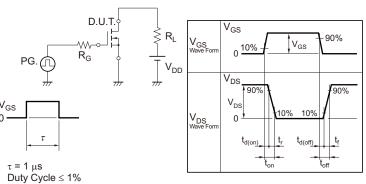
Note: *1 Pulsed test

Note: *2 Not subject of production test. Verified by design/characterization.

TEST CIRCUIT 1 AVALANCHE CAPABILITY

TEST CIRCUIT 2 SWITCHING TIME



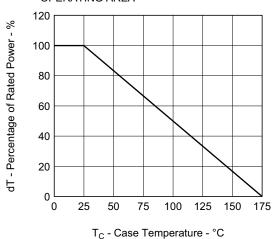


TEST CIRCUIT 3 GATE CHARGE

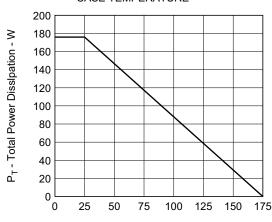
$$\begin{array}{c|c} D.U.T. \\ \hline I_G = 2 \text{ mA} \\ \hline WV \\ \hline \end{array} \begin{array}{c} PG. \\ \hline \end{array} \begin{array}{c} S \\ S \\ S \\ \hline \end{array} \begin{array}{c} O.U.T. \\ \hline \end{array} \begin{array}{c} S \\ C \\ \hline \end{array} \begin{array}{c} O.U.T. \\ \end{array}$$

Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

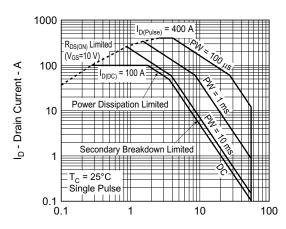


TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



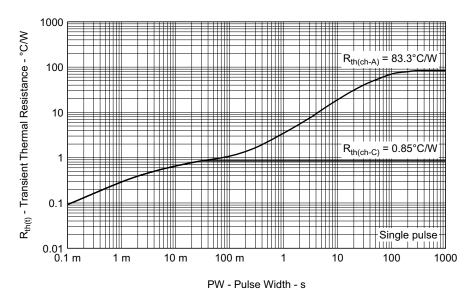
T_C - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



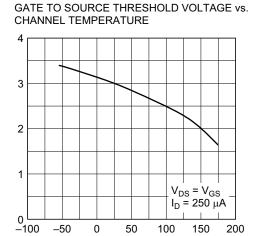
 V_{DS} - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

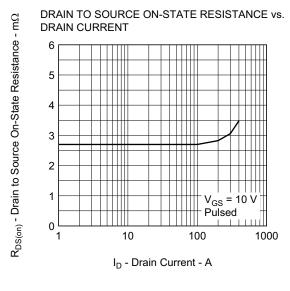


V_{GS(th)} - Gate to Source Threshold Voltage - V

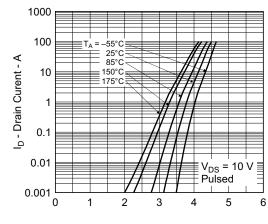
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE 500 400 I_D - Drain Current - A 300 200 100 $V_{GS} = 10 \text{ V}$ Pulsed 0 0 0.2 0.4 0.6 8.0 1.0 1.2 1.4 1.6 V_{DS} - Drain to Source Voltage - V



 $\rm T_{ch}$ - Channel Temperature - $^{\circ}\rm C$

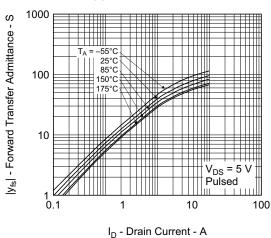


FORWARD TRANSFER CHARACTERISTICS

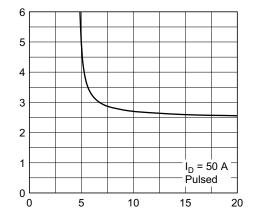


V_{GS} - Gate to Source Voltage - V

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

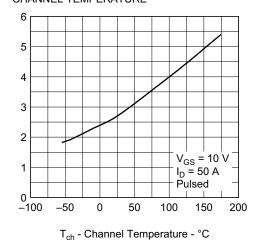


V_{GS} - Gate to Source Voltage - V

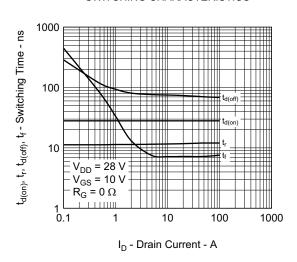
 $R_{DS(on)}$ - Drain to Source On-State Resistance - $m\Omega$

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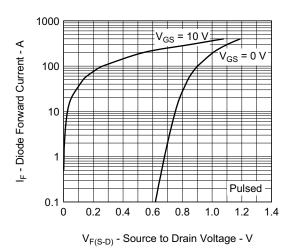
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



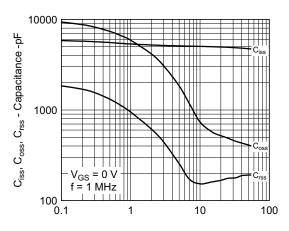
SWITCHING CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

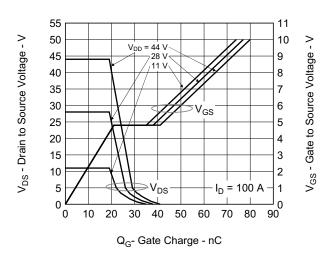


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

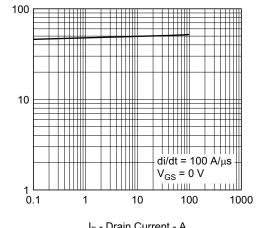


V_{DS} - Drain to Source Voltage - V

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT

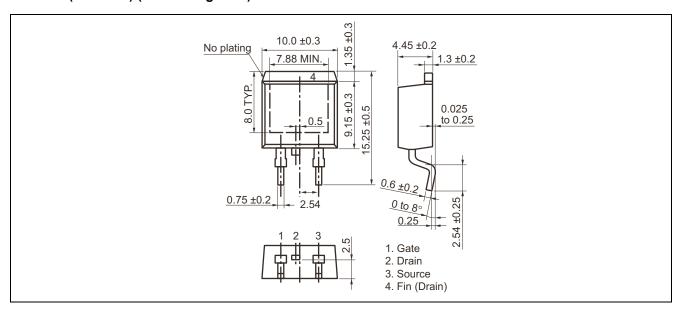


IF - Drain Current - A

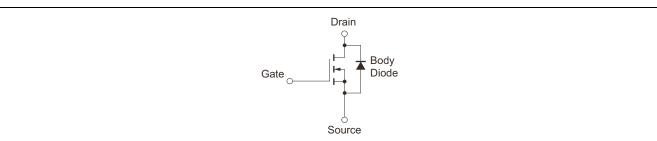
t_{rr} - Reverse Recovery Time - ns

Package Drawing (Unit: mm)

TO-263 (MP-25ZP) (Mass: 1.5 g TYP.)



Equivalent Circuit



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History

NP100N055PUK Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Dec 12, 2011	_	First Edition Issued	
2.00	May 24 ,2018	1	Note 3 was added	
		2	Note 2 was added	

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