Data Sheet

NP75P04YLG

MOS FIELD EFFECT TRANSISTOR

R07DS0183EJ0200
Rev.2.00
Mar 16, 2011

Description

The NP75P04YLG is P-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
  — $R_{DS(on)}$ = 9.7 mΩ MAX. (V_{GS} = –10 V, I_D = –37.5 A)
  — $R_{DS(on)}$ = 14 mΩ MAX. (V_{GS} = –5 V, I_D = –37.5 A)
- Logic level drive type
- Gate to Source ESD protection diode built in
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP75P04YLG -E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	8-pin HSON, Taping (E1 type)
NP75P04YLG -E2-AY *1			8-pin HSON, Taping (E2 type)

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	∓75	A
Drain Current (pulse) *1	$I_{D(pulse)}$	∓225	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	138	W
Total Power Dissipation (T_A = 25°C) *2	P_{T2}	1.0	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
<R> Single Avalanche Current *3	I_{AS}	35	A
<R> Single Avalanche Energy *3	E_{AS}	123	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.09	°C/W
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	150	°C/W

Notes: *1. T_C = 25°C, PW ≤ 10 μs, Duty Cycle ≤ 1%
*2. Mounted on glass epoxy substrate of 40 mm x 40 mm x 0.8 mmt
*3. Starting T_{ch} = 25°C, V_{DD} = –20 V, R_G = 25 Ω, L = 100 μH, V_{GS} = –20 → 0 V

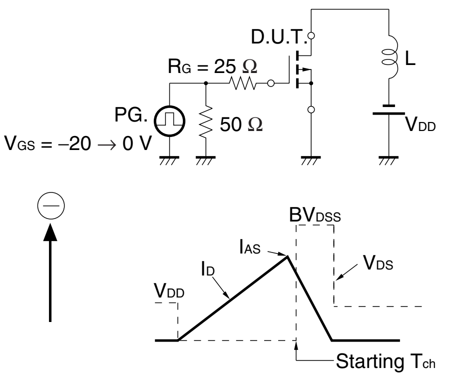
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

Electrical Characteristics (T_A = 25°C)

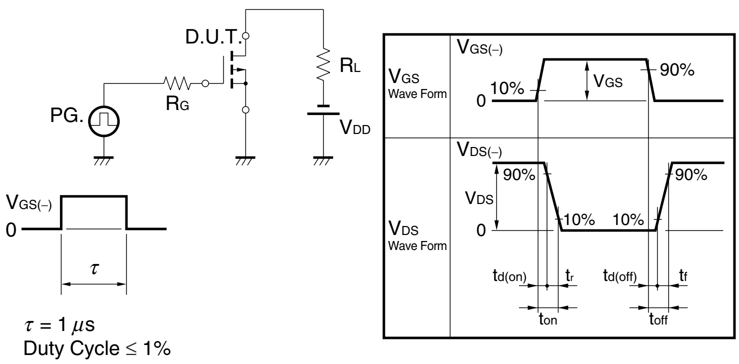
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			–1	μA	V_{DS} = –40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			∓10	μA	V_{GS} = ∓20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	–1.0	–1.7	–2.5	V	V_{DS} = V_{GS}, I_D = –250 μA
Forward Transfer Admittance *1	$\mid y_{fs} \mid$	31	63		S	V_{DS} = –5 V, I_D = –37.5 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$		7.7	9.7	mΩ	V_{GS} = –10 V, I_D = –37.5 A
	$R_{DS(on)2}$		9.3	14	mΩ	V_{GS} = –5 V, I_D = –37.5 A
Input Capacitance	C_{iss}		3200	4800	pF	V_{DS} = –25 V,
Output Capacitance	C_{oss}		460	600	pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		250	450	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		12	24	ns	V_{DD} = –20 V, I_D = –37.5 A,
Rise Time	t_r		11	27	ns	V_{GS} = –10 V,
Turn-off Delay Time	$t_{d(off)}$		320	640	ns	R_G = 0 Ω
Fall Time	t_f		180	440	ns	
Total Gate Charge	Q_G		91	140	nC	V_{DD} = –32 V,
Gate to Source Charge	Q_{GS}		14		nC	V_{GS} = –10 V,
Gate to Drain Charge	Q_{GD}		26		nC	I_D = –75 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		1.02	1.5	V	I_F = –75 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		43		ns	I_F = –75 A, V_{GS} = 0 V,
Reverse Recovery Charge	Q_{rr}		57		nC	di/dt = –100 A/μs

Note: *1. Pulsed

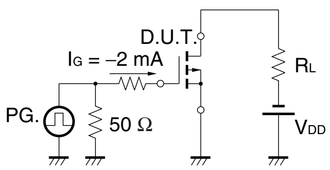
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

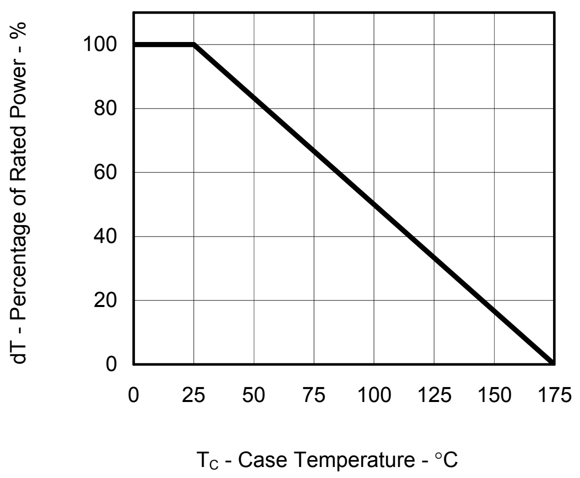


TEST CIRCUIT 3 GATE CHARGE

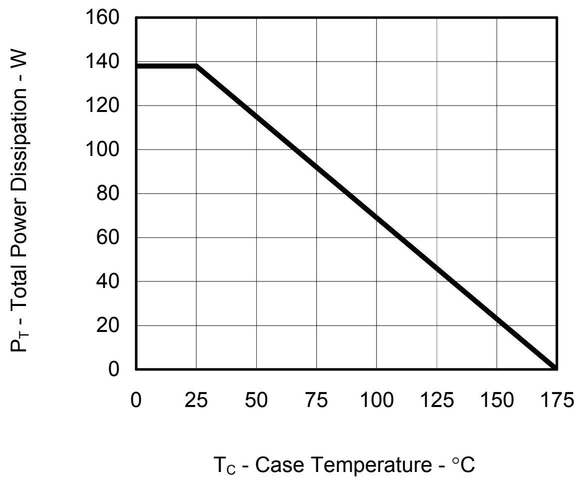


Typical Characteristics (T_A = 25°C)

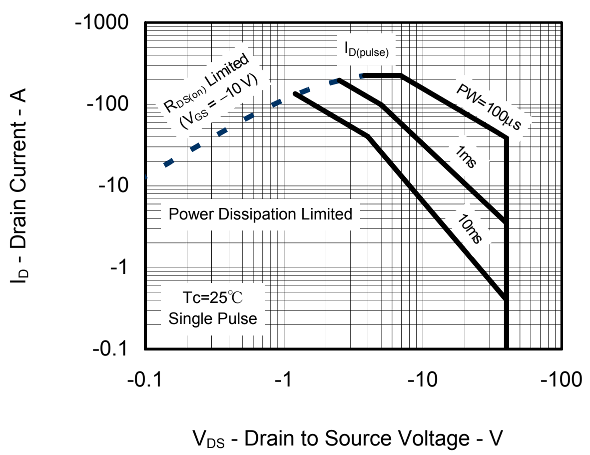
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



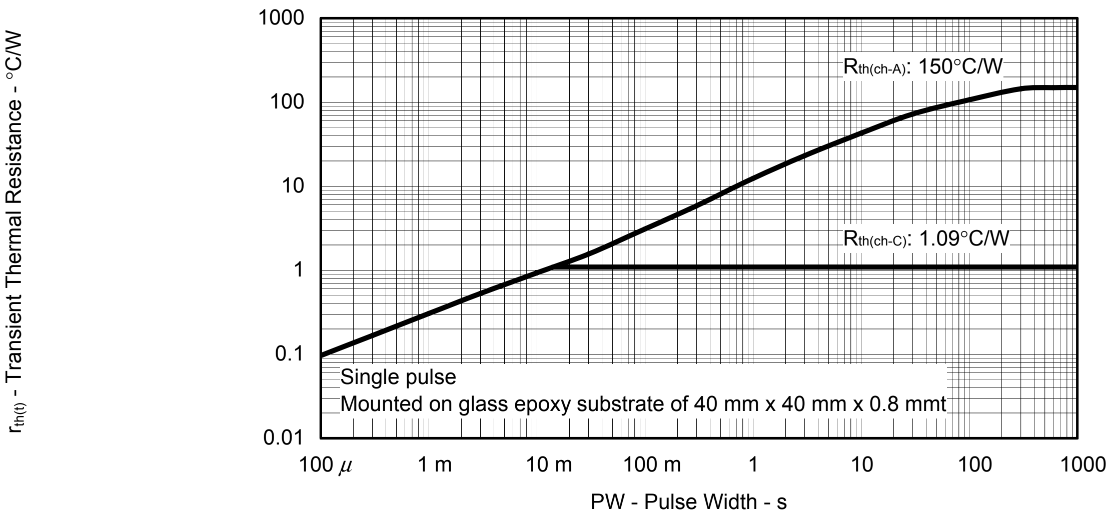
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



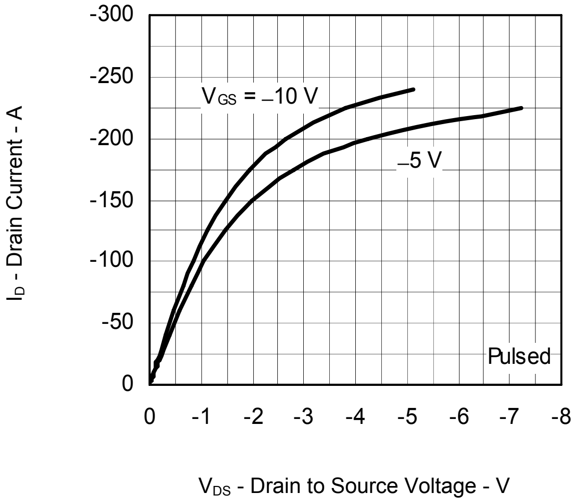
FORWARD BIAS SAFE OPERATING AREA



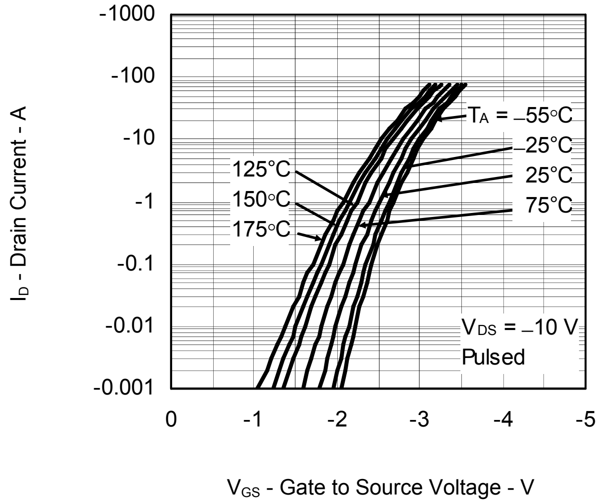
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



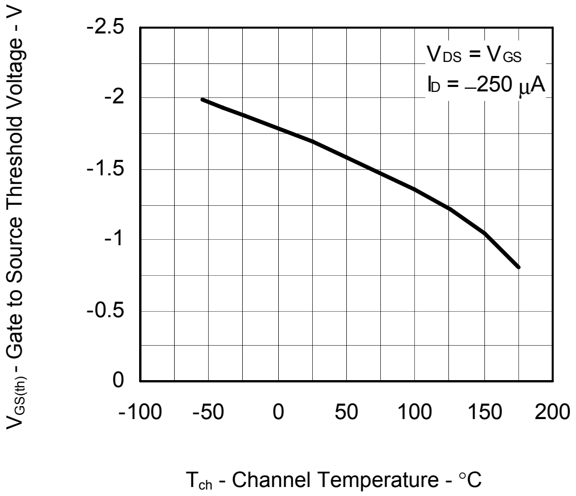
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



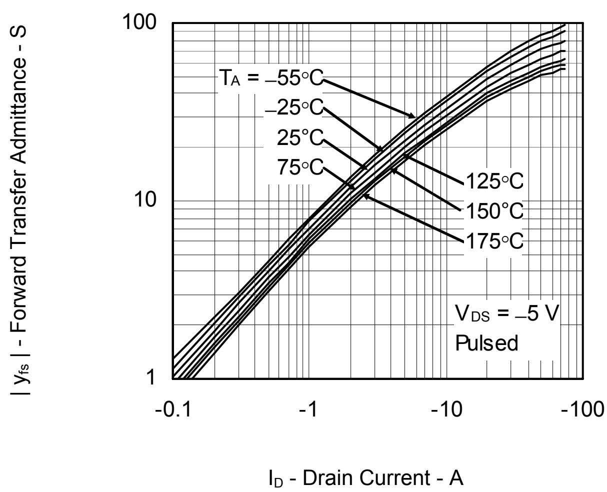
FORWARD TRANSFER CHARACTERISTICS



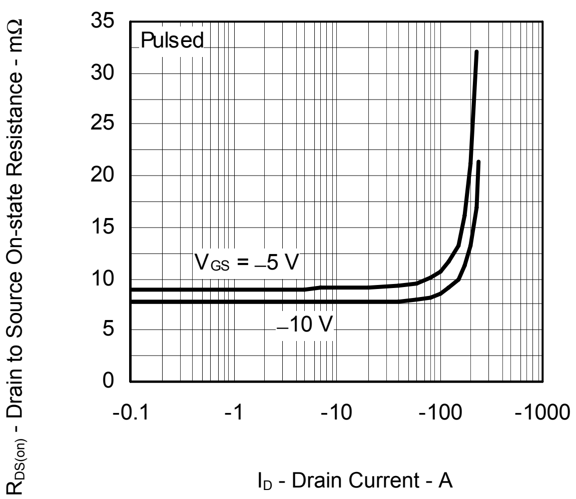
GATE TO SOURCE THRESHOLD VOLTAGE
vs. CHANNEL TEMPERATURE



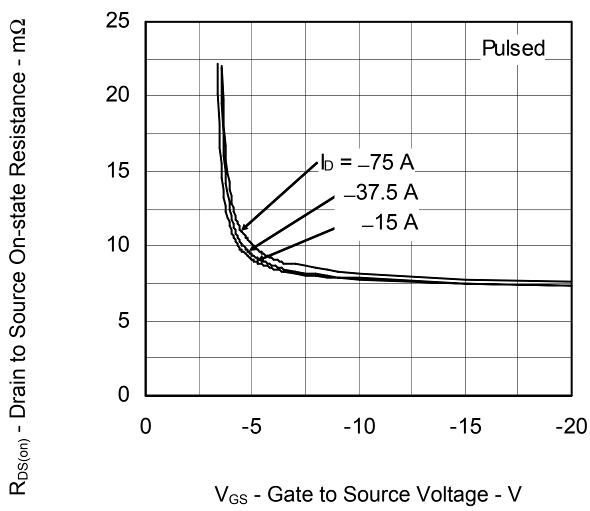
FORWARD TRANSFER ADMITTANCE vs. DRAIN
CURRENT



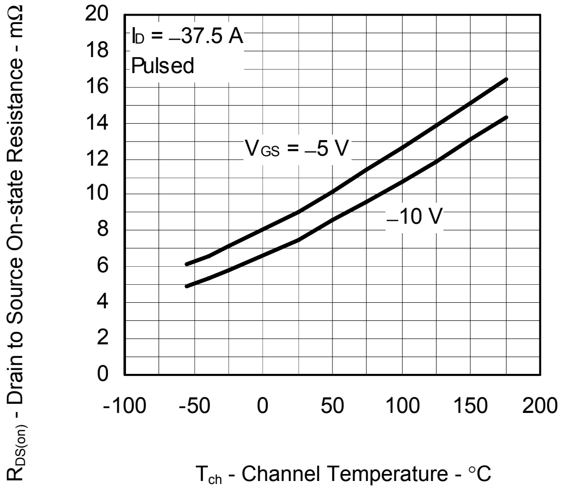
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



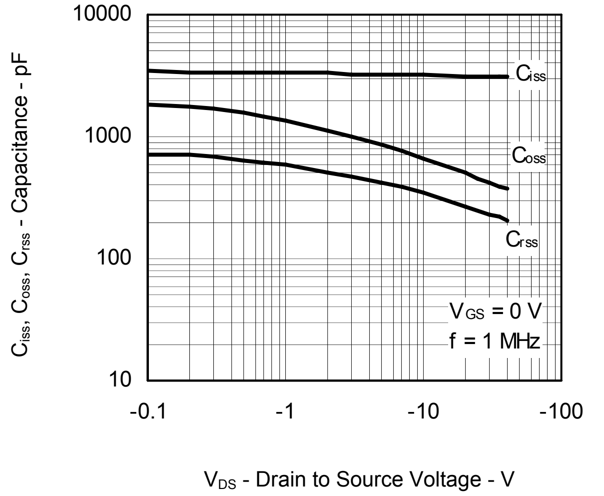
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



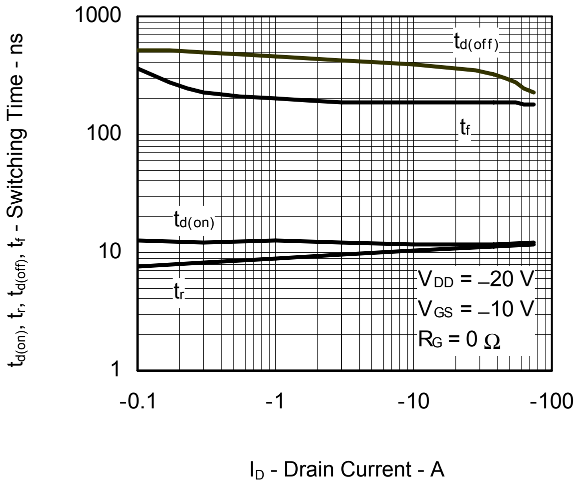
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



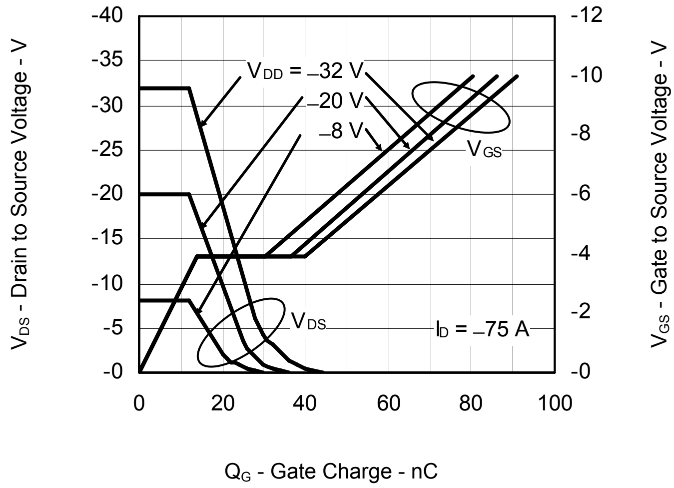
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



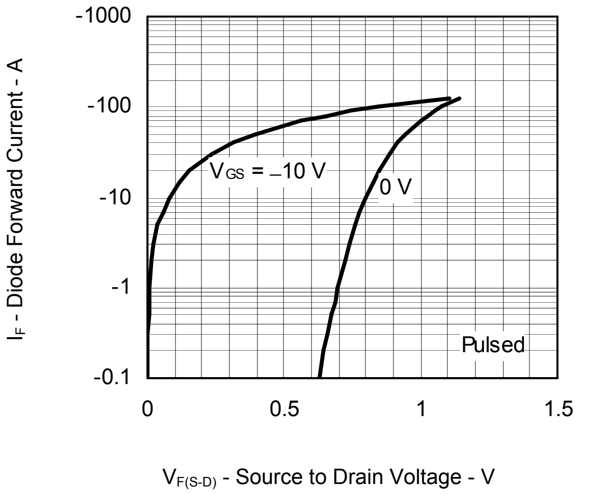
SWITCHING CHARACTERISTICS



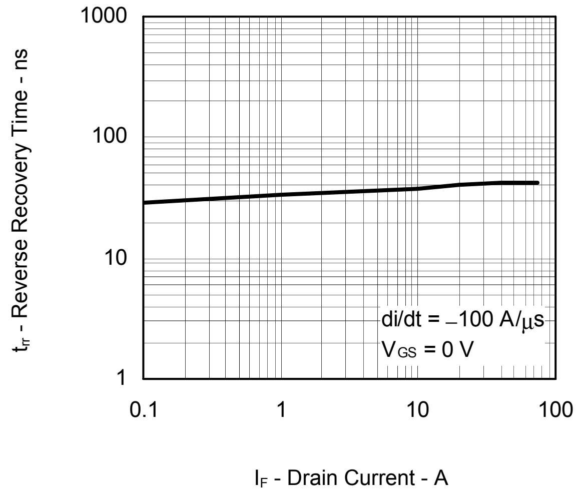
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

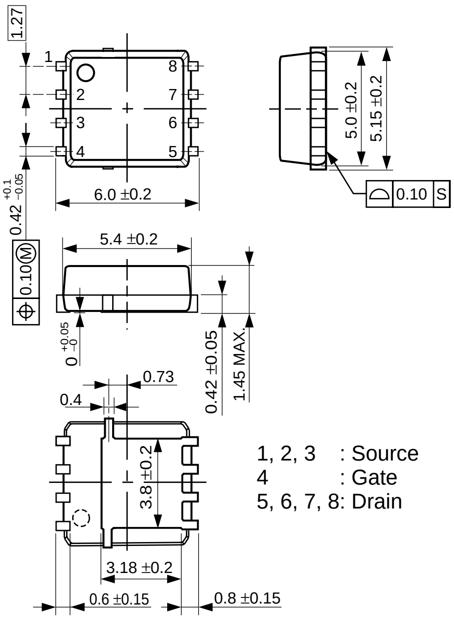


REVERSE RECOVERY TIME vs. DRAIN CURRENT

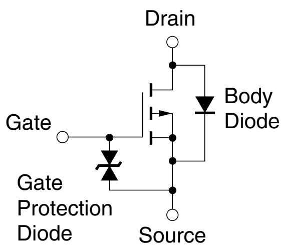


Package Drawings (Unit: mm)

8-pin HSON (Mass: 0.13 g TYP.)



Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Revision History	NP75P04YLG Data Sheet

Rev.	Date	Description	
		Page	**Summary**
1.00	Oct 22, 2010	–	First Edition Issued
2.00	Mar 16, 2011	p.1	Repetitive Avalanche Current -> Single Avalanche Current Repetitive Avalanche Energy -> Single Avalanche Energy Modification of Note *3

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