

# RJE0615JSP

-60 V, -10A Silicon P Channel Thermal FET  
Power Switching

R07DS0124EJ0300  
Rev.3.00  
Oct 27, 2014

## Description

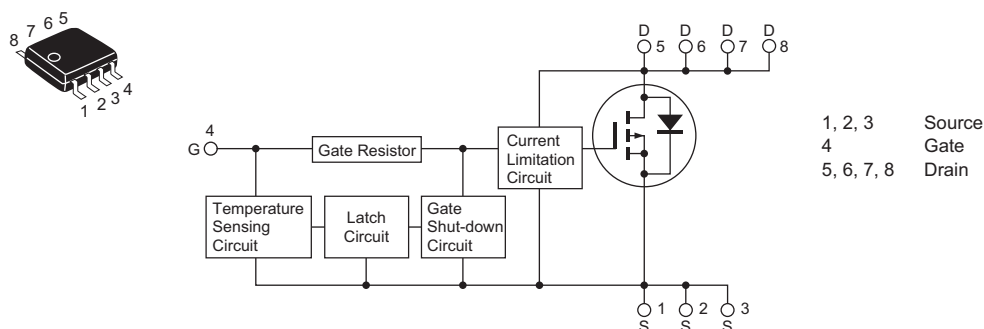
This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

## Features

- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Latch type shut down operation (need 0 voltage recovery).
- Built-in the current limitation circuit.
- Low on-resistance  $R_{DS(on)}$  : 53 m $\Omega$  Typ, 65 m $\Omega$  Max ( $V_{GS} = -10$  V)
- High density mounting

## Outline

RENESAS Package code: PRSP0008DD-D  
(Package name: SOP-8)



## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-60	V
Gate to source voltage	$V_{GSS}$	-16	V
	$V_{GSS}$	2.5	V
Drain current	$I_D$ <sup>Note 3</sup>	-10	A
Body-drain diode reverse drain current	$I_{DR}$	-10	A
Avalanche current	$I_{AP}$ <sup>Note 2</sup>	-4.7	A
Avalanche energy	$E_{AR}$ <sup>Note 2</sup>	94.7	mJ
Channel dissipation	$P_{ch}$ <sup>Note 1</sup>	2.5	W
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Notes: 1 1 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm),  $PW \leq 10$  s

2.  $T_{ch} = 25^\circ\text{C}$ ,  $R_g \geq 50 \Omega$

3. It provides by the current limitation lower bound value.

## Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>	-3.5	—	—	V	
	V <sub>IL</sub>	—	—	-1.2	V	
Input current (Gate non shut down)	I <sub>IH1</sub>	—	—	-100	μA	V <sub>i</sub> = -8 V, V <sub>DS</sub> = 0
	I <sub>IH2</sub>	—	—	-50	μA	V <sub>i</sub> = -3.5 V, V <sub>DS</sub> = 0
	I <sub>IL</sub>	—	—	-10	μA	V <sub>i</sub> = -1.2 V, V <sub>DS</sub> = 0
Input current (Gate shut down)	I <sub>IH(sD)1</sub>	—	-0.8	—	mA	V <sub>i</sub> = -8 V, V <sub>DS</sub> = 0
	I <sub>IH(sD)2</sub>	—	-0.35	—	mA	V <sub>i</sub> = -3.5 V, V <sub>DS</sub> = 0
Shut down temperature	T <sub>SD</sub>	—	175	—	°C	Channel temperature (dv/dt V <sub>GS</sub> ≥ 500 V/ms)
Gate operation voltage	V <sub>OP</sub>	-3.5	—	-12	V	
Drain current (Current limitation value)	I <sub>D limit</sub>	-10	—	—	A	V <sub>GS</sub> = -12 V, V <sub>DS</sub> = -10 V <sup>Note 4</sup>

Notes; 4. Pulse test

## Electrical Characteristics

(Ta = 25°C)

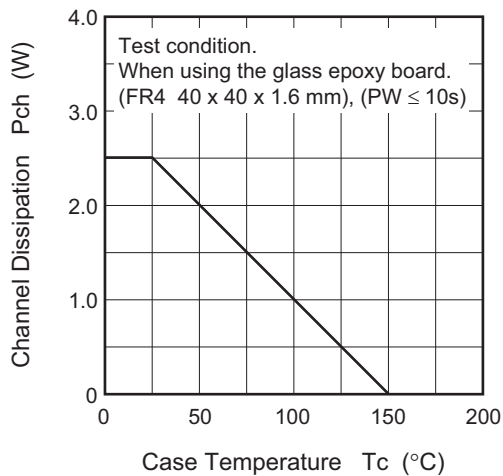
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I <sub>D1</sub>	—	—	-4	A	V <sub>GS</sub> = -3.5 V, V <sub>DS</sub> = -10 V
	I <sub>D2</sub>	—	—	-10	mA	V <sub>GS</sub> = -1.2 V, V <sub>DS</sub> = -10 V
	I <sub>D3</sub>	-10	—	—	A	V <sub>GS</sub> = -12 V, V <sub>DS</sub> = -10 V <sup>Note 5</sup>
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	-60	—	—	V	I <sub>D</sub> = -10 mA, V <sub>GS</sub> = 0
Gate to source breakdown voltage	V <sub>(BR)GSS</sub>	-16	—	—	V	I <sub>G</sub> = -800 μA, V <sub>DS</sub> = 0
	V <sub>(BR)GSS</sub>	2.5	—	—	V	I <sub>G</sub> = 100 μA, V <sub>DS</sub> = 0
Gate to source leak current	I <sub>GSS1</sub>	—	—	-100	μA	V <sub>GS</sub> = -8 V, V <sub>DS</sub> = 0
	I <sub>GSS2</sub>	—	—	-50	μA	V <sub>GS</sub> = -3.5 V, V <sub>DS</sub> = 0
	I <sub>GSS3</sub>	—	—	-10	μA	V <sub>GS</sub> = -1.2 V, V <sub>DS</sub> = 0
	I <sub>GSS4</sub>	—	—	100	μA	V <sub>GS</sub> = 2.4 V, V <sub>DS</sub> = 0
Input current (shut down)	I <sub>GS(OP)1</sub>	—	-0.8	—	mA	V <sub>GS</sub> = -8 V, V <sub>DS</sub> = 0
	I <sub>GS(OP)2</sub>	—	-0.35	—	mA	V <sub>GS</sub> = -3.5 V, V <sub>DS</sub> = 0
Zero gate voltage drain current	I <sub>DSS1</sub>	—	—	-10	μA	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0
Zero gate voltage drain current	I <sub>DSS2</sub>	—	—	-10	μA	V <sub>DS</sub> = -48 V, V <sub>GS</sub> = 0, Ta = 125°C
Gate to source cutoff voltage	V <sub>GS(off)</sub>	-2.2	—	-3.4	V	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA
Static drain to source on state resistance	R <sub>DS(on)</sub>	—	70	95	mΩ	I <sub>D</sub> = -5 A, V <sub>GS</sub> = -6 V <sup>Note 5</sup>
	R <sub>DS(on)</sub>	—	53	65	mΩ	I <sub>D</sub> = -5 A, V <sub>GS</sub> = -10 V <sup>Note 5</sup>
Output capacitance	C <sub>oss</sub>	—	356	—	pF	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0, f = 1MHz
Turn-on delay time	t <sub>d(on)</sub>	—	4.4	—	μs	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -5 A, R <sub>L</sub> = 6 Ω
Rise time	t <sub>r</sub>	—	4.5	—	μs	
Turn-off delay time	t <sub>d(off)</sub>	—	2.0	—	μs	
Fall time	t <sub>f</sub>	—	1.6	—	μs	
Body-drain diode forward voltage	V <sub>DF</sub>	—	-0.87	—	V	I <sub>F</sub> = -10 A, V <sub>GS</sub> = 0
Body-drain diode reverse recovery time	t <sub>rr</sub>	—	90	—	ns	I <sub>F</sub> = -10 A, V <sub>GS</sub> = 0 di/dt = 50 A/μs
Over load shut down operation time <sup>Note 6</sup>	t <sub>os1</sub>	—	2.6	—	ms	V <sub>GS</sub> = -6 V, V <sub>DD</sub> = -16 V

Notes: 5. Pulse test

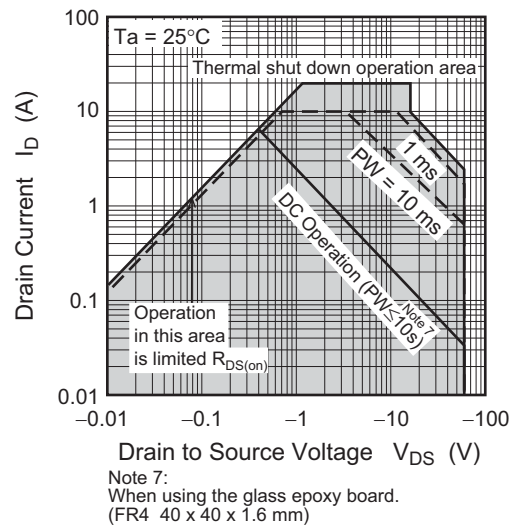
6. Including the junction temperature rise of the over loaded condition.

## Main Characteristics

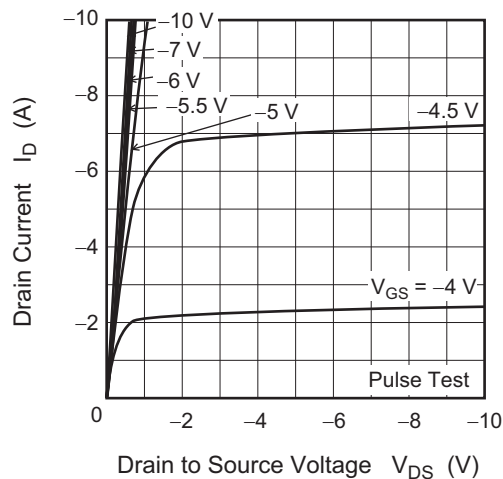
Power vs. Temperature Derating



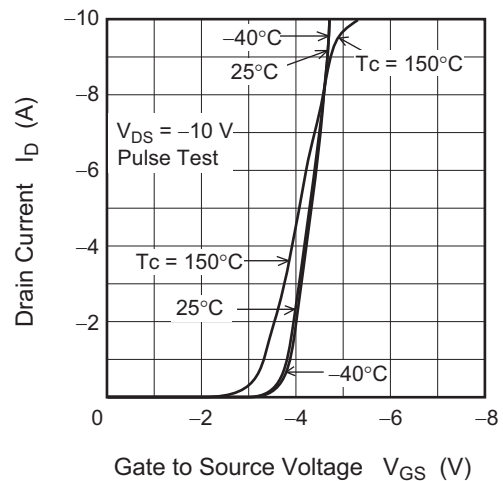
Maximum Safe Operation Area



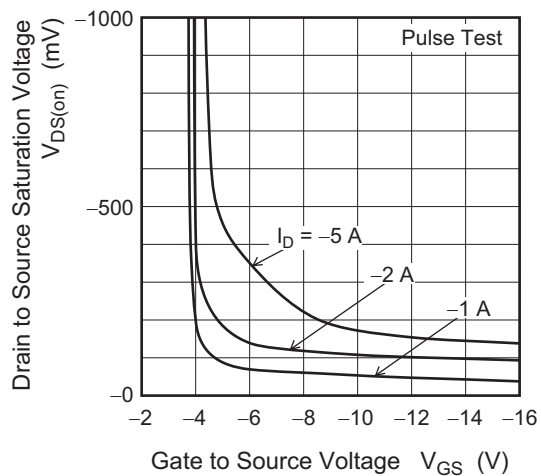
Typical Output Characteristics



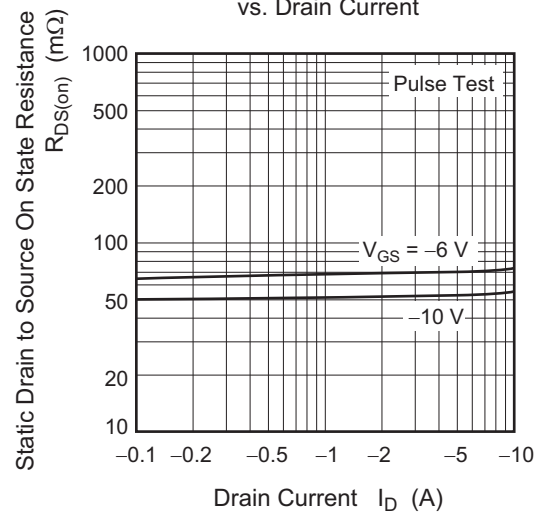
Typical Transfer Characteristics



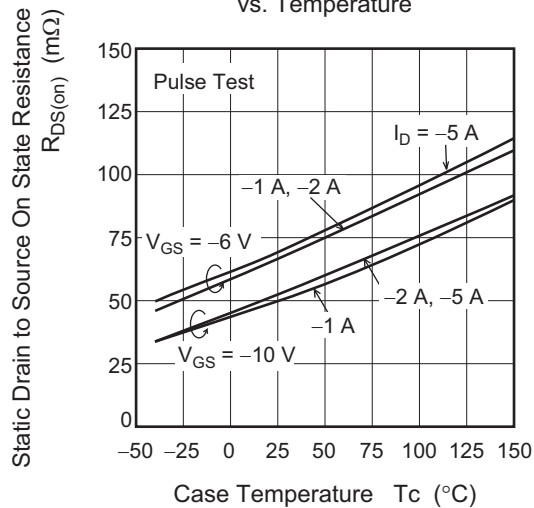
Drain Source Saturation Voltage vs. Gate to Source Voltage



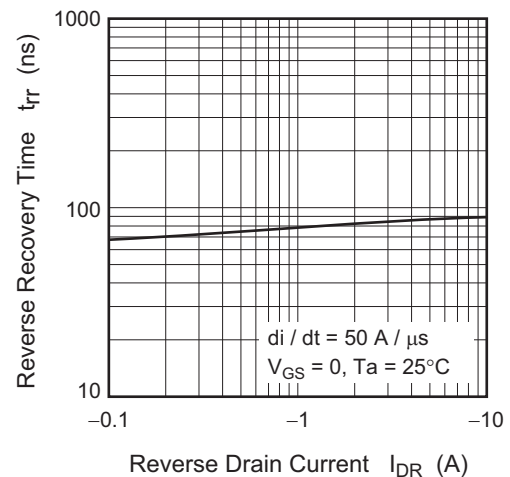
Static Drain to Source On State Resistance vs. Drain Current



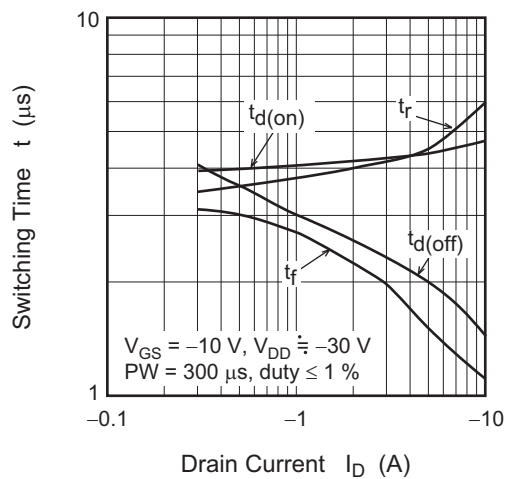
Static Drain to Source On State Resistance vs. Temperature



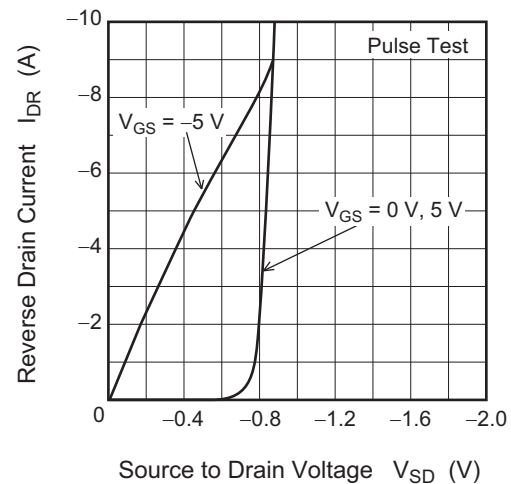
Body-Drain Diode Reverse Recovery Time



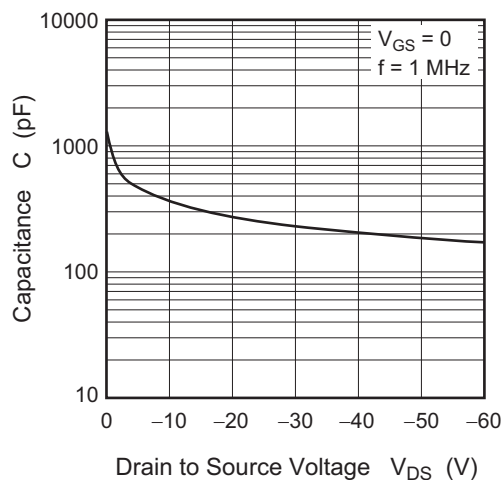
Switching Characteristics



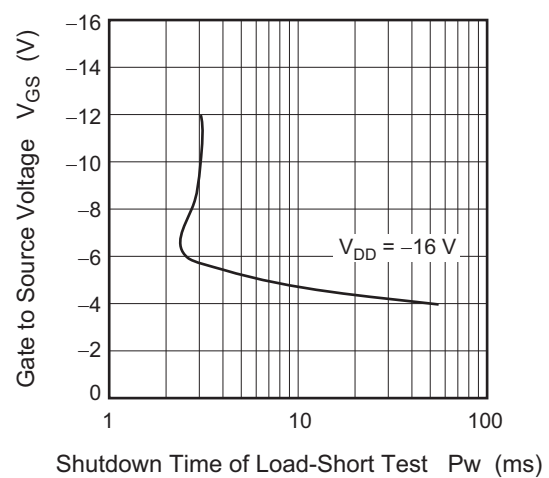
Reverse Drain Current vs. Source to Drain Voltage

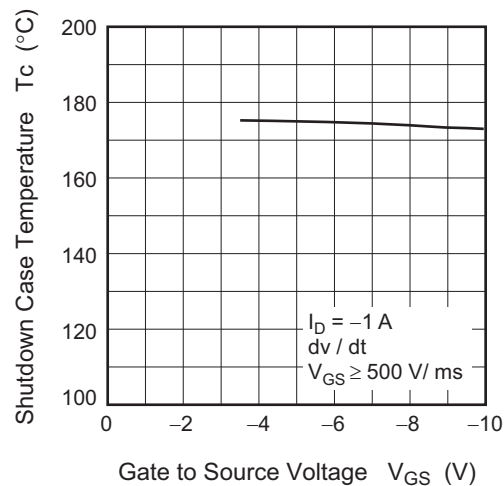


Typical Capacitance vs. Drain to Source Voltage

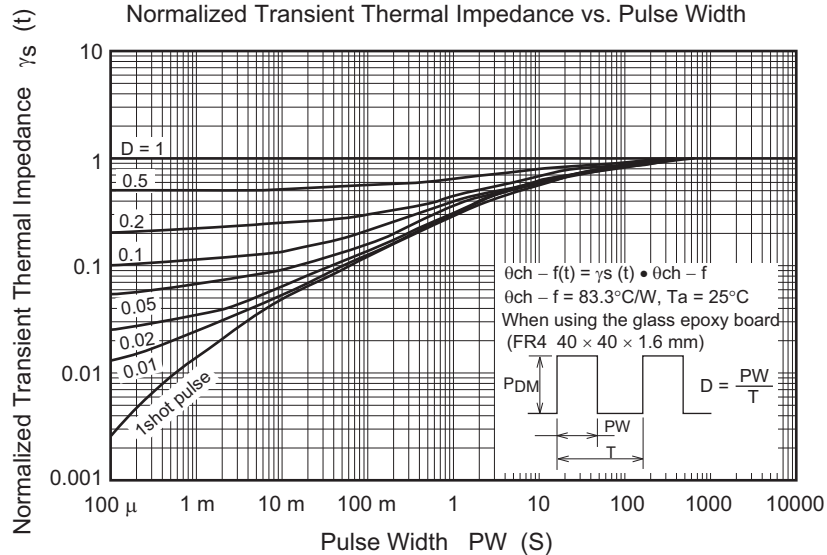


Gate to Source Voltage vs. Shutdown Time of Load-Short Test

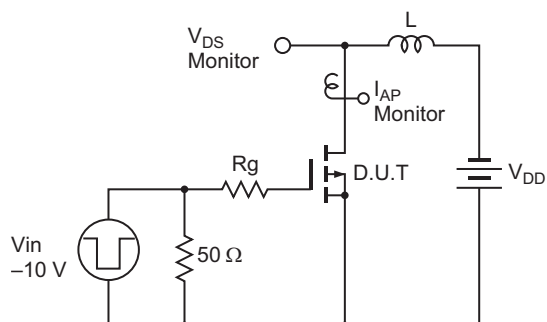


Shutdown Case Temperature vs.  
Gate to Source Voltage

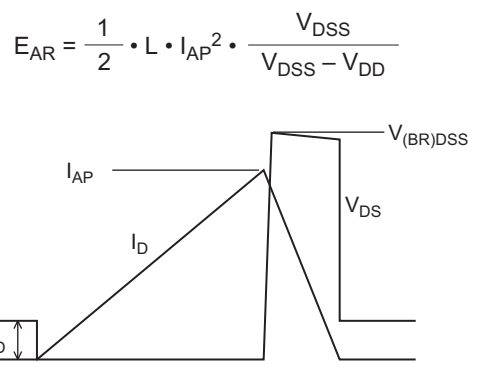
Normalized Transient Thermal Impedance vs. Pulse Width



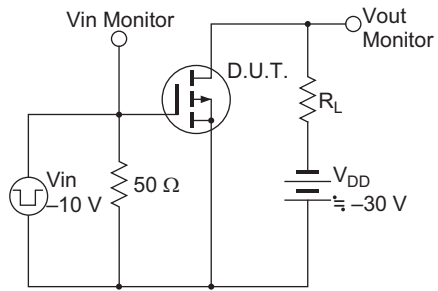
Avalanche Test Circuit



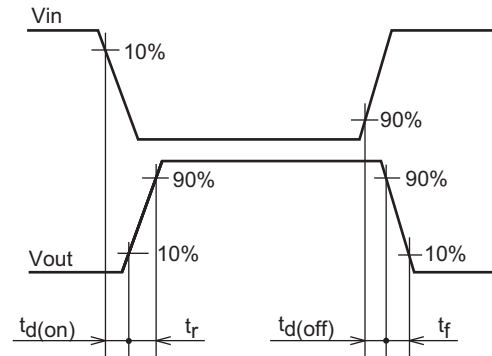
Avalanche Waveform



Switching Time Test Circuit

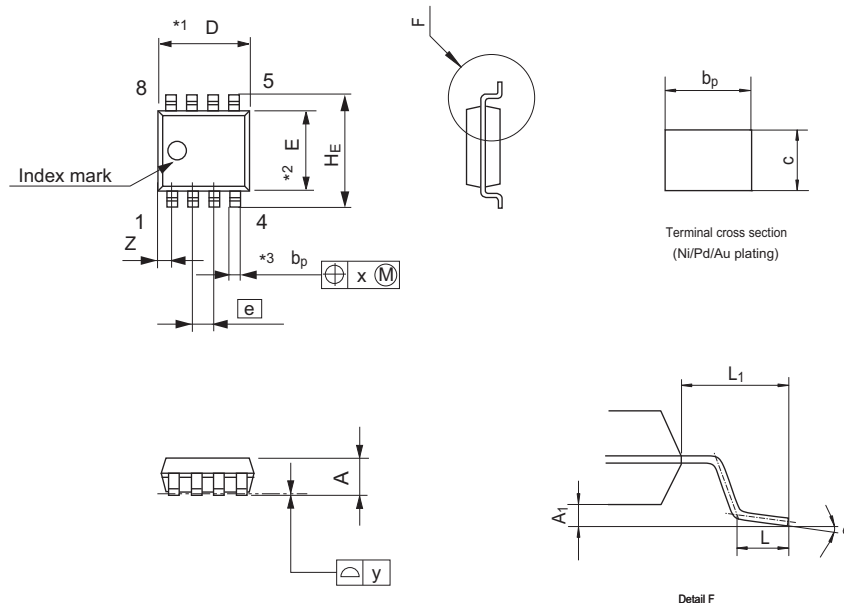


Switching Time Waveform



## Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SOP-8	P-SOP8-3.95 × 4.9-1.27	PRSP0008DD-D	FP-8DAV	0.085g



NOTE)  
 1. DIMENSIONS "\*"1(Nom)" AND "\*"2"  
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION "\*"3" DOES NOT  
 INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.90	5.3
E	—	3.95	—
A <sub>2</sub>	—	—	—
A <sub>1</sub>	0.10	0.14	0.25
A	—	—	1.75
b <sub>p</sub>	0.34	0.40	0.46
b <sub>1</sub>	—	—	—
c	0.15	0.20	0.25
c <sub>1</sub>	—	—	—
θ	0°	—	8°
H <sub>E</sub>	5.80	6.10	6.20
Ⓜ	—	1.27	—
x	—	—	0.25
y	—	—	0.1
Z	—	—	0.75
L	0.40	0.60	1.27
L <sub>1</sub>	—	1.08	—

## Ordering Information

Part No.	Quantity	Shipping Container
RJE0615JSP-00-J0	2500 pcs	Taping

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