

# μPC258, 4558

## Low Noise Dual Operational Amplifier

R03DS0145EJ0100

Rev.1.00

2019.06.13

### DESCRIPTION

The μPC258 and 4558 are dual operational amplifier with a built-in phase compensation circuit, feature high speed, wide band and low noise.

Therefore, applications such as active filters, audio amplifiers and VCOs can be realized with a simple circuit configuration.

Depending on the operating ambient temperature, μPC258 is suitable for communication application while μPC4558 is suitable for general-purpose usage.

In addition, special arrangement products with sorted DC items are available.

Along with this series of lineup, the quad type op-amp μPC458 and 4741 with same circuit configuration are also available.

### FEATURES

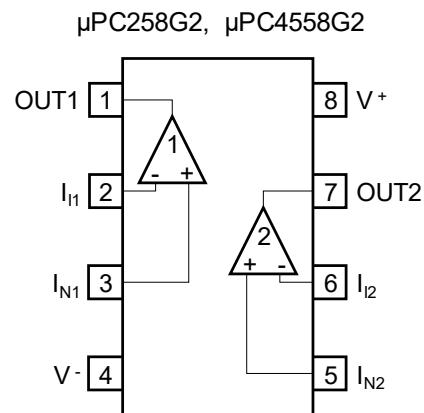
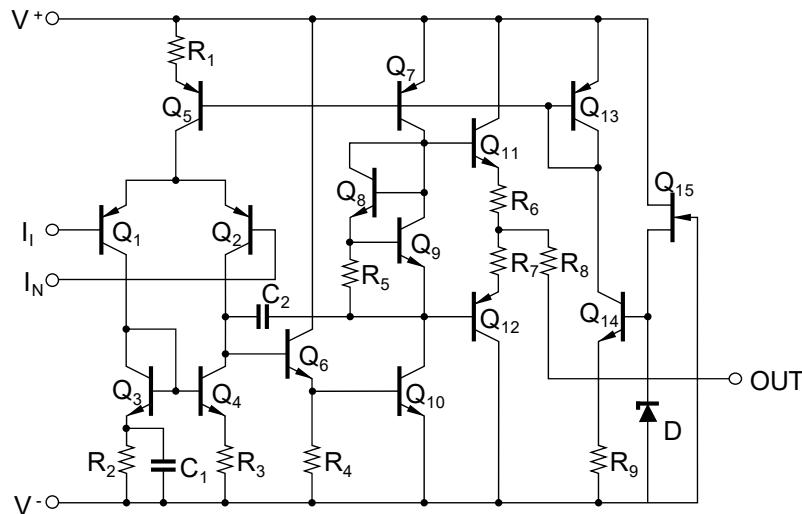
- Input Offset Voltage  $\pm 0.5 \text{ mV}$  (TYP.)
- Input Offset Current  $\pm 5 \text{ nA}$  (TYP.)
- Input Bias Current  $60 \text{ nA}$  (TYP.)
- Slew Rate  $1.0 \text{ V}/\mu\text{s}$  (TYP.)
- Input Equivalent Noise Voltage (RIAA)  $1.0 \mu\text{V}_{\text{r.m.s.}}$  (TYP.)
- Built-In Phase Compensation Circuit
- Built-In Output Short Circuit Protection
- Standard Dual Op-Amp terminal connection (pin compatible)

### ORDERING INFORMATION

Ordering Name	Sorting Content	Package
μPC258G2-A	General product	8-pin plastic SOP ( 5.72 mm ( 225 mil))
μPC258G2(5)-A	DC item sorted product	8-pin plastic SOP ( 5.72 mm ( 225 mil))
μPC4558G2-A	General product	8-pin plastic SOP ( 5.72 mm ( 225 mil))
μPC4558G2 (5)-A	DC item sorted product	8-pin plastic SOP ( 5.72 mm ( 225 mil))

## EQUIVALENT CIRCUIT (1/2 Circuit)

## PIN CONFIGURATION (Top View)



## ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

PARAMETER	SYMBOL	μPC258G2 μPC258G2(5)	μPC4558G2 μPC4558G2(5)	UNIT
Supply Voltage <sup>Note1</sup>	V+ - V-	-0.3 ~ +36		V
Differential Input Voltage	V <sub>ID</sub>	±30		V
Input Voltage <sup>Note2</sup>	V <sub>I</sub>	V- -0.3 ~ V+ +0.3		V
Output Applied Voltage <sup>Note3</sup>	V <sub>O</sub>	V- -0.3 ~ V+ +0.3		V
Total Power Dissipation <sup>Note4</sup>	P <sub>T</sub>	440		mW
Output Short Circuit Duration <sup>Note5</sup>		indefinite		s
Operating Ambient Temperature	T <sub>A</sub>	-40 ~ +85	-20 ~ +80	°C
Storage Temperature	T <sub>stg</sub>	-55 ~ +125		°C

[Note]

1. Note that reverse connections of the power supply may damage the ICs.
2. The input terminal must be apply within the input voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp input voltage must operates within the electrical characteristics range of input common-mode voltage.
3. The output terminal must be apply within the output voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp output voltage must operates within the electrical characteristics range of maximum output voltage.
4. This is the value at TA  $\leq$  +25 °C. De-rate value at -4.4 mW/°C when TA > 25 °C.
5. Please use the total loss and the de-rating value from Note 4.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage	V $\pm$	±4		±16	V

**ELECTRICAL CHARACTERISTICS****μPC258, μPC4558 (T<sub>A</sub> = 25 °C, V<sup>±</sup> = ±15 V)**

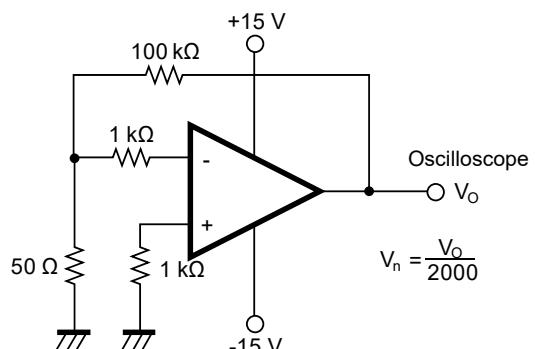
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Offset Voltage	V <sub>IO</sub>		±0.5	±6.0	mV	R <sub>S</sub> ≤ 10 kΩ
Input Offset Current	I <sub>IO</sub>		±5	±200	nA	
Input Bias Current <sup>Note6</sup>	I <sub>B</sub>		60	500	nA	
Large Signal Voltage Gain	A <sub>V</sub>	20000	100000			R <sub>L</sub> ≥ 2 kΩ, V <sub>O</sub> = ±10 V
Power Consumption	P <sub>d</sub>		90	170	mW	I <sub>O</sub> = 0 A
Common Mode Rejection Ratio	CMR	70	90		dB	R <sub>S</sub> ≤ 10 kΩ
Supply Voltage Rejection Ratio	SVR		30	150	μV/V	R <sub>S</sub> ≤ 10 kΩ
Output Voltage Swing	V <sub>OM</sub>	±12	±14		V	R <sub>L</sub> ≥ 10 kΩ
Output Voltage Swing	V <sub>OM</sub>	±10	±13		V	R <sub>L</sub> ≥ 2 kΩ
Common Mode Input Voltage Range	V <sub>ICM</sub>	±12	±14		V	
Slew Rate	SR		1.0		V/μs	A <sub>V</sub> = 1
Input Equivalent Noise Voltage	V <sub>n</sub>		6		μV <sub>p-p</sub>	R <sub>S</sub> = 1 kΩ, f = 1 Hz ~ 1 kHz (Fig 1)
Channel Separation			105		dB	f = 1 kHz (Fig 2)

**μPC258(5), μPC4558(5) (T<sub>A</sub> = 25 °C, V<sup>±</sup> = ±15 V)**

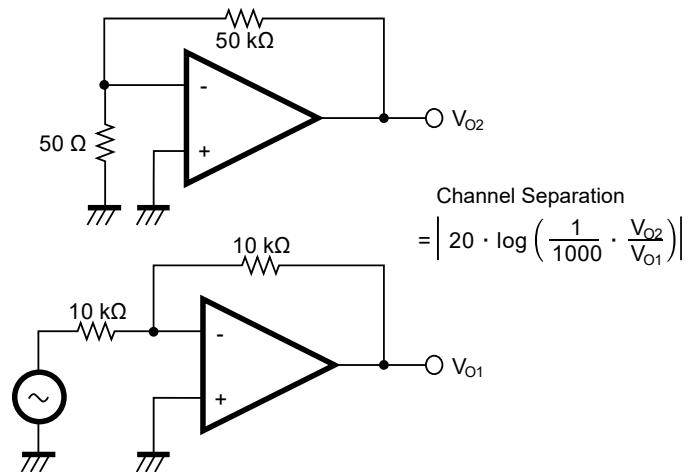
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Offset Voltage	V <sub>IO</sub>		±0.5	±2.0	mV	R <sub>S</sub> ≤ 10 kΩ
Input Offset Current	I <sub>IO</sub>		±5	±50	nA	
Input Bias Current <sup>Note6</sup>	I <sub>B</sub>		60	100	nA	
Large Signal Voltage Gain	A <sub>V</sub>	50000	100000			R <sub>L</sub> ≥ 2 kΩ, V <sub>O</sub> = ±10 V
Power Consumption	P <sub>d</sub>		90	135	mW	I <sub>O</sub> = 0 A
Common Mode Rejection Ratio	CMR	85	90		dB	R <sub>S</sub> ≤ 10 kΩ
Supply Voltage Rejection Ratio	SVR		30	75	μV/V	R <sub>S</sub> ≤ 10 kΩ
Output Voltage Swing	V <sub>OM</sub>	±12.5	±14		V	R <sub>L</sub> ≥ 10 kΩ
Output Voltage Swing	V <sub>OM</sub>	±11	±13		V	R <sub>L</sub> ≥ 2 kΩ
Common Mode Input Voltage Range	V <sub>ICM</sub>	±13	±14		V	
Slew Rate	SR		1.0		V/μs	A <sub>V</sub> = 1
Input Equivalent Noise Voltage	V <sub>n</sub>		6		μV <sub>p-p</sub>	R <sub>S</sub> = 1 kΩ, f = 1 Hz ~ 1 kHz (Fig 1)
Channel Separation			105		dB	f = 1 kHz (Fig 2)

[Note] 6. The direction of the input bias current is the same direction that flows out from the IC because the first stage is composed of PNP transistor.

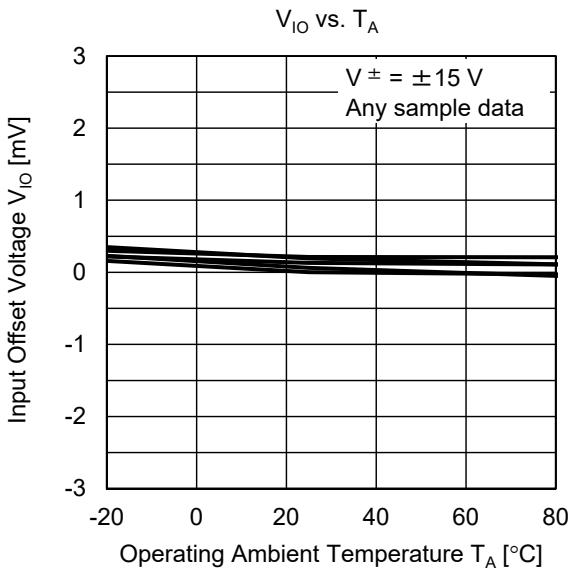
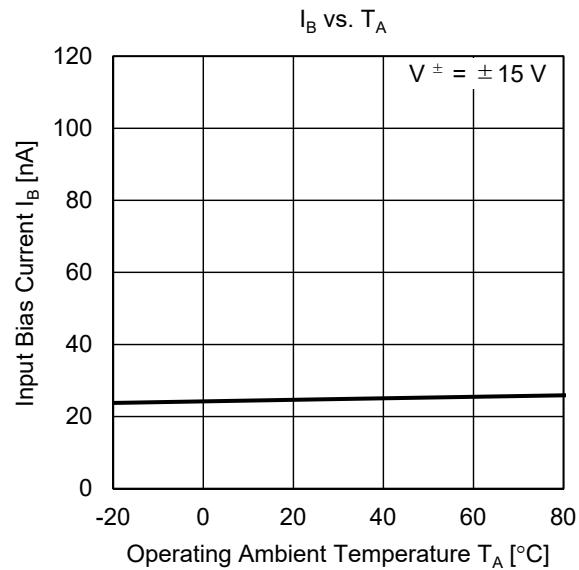
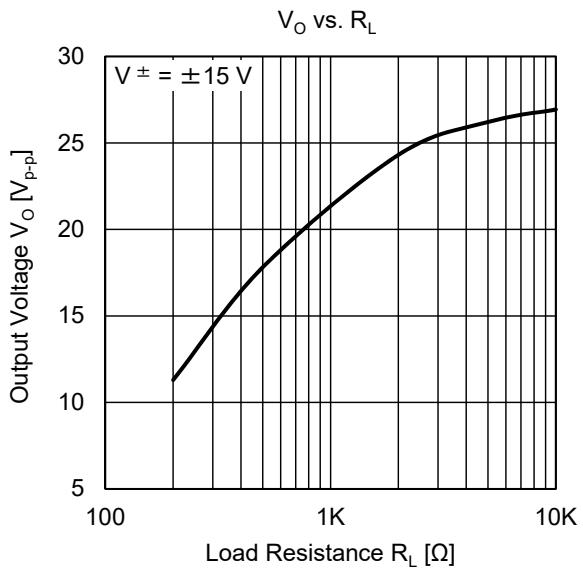
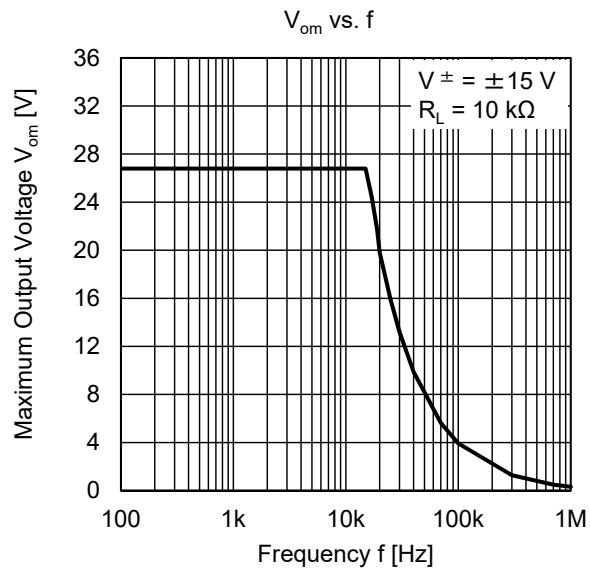
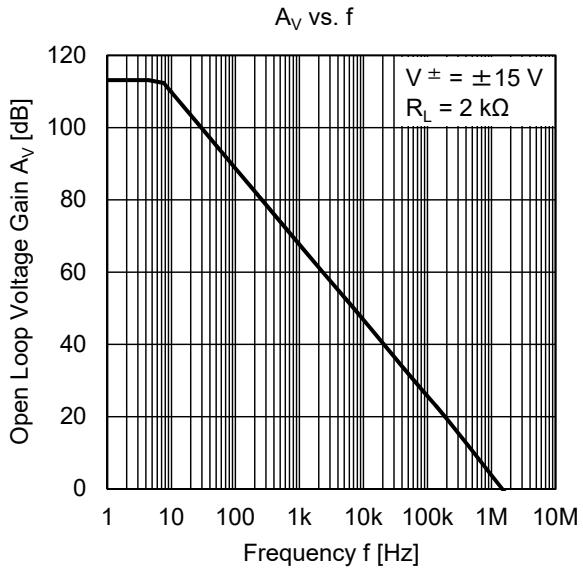
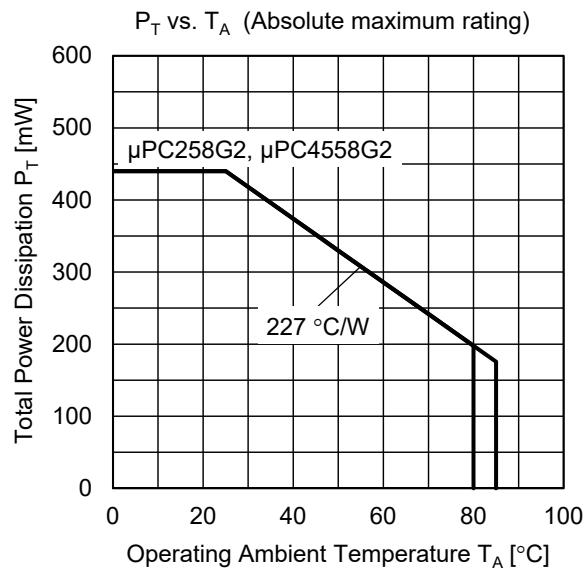
**Fig 1 Noise Test Circuit**

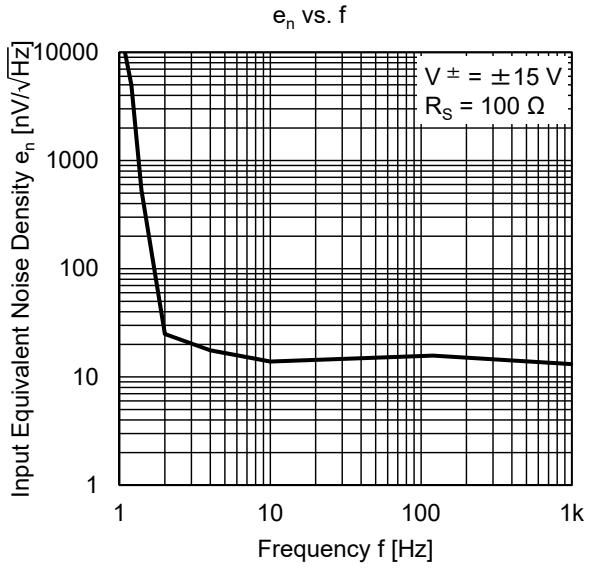
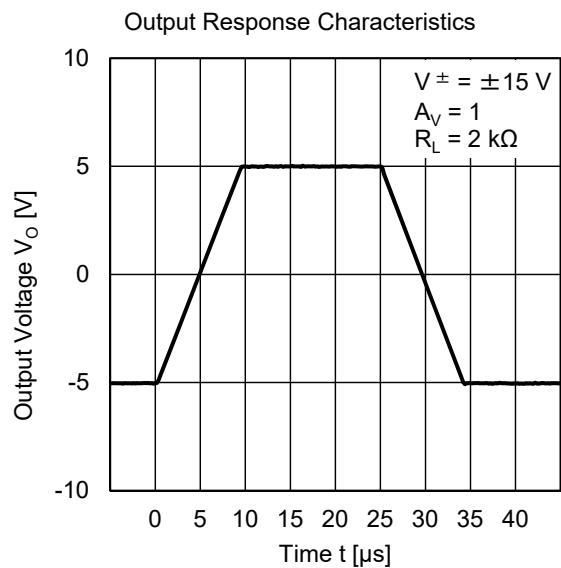
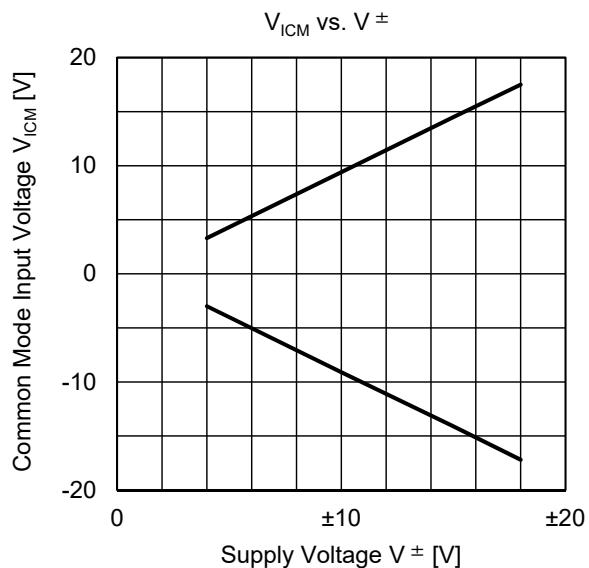
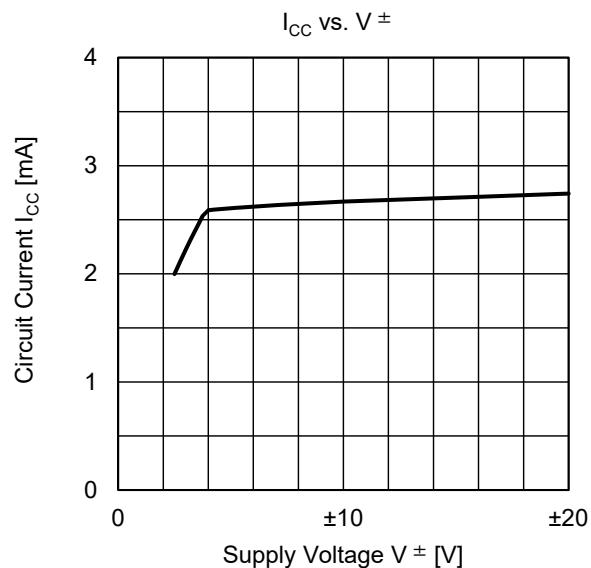


**Fig 2 Channel Separation Test Circuit**



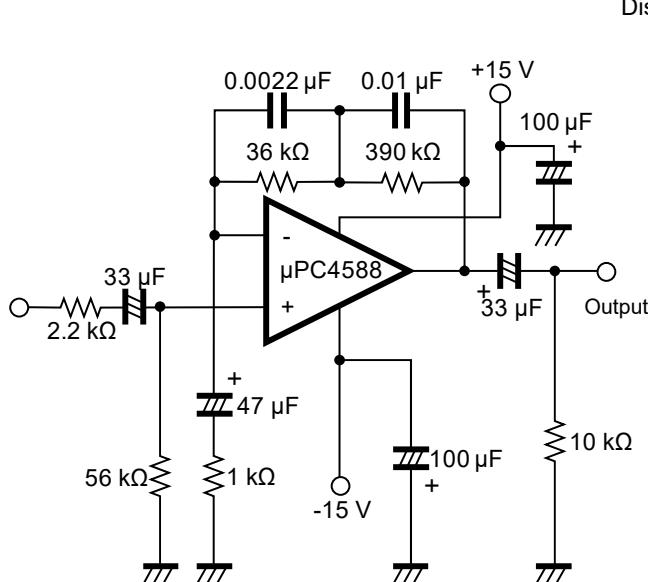
## ELECTRICAL CHARACTERISTICS CURVE ( $T_A = 25^\circ\text{C}$ , TYP.) (REFERENCE VALUE)



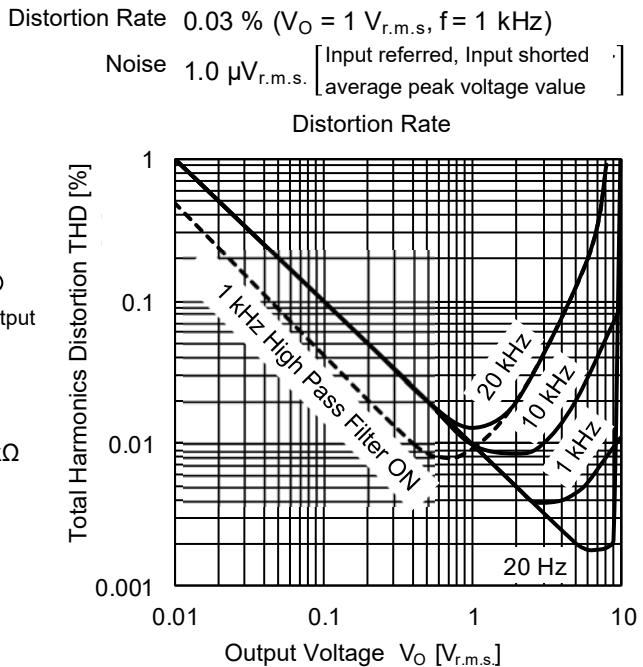


## APPLICATION CIRCUIT

### RIAA Pre-amplifier $A_v = 32.5$ dB



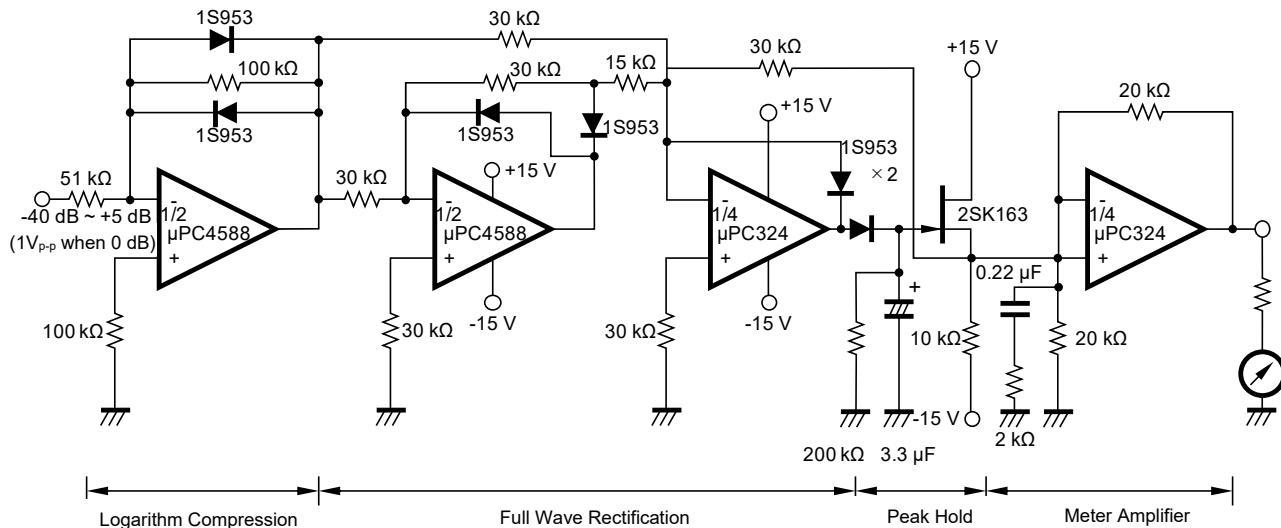
### Standard Characteristics (Reference Value)



### Peak Level Meter

This circuit converts the peak voltage (about  $\pm 10$  mV  $\sim \pm 10$  V) of the input signal to a DC voltage (about 0.2 V  $\sim$  1.3 V) and drives the meter.

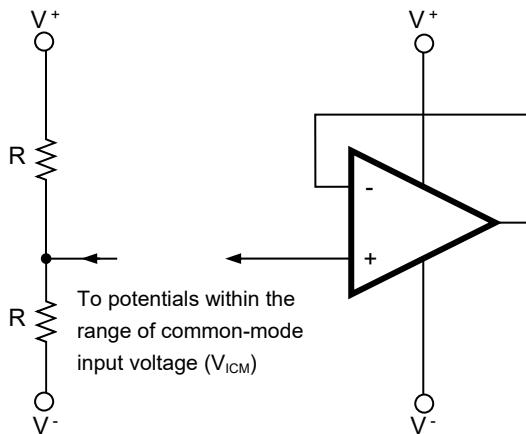
This output voltage is proportional to the logarithmic value of input peak voltage, thus providing a wider dynamic range indication compared to conventional linear indication methods.



## USE WITH PRECAUTIONS

- Managing unused circuits  
If there is an unused circuit, the following connection is recommended.

### Example of handling unused circuit



Note in this example, an intermediate voltage of  $V^+$  and  $V^-$  is applied.

#### • Power Supply (Dual Power Supply / Single Power Supply)

The op amp operates when a predetermined voltage is applied between  $V^+ - V^-$ . Therefore, while it operates from a single power supply ( $V^- = GND$ ), it is not possible to operate the input and output near GND. So please be careful of the common-mode input voltage range and maximum output voltage.

#### • Ratings of input/output pin voltage

When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than  $V^-$ , or the output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

#### • Range of common-mode input voltage

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

$$V_{ICM} (\text{TYP.}) : V^- + 1 \sim V^+ - 1 [\text{V}] (\text{T}_A = 25^\circ\text{C})$$

During designing, do include some margin by considering characteristics variation, temperature characteristics etc.

#### • Maximum Output Voltage

The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

$$V_{om^+} (\text{TYP.}) : V^+ - 1 [\text{V}] (\text{T}_A = 25^\circ\text{C}), V_{om^-} (\text{TYP.}) : V^- + 1 [\text{V}] (\text{T}_A = 25^\circ\text{C})$$

During designing, do include some margin by considering characteristics variation, temperature characteristics and so on. In addition, also note that the output voltage range ( $V_{om^+} - V_{om^-}$ ) will become narrow when the output current increases.

#### • Handling of ICs

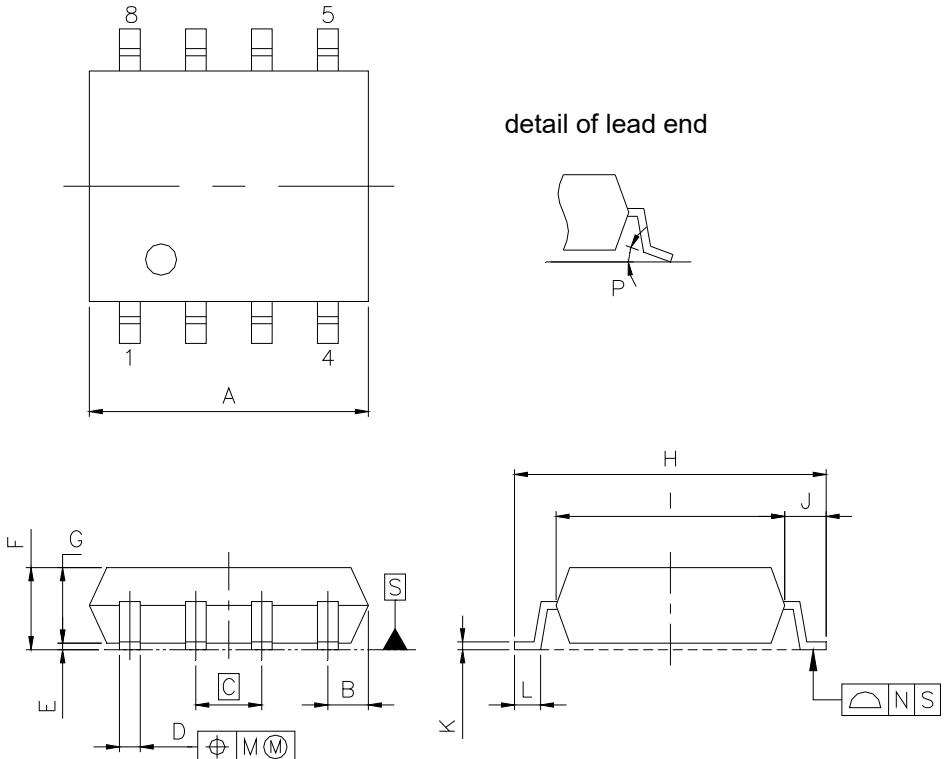
When stress is added to the ICs due to warpage or bending of a board, the characteristic may fluctuate due to piezoelectric (piezo) effect. Therefore, pay attention to warpage or bending of a board.

## PACKAGE DRAWINGS

### 8-PIN PLASTIC SOP

JEITA Package code	RENESAS code	Previous code	MASS (TYP.) [g]
P-SOP8-0225-1.27	PRSP0008DL-A	S8GM-50-225B	0.08

Unit: mm



#### NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.2 <sup>+0.17</sup> <sub>-0.20</sub>
B	0.78 MAX
C	1.27 (T.P.)
D	0.42 <sup>+0.08</sup> <sub>-0.07</sub>
E	0.1 $\pm 0.1$
F	1.59 $\pm 0.21$
G	1.49
H	6.5 $\pm 0.3$
I	4.4 $\pm 0.15$
J	1.1 $\pm 0.2$
K	0.17 <sup>+0.08</sup> <sub>-0.07</sub>
L	0.6 $\pm 0.2$
M	0.12
N	0.10
P	3° <sup>+7°</sup> <sub>-3°</sub>

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8. 关于环境保护方面的详细内容，例如每种瑞萨电子产品的环境兼容性等，请与瑞萨电子的营业部门联系。用户负责仔细并充分查阅对管制物质的使用或含量进行管理的所有适用法律法规（包括但不限于《欧盟RoHS指令》），并在使用瑞萨电子产品时遵守所有适用法律法规。对于因用户未遵守相应法律法规而导致的损害或损失，瑞萨电子概不承担任何责任。
9. 不可将瑞萨电子产品和技术用于或者嵌入日本国内或海外相应的法律法规所禁止生产、使用及销售的任何产品或系统中。也不可将瑞萨电子产品或技术用于(1)与大规模杀伤性武器（例如核武器、化学武器、生化武器或运送此类武器的导弹，包括无人机(UAV)）的开发、设计、制造、使用、存储等相关的任何目的；(2)与常规武器的开发、设计、制造或使用相关的任何目的；(3)扰乱国际和平与安全的任何其他目的，并且不可向任何第三方销售、出口、租赁、转让、或让与瑞萨电子产品或技术。无论直接或间接知悉或者有理由知悉该第三方或任何其他方将从事上述活动。用户必须遵守对各方或交易行使司法管辖权的任意国家/地区政府所公布和管理的任何适用出口管制法律法规。
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12. 如果对本文档所记载的信息或瑞萨电子产品有任何疑问，请向瑞萨电子的营业部门咨询。

(注1) 瑞萨电子：在本文档中指瑞萨电子株式会社及其控股子公司。

(注2) 瑞萨电子产品：指瑞萨电子开发或生产的任何产品。

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