

μPC842A

Single Power Supply, High Speed, Wide Band,
Dual Bipolar Operational Amplifier

R03DS0133EJ0100
Rev.1.00
2018.12.19

DESCRIPTION

The μPC842A is a high-speed version of the single-power general-purpose operational amplifier μPC1251, realizing high-speed response and high stability. A high speed PNP transistor is used in the circuit which improves the characteristics such as slew rate, gain-bandwidth product, stabilization of the withstand load capacitance, with no crossover distortion compared to μPC1251.

As this is a high slew rate product, it is able to provide high-speed signal amplification and can be applied to a wide range of sensor applications such as motors. Moreover, due to its small package (MSOP), mounting on the vicinity of the sensor becomes possible, which makes the board smaller and increases design freedom.

FEATURES

AEC-Q100 Compliant

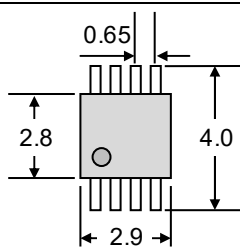
Absolute Maximum Ratings

- Power Supply Voltage -0.3 ~ +36 V
- Operating Ambient Temperature Range -40 °C ~ +125 °C

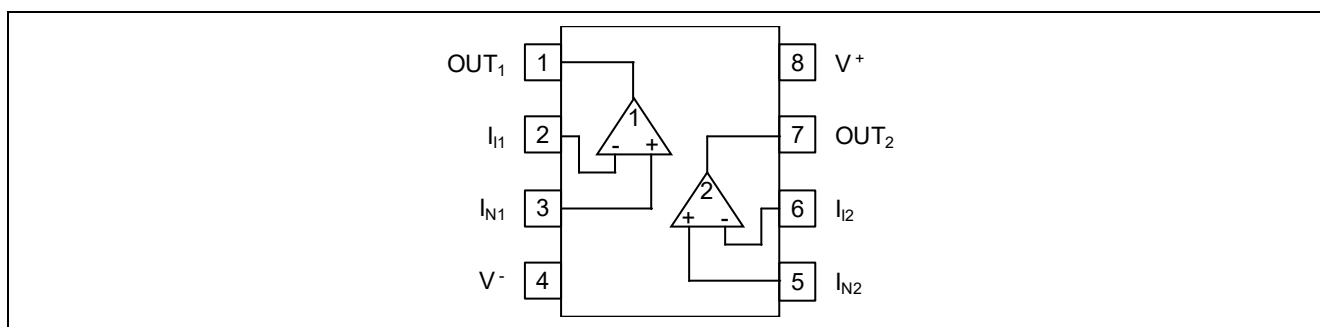
Electrical Characteristics

- Power Supply Voltage (MIN. MAX.) +3 V to 32 V
- Input Offset Voltage (TYP.) ± 2.0 mV ($V^+ = \pm 15$ V)
- Gain Bandwidth Product (TYP.) 3.5 MHz
- Slew Rate (TYP.) 7 V/μs ($V^+ = 5$ V, $V^- = \text{GND}$)

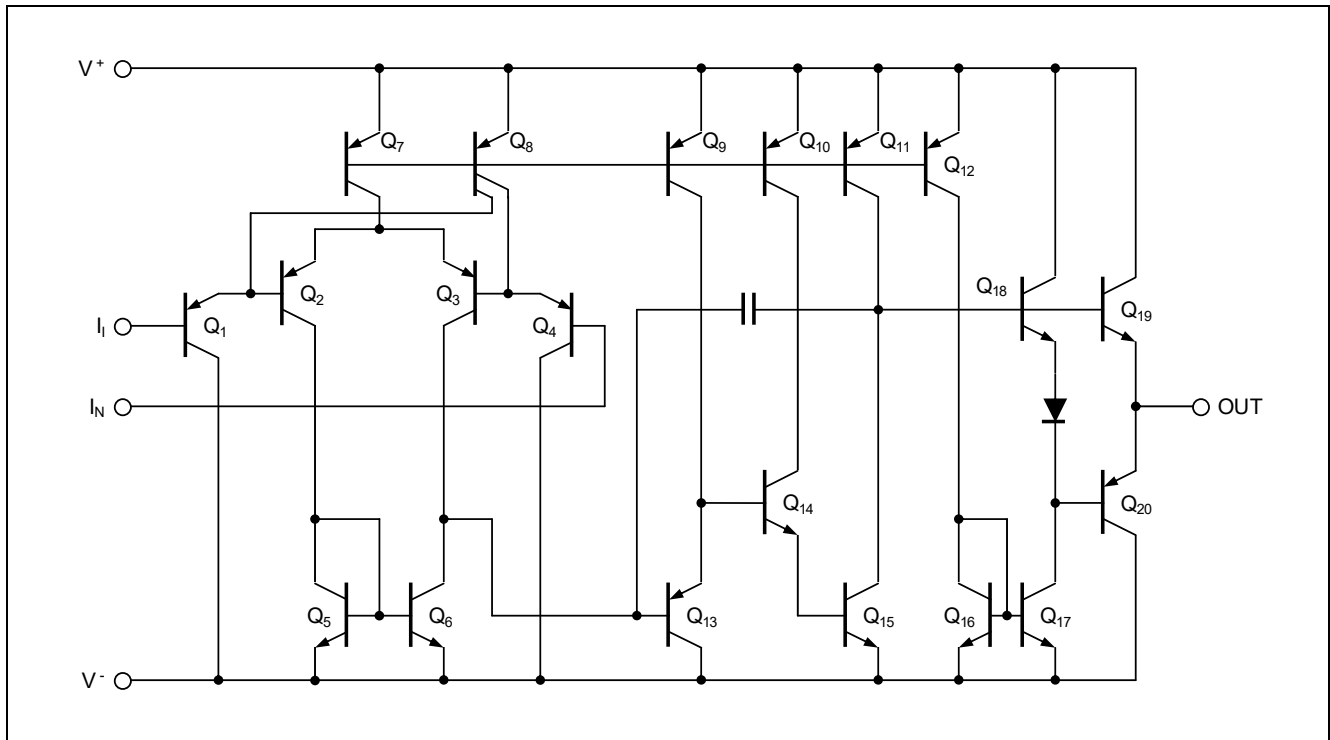
PRODUCT LINEUP

Package	MSOP (2.8 × 2.9)
Product Name	μPC842AMP
Outline	

PIN CONFIGURATION (Marking Side)



EQUIVALENT CIRCUIT (1/2 CIRCUIT)



ABSOLUTE MAXIMUM RATINGS

(T_A = 25 °C)

Parameter	Symbol	Rated Value	Unit
Power Supply Voltage ^{Note 1}	V ⁺ - V ⁻	-0.3 ~ +36	V
Differential Input Voltage	V _{ID}	±36	V
Input Voltage ^{Note 2}	V _I	V ⁻ -0.3 ~ V ⁻ +36	V
Output Applied Voltage ^{Note 3}	V _O	V ⁻ -0.3 ~ V ⁺ +0.3	V
Total Power Dissipation ^{Note 4}	P _T	440	mW
Output Short Circuit Duration ^{Note 5}	t _s	Infinity	s
Operating Ambient Temperature	T _A	-40 ~ +125	°C
Storage Temperature	T _{stg}	-55 ~ +150	°C

- 【Note】
- Note that reverse connections of the power supply may damage the ICs.
 - The allowable input voltage range without damaging or destructing the device. Independent to power supply voltage range.
Do not apply voltage equivalent to V⁻ (GND) - 0.3 V or less.
 - The input voltage range that can be applied to the output pin externally without deteriorating or damaging the device characteristic. The permitted input voltage that can be applied regardless of the power supply voltage. This specification also includes precaution during transition state such as ON/OFF, etc.
 - This is the value when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted.
Note that restrictions will be made to the following conditions for each product, and the de-rating ratio depending on the operating ambient temperature.
μPC842AMP : De-rate 4.8 mW/°C when T_A > 58 °C.
 - A short circuit at the V⁺ side may destroy the IC. Please use below the total loss and the de-rating of Note 4.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage ($V^- = \text{GND}$)	V^+	+3	+5 ~ +30	+32	V
Power Supply Voltage (Dual Supply)	$V^\pm$	± 1.5		± 16	V
Output Current	I_O			± 10	mA
Capacitive Load ($A_V = +1$)	C_L			1000 ^{Note 6}	pF

【Note】 6. This is the value when feedback resistor (R_f) = 0.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $V^\pm = \pm 15\text{ V}$)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V_{IO}		± 2	± 4.5	mV	
Input Offset Current	I_{IO}		± 6	± 75	nA	
Input Bias Current ^{Note 7}	I_B		120	500	nA	
Large Signal Voltage Gain	A_V	25000	300000			$R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$
Circuit Current ^{Note 8}	I_{CC}		4.3	5.5	mA	$I_O = 0\text{ A}$
Common Mode Rejection Ratio	CMR	70	86		dB	
Supply Voltage Rejection Ratio	SVR	70	93		dB	
Output Voltage Swing	V_{om1}	± 13.7	+14 -14.3		V	$R_L \geq 10\text{ k}\Omega$
	V_{om2}	± 13.5			V	$R_L \geq 2\text{ k}\Omega$
Common Mode Input Voltage Range	V_{ICM}	V^-		$V^+ - 1.8$	V	
Slew Rate	SR		8.5		V/ μs	$A_V = +1$ (Rise Edge)
Gain Bandwidth Product	GBW		3.5		MHz	$f = 100\text{ kHz}$
Channel Separation			120		dB	$f = 20\text{ Hz} \sim 20\text{ kHz}$

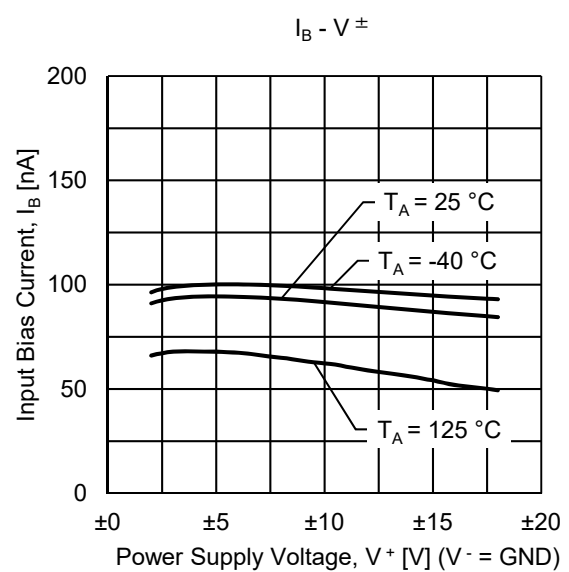
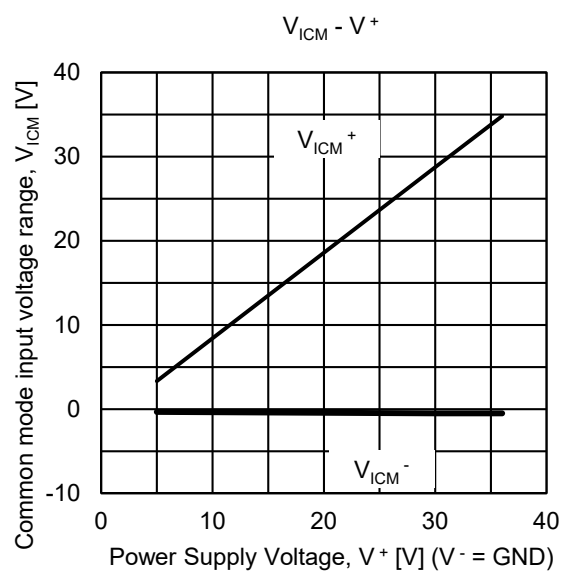
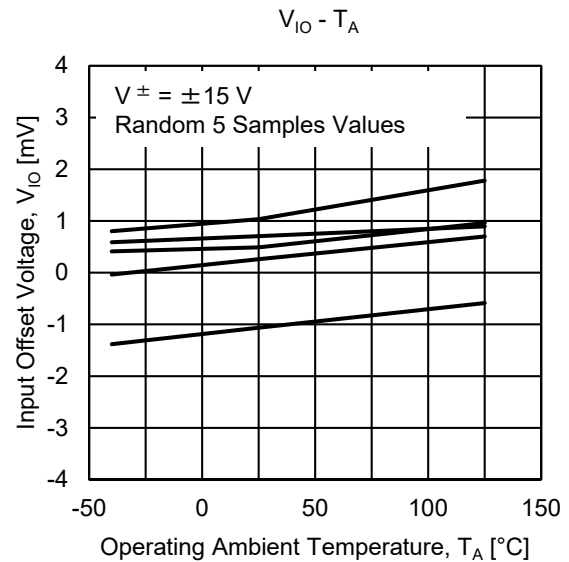
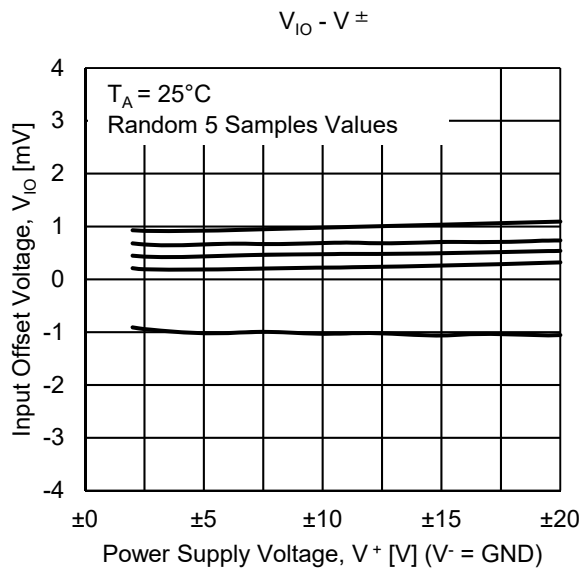
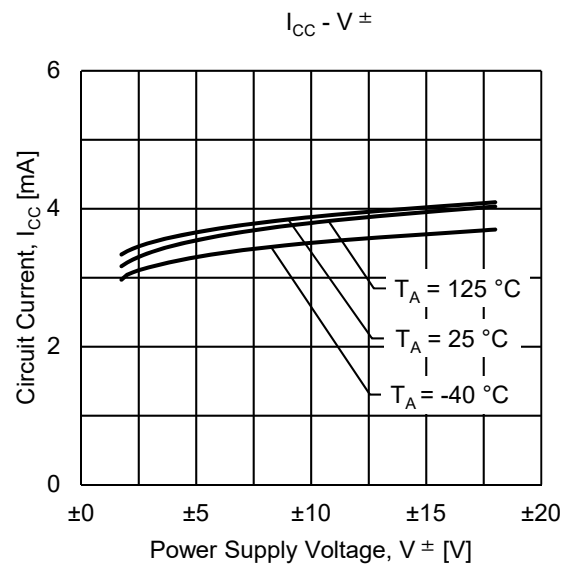
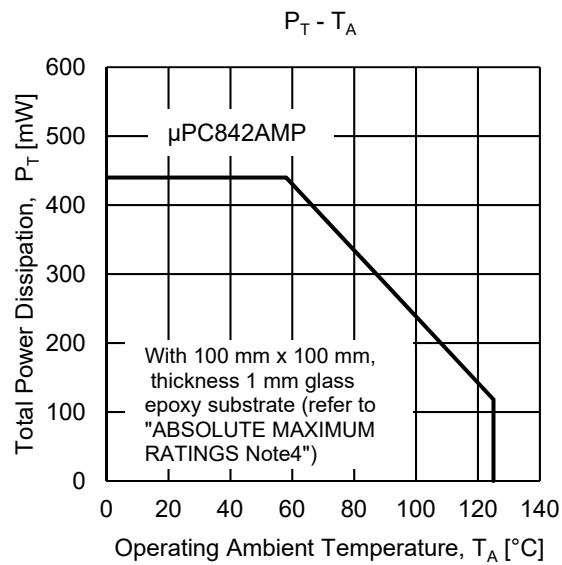
($T_A = 25^\circ\text{C}$, $V^+ = +5\text{ V}$, $V^- = \text{GND}$)

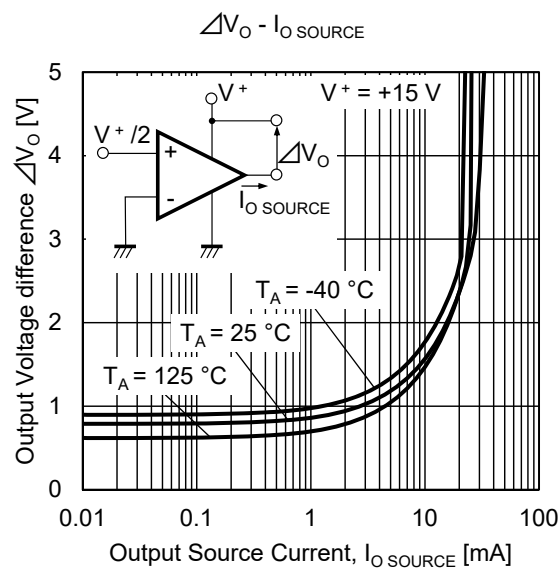
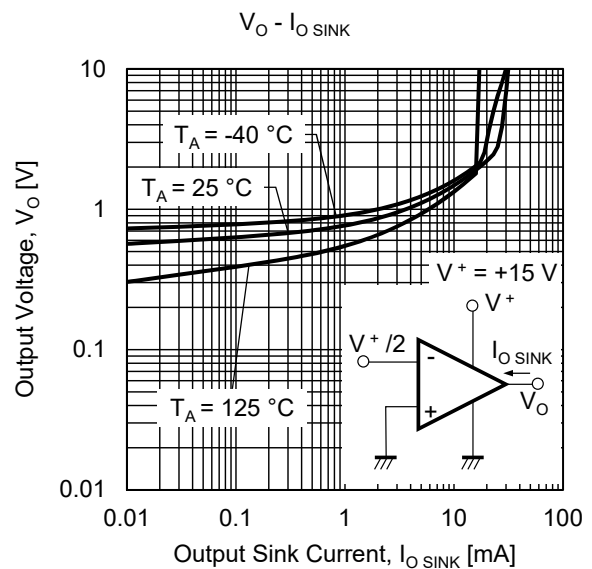
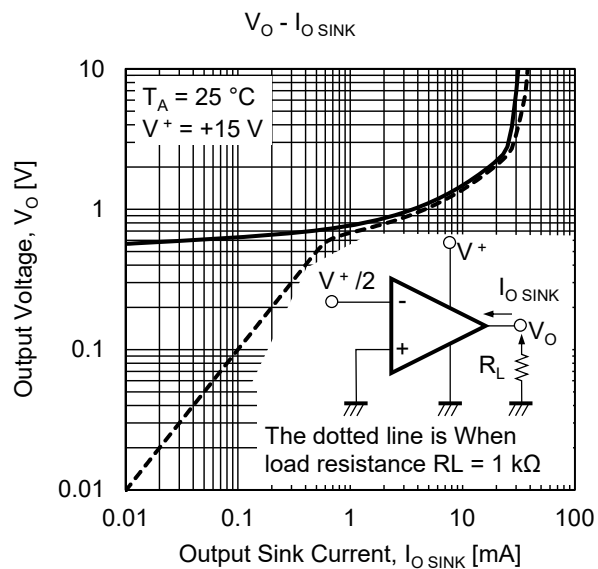
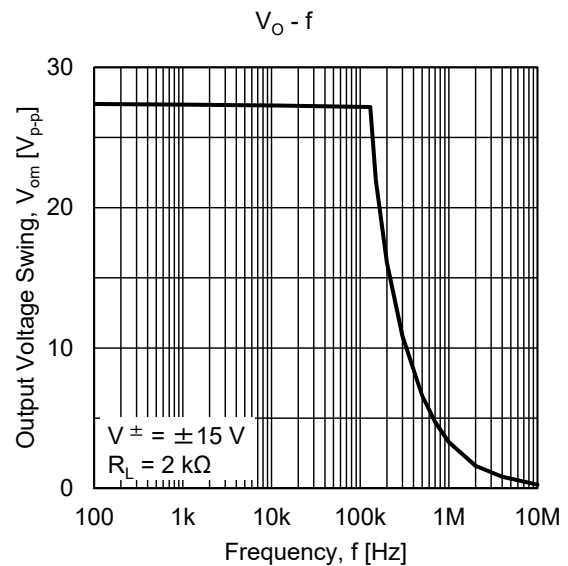
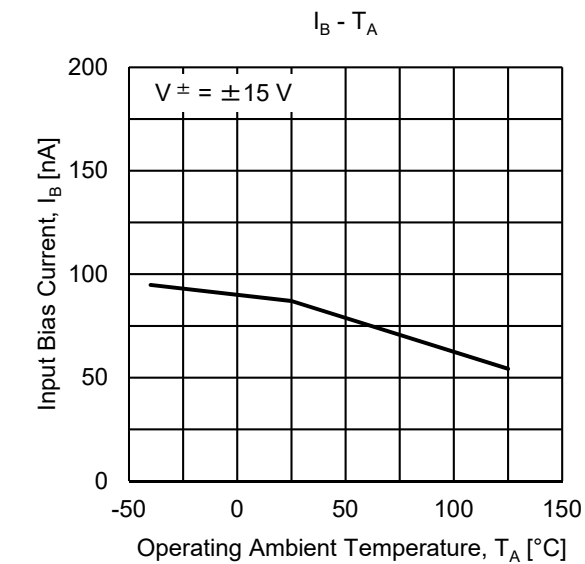
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V_{IO}		± 2	± 5.0	mV	
Input Offset Current	I_{IO}		± 6	± 75	nA	
Input Bias Current ^{Note 7}	I_B		140	500	nA	
Large Signal Voltage Gain	A_V	25000	300000			$R_L \geq 2\text{ k}\Omega$
Circuit Current ^{Note 8}	I_{CC}		3.3	4.5	mA	$I_O = 0\text{ A}$
Common Mode Rejection Ratio	CMR	70	80		dB	
Supply Voltage Rejection Ratio	SVR	70	95		dB	
Output Voltage Swing	V_{om}	3.7	4.0		V	$R_L \geq 2\text{ k}\Omega$ (Connected to GND)
		0	0			
Common Mode Input Voltage Range	V_{ICM}	0		$V^+ - 1.8$	V	
Output Source Current	$I_{O\text{ SOURCE}}$	10	30		mA	$V_{IN(+)} = +1\text{ V}$, $V_{IN(-)} = 0\text{ V}$
Output Sink Current	$I_{O\text{ SINK}}$	10	30		mA	$V_{IN(+)} = 0\text{ V}$, $V_{IN(-)} = +1\text{ V}$
Slew Rate	SR		7		V/ μs	$A_V = +1$ (Rise Edge)

【Note】 7. The current flow direction of the input bias is out from the IC because the first stage of the IC composed of PNP transistor.

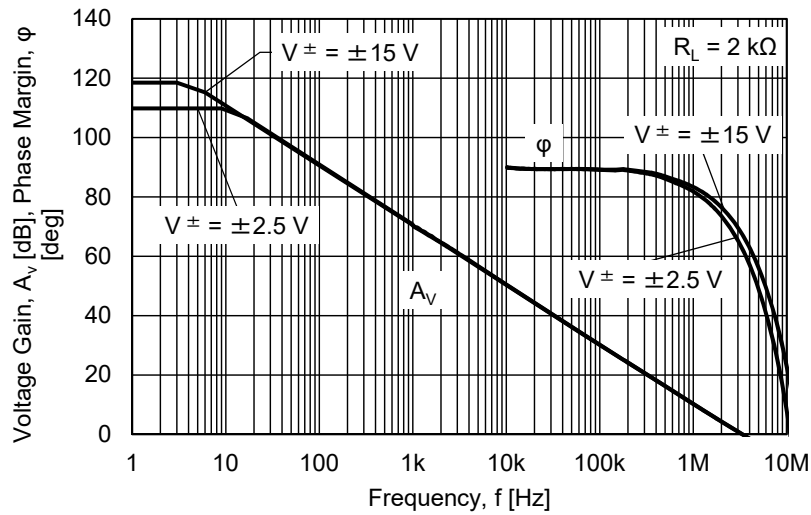
8. Current flowing through the internal circuit of this IC. This current flow regardless of the channel used.

CHARACTERISTICS CURVE ($T_A = 25\text{ }^{\circ}\text{C}$, TYP.) (REFERENCE VALUE)

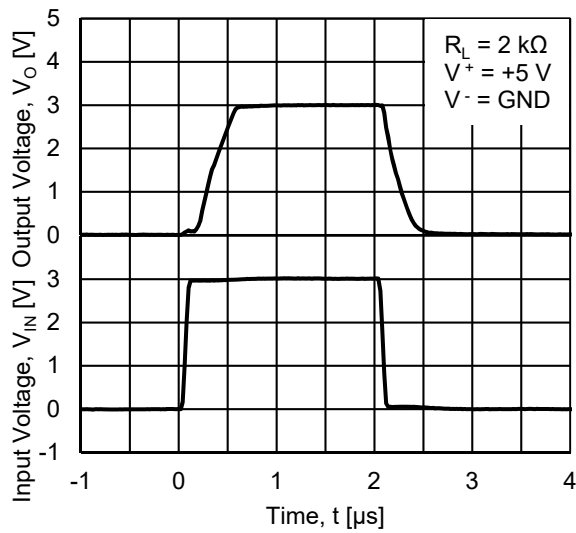




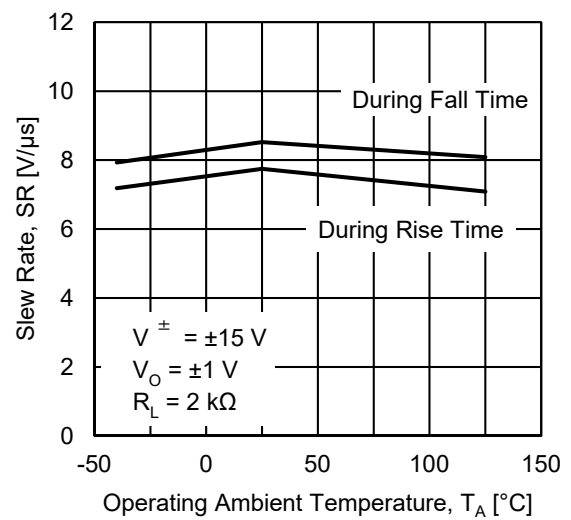
$A_V, \phi - f$



Pulse Response



SR - T_A

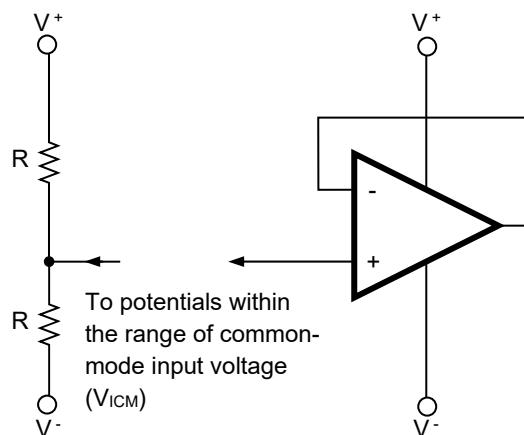


USE WITH PRECAUTIONS

- **Managing unused circuits**

If there is an unused circuit, the following connection is recommended.

Process example of unused circuits



Remark: In this example, an intermediate potential between V^+ and V^- is applied.

- **Ratings of input/output pin voltage**

When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than V^- , or the output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- **Range of common-mode input voltage**

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

$$V_{ICM} \text{ (TYP.)} : V^- \sim V^+ - 1.8 \text{ [V]} \text{ (} T_A = 25 \text{ } ^\circ\text{C)} \text{ }$$

During designing, do include some tolerance by considering temperature characteristics etc.

- **Maximum Output Voltage**

The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

$$V_{Om+} \text{ (TYP.)} : V^+ - 1 \text{ [V]} \text{ (} T_A = 25 \text{ } ^\circ\text{C)}, V_{Om-} \text{ (TYP.)} : V^- + 0.7 \text{ [V]} \text{ (} T_A = 25 \text{ } ^\circ\text{C)} \text{ }$$

During designing, do include some tolerance by considering characteristics variation, temperature characteristics and so on. In addition, also note that the output voltage range ($V_{Om+} - V_{Om-}$) will become narrow when the output current increases.

- **Output Operation**

This IC will not be able to sink output current when the output voltage is $V^- + 0.7 \text{ V}$ and below. In this case, the output voltage level can be improved to the V^- side by connecting the load resistor between the output terminal and V^- to sink the current at the load resistor. (The effect will differ depending on the flow of current in the load resistance.)

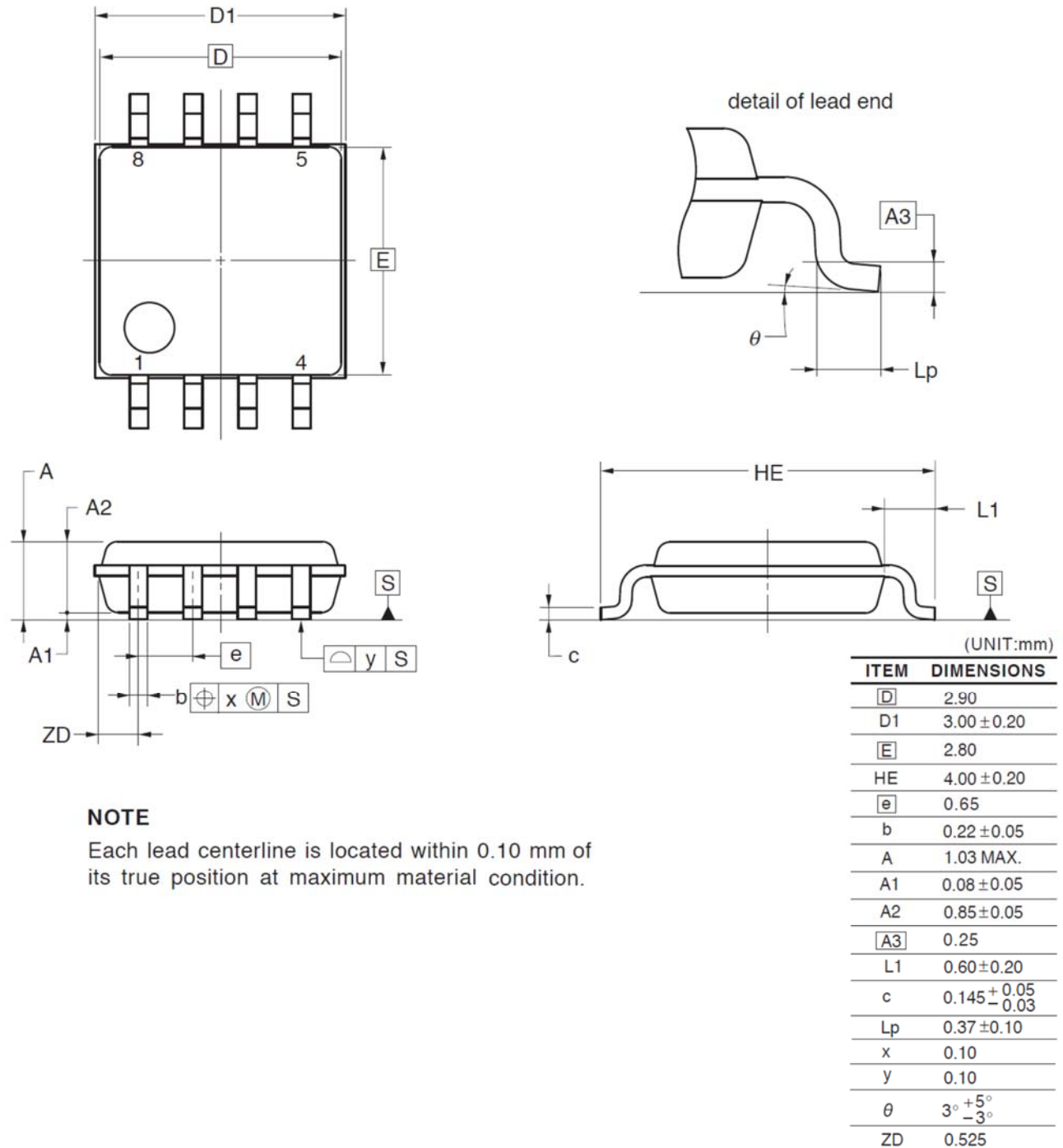
- **Handling of ICs**

When stress is added to the ICs due to warpage or bending of a board, the characteristic may fluctuates due to piezoelectric effect. Therefore, pay attention to warpage or bending of a board.

PACKAGE DRAWINGS

8-PIN PLASTIC MSOP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-TSSOP8-2.8x2.9-0.65	PTSP0008JF-A	P8MP-65-KAA-1	0.02



NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

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Renesas Electronics Corporation
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700

Renesas Electronics Europe GmbH
Arcadistrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6505-0, Fax: +49-211-6505-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langan Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0989

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.77C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

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