

R2A20113ASP

R03DS0026EJ0501

Rev.5.01

Jan 08, 2016

Critical Conduction Mode PFC Control IC

Description

The R2A20113A controls a boost converter to provide an active power factor correction.

The R2A20113A adopts critical conduction mode for power factor correction and realizes high efficiency and a low switching noise by zero current switching.

Because the zero current is detected by using the GND current, the ZCD Auxiliary winding is unnecessary.

The feedback loop open detection, two mode overvoltage protection, overcurrent protection are built in the R2A20113A, and can constitute a power supply system of high reliability with few external parts.

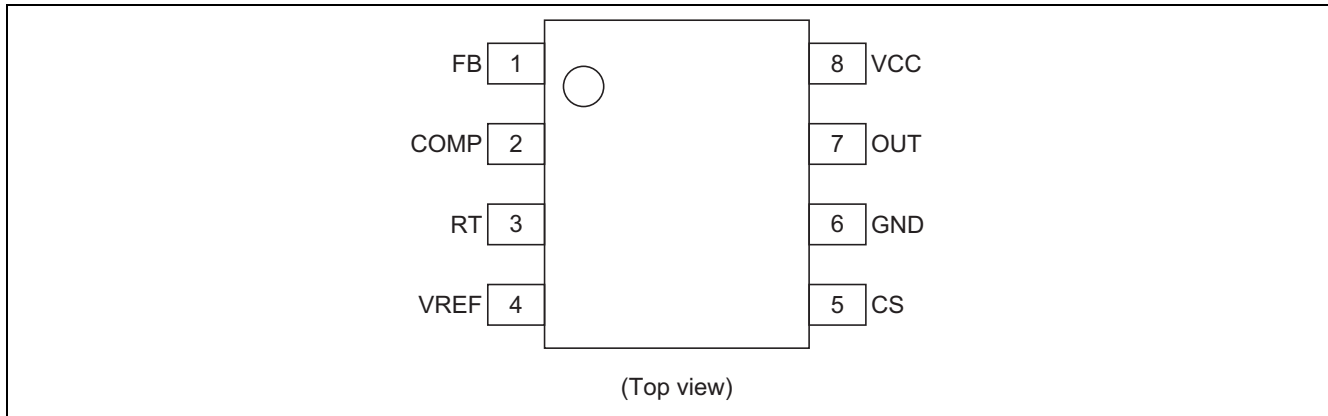
Features

- Absolute Maximum Ratings
 - Supply voltage V_{CC} : 24 V
 - Junction temperature T_j : -40 to $+150^{\circ}\text{C}$
- Electrical characteristics
 - UVLO operation start voltage V_H : $12\text{ V} \pm 0.8\text{ V}$
 - UVLO operation shutdown voltage V_L : $9.2\text{ V} \pm 0.7\text{ V}$
 - UVLO hysteresis voltage H_{ysv} : $2.8\text{ V} \pm 0.7\text{ V}$
- Functions
 - Boost converter control with critical conduction mode
 - Two mode overvoltage protection
 - Mode 1: Dynamic OVP corresponding to a voltage rise by load change
 - Mode 2: Static OVP corresponding to overvoltage in stable.
 - Feedback loop open detection
 - Overcurrent protection
 - Dynamic UVP corresponding to a voltage fall by load change
 - Off Time Control function (Frequency Limiter)
 - Package lineup: Pb-free SOP-8 (JEDEC)

Ordering Information

Part No.	Package Name	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
R2A20113ASP#W5	—	PRSP0008DJ-A	SP	W (2,500 pcs/reel)

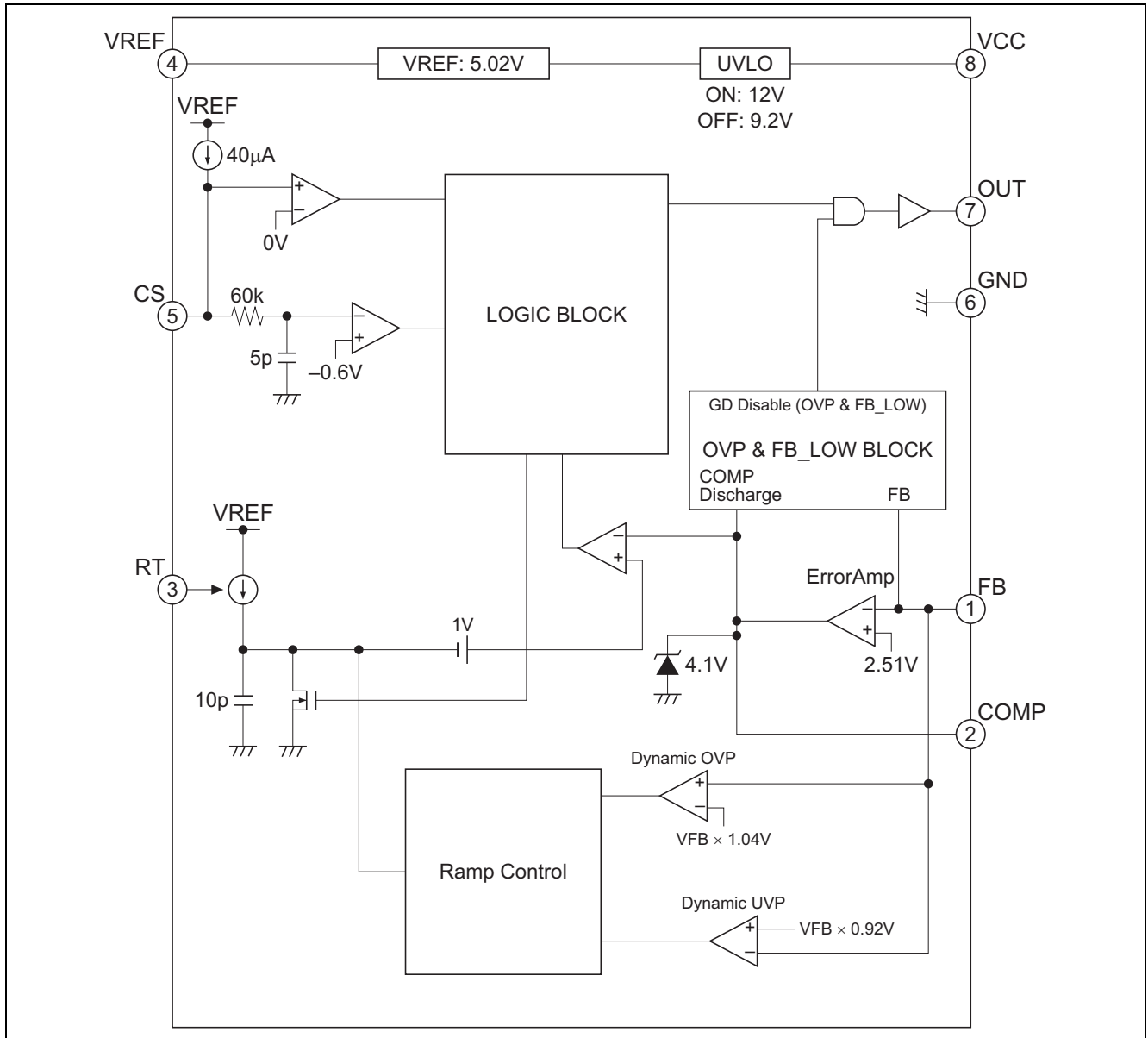
Pin Arrangement



Pin Function

Pin No.	Pin Name	Function
1	FB	Error amplifier input terminal
2	COMP	Error amplifier output terminal
3	RT	A resistor connection terminal for RAMP current setting
4	VREF	Reference voltage output terminal
5	CS	Zero current detection and overcurrent detection input terminal
6	GND	Ground
7	OUT	Power MOSFET drive terminal
8	VCC	Supply voltage terminal

Block Diagram



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Power Supply Voltage	VCC	−0.3 to +24	V	
OUT terminal peak current	Ip _k -snk-out	0.9	A	3
	Ip _k -src-out	−0.50		
OUT terminal DC current	Idc-snk-out	100	mA	
	Idc-src-out	−50		
COMP terminal current	I _{comp}	+1 −1	mA	
RT terminal current	I _{rt}	−60 to −2	μA	
Vref terminal current	I _{ref}	−5	mA	
Vref terminal voltage	V _{t-ref}	−0.3 to V _{ref} + 0.3	V	
Vref terminal load capacitor	C _{ref}	0.1 to 1	μF	
FB terminal voltage	V _{t-fb}	−0.3 to +5	V	
CS terminal voltage	V _{cs}	−5 to +0.3	V	
Power dissipation	P _t	0.68	W	4
Operating ambient temperature	T _{a-opr}	−40 to +125	°C	
Junction temperature	T _j	−40 to +150	°C	5
Storage temperature	T _{stg}	−55 to +150	°C	

- Notes:
1. Rated voltages are with reference to the GND terminal.
 2. For rated currents, inflow to the IC is indicated by (+), and outflow by (−).
 3. Shows the transient current when driving a capacitive load.
 4. In case of R2A20113ASP (SOP): $\theta_{ja} = 120^{\circ}\text{C/W}$
This value is a thing mounting on $40 \times 40 \times 1.6$ [mm], a glass epoxy board of wiring density 10%.
 5. Stresses exceeding the absolute maximum ratings may damage the device.
These are stress ratings only. Functional operation above the recommended operating ambient temperature range is not implied.
Extended exposure to stresses above the absolute maximum ratings may affect device reliability.

Electrical Characteristics

(Ta = 25°C, VCC = 12 V, CS = 0.1 V, FB = COMP, RRT = 200 kΩ)

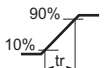
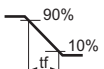
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	UVLO turn-on threshold	Vuvlh	11.2	12	12.8	V
	UVLO turn-off threshold	Vuvll	8.5	9.2	9.9	V
	UVLO hysteresis	Hysuvl	2.1	2.8	3.5	V
	Standby current	Istby	—	130	250	μA
	Operating current	Icc	—	1.8	2.6	mA
VREF	Reference voltage	Vref	4.945	5.020	5.095	V
	Line regulation	Vref-line	—	5	20	mV
	Load regulation	Vref-load	—	5	20	mV
	Temperature stability	dVref	—	±80	—	ppm/°C
	OVP-VREF threshold voltage	ovp-vref	Vref+ 0.2	Vref+ 0.4	Vref+ 0.6	V
Error amplifier	Feedback voltage	Vfb	2.472	2.510	2.548	V
	Input bias current	Ifb	−0.40	−0.15	−0.05	μA
	Open loop gain	Av	—	65	—	dB
	Upper clamp voltage	Vclamp-comp	3.65	4.10	4.3	V
	Low voltage	Vl-comp	—	0.1	0.3	V
	Source current	Isrc-comp	−13.5	−10	−6	μA
	Sink current	Isnk-comp	6	10	13.5	μA
	Transconductance	gm	25	46	75	μs
RT	RAMP offset voltage	Voff_ramp	—	1.0	—	V
	RAMP amplitude	dVramp	2.90	3.1	3.3	V
	RT voltage	V-rt	1.9	2.0	2.1	V
Zero current detector	ZCD threshold voltage	Vzcd	−4	0	4	mV
	Input bias current	Ics	−58	−42	−25	μA
Restart	Restart time delay	Tstart	75	150	330	μs
Off time control	Minimum off time	Toff-min	1.0	1.4	1.8	μs

Notes: *1 Design spec

*2 dVramp = Vclamp_comp − Voff_ramp

Electrical Characteristics (cont.)

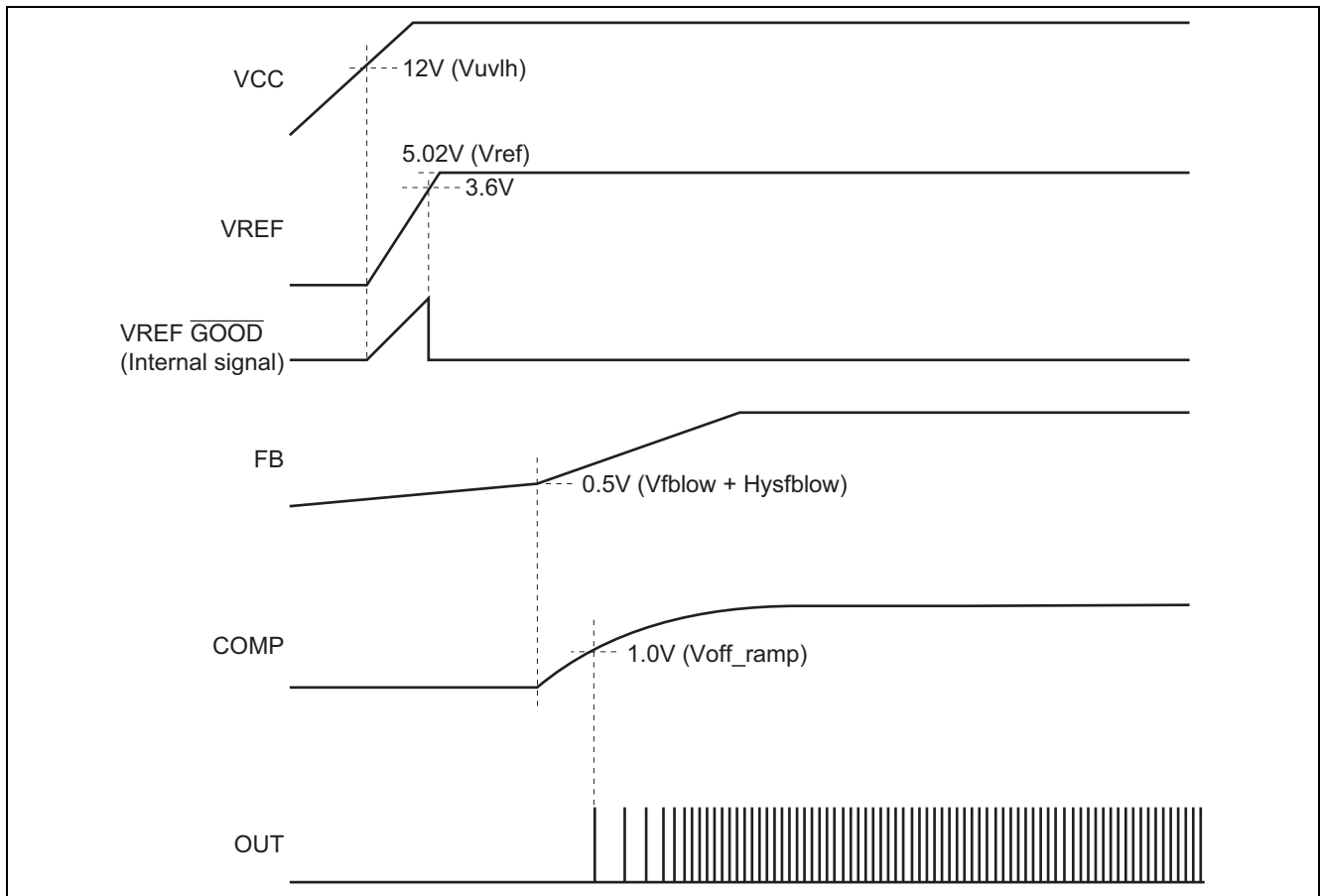
(Ta = 25°C, VCC = 12 V, CS = 0.1 V, FB = COMP, RRT = 200 kΩ)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Out	Rise time	tr-out	—	35	100	ns	CL = 1000 pF 
	Fall time	tf-out	—	35	100	ns	CL = 1000 pF 
	Out low voltage	Vol1-out	—	0.08	0.2	V	Isink = 20 mA
		Vol2-out	—	0.05	0.7	V	Isink = 10 mA, VCC = 5 V
	Out high voltage	Voh-out	11.5	11.8	—	V	Isource = -20 mA
Over current protection	OCP threshold voltage	Vocp	-0.63	-0.6	-0.57	V	
Over & Under voltage protection	Dynamic OVP threshold voltage	Vdovp	—	Vfb× 1.040	—	V	*1
	Dynamic UVP threshold voltage	Vduvp	—	Vfb× 0.920	—	V	*1
	Static OVP threshold voltage	Vsovp	Vfb× 1.075	Vfb× 1.090	Vfb× 1.105	V	
	Static OVP hysteresis	Hys-sovp	50	100	150	mV	
	FB low detect threshold voltage	Vfblow	0.25	0.3	0.35	V	
	FB low detect hysteresis	Hysfblow	0.16	0.20	0.24	V	

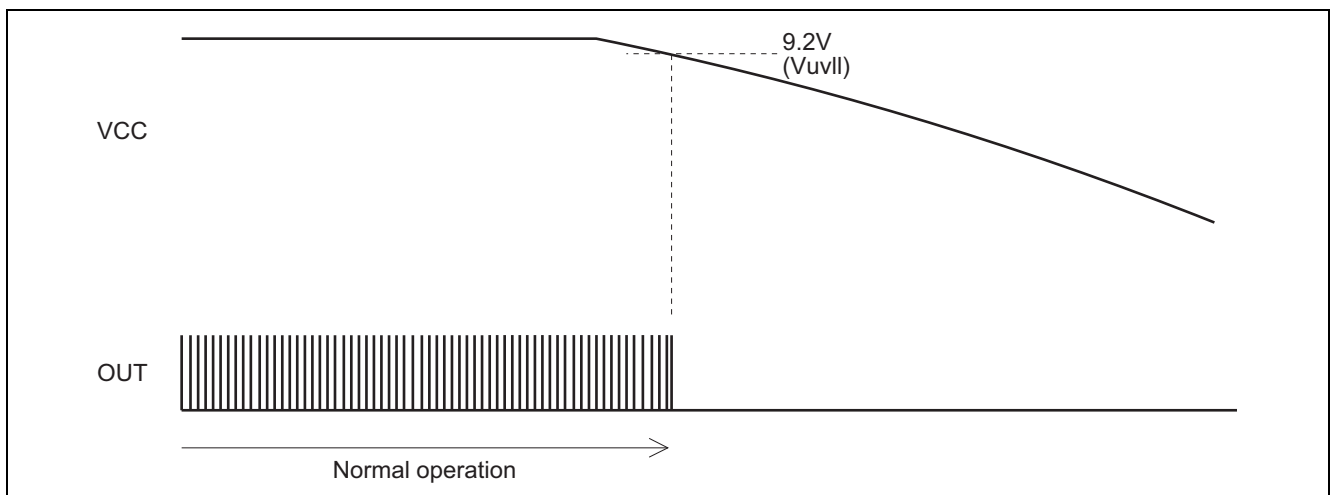
Note: *1 Design spec

Waveforms

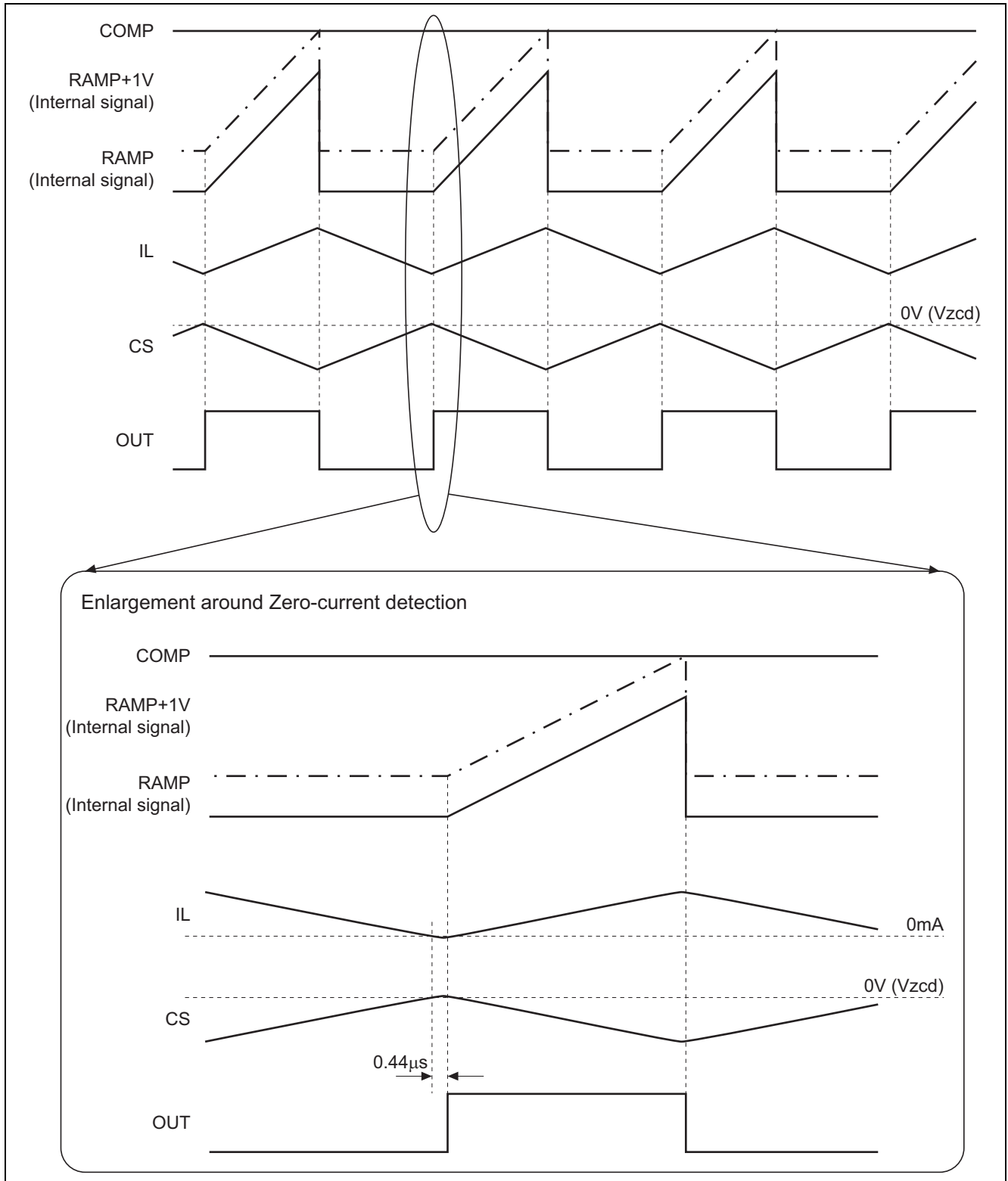
1. Start-up



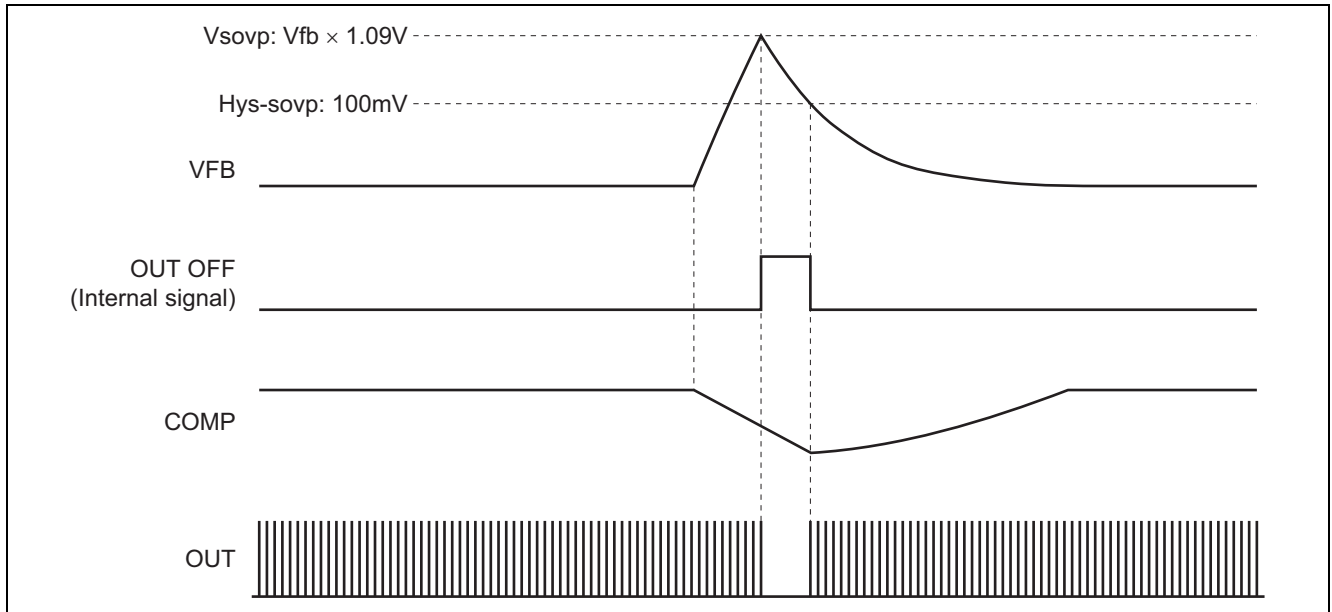
2. Shut-down



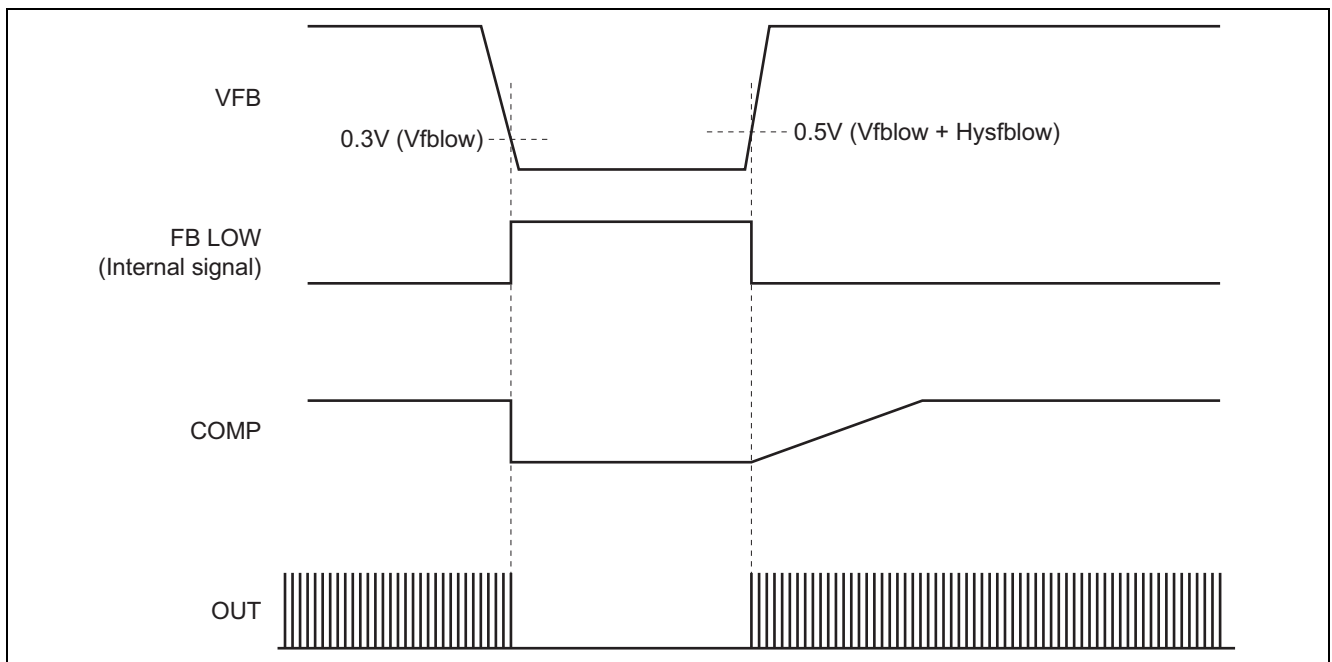
3. Gate Drive Output



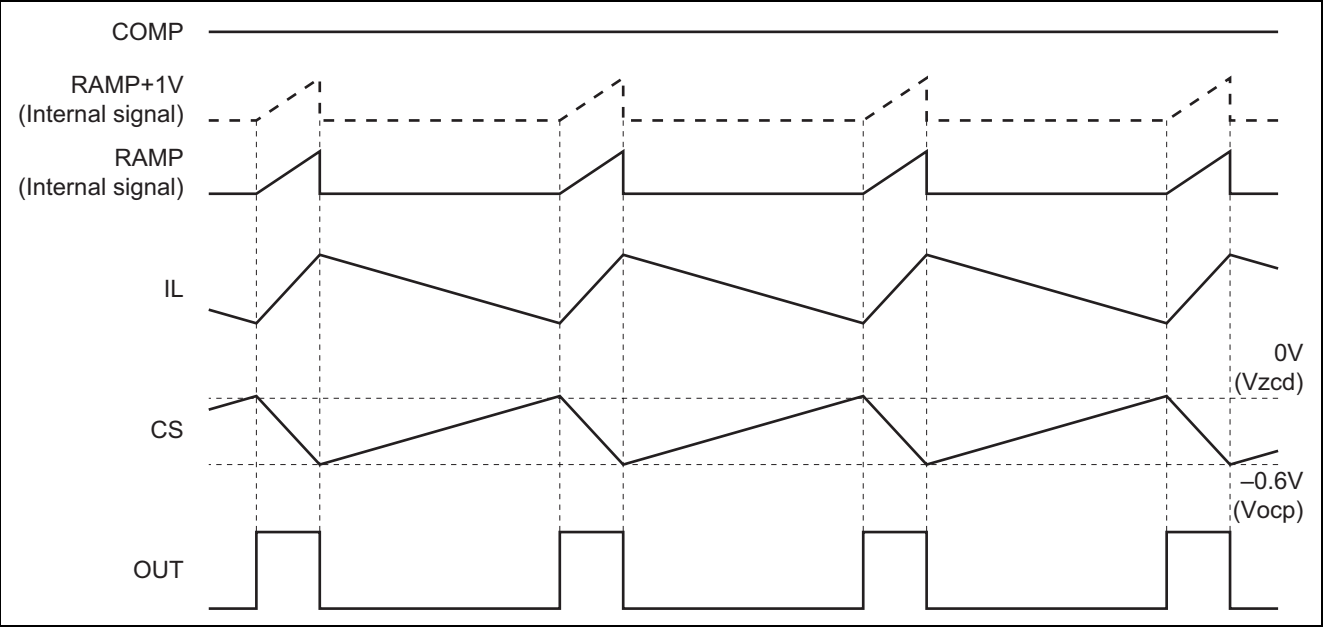
4. Overvoltage Protection (OVP)



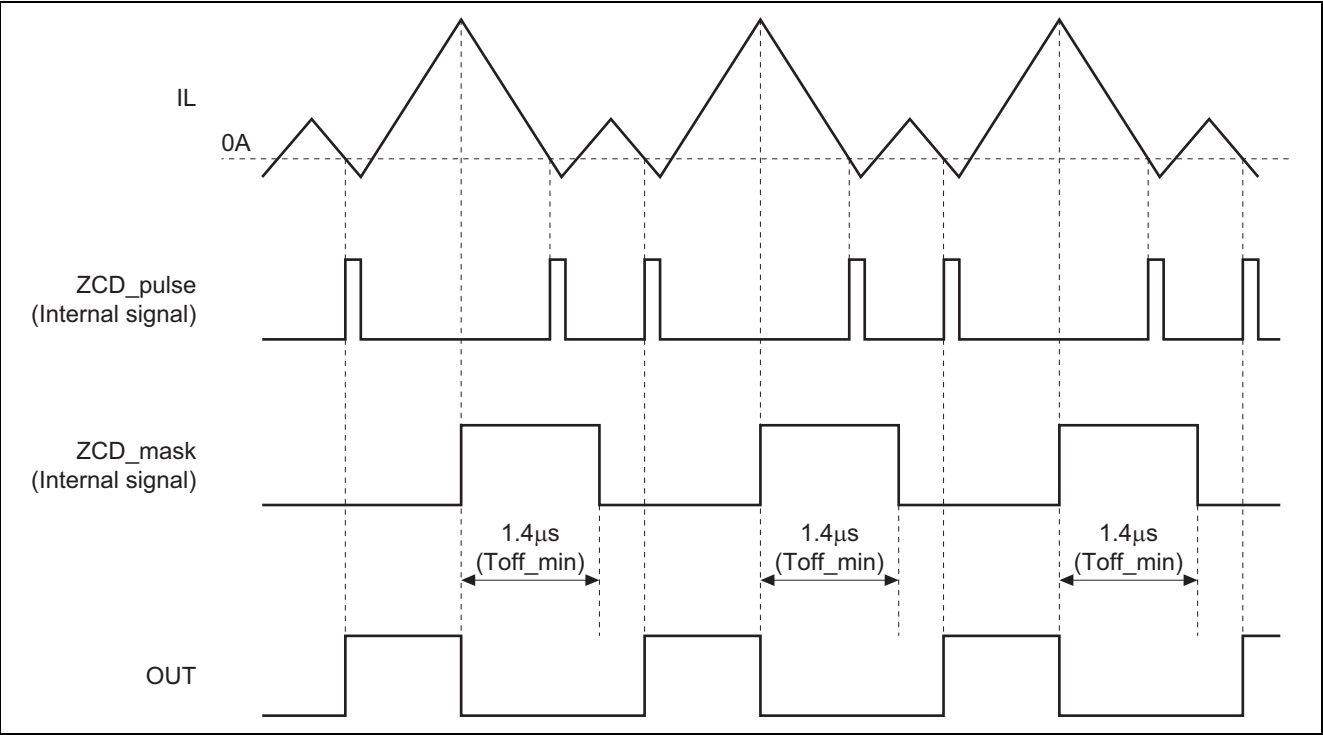
5. FB Low Detection



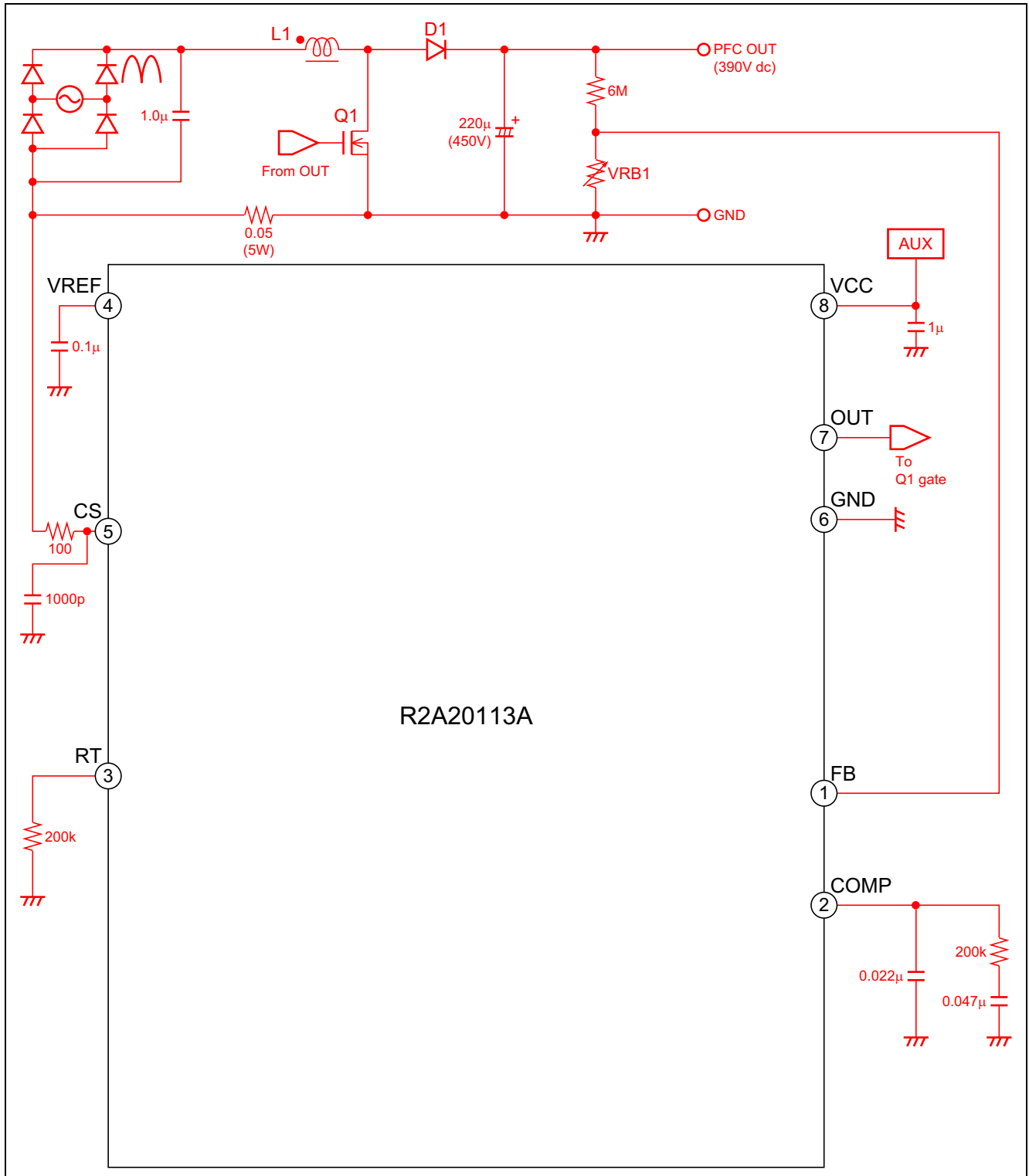
6. Overcurrent Protection (OCP)



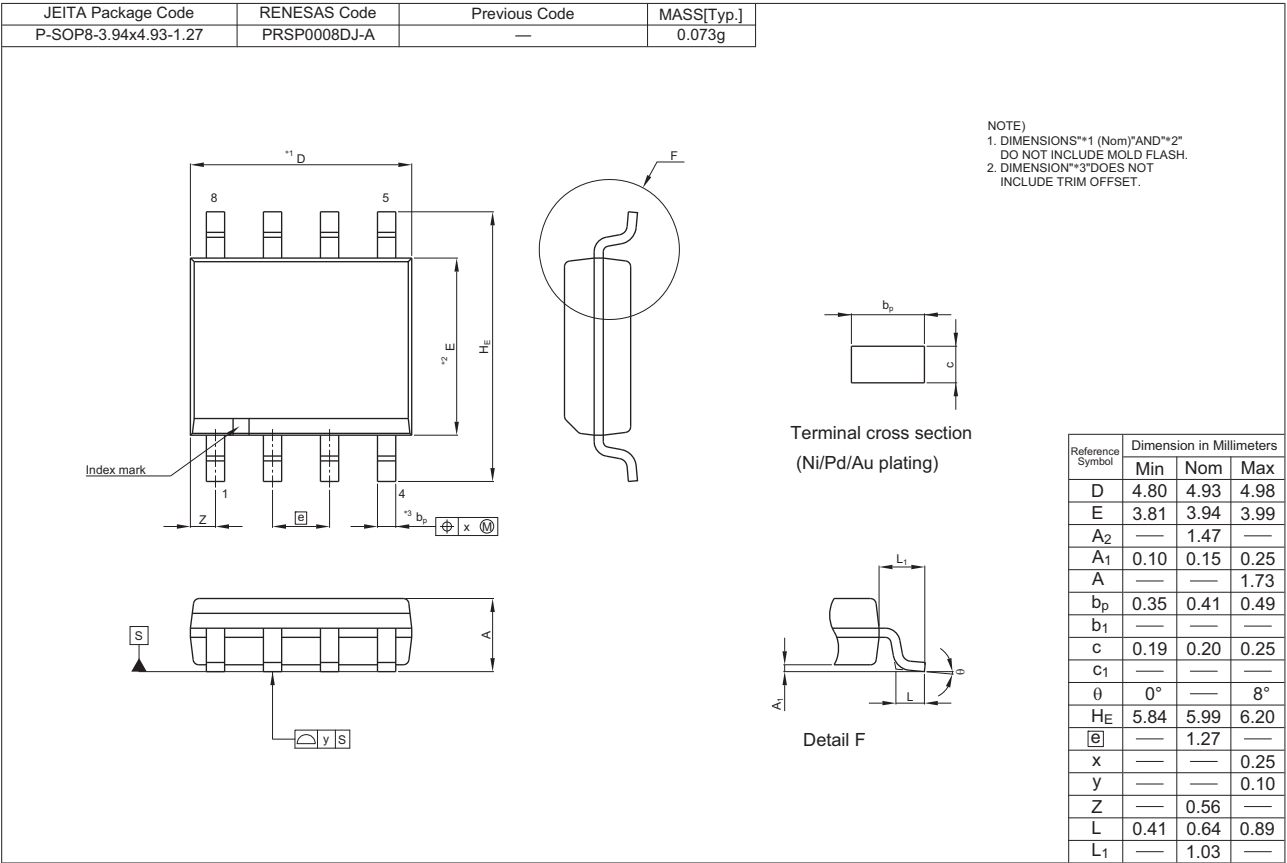
7. Off Time Control (Frequency Limiter)



System Diagram



Package Dimensions



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