

R2A20178NP

8-bit 8ch Multiplying D/A Converter with Buffer Amplifiers

R03DS0021EJ0100 Rev.1.00 2011.09.05

Description

The R2A20178 is a CMOS 8-bit 8ch D/A converter having a multiplying function and output buffer amplifiers. It has a serial data input and can easily communicate with a microcontroller by simple three-wiring method (DI, CLK, LD), and it is suitable for a use in automatic adjustment applications in conjunction with a MCU. The reference voltage terminals (VDAref1, VDAref2) are 4ch x 2 configuration, and the 4 quadrant operation is possible.

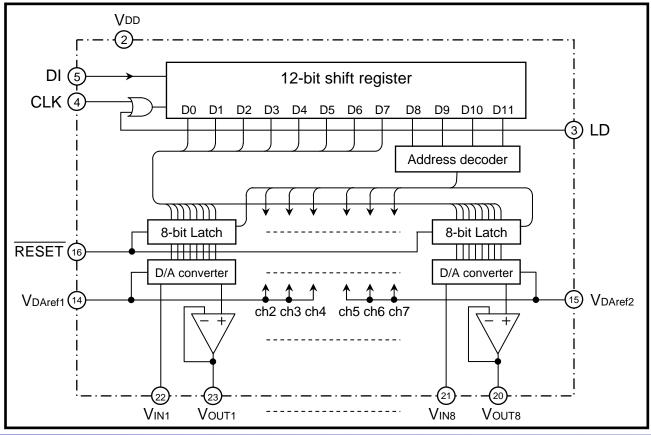
Features

- Guarantee Nonlinearity error : +/-1.0LSB, Differential nonlinearity error : +/-0.7LSB
- Three-wiring serial data transmission
- High performance 8ch D/A converter employing an R-2R with higher-order segment method
- 8 buffer amplifiers operating in a whole supply voltage range from Vod to GND
- High anti-oscillation stability for capacitive loads
- 4 quadrant multiplication
- Very small package : QFN (pin pitch 0.5mm)

Application

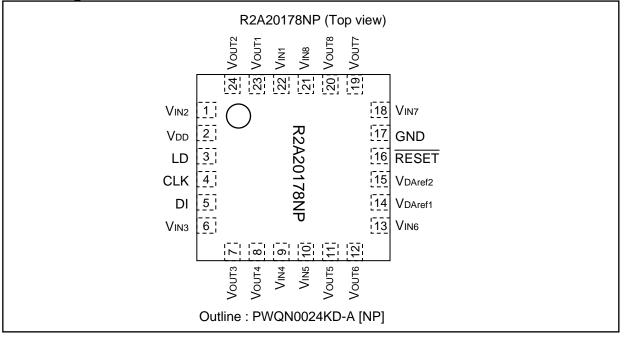
- Digital to analog conversion for consumer and industrial equipment.
- Self adjustment by combination with microcomputer and EEPROM (substitution of half fixed resistance)
- Signal gain control or automatic adjustment of LCD-TV, PDP-TV or LCD display-monitor.
- Voltage control of transmission power amplifier of transceiver

Block Diagram



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Pin Arrangement



Pin Description

Pin No.	Pin Name	Function							
3	LD	A low state of LD enables data of DI loading to the 12-bit resister. During a rising edge of LD, the data in the 12-bit shift register on a rising edge of register.							
4	CLK	hift clock input. Input data of DI are taken into the 12-bit shift register on a rising edge f the clock.							
5	DI	Serial data input. The serial data length is 12-bit.							
16	RESET	Reset 8-bit latches. A low state of RESET clear the all 8-bit latches.							
23	V _{OUT1}								
24	V _{OUT2}								
7	V _{OUT3}								
8	V _{OUT4}	D/A converter output with 8-bit resolution							
11	V _{OUT5}								
12	V _{OUT6}								
19	V _{OUT7}								
20	V _{OUT8}								
2	VDD	Power supply							
17	GND	Ground							
22	V _{IN1}								
1	V _{IN2}								
6	V _{IN3}]							
9	V _{IN4}								
10	V _{IN5}	D/A converter input							
13	V _{IN6}]							
18	V _{IN7}]							
21	V _{IN8}]							
14	V _{DAref1}	D/A converter reference voltage input (ch1 to ch4). Vout= (VIN-VDAref) x n/256+VDAref1							
15	V _{DAref2}	D/A converter reference voltage input (ch5 to ch8). Vout= (VIN-VDAref) x n/256+VDAref2							



Absolute Maximum Ratings

(Ta= +25deg	unless otherwise noted)
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	•			-
ltem	Symbol	Conditions	Ratings	Unit
Supply voltage (for digital)	V _{DD}		-0.3 to +6.5	V
Digital input voltage	Vind		-0.3 to +6.5	V
Analog input voltage	Vin		-0.3 to VDD+0.3 <+6.5	V
Analog output voltage	Vout		-0.3 to VDD+0.3 <+6.5	V
D/A reference voltage	VDAref		-0.3 to VDD+0.3 <+6.5	V
Power dissipation	Pd	Ta= +85deg	300	mW
Thermal derating	K theta	Ta> +25deg	7.5	mW/deg
Operating temperature	Topr		-30 to +85	deg
Storage temperature	Tstg		-40 to +125	deg

Electrical Characteristics

< Analog/Digital Common Part >

(VDD, VIN= +5V +/-10%, VDD>VIN, GND=VDAref1=VDAref2 = 0V, Ta = -30 to +85deg, unless otherwise noted.)

Symbol	Conditions		Unit			
Symbol	Conditions	Min Typ Max			Unit	
Vdd		2.7	5.0	5.5	V	
ldd	CLK =1MHz, VDD =5V, IAO =0µA	-	-	2.0	mA	
		VDD	VDD Min 2.7	VDD Min Typ VDD 2.7 5.0	Symbol Conditions Min Typ Max V_DD 2.7 5.0 5.5	

< Digital Part > (VDD, VIN = +5V +/-10%, VDD>VIN, GND=VDAref1=VDAref2 = 0V, Ta = -30 to +85deg, unless otherwise noted.)

ltem	Symbol	Conditions		Unit		
hem	Cymbol	Conditions	Min	Тур	Max	onic
Input leak current	Iilk	VIN = 0 to VDD	-10	-	10	μA
Digital input "Low" voltage	VIL		-	-	0.2 Vdd	V
Digital input "High" voltage	Vін		0.8 Vdd	-	-	V

< Analog Part > (VDD, VIN = +5V +/-10%, VDD>VIN, GND=VDAref1=VDAref2 = 0V, Ta = -30 to +85deg, unless otherwise noted.)

ltem	Symbol	Conditions		Unit		
nem	Cymbol	Conditions	Min	Тур	Max	Onic
Input current	lin	$V_{IN} = 5V$, $V_{DAref} = 0$ V, Proportional to Max. input current condition ($V_{IN} - V_{DAref}$) and digital data of each channels	-	-	0.3	mA
D/A reference input current	DAref	VIN1 to VIN8 =5V, VDAref =0 V, Proportional to Max. input current condition (VIN $-$ VDAref) and digital data of each channels	-2.4	-	-	mA
Resolution	RES		-	8	-	bit
Differential nonlinearity	DNL	VDAref1 =VDAref2 =0.05V,	-0.7	-	0.7	LSB
nonlinearity	NL	Without load (Ivout= 0µA)	-1	-	1	LSB
Buffer amplifier output	N	I _{AO} = +/-100 μA	0.1	-	Vcc-0.1	V
voltage range	Vao	I _{AO} = +/-500 μA	0.2	-	Vcc-0.2	V
Buffer amplifier output current range	Iao	Upper saturation voltage =0.4V, Lower saturation voltage =0.4V	-1	-	1	mA
Output capacitive load	Co		-	-	0.1	μF
Buffer amplifier output impedance	Ro		-	5	-	ohm

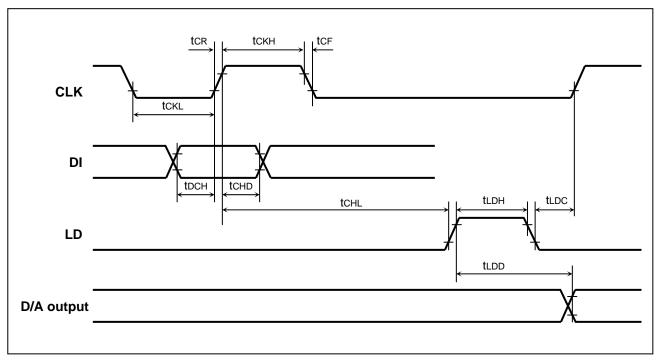


AC Characteristics

(VDD,VIN = +5V +/-10%, VDD>VIN, GND=VDAref1=VDAref2 = 0V, Ta = -30 to +85deg, unless otherwise noted.)

ltom	Symbol	Conditions		Unit		
ltem	Symbol	Conditions	Min	Min Typ Max		Unit
Clock "L" pulse width	t CKL		200	-	-	ns
Clock "H" pulse width	tскн		200	-	-	ns
Clock rise time	tcr		-	-	200	ns
Clock fall time	t CF		-	-	200	ns
Data setup time	tdcн		60	-	-	ns
Data hold time	tснр		100	-	-	ns
LD setup time	t CHL		200	-	-	ns
LD hold time	t LDC		100	-	-	ns
LD "H" pulse duration time	t ldh		100	-	-	ns
D/A output settling time	tldd	C _L <100pF, V _{OUT} : 0.5 ↔ 4.5 V, Time until the output becomes the final value of 1/2 LSB	-	-	300	μs
RESET "Low" level minimum pulse width	trl		200	-	-	ns

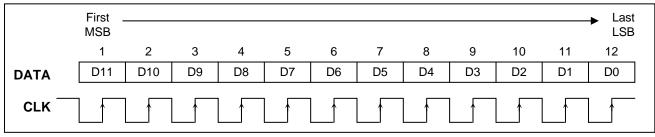
Timing Chart





Digital Data Format

12-bit serial data



Data Assignment

D8	D9	D10	D11	: DAC select data					
D0	D1	D2	D3	D4	D5	D6	D7	: DAC data	

DAC select data

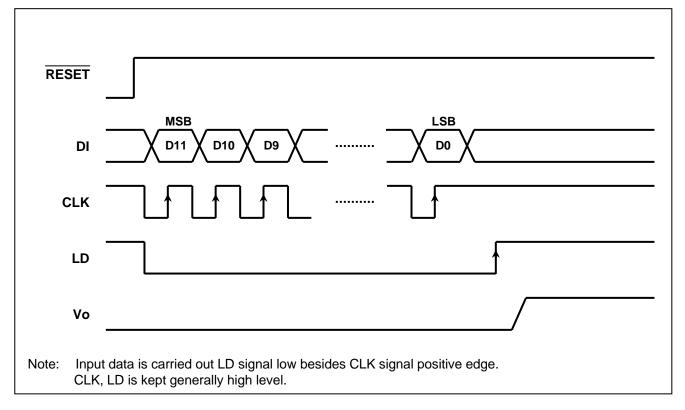
D8	D9	D10	D11	DAC Selection
0	0	0	0	Don't care
0	0	0	1	Vout1 selection
0	0	1	0	VOUT2 selection
0	0	1	1	Vout3 selection
0	1	0	0	Vout4 selection
0	1	0	1	Vouт₅ selection
0	1	1	0	Voute selection
0	1	1	1	Vout7 selection
1	0	0	0	Vouts selection
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

DAC data

D0	D1	D2	D3	D4	D5	D6	D7	DAC Output
0	0	0	0	0	0	0	0	VDAref
1	0	0	0	0	0	0	0	(VIN-VDAref) / 256 x 1+ V _{DAref}
0	1	0	0	0	0	0	0	(VIN - VDAref) / 256 x 2 + V _{DAref}
1	1	0	0	0	0	0	0	(VIN – VDAref) / 256 x 3 + V _{DAref}
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	(VIN – VDAref) / 256 x 255 + V _{DAref}



Timing Chart (Model)

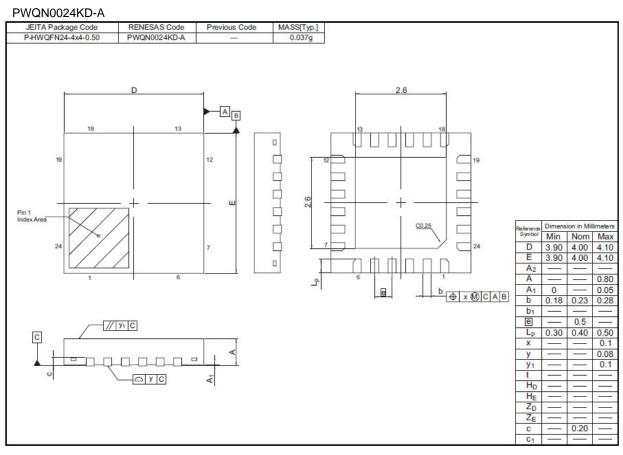


Ordering Information

Order part No.	Package Name	Package Code	Package type No.	Packing/Quantity
R2A20178NP	QFN-24	PWQN0024KD-A	NP	Embossed Taping/2,500 pcs.



Package Dimensions





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