

# R2A20164NP/SA

8-bit 4ch D/A Converter with Buffer Amplifiers

R03DS0017EJ0100

Rev.1.00

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## Description

The R2A20164 is an integrated circuit semiconductor of CMOS structure with 4 channels of built in D/A unnecessary and enabling configuration of a system with few component parts.

Serial data transfer type input can easily be used through a combination of three lines: DI, CLK, and LD.

Outputs incorporate buffer op-amps that have a drive capacity of 1 mA or above for both sink source, and can operate over the entire voltage range from almost ground to Vcc ( 0 to 5V ), making peripheral elements unnecessary and enabling configuration of a system with few component parts.

Very small QFN package is added to lineup. It is suitable for a small mounting and reduces the mounting area.

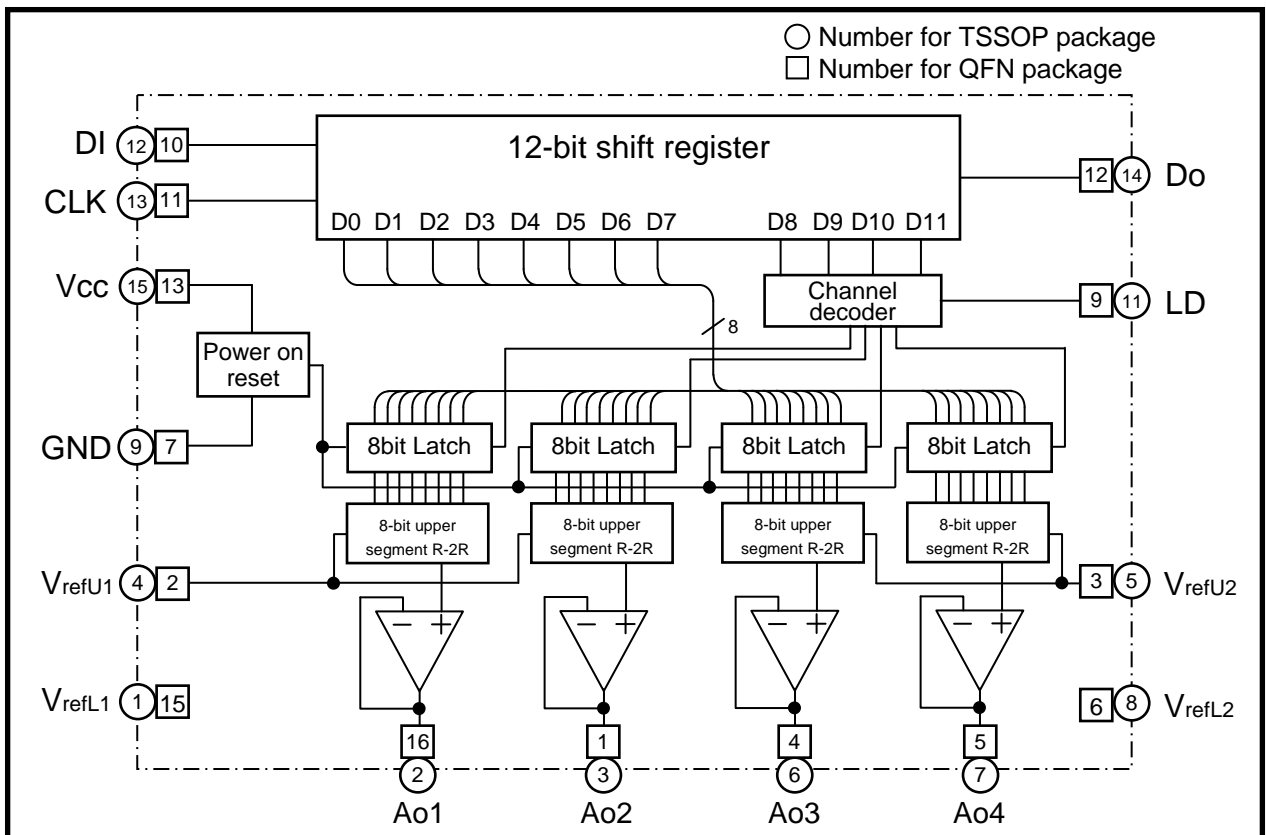
## Features

- Guarantee Differential nonlinearity error :  $\pm 0.7\text{LSB}$ , Nonlinearity error :  $\pm 1.0\text{LSB}$
- Data transfer format: 12-bit serial data input type by 3 wire ( DI, SCK, LD )
- Output buffer op-amps: Operable over entire voltage range from almost ground to Vcc ( 0 to 5V )
- 4 reference voltage terminals ( 2ch  $\times$  2 composition and completely independent of the power supply terminal)
- Very small size package line-up: QFN-16 (pin pitch: 0.5mm), TSSOP-16 (pin pitch 0.65mm)

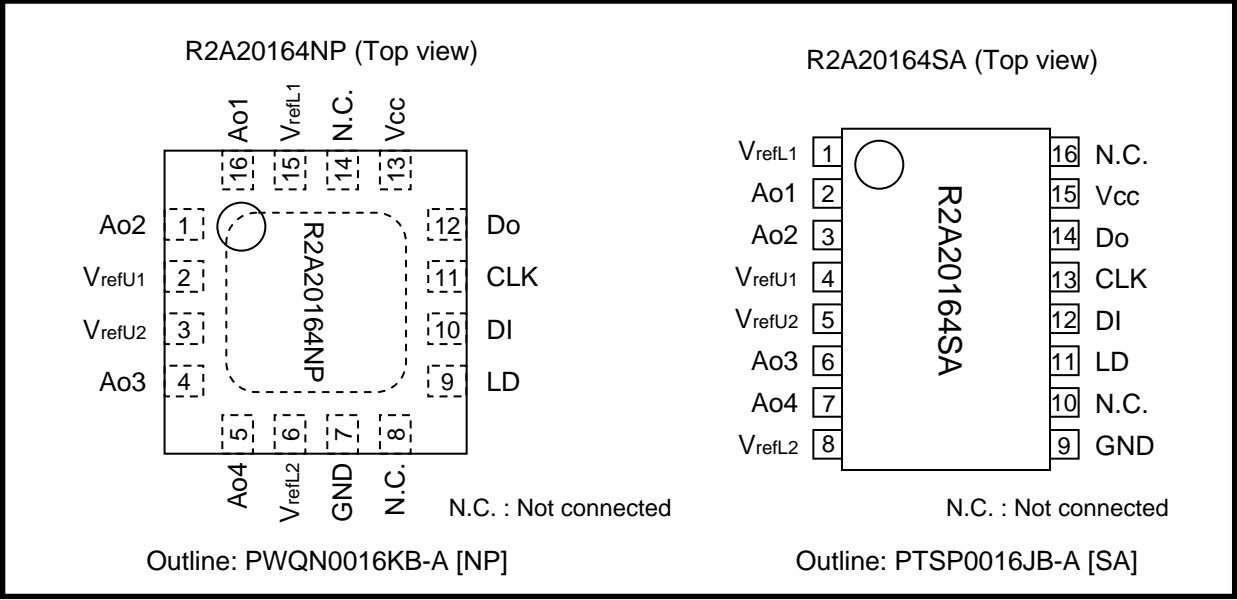
## Application

- Conversion from digital data to analog control data for home-use and industrial equipment.
- Signal gain control or automatic adjustment of LCD-TV, PDP-TV or LCD display-monitor.
- Blurring correction control or various control of the interchangeable lens of digital still camera.
- Automatic adjustment by combination with microcomputer and EEPROM.  
(substitution of half fixed resistance)

## Block Diagram



Pin Arrangement



Pin Description

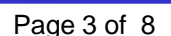
Pin No.		Symbol	Function
[QFN]	[TSSOP]		
10	12	DI	Serial data input terminal. ( Input serial data with a 12-bit data length )
11	13	CLK	Serial clock input terminal (Input signal from DI terminal is input to 12-bit shift register at rise of serial clock.)
9	11	LD	Load terminal (When High level is input to LD terminal, value in 12-bit shift register is loaded into decoder and 8-bit latch.)
12	14	Do	Serial data output terminal (Data is sequentially output from the MSB bit.)
16	2	Ao1	8-bit resolution D/A converter output terminals (After power on, all channels are reset and DAC data 00h is output.)
1	3	Ao2	
4	6	Ao3	
5	7	Ao4	
13	15	Vcc	Power supply terminal
7	9	GND	GND terminal
2	4	VrefU1	D/A converter upper reference voltage input terminal for ch1 and ch2
3	5	VrefU2	D/A converter upper reference voltage input terminal for ch3 and ch4
15	1	VrefL1	D/A converter lower reference voltage input terminal for ch1 and ch2
6	8	VrefL2	D/A converter lower reference voltage input terminal for ch3 and ch4
8	10	N.C.	Not connected
14	16	N.C.	Not connected

(Ta= +25deg unless otherwise noted)

## Electrical Characteristics

(V<sub>CC</sub>, V<sub>refU1</sub>, V<sub>refU2</sub> = +5V +/-10%, V<sub>CC</sub> > V<sub>refU1</sub>, V<sub>refU2</sub>, GND=V<sub>refL1</sub>=V<sub>refL2</sub>= 0V, T<sub>a</sub>= -30 to +85deg unless otherwise noted)

\*1 : When power supply is turned on, internal circuit is initialized by power on reset circuit. But, if re-powered on quickly, initialize is not operate. So, keep the time period of re-powered on ( $t_{POR}$ ).



## « Analog Part »

(V<sub>CC</sub>, V<sub>refU1</sub>, V<sub>refU2</sub> = +5V +/-10%, V<sub>CC</sub>>V<sub>refU1</sub>, V<sub>refU2</sub>, GND=V<sub>refL1</sub>=V<sub>refL2</sub>= 0V, T<sub>a</sub>= -30 to +85deg unless otherwise noted)

Item	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Current dissipation	I <sub>refU1, 2</sub>	V <sub>refU1</sub> =V <sub>refU2</sub> =5V, V <sub>refL1</sub> =V <sub>refL2</sub> =0V, I <sub>AO</sub> =0μA, Data condition: at maximum current for each terminal	-	0.3	0.6	mA
D/A converter upper reference voltage range *2	V <sub>refU</sub>		0.7V <sub>CC</sub>	-	V <sub>CC</sub>	V
D/A converter lower reference voltage range *2	V <sub>refL</sub>		GND	-	0.3V <sub>CC</sub>	V
Buffer amplifier output voltage range	V <sub>AO</sub>	I <sub>AO</sub> = +/- 100 μA	0.1	-	V <sub>CC</sub> - 0.1	V
		I <sub>AO</sub> = +/- 500 μA	0.2	-	V <sub>CC</sub> - 0.2	V
Buffer amplifier output drive range	I <sub>AO</sub>	Upper side saturation voltage = 0.3V, Lower side saturation voltage = 0.2V	-1.0	-	1.0	mA
Differential nonlinearity	S <sub>DL</sub>	V <sub>refU</sub> = 4.79V, V <sub>refL</sub> = 0.95V, V <sub>CC</sub> = 5.5V (15mV/LSB), Without load (I <sub>AO</sub> = 0μA)	-0.7	-	0.7	LSB
Nonlinearity	S <sub>L</sub>		-1.0	-	1.0	LSB
Zero code error	S <sub>ZERO</sub>		-2.0	-	2.0	LSB
Full scale error	S <sub>FULL</sub>		-2.0	-	2.0	LSB
Output capacitive load	Co		-	-	0.1	μF
Buffer amplifier output impedance	Ro		-	5.0	-	ohm

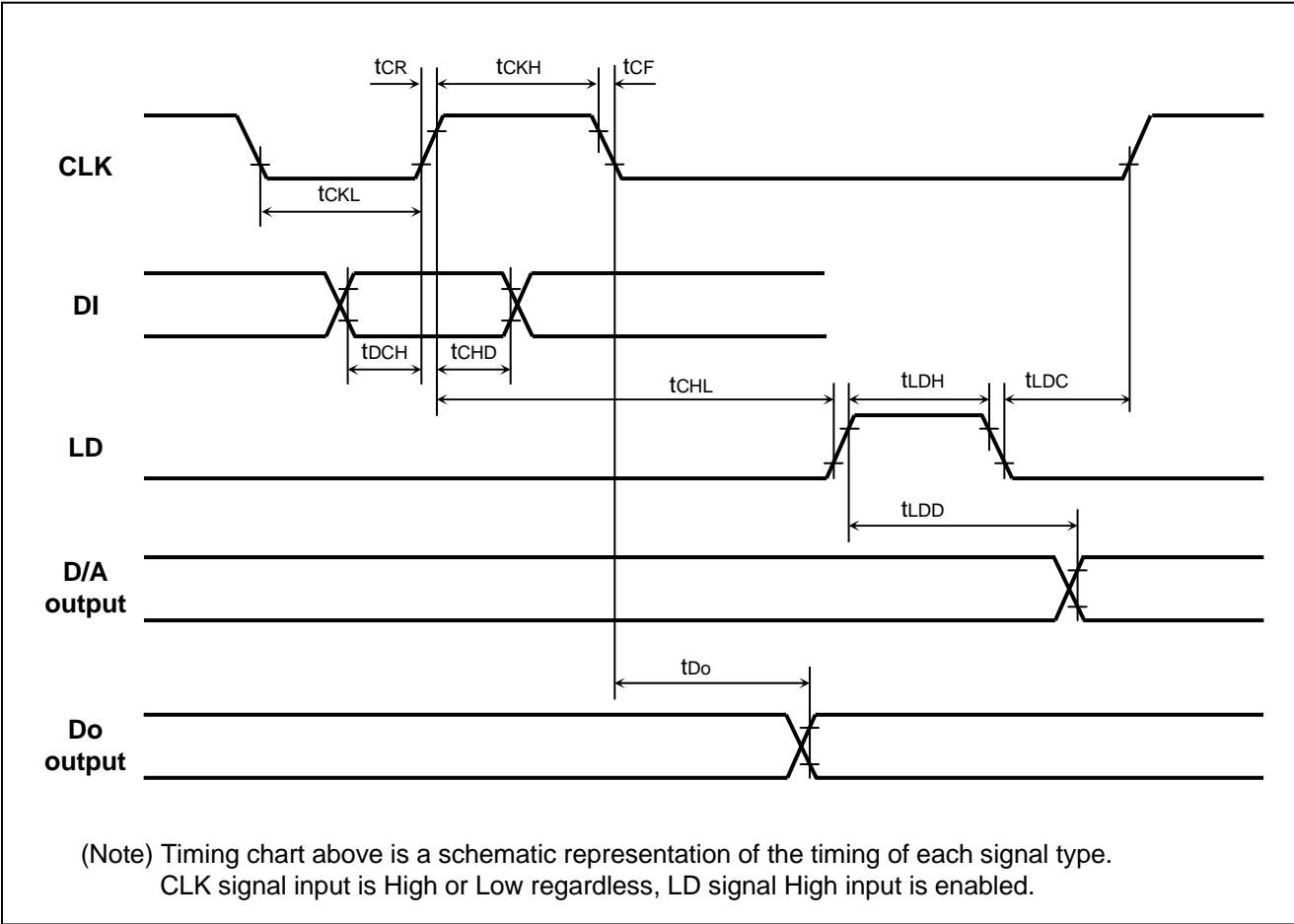
\*2 : The output does not necessary be the value with the reference voltage setting range.  
The output value is determined by the buffer amplifier output voltage range (V<sub>AO</sub>).

AC Characteristics

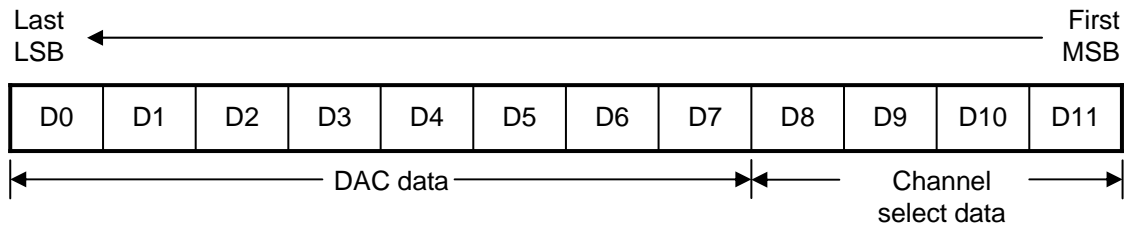
(V<sub>CC</sub>,V<sub>refU1</sub>,V<sub>refU2</sub> = +5V +/-10%, V<sub>CC</sub> >V<sub>refU1</sub>,V<sub>refU2</sub>, GND=V<sub>refL1</sub>=V<sub>refL2</sub>= 0V, Ta= -30 to +85deg unless otherwise noted)

Item	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Clock frequency	f <sub>CLK</sub>		-	1.0	10	MHz
Clock low pulse width	t <sub>CKL</sub>		40	-	-	ns
Clock high pulse width	t <sub>CKH</sub>		40	-	-	ns
Clock rise time	t <sub>CR</sub>		-	-	200	ns
Clock fall time	t <sub>CF</sub>		-	-	200	ns
Data setup time	t <sub>DCH</sub>		4	-	-	ns
Data hold time	t <sub>CHD</sub>		30	-	-	ns
LD setup time	t <sub>CHL</sub>		40	-	-	ns
LD hold time	t <sub>LDC</sub>		40	-	-	ns
LD high pulse width	t <sub>LDH</sub>		40	-	-	ns
Data output delay time	t <sub>DO</sub>	C <sub>L</sub> < 100 pF	-10	-	50	ns
D/A output settling time	t <sub>LDD</sub>	Ta=25deg, C <sub>L</sub> <100pF, V <sub>AO</sub> : 0.5↔4.5V, The time until the output becomes the final value of 1/2 LSB.	-	-	150	μs

Timing Chart



Digital Data Format



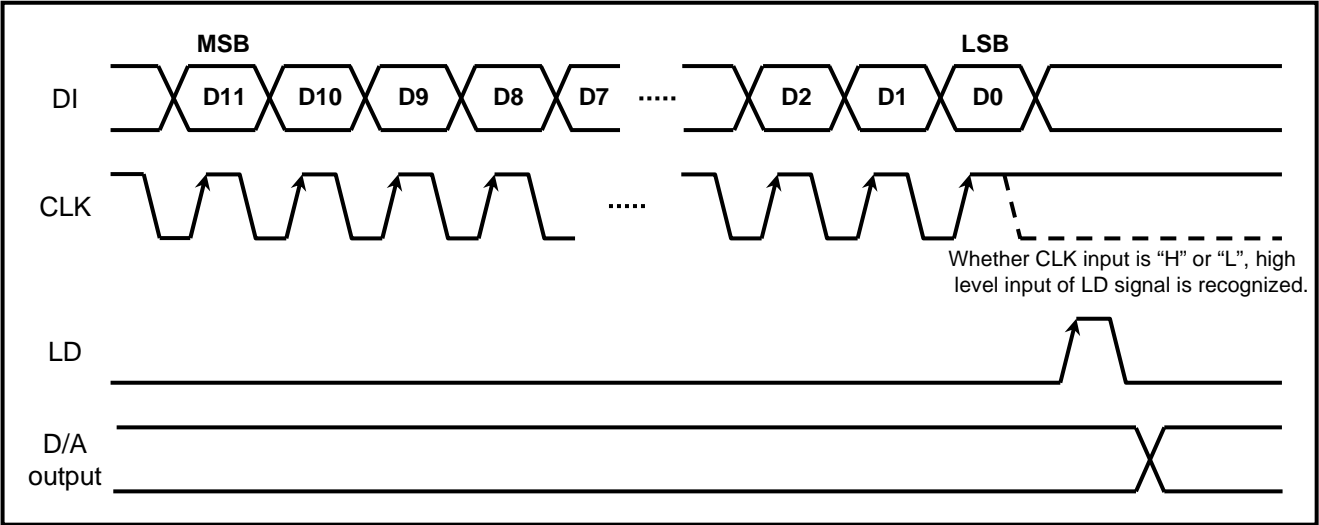
Channel select data

D8	D9	D10	D11	Chanel Selection
0	0	0	0	Don't care
0	0	0	1	Ao1 select
0	0	1	0	Ao2 select
0	0	1	1	Ao3 select
0	1	0	0	Ao4 select
0	1	0	1	Don't care
:	:	:	:	:
1	1	1	0	Don't care
1	1	1	1	Don't care

DAC data

D0	D1	D2	D3	D4	D5	D6	D7	D/A Output
0	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 1 + V_{refL}$
1	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 2 + V_{refL}$
0	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 3 + V_{refL}$
1	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 4 + V_{refL}$
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	$(V_{refU} - V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	$V_{refU}$

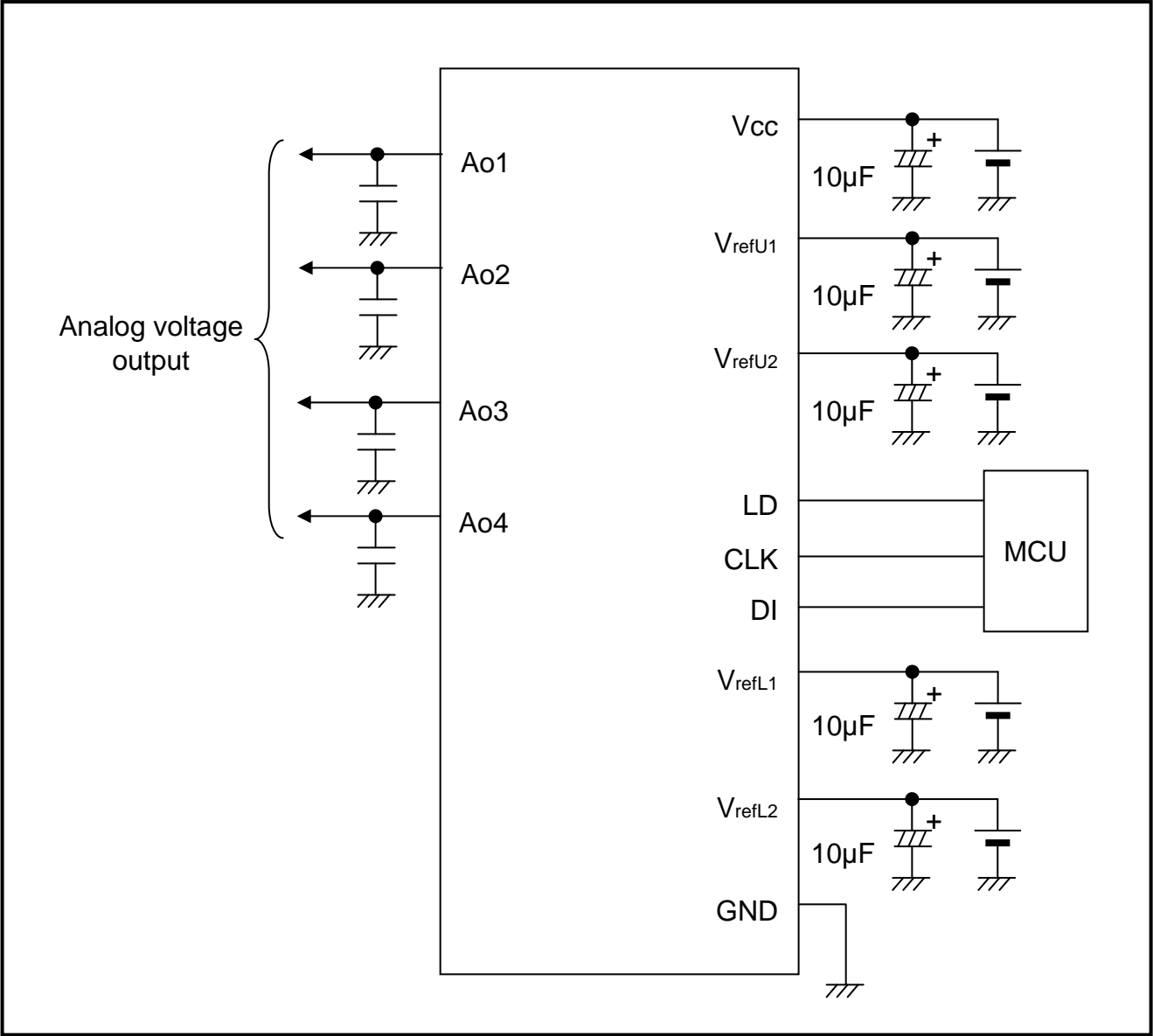
Data Timing Chart ( Model )



Precaution For use

- There are five terminals ( $V_{CC}$ ,  $V_{refU1,2}$ ,  $V_{refL1,2}$ ) that should be impressed a constant voltage. When ripple or spike noise is input to this terminal, there is fear that the accuracy of D/A conversion becomes lower and this IC malfunction. So, when use this IC, please connect capacitor between these terminals ( $V_{CC}$ ,  $V_{refU1,2}$ ,  $V_{refL1,2}$ ) and GND for stable D/A conversion.
- This IC's output amplifier has an advantage to capacitive load, So, it's no problem at device action when connect capacitor ( 0.1 $\mu$ F Max ) among output to GND for every noise elimination.

Standard Application Circuit

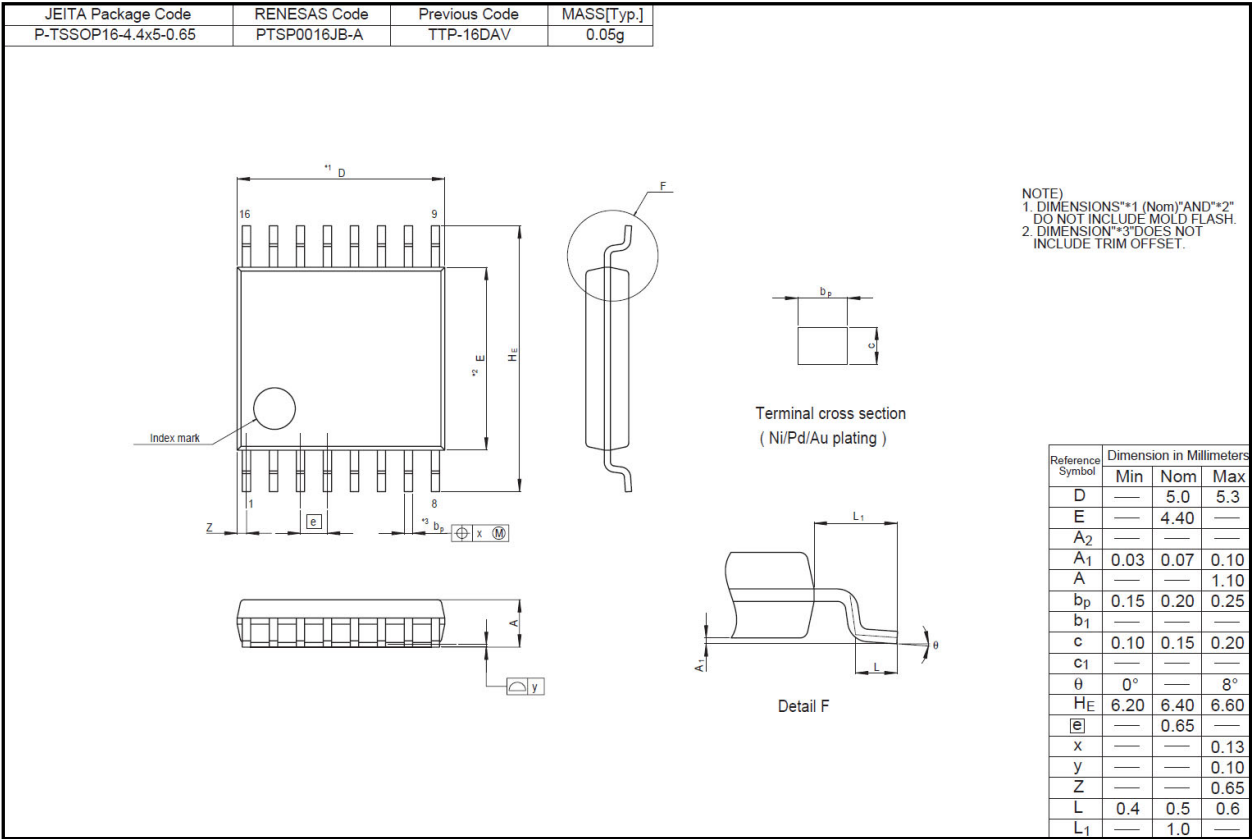


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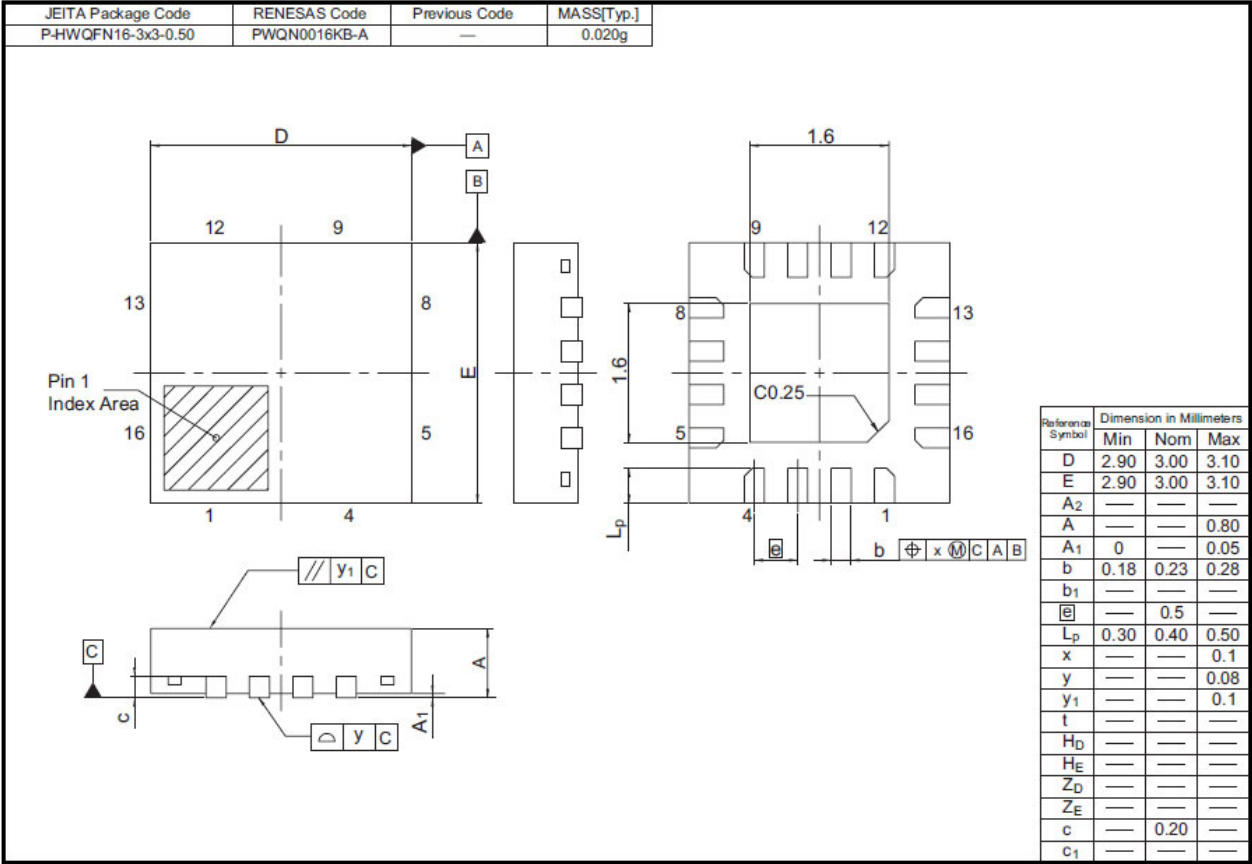
Order part No.	Package Name	Package Code	Package type No.	Packing/Quantity
R2A20164SA	TSSOP-16	RTSP0016JB-A	SA	Embossed Taping/2,000 pcs.
R2A20164NP	QFN-16	PWQN0016KB-A	NP	Embossed Taping/3,000 pcs.

Package Dimensions

PTSP0016JB-A [SA]



PWQN0016KB-A [NP]





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