RL78/G1P

RENESAS MCU

R01DS0371EJ0100
Rev.1.00
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True low-power platform (66 µA/MHz, and 0.31 µA for LVD) for the general-purpose and sensor control applications, with 2.7-V to 3.6-V operation, low pin counts (24 or 32 pins), small ROM capacity (16 Kbytes), and highly-functional analog circuits (12-bit A/D and 10-bit D/A converters)

1. OUTLINE

1.1 Features

- Minimum instruction execution time can be changed from high speed (0.03125 µs: @ 32 MHz operation with high-speed on-chip oscillator) to low-speed (1 µs: @ 1 MHz operation with high-speed on-chip oscillator)
- General-purpose registers: 8 bits × 32 registers (8 bits × 8 registers × 4 banks)
- ROM: 16 KB, RAM: 1.5 KB, Data flash: 2 KB
- High-speed on-chip oscillator
  - Select from 32 MHz (TYP.), 24 MHz (TYP.), 16 MHz (TYP.), 12 MHz (TYP.), 8 MHz (TYP.), 6 MHz (TYP.), 4 MHz (TYP.), 3 MHz (TYP.), 2 MHz (TYP.), and 1 MHz (TYP.)
- On-chip single-power supply flash memory (with prohibition of block erase/writing function)
- Self-programming
- On-chip debug function
- On-chip power-on-reset (POR) circuit and voltage detector (LVD)
- On-chip watchdog timer (operable with the dedicated low-speed on-chip oscillator)
- On-chip clock output/buzzer output controller
- On-chip BCD adjustment
- I/O ports: 26 or 28 (N-ch open drain: 2)
- Timer
  - 16-bit timer TAU: 4 channels
  - Watchdog timer: 1 channel
- Serial interface
  - CSI: 1 channel
  - UART: 1 channel
  - I^2C 1 channel (2 slave addresses)
- 8/12-bit resolution A/D converter (V_{DD} = 2.7 to 3.6 V): 6 or 8 channels
- Standby function: HALT, STOP, SNOOZE mode
- On-chip 10-bit D/A converter
- DMA controller: 2 channels
- On-chip event link controller (ELC)
- Power supply voltage: V_{DD} = 2.7 to 3.6 V
- Operating ambient temperature: T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications)

Remark The functions mounted depend on the product. See **1.6 Outline of Functions.**

○ ROM, RAM capacities

Flash ROM	Data Flash	RAM Note	24-pin	32-pin
16 KB	2 KB	1.5 KB	R5F11Z7AANA, R5F11Z7ADNA	R5F11ZBAAFP, R5F11ZBADFP

Note The flash libraries use the on-chip RAM area from FFE20H to FFEFFH and the parts of the RAM area referred to as self RAM (RAM for use in self-programming), which are listed in the table below, for self-programming or rewriting of the data flash memory.

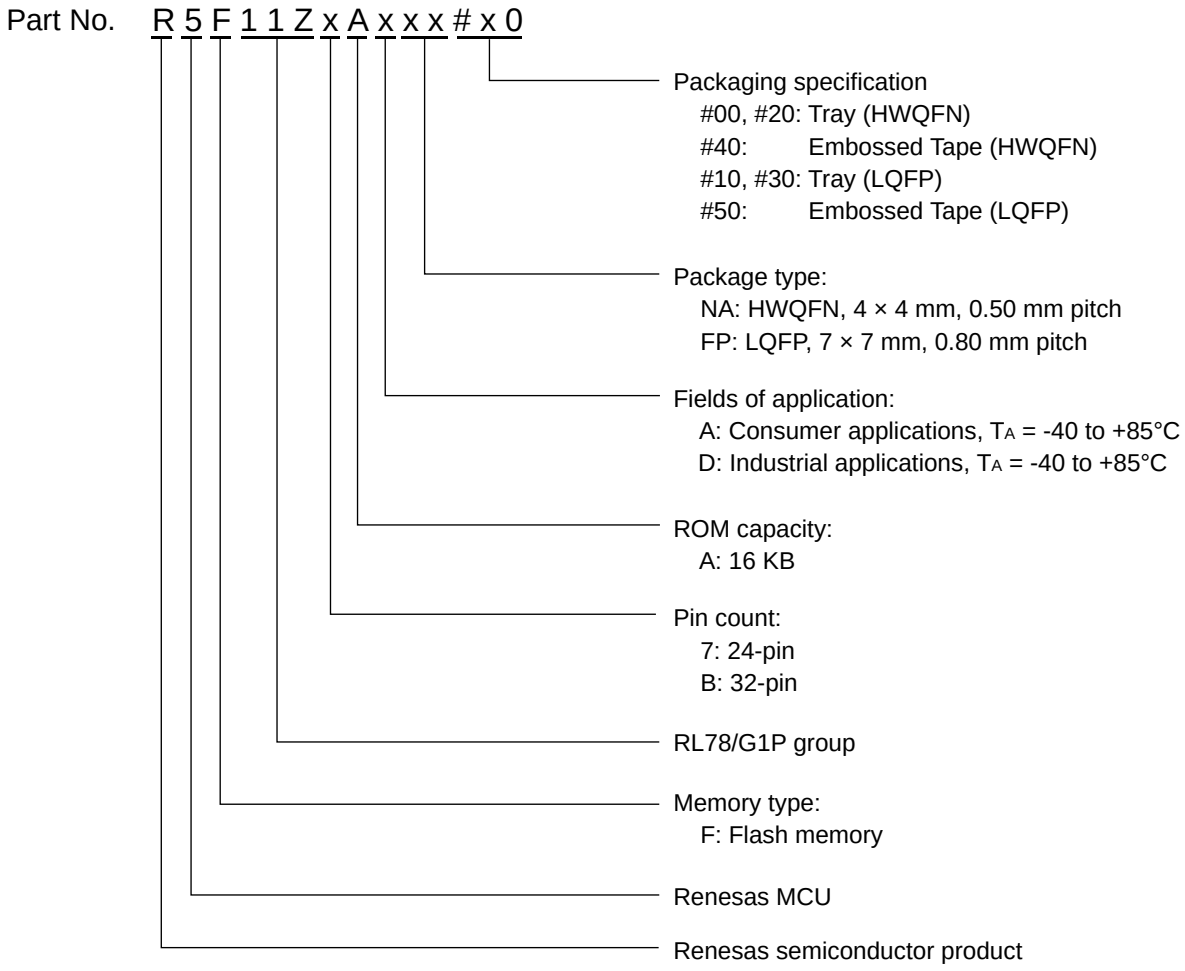
See below for the RAM areas used by the flash library.

	RAM	FSL Type01	FDL Type04	EEL Pack01, EEL Pack02
		Self RAM size 896 bytes Note	Self RAM size 136 bytes	
R5F11Z7AANA R5F11Z7ADNA R5F11ZBAAFP R5F11ZBADFP	1.5 KB	FF900H to FFC7FH	FF900H to FF987H	Not available

Note Functions supported in FSL Type01 are only basic functions. Other functions are not supported.
Basic functions: FSL_Init, FSL_Open, FSL_Close, FSL_PrepareFunctions, FSL_BlankCheck, FSL_Erase, FSL_IVerify, FSL_Write, and FSL_StatusCheck

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package

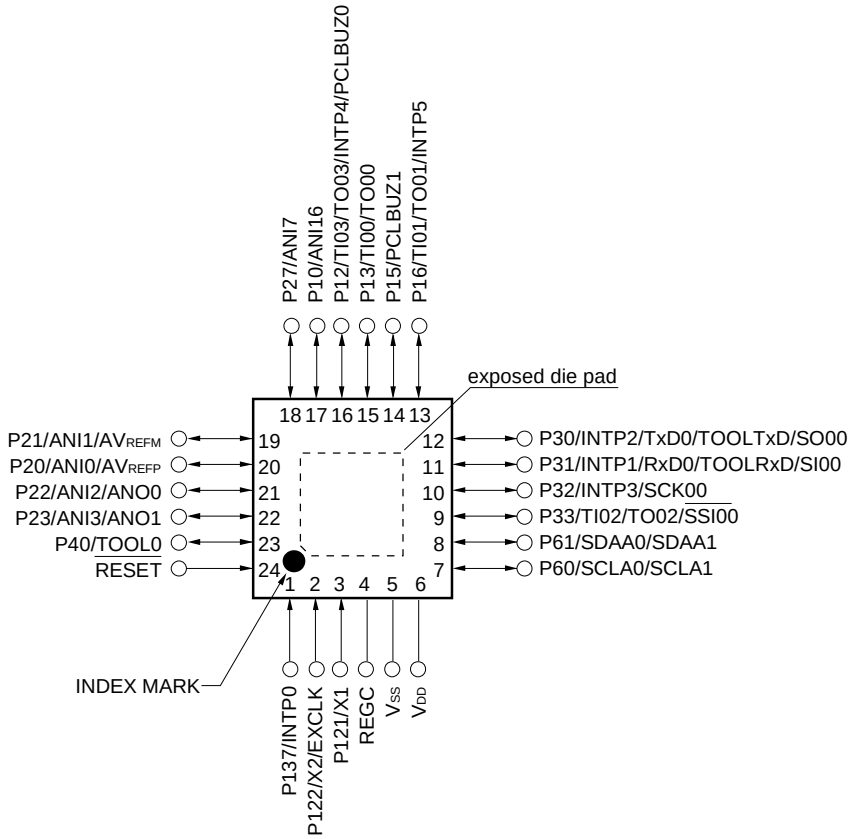


Pin Count	Package	Data Flash	Fields of Application	Packaging Specification	Part Number
24 pins	24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)	2 KB	A	Tray	R5F11Z7AANA#00, R5F11Z7AANA#20
				Embossed Tape	R5F11Z7AANA#40
			D	Tray	R5F11Z7ADNA#00, R5F11Z7ADNA#20
				Embossed Tape	R5F11Z7ADNA#40
32 pins	32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)		A	Tray	R5F11ZBAAFP#10, R5F11ZBAAFP#30
				Embossed Tape	R5F11ZBAAFP#50
			D	Tray	R5F11ZBADFP#10, R5F11ZBADFP#30
				Embossed Tape	R5F11ZBADFP#50

1.3 Pin Configuration (Top View)

1.3.1 24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)



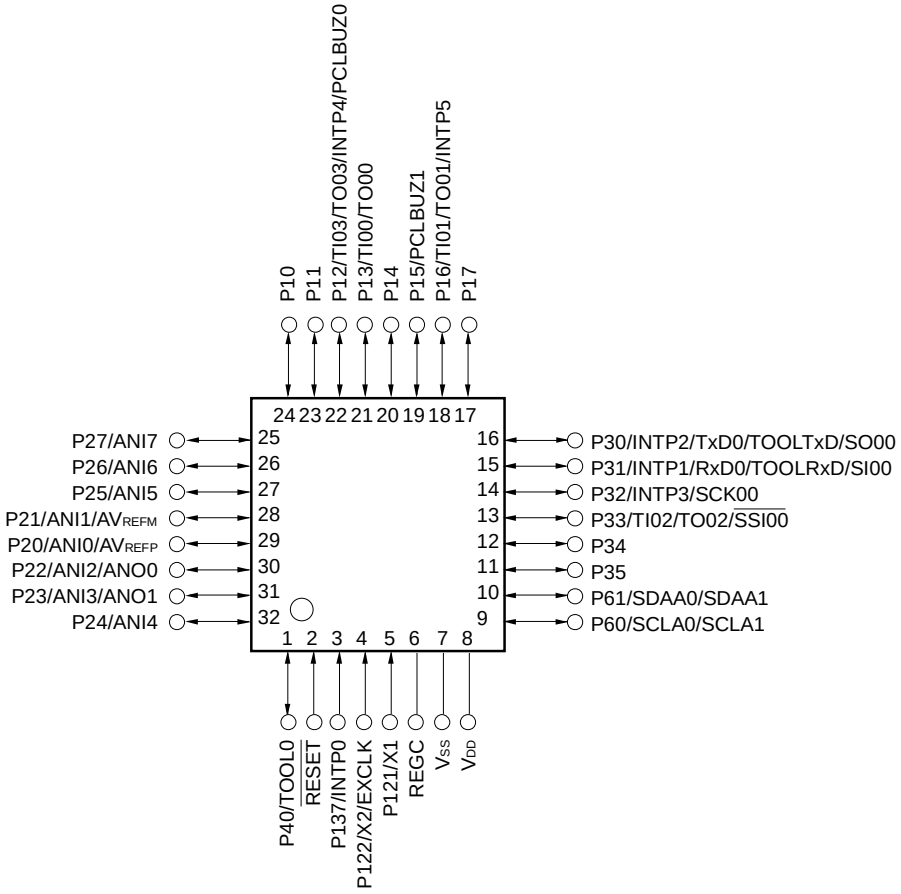
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. It is recommended to connect an exposed die pad to V_{SS}.

1.3.2 32-pin products

- 32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

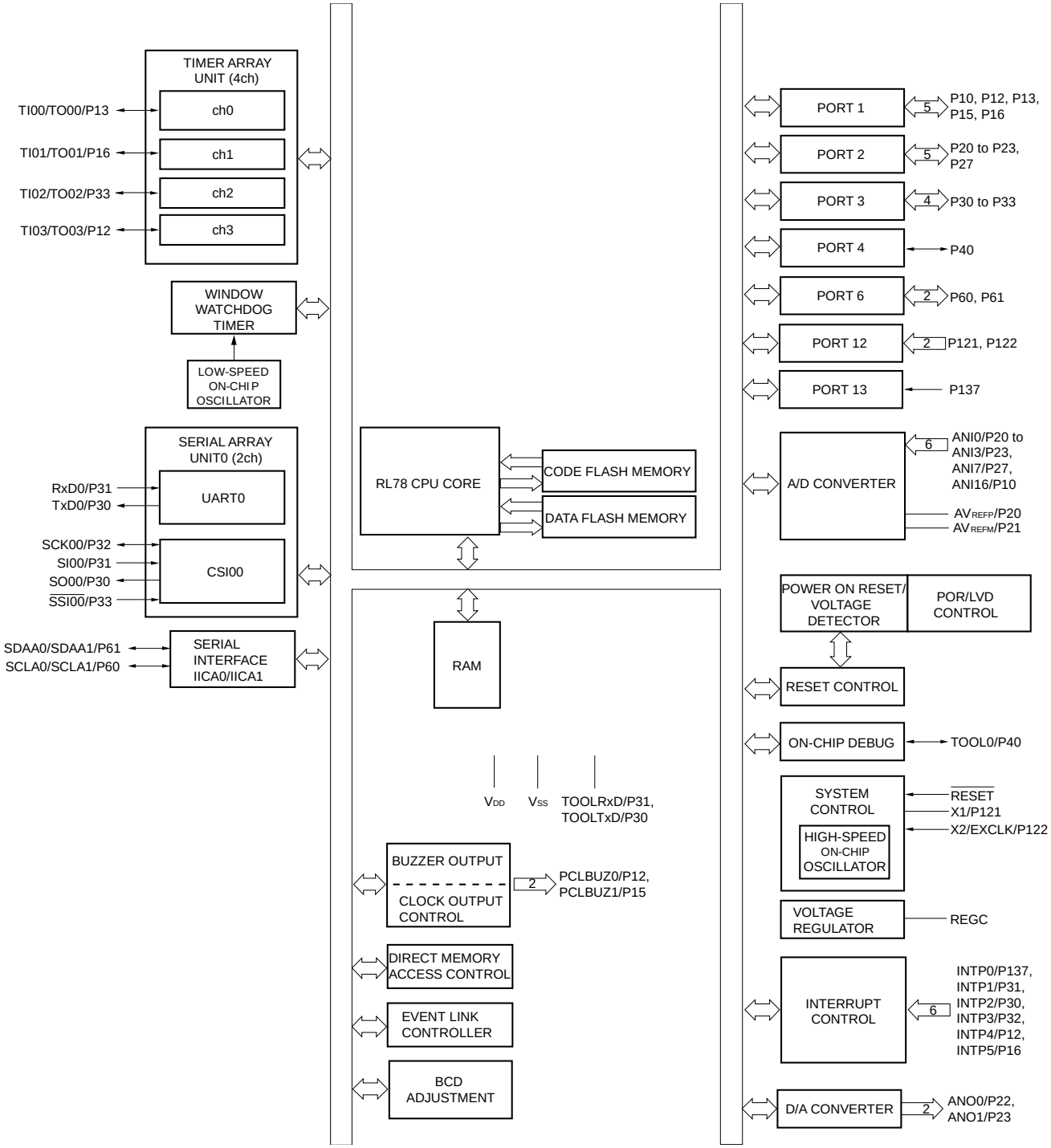
Remark For pin identification, see **1.4 Pin Identification**.

1.4 Pin Identification

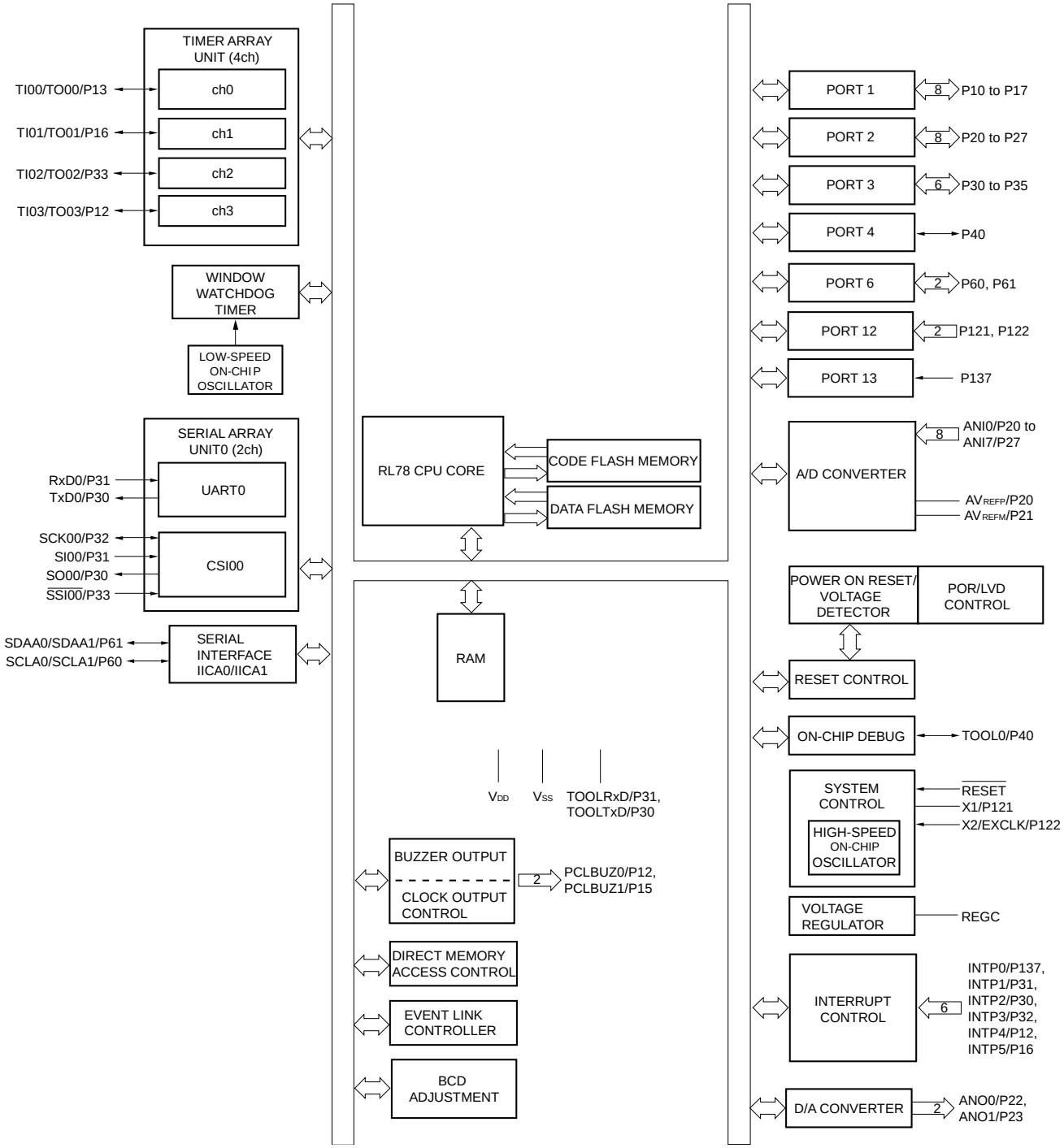
ANI0 to ANI7, ANI16:	Analog input
ANO0, ANO1:	Analog output
AV_{REFM}:	Analog reference voltage minus
AV_{REFP}:	Analog reference voltage plus
EXCLK:	External clock input (main system clock)
INTP0 to INTP5:	External Interrupt Input
P10 to P17:	Port 1
P20 to P27:	Port 2
P30 to P35:	Port 3
P40:	Port 4
P60, P61:	Port 6
P121, P122:	Port 12
P137:	Port 13
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output
REGC:	Regulator capacitance
$\overline{RESET}$:	Reset
RxD0:	Receive data
SCK00:	Serial clock input/output
SCLA0, SCLA1:	Serial clock input/output
SDAA0, SDAA1:	Serial data input/output
SI00:	Serial data input
SO00:	Serial data output
$\overline{SSI00}$:	Serial interface chip select input
TI00 to TI03:	Timer input
TO00 to TO03:	Timer output
TOOL0:	Data input/output for tool
TOOLRxD, TOOLTxD:	Data input/output for external device
TxD0:	Transmit data
V_{DD}:	Power supply
V_{SS}:	Ground
X1, X2:	Crystal oscillator (main system clock)

1.5 Block Diagram

1.5.1 24-pin products



1.5.2 32-pin products



1.6 Outline of Functions

(1/2)

Item		24-pin	32-pin
		R5F11Z7AANA, R5F11Z7ADNA	R5F11ZBAAFP, R5F11ZBADFP
Code flash memory		16 KB	
Data flash memory		2 KB	
RAM		1.5 KB[Note]	
Memory space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V_{DD} = 2.7 to 3.6 V	
	High-speed on-chip oscillator clock (f_{IH})	High-speed operation: 32 MHz (V_{DD} = 2.7 to 3.6 V)	
Low-speed on-chip oscillator clock		15 kHz (TYP.): V_{DD} = 2.7 to 3.6 V	
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)	
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and boolean operation), etc.	
I/O port	Total	20	28
	CMOS I/O	15	23
	CMOS input	3	3
	N-ch O.D I/O (6 V tolerance)	2	2
Timer	16-bit timer	4 channels (TAU)	
	Watchdog timer	1 channel	
	Timer output	4 PWM outputs: 3	
Clock output/buzzer output		2	
		• 2.44 kHz, 4.88 kHz, 9.77 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation)	
8/12-bit resolution A/D converter		6 channels	8 channels
10-bit D/A converter		2 channels	
Serial interface		• CSI: 1 channel/UART: 1 channel	
	I^2C bus	1 channel (2 slave addresses)	
DMA controller		2 channels	
Event link controller (ELC)		Event input: 10, Event trigger output: 3	
Vectored interrupt sources	Internal	12	
	External	6	

Note This is about 0.5 KB when the self-programming function and data flash function are used. For details, see **CHAPTER 3** in the RL78/G1P User's Manual.

(2/2)

Item	24-pin	32-pin
	R5F11Z7AANA, R5F11Z7ADNA	R5F11ZBAAFP, R5F11ZBADFP
Reset	• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution[Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit	• Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V	
Voltage detector	2.75 V to 3.13 V (4 stages)	
On-chip debug function	Provided	
Power supply voltage	V_{DD} = 2.7 to 3.6 V	
Operating ambient temperature	T_A = –40 to +85°C	

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS

Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. See 2.1 Pin Function List to 2.2.1 With functions for each product in the RL78/G1P User's Manual.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +4.6	V
	V_{SS}		−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3 Note 1	V
Input voltage	V_{I1}	P10 to P17, P20 to P27, P30 to P35, P40, P121, P122, P137	−0.3 to V_{DD} +0.3 Note 2	V
	V_{I2}	P60, P61 (N-ch open-drain)	−0.3 to +6.5	V
Output voltage	V_{O1}	P10 to P17, P20 to P27, P30 to P35, P40, P60, P61, P121, P122, P137	−0.3 to V_{DD} +0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI0 to ANI7, ANI16	−0.3 to V_{DD} +0.3 and −0.3 to $AV_{REF(+)}$ +0.3 Notes 2, 3	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 4.6 V or lower.

3. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. V_{SS}: Reference voltage

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P10 to P17, P30 to P35, P40	−40	mA
		Total of all pins −140 mA	P40	−40	mA
			P10 to P17, P30, P35	−100	mA
	I_{OH2}	Per pin	P20 to P27	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P10 to P17, P30 to P35, P40, P60, P61	40	mA
		Total of all pins 140 mA	P40	40	mA
			P10 to P17, P30 to P35, P60, P61	100	mA
	I_{OL2}	Per pin	P20 to P27	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode		0 to +40	
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1 oscillator characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 3.6 V	1.0		20.0	MHz

Note Indicates only oscillator characteristics. See **2.4 AC Characteristics** for instruction execution time.
Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G1P User's Manual.

2.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequencyNotes 1, 2	f_{IH}	32 MHz selected		1		32	MHz
		24 MHz selected		1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	2.7 V ≤ V_{DD} ≤ 3.6 V	-1.0		+1.0	%
		-40 to -20°C	2.7 V ≤ V_{DD} ≤ 3.6 V	-1.5		+1.5	%
Low-speed on-chip oscillator clock frequencyNote 2	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. See **2.4 AC Characteristics** for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) (1/3)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P10 to P17, P30 to P35, P40			–2.0[Note 2]	mA
		Total of P10 to P17, P30 to P35 (When duty ≤ 70%[Note 3])			–19.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])			–21.0	mA
	I_{OH2}	Per pin for P20 to P27			–0.1	mA
		Total of all pins (When duty ≤ 70%[Note 3])			–0.8	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –19.0 mA

Total output current of pins = (–19.0 × 0.7)/(80 × 0.01) = –16.625 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) (2/3)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P10 to P17, P30 to P35, P40			3.0[Note 2]	mA
		Per pin for P60, P61			3.0[Note 2]	mA
		Total of P10 to P17, P30 to P35, P60, P61 (When duty ≤ 70%[Note 3])			35.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])			38.0	mA
	I_{OL2}	Per pin for P20 to P27			0.4	mA
		Total of all pins (When duty ≤ 70%[Note 3])			3.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 35.0 mA

Total output current of pins = (35.0 × 0.7)/(80 × 0.01) = 30.625 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) (3/3)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P30 to P35, P40, P121, P122, P137, EXCLK, $\overline{\text{RESET}}$			0.8V_{DD}		V_{DD}	V
	V_{IH2}	P20 to P27			0.7V_{DD}		V_{DD}	V
	V_{IH3}	P60, P61			0.7V_{DD}		6.0	V
Input voltage, low	V_{IL1}	P10 to P17, P30 to P35, P40, P121, P122, P137, EXCLK, $\overline{\text{RESET}}$			0		0.2V_{DD}	V
	V_{IL2}	P20 to P27, P60, P61			0		0.3V_{DD}	V
Output voltage, high	V_{OH1}	P10 to P17, P30 to P35, P40	I_{OH1} = –2.0 mA		V_{DD} – 0.6			V
	V_{OH2}	P20 to P27	I_{OH1} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P10 to P17, P30 to P35, P40	I_{OL1} = 3.0 mA				0.6	V
			I_{OL1} = 1.5 mA				0.4	V
	V_{OL2}	P20 to P27	I_{OL2} = 400 μA				0.4	V
	V_{OL3}	P60, P61	I_{OL3} = 3.0 mA				0.4	V
Input leakage current, high	I_{LIH1}	P10 to P17, P20 to P27, P30 to P35, P40, P137, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P121, P122 (X1, X2, EXCLK)	$V_I = V_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P10 to P17, P20 to P27, P30 to P35, P40, P137, $\overline{\text{RESET}}$	$V_I = V_{SS}$				–1	μA
	I_{LIL2}	P121, P122 (X1, X2, EXCLK)	$V_I = V_{SS}$	In input port or external clock input			–1	μA
				In resonator connection			–10	μA
On-chip pull-up resistance	R_U	P10 to P17, P30 to P35, P40	$V_I = V_{SS}$, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) (1/3)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} Note 1	Operating mode	HS (high-speed main) mode Note 4	f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 3.0 V		2.1		mA
					Normal operation	V_{DD} = 3.0 V		4.8	7.0	mA
				f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 3.0 V		3.8	5.5	mA
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 3.0 V		2.8	4.0	mA
			LS (low-speed main) mode Note 4	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	2.0	mA
			HS (high-speed main) mode Note 4	f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.3	4.6	mA
						Resonator connection		3.5	4.8	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.0	2.7	mA
						Resonator connection		2.1	2.7	
			LS (low-speed main) mode Note 4	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator is stopped.

3. When high-speed system clock is stopped.

4. Relationship between operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: @1 MHz to 32 MHz

LS (low-speed main) mode: @1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) (2/3)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}[Note 2]	HALT mode	HS (high-speed main) mode[Note 6]	f_{IH} = 32 MHz[Note 4]	V_{DD} = 3.0 V		0.60	1.63	mA
				f_{IH} = 24 MHz[Note 4]	V_{DD} = 3.0 V		0.49	1.28	mA
				f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V		0.45	1.00	mA
			LS (low-speed main) mode[Note 6]	f_{IH} = 8 MHz[Note 4]	V_{DD} = 3.0 V		320	530	μA
			HS (high-speed main) mode[Note 6]	f_{MX} = 20 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.49	1.17	mA
				f_{MX} = 10 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.30	0.67	mA
			LS (low-speed main) mode[Note 6]	f_{MX} = 8 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	
	I_{DD3}[Note 5]	STOP mode	T_A = –40°C				0.18		μA
			T_A = +25°C				0.23	0.50	
			T_A = +50°C				0.26	1.10	
			T_A = +70°C				0.29	1.90	
			T_A = +85°C				0.90	3.30	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator is stopped.

4. When high-speed system clock is stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.

6. Relationship between operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: @1 MHz to 32 MHz

LS (low-speed main) mode: @1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. Except STOP mode, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) (3/3)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Watchdog timer operating current	I_{WDT} Notes 1, 2, 3	f_{IL} = 15 kHz		0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 4	V_{DD} = 3.0 V, When conversion at maximum speed		0.58	0.82	mA
A/D converter reference voltage current	I_{ADREF} Note 1			75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1			75.0		μA
D/A converter operating current	I_{DAC} Notes 1, 5				2	mA
LVD operating current	I_{LVI} Notes 1, 6			0.08		μA
Self-programming operating current	I_{FSP} Notes 1, 8			2.50	12.20	mA
BGO operating current	I_{BGO} Notes 1, 7			2.50	12.20	mA

Notes 1. Current flowing to V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the watchdog timer (including the operating current of the 15 kHz low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

4. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

5. Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{DAC} when the D/A converter operates in an operation mode or the HALT mode.

6. Current flowing only to the LVD circuit. The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

7. Current flowing during programming of the data flash.

8. Current flowing during self-programming.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{CLK}: CPU/peripheral hardware clock frequency

3. Temperature condition of the TYP. value is T_A = 25°C

2.4 AC Characteristics

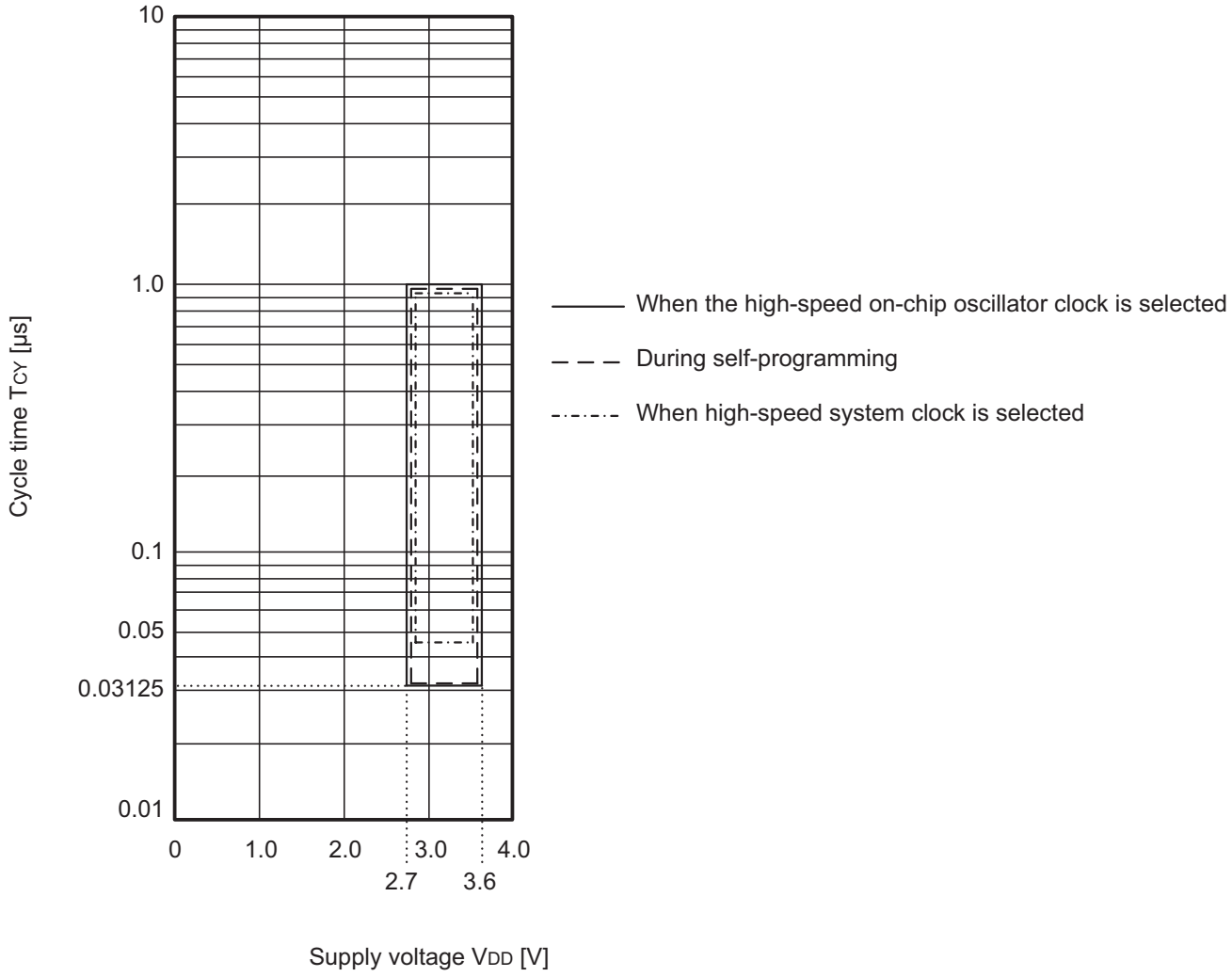
(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	0.03125		1	μs
			LS (low-speed main) mode	0.125		1	μs
		In the self-programming mode	HS (high-speed main) mode	0.03125		1	μs
			LS (low-speed main) mode	0.125		1	μs
External system clock frequency	f_{EX}			1.0		20.0	MHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}			24			ns
TI00 to TI03 input high-level width, low-level width	t_{TIH}, t_{TIL}			1/f_{MCK}+10			ns
TO00 to TO03 output frequency	f_{TO}	HS (high-speed main) mode				8	MHz
		LS (low-speed main) mode				4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode				8	MHz
		LS (low-speed main) mode				4	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP5		1			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

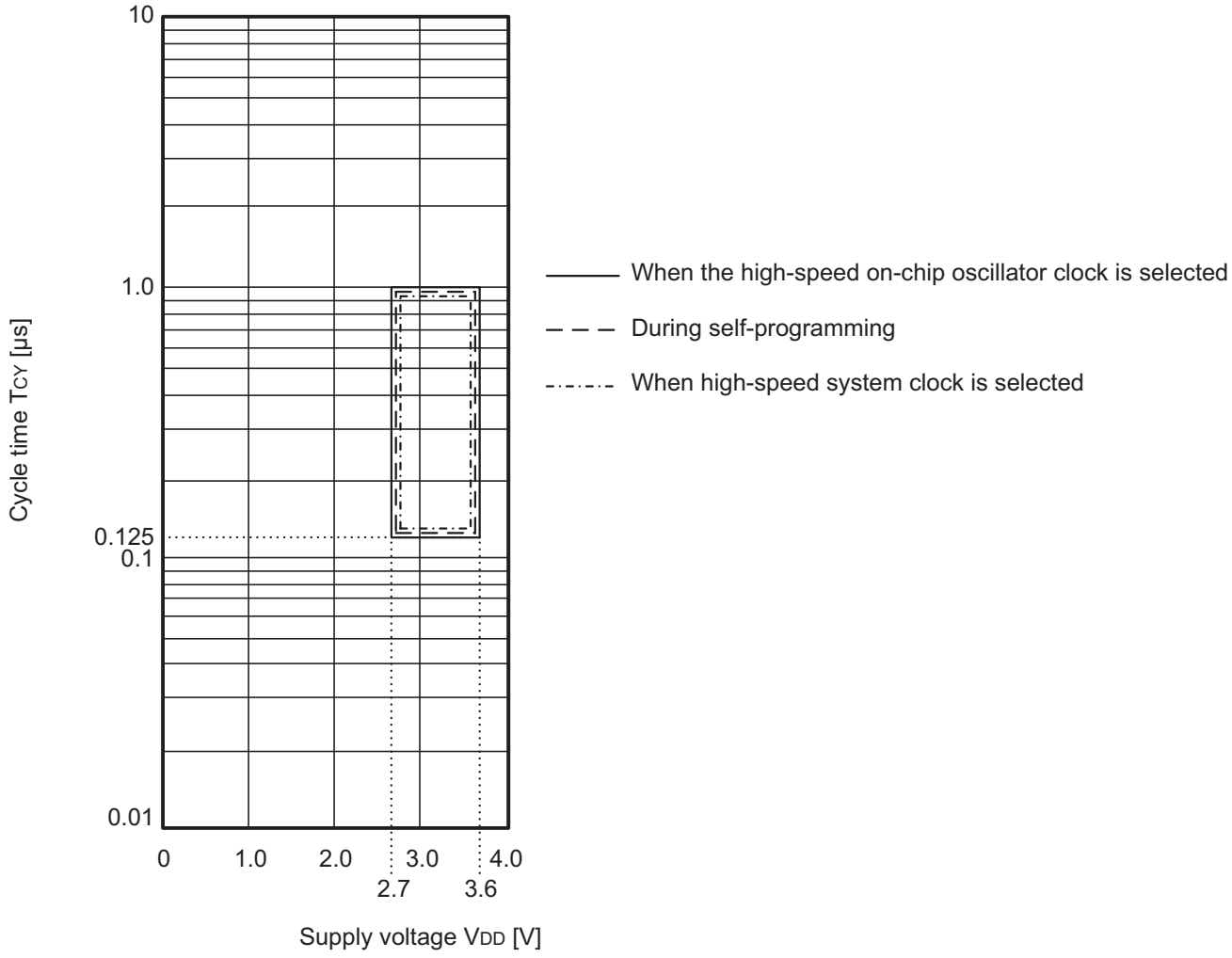
Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn0 and CKSmn1 bits of timer mode register mn (TMRmn).
m: Unit number (m = 0), n: Channel number (n = 0 to 3))

Minimum Instruction Execution Time during Main System Clock Operation

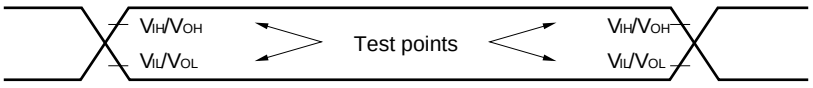
TCY vs V_{DD} (HS (high-speed main) mode)



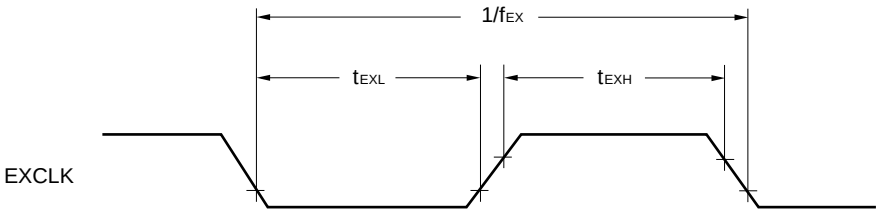
TCY vs V_{DD} (LS (low-speed main) mode)



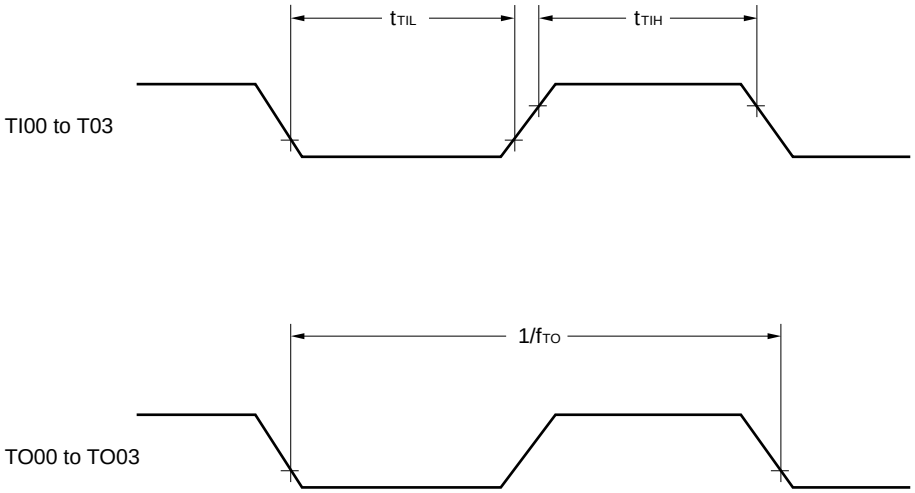
AC Timing Test Points



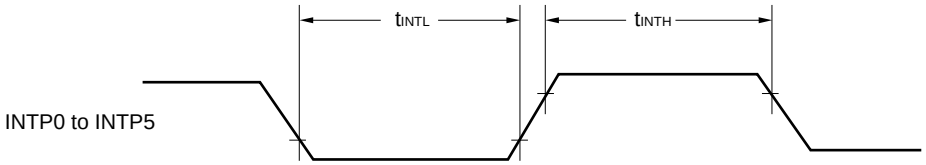
External System Clock Timing



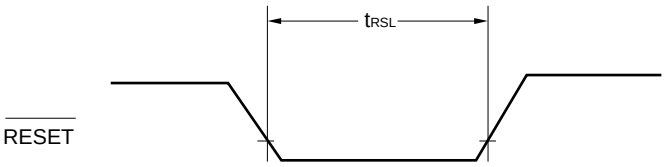
TI/TO Timing



Interrupt Request Input Timing

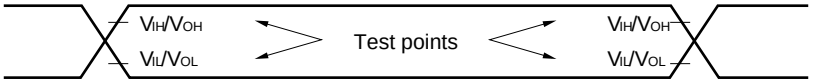


$\overline{\text{RESET}}$ Input Timing



2.5 Peripheral Functions Characteristics

AC Timing Test Points



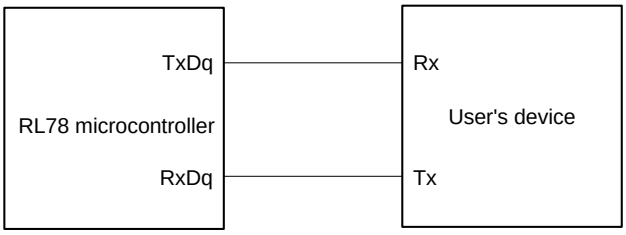
2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

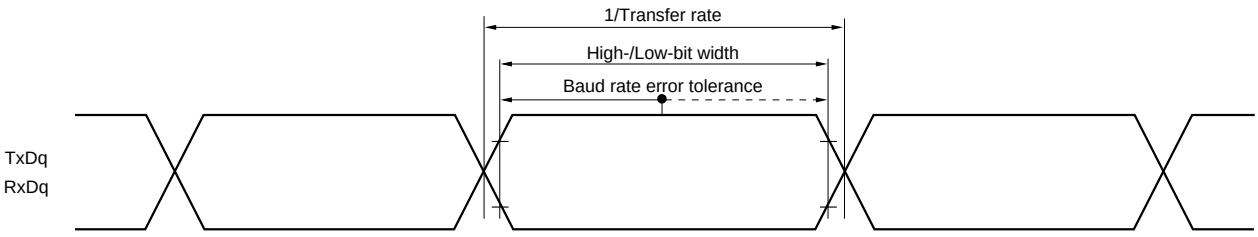
(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	TYP.	MIN.	MAX.	
Transfer rate[Note 1]		2.7 V ≤ V_{DD} ≤ 3.6 V		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 2]		5.3		1.3	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 3.6 V)
LS (low-speed main) mode: 8 MHz (2.7 V ≤ V_{DD} ≤ 3.6 V).

Remarks 1. q: UART number (q = 0)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}		83.3		250		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}		t_{KCY1}/2 - 10		t_{KCY1}/2 - 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}		33		110		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}		10		10		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO1}	C = 20 pF Note 3		10		10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" and the SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCKp cycle time[Note 4]	t_{KCY2}	16 MHz < f_{MCK}	8/f_{MCK}		-		ns
		f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}		t_{KCY2}/2-8		t_{KCY2}/2-8		ns
SIp setup time (to SCKp↑)[Note 1]	t_{SIK2}		1/f_{MCK}+20		1/f_{MCK}+30		ns
SIp hold time (from SCKp↑)[Note 1]	t_{KSI2}		1/f_{MCK}+31		1/f_{MCK}+31		ns
Delay time from SCKp↓ to SOp output[Note 2]	t_{KSO2}	C = 30 pF[Note 3]		2/f_{MCK}+44		2/f_{MCK}+110	ns
$\overline{SSI00}$ setup time	t_{SSIK}	DAPmn = 0	120		120		ns
		DAPmn = 1	1/f_{MCK}+120		1/f_{MCK}+120		ns
$\overline{SSI00}$ hold time	t_{KSSI}	DAPmn = 0	1/f_{MCK}+120		1/f_{MCK}+120		ns
		DAPmn = 1	120		120		ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" and the SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

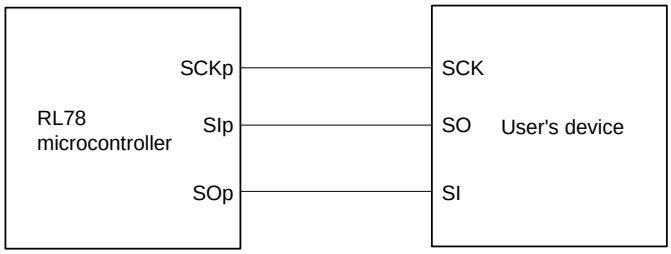
3. C is the load capacitance of the SOp output lines.

4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

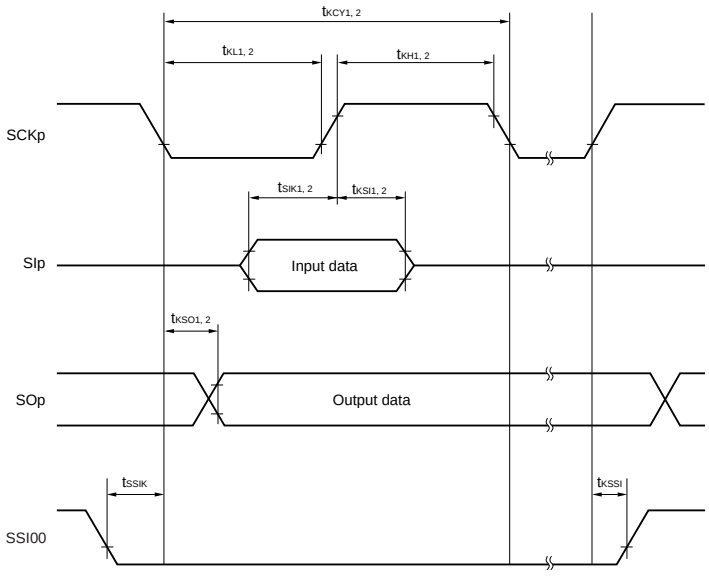
Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

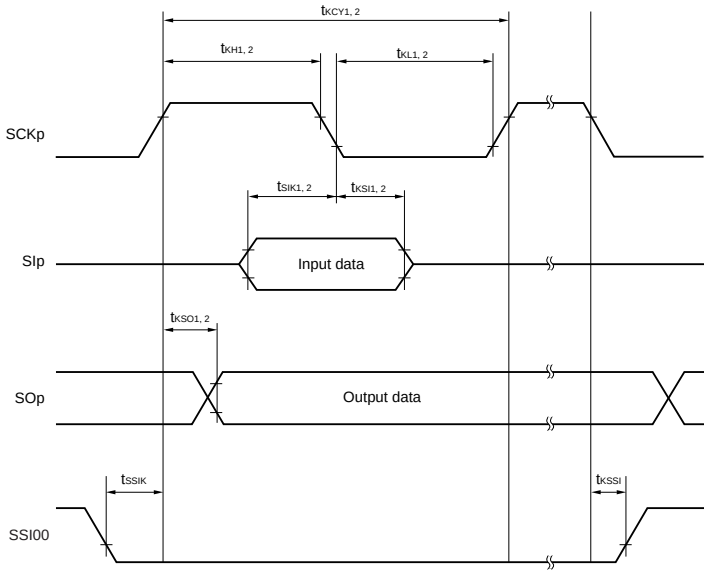
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00)

2. m: Unit number, n: Channel number (mn = 00)

2.5.2 Serial interface IICA

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Fast Mode Plus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLAn clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz					0	1000	kHz
		Fast mode: f_{CLK} ≥ 3.5 MHz			0	400			kHz
		Normal mode: f_{CLK} ≥ 1 MHz	0	100					kHz
Setup time of restart condition	$t_{SU:STA}$		4.7		0.6		0.26		μs
Hold time[Note 1]	$t_{HD:STA}$		4.0		0.6		0.26		μs
Hold time when SCLAn = “L”	t_{LOW}		4.7		1.3		0.5		μs
Hold time when SCLAn = “H”	t_{HIGH}		4.0		0.6		0.26		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		50		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	3.45	0	0.9	0	0.45	μs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		0.26		μs
Bus-free time	t_{BUF}		4.7		1.3		0.5		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remarks 1. The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

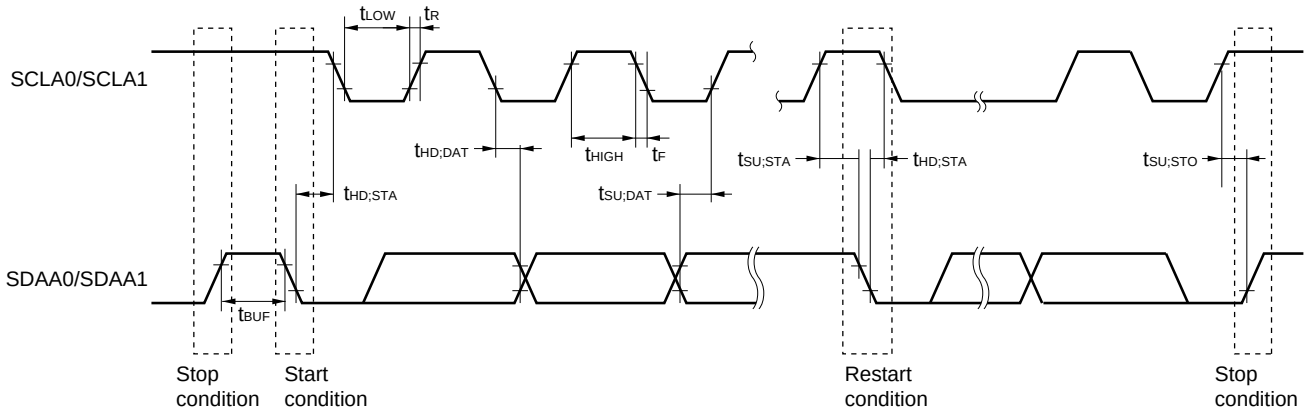
Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

2. n = 0, 1

IICA serial transfer timing



2.5.3 Dedicated Flash Memory Programmer Communication (UART)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate			115.2 k		1 M	bps

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage / Input channel	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (-) = AV_{REFM}.
ANI0 to ANI7	Refer to **2.6.1 (1)**	Refer to **2.6.1 (2)**	Refer to **2.6.1 (5)**
ANI16	Refer to **2.6.1 (3)**	Refer to **2.6.1 (4)**	
Internal reference voltage Temperature sensor output voltage	Refer to **2.6.1 (3)**	Refer to **2.6.1 (4)**	–

(1) When $AV_{REF(+)}$ = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF(-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin: ANI0 to ANI7

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		12	bit
Overall error[Note 1]	AINL	12-bit resolution AV_{REFP} = V_{DD}			±6.0	LSB
Conversion time	t_{CONV}	12-bit resolution AV_{REFP} = V_{DD}	3.375		108	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	12-bit resolution AV_{REFP} = V_{DD}			±0.10	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	12-bit resolution AV_{REFP} = V_{DD}			±0.10	%FSR
Integral linearity error[Note 1]	ILE	12-bit resolution AV_{REFP} = V_{DD}			±2.5	LSB
Differential linearity error[Note 1]	DLE	12-bit resolution AV_{REFP} = V_{DD}			±1.5	LSB
Reference voltage (+)	AV_{REFP}		2.7		V_{DD}	V
Reference voltage (–)	AV_{REFM}		–0.5		0.3	V
Analog input voltage	V_{AIN}		0		AV_{REFP}	V
	V_{BGR}	Select internal reference voltage output 2.7 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode	1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(2) When $AV_{REF(+)} = V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), $AV_{REF(-)} = V_{SS}$ (ADREFM = 0), target ANI pin: ANI0 to ANI7

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, Reference voltage (+) = V_{SS}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		12	bit
Overall error[Note 1]	AINL	10-bit resolution			±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution	3.375		108	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution			±0.60	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution			±4.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution			±2.0	LSB
Analog input voltage	V_{AIN}		0		AV_{REFP}	V
	V_{BGR}	Select internal reference voltage output 2.7 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode	1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(3) When $AV_{REF(+)} = AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF(-)} = AV_{REFM}$/ANI1 (ADREFM = 1), target ANI pin: ANI16, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM}= 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		12	bit
Overall error[Note 1]	AINL	12-bit resolution $AV_{REFP} = V_{DD}$			±7.0	LSB
Conversion time	t_{CONV}	12-bit resolution $AV_{REFP} = V_{DD}$	4.125		132	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	12-bit resolution $AV_{REFP} = V_{DD}$			±0.10	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	12-bit resolution $AV_{REFP} = V_{DD}$			±0.10	%FSR
Integral linearity error[Note 1]	ILE	12-bit resolution $AV_{REFP} = V_{DD}$			±3.0	LSB
Differential linearity error[Note 1]	DLE	12-bit resolution $AV_{REFP} = V_{DD}$			±2.0	LSB
Reference voltage (+)	AV_{REFP}		2.7		V_{DD}	V
Reference voltage (–)	AV_{REFM}		–0.5		0.3	V
Analog input voltage	V_{AIN}		0		AV_{REFP}	V
	V_{BGR}	Select internal reference voltage output 2.7 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode	1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(4) When $AV_{REF(+)} = V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), $AV_{REF(-)} = V_{SS}$ (ADREFM = 0), target ANI pin: ANI16, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		12	bit
Overall error[Note 1]	AINL	10-bit resolution			±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution	4.125		132	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution			±0.60	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution			±4.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution			±2.5	LSB
Analog input voltage	V_{AIN}		0		V_{DD}	V
	V_{BGR}	Select internal reference voltage output 2.7 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode	1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(5) When $AV_{REF(+)}$ = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), $AV_{REF(-)} = AV_{REFM}$/ANI1 (ADREFM = 1), target ANI pin: ANI0 to ANI7, ANI16

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, Reference voltage (+) = V_{BGR}, Reference voltage (–) = AV_{REFM} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8			bit
Conversion time	t_{CONV}	8-bit resolution	16		108	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	8-bit resolution			±1.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution			±2.5	LSB
Differential linearity error[Note 1]	DLE	8-bit resolution			±2.5	LSB
Analog input voltage	V_{AIN}		0		V_{BGR}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

2.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

2.6.3 D/A converter

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

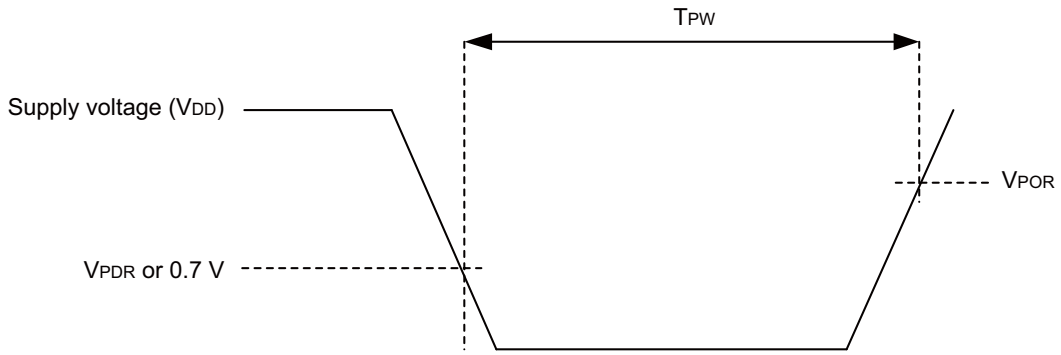
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				10	bit
Overall error	AINL	Load current = 0 mA, 0.2 V ≤ output voltage ≤ V_{DD} – 0.2 V		±2.0	±4.0	LSB
		Load = 2.5 kΩ, 0.2 V ≤ output voltage ≤ V_{DD} – 0.2 V		±5.0	±10.0	LSB
Settling time	t_{SET}	Rload = 47 kΩ, Cload = 20 pF			10	μs
D/A output resistance	R_O	Per channel Output voltage = 0 V to 0.2 V or Output voltage = V_{DD} – 0.2 V to V_{DD}		40	60	Ω
		Per channel Output voltage = 0.2 V to V_{DD} – 0.2 V		8	12	Ω

2.6.4 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width Note	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.5 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq$ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
		Power supply fall time	3.00	3.06	3.12	V
	V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
		Power supply fall time	2.90	2.96	3.02	V
	V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
		Power supply fall time	2.80	2.86	2.91	V
	V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
		Power supply fall time	2.70	2.75	2.81	V
Minimum pulse width	t_{LW}		300			μs
Detection delay time					300	μs

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq$ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVD5}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V_{LVD4}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVD3}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V

2.6.6 Power supply voltage rising slope characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

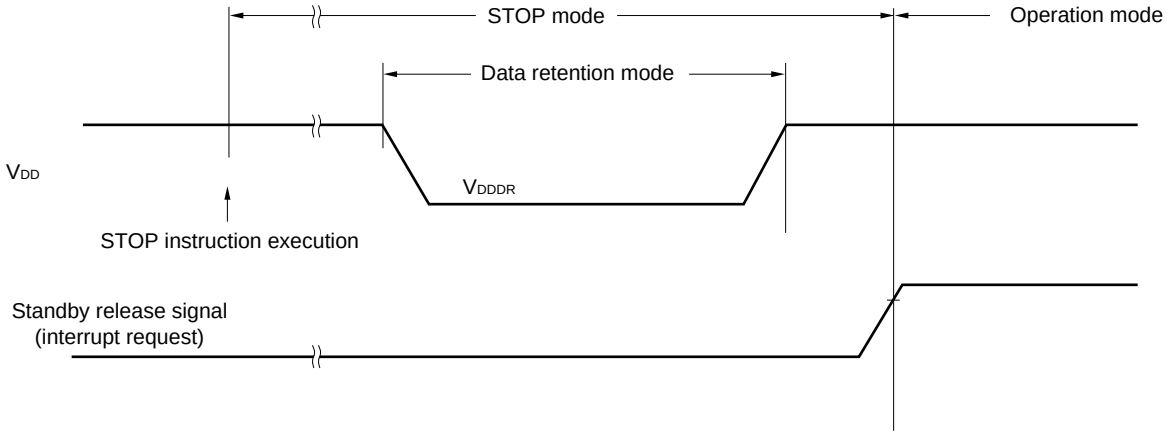
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

2.7 RAM data retention characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46[Note]		3.6	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



2.8 Flash Memory Programming Characteristics

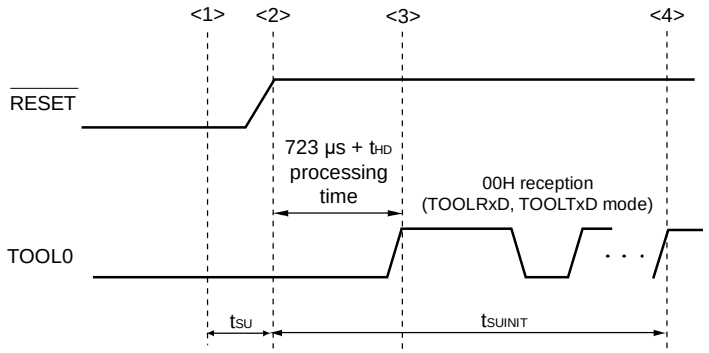
(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	2.7 V ≤ V_{DD} ≤ 3.6 V	1		32	MHz
Number of code flash rewrites Note 1, 2, 3	C_{erwr}	Retained for 20 years T_A = 85°C	1,000			Times
Number of data flash rewrites Note 1, 2, 3		Retained for 1 years T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C	100,000			
Operating ambient temperature		In flash memory programming mode	0 to +40			°C
		In the self-programming mode	–40 to +85			°C

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.
2. When using flash memory programmer and Renesas Electronics self programming library
3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Timing of Entry to Flash Memory Programming Modes

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

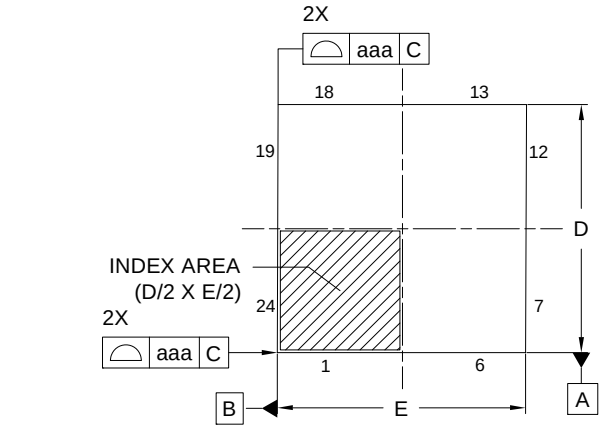
Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until an external reset ends (MIN. 10 μs)
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except software processing time)

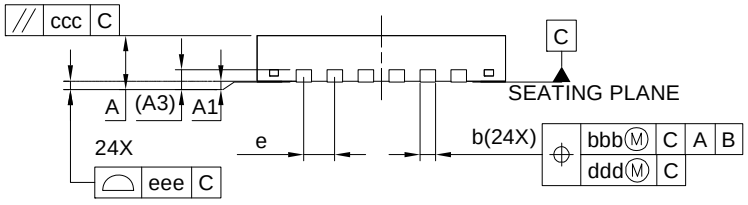
3. PACKAGE DRAWINGS

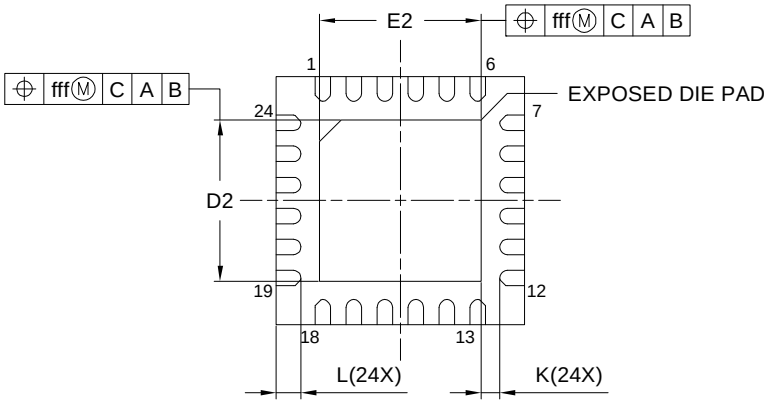
3.1 24-pin Products

R5F11Z7AANA, R5F11Z7ADNA

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN024-4x4-0.50	PWQN0024KF-A	0.04



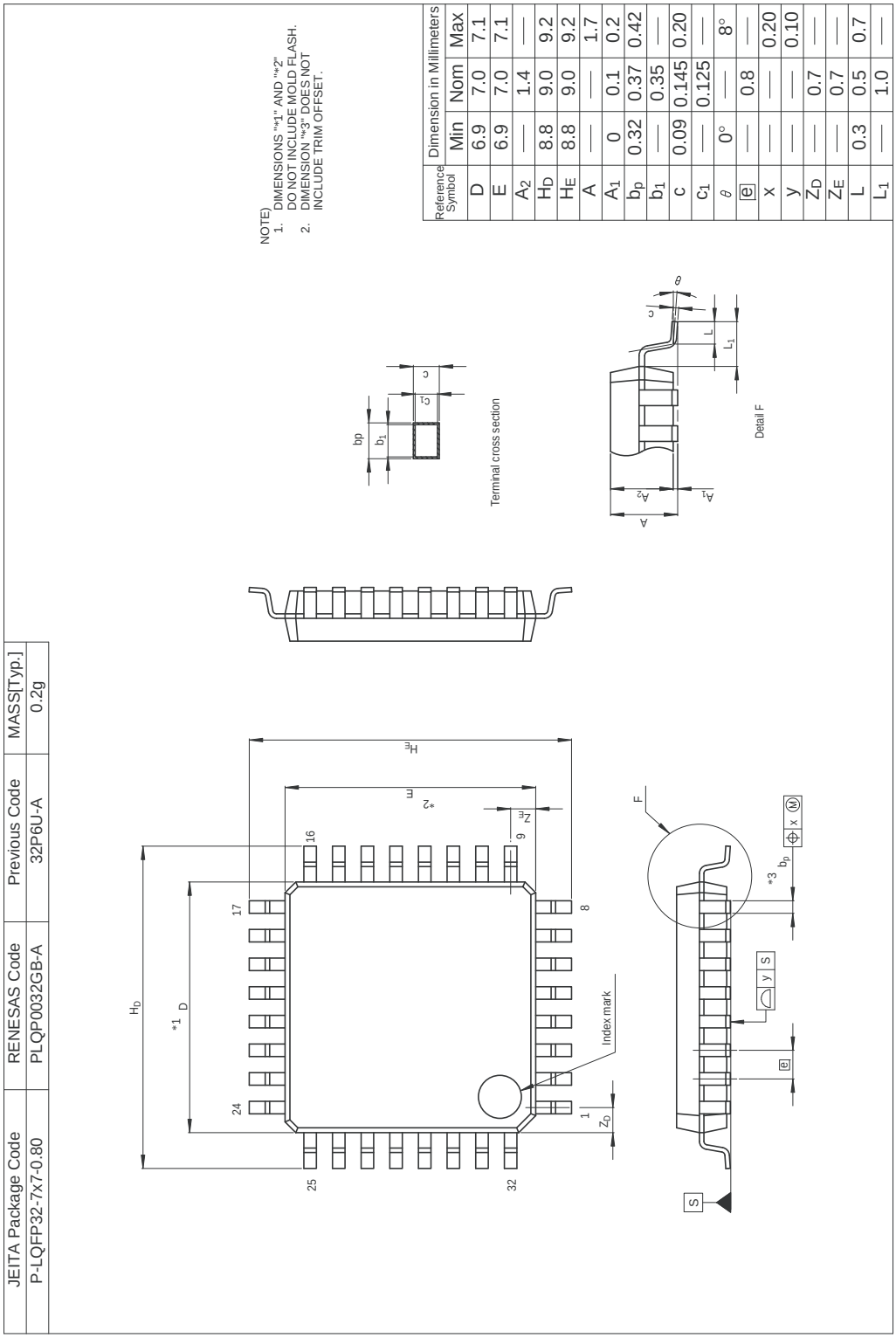




Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.18	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	–	–
D2	2.55	2.60	2.65
E2	2.55	2.60	2.65
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

3.2 32-pin Products

R5F11ZBAAFP, R5F11ZBADFP



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g

Revision History	RL78/G1P Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Nov 29, 2019	—	First edition issued

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The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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