

RL78/G1C

RENESAS MCU

R01DS0348EJ0120

Rev.1.20

Sep 30, 2016

Integrated USB Controller, True Low Power Platform (as low as 112.5 $\mu\text{A}/\text{MHz}$, and 0.61 μA for RTC + LVD), 2.4 V to 5.5 V Operation, 32 Kbyte Flash, 31 DMIPS at 24 MHz, for All USB Based Applications

1. OUTLINE

1.1 Features

Ultra-Low Power Technology

- 2.4 V to 5.5 V operation from a single supply
- Stop (RAM retained): 0.23 μA , (LVD enabled): 0.31 μA
- Halt (RTC + LVD): 0.57 μA
- Supports snooze
- Operating: 71 $\mu\text{A}/\text{MHz}$

16-bit RL78 CPU Core

- Delivers 31 DMIPS at maximum operating frequency of 24 MHz
- Instruction Execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC Architecture (Harvard) with 3-stage pipeline
- Multiply Signed & Unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

Code Flash Memory

- Density: 32 KB
- Block size: 1 KB
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with secure boot swap function and flash shield window function

Data Flash Memory

- Data Flash with background operation
- Data flash size: 2 KB
- Erase Cycles: 1 Million (typ.)
- Erase/programming voltage: 2.4 V to 5.5 V

RAM

- 5.5 KB size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator

- 24 MHz with $\pm 1\%$ accuracy over voltage (2.4 V to 5.5 V) and temperature (-20°C to $+85^\circ\text{C}$)
- Pre-configured settings: 48 MHz, 24 MHz (TYP.)

Reset and Supply Management

- Power-on reset (POR) monitor/generator
- Low voltage detection (LVD) with 9 setting options (Interrupt and/or reset function)

USB

- Complying with USB version 2.0, incorporating host/function controller
- Corresponding to full-speed transfer (12 Mbps) and low-speed (1.5 Mbps)
- Complying with Battery Charging Specification Revision 1.2
- Compliant with the 2.1A/1.0A charging mode prescribed in the Apple Inc. MFi specification in the USB power supply component specification ^{Note}

Direct Memory Access (DMA) Controller

- Up to 2 fully programmable channels
- Transfer unit: 8- or 16-bit

Multiple Communication Interfaces

- Up to 2 x I²C master
- Up to 1 x I²C multi-master
- Up to 2 x CSI (7-, 8-bit)
- Up to 1 x UART (7-, 8-, 9-bit)

Extended-Function Timers

- Multi-function 16-bit timer TAU: Up to 4 channels (remote control output available)
- Real-time clock (RTC): 1 channel (full calendar and alarm function with watch correction function)
- 12-bit interval timer: 1 channel
- 15 kHz watchdog timer: 1 channel (window function)

Rich Analog

- ADC: Up to 9 channels, 8/10-bit resolution, 2.1 μs minimum conversion time
- Internal voltage reference (1.45 V)
- On-chip temperature sensor

Safety Features (IEC or UL 60730 compliance)

- Flash memory CRC calculation
- RAM parity error check
- RAM write protection
- SFR write protection
- Illegal memory access detection
- Clock stop/frequency detection
- ADC self-test
- I/O port read back function (echo)

General Purpose I/O

- 5 V tolerant, high-current (up to 20 mA per pin)
- Open-Drain, Internal Pull-up support

Operating Ambient Temperature

- Standard: -40°C to $+85^\circ\text{C}$
- Extended: -40°C to $+105^\circ\text{C}$

Package Type and Pin Count

- 32-pin plastic HWQFN (5 x 5)
- 32-pin plastic LQFP (7 x 7)
- 48-pin plastic LFQFP (7 x 7)
- 48-pin plastic HWQFN (7 x 7)

Note To use the Apple Inc. battery charging mode, you must join in Apple's Made for iPod/iPhone/iPad (MFi) licensing program. Before requesting this specification from Renesas Electronics, please join in the Apple's MFi licensing program.

ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G1C	
			32-pin	48-pin
32 KB	2 KB	5.5 KB ^{Note}	R5F10JBC, R5F10KBC	R5F10JGC, R5F10KGC

Note This is about 4.5 KB when the self-programming function is used.

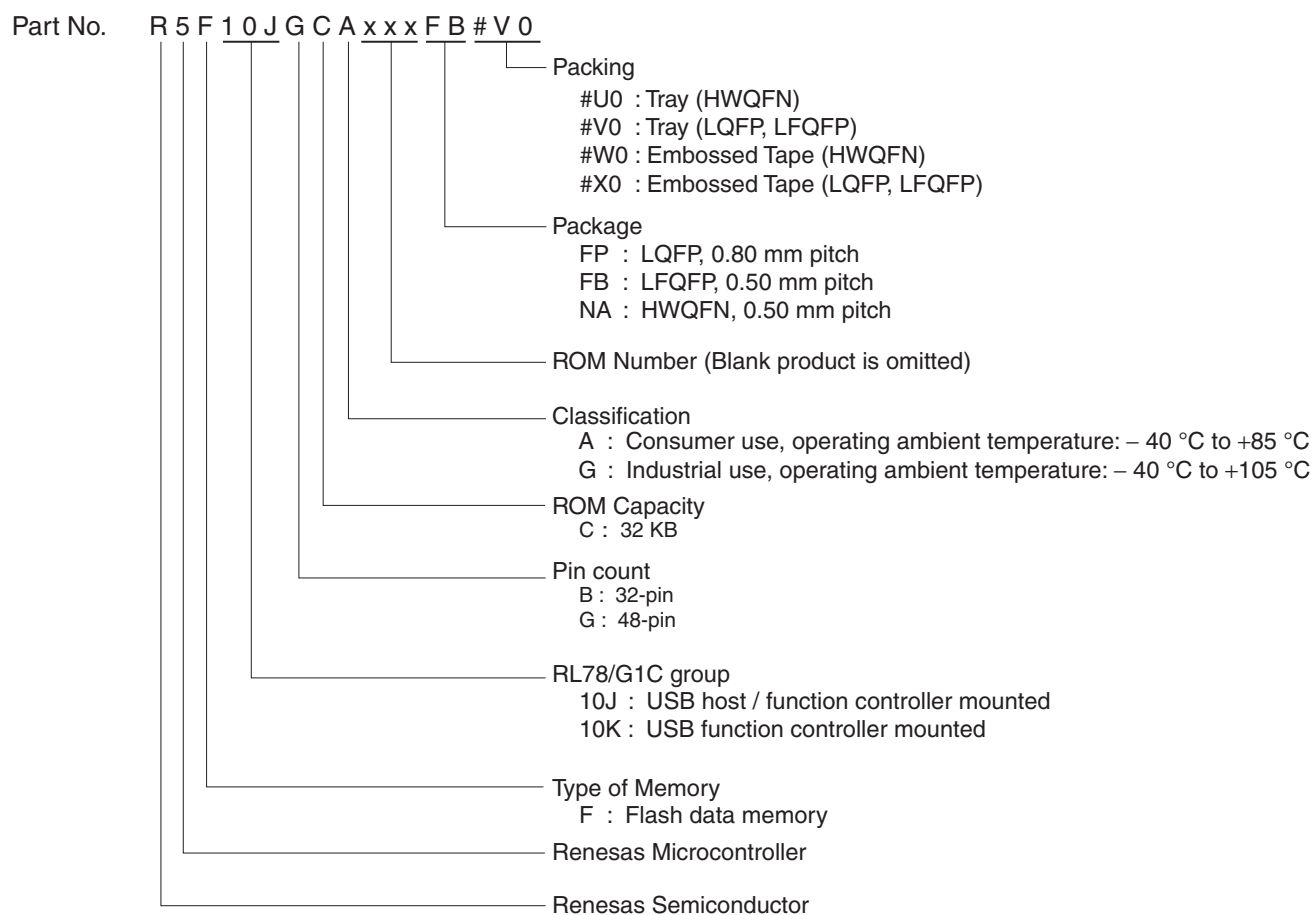
Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

1.2 List of Part Numbers

Pin count	Package	USB Function	Fields of Application ^{Note}	Part Number
32 pins	32-pin plastic HWQFN (5 × 5 , 0.5 mm pitch)	Host/Function controller	A	R5F10JBCANA#U0, R5F10JBCANA#W0
			G	R5F10JBCGNA#U0, R5F10JBCGNA#W0
		Function controller only	A	R5F10KBCANA#U0, R5F10KBCANA#W0
			G	R5F10KBCGNA#U0, R5F10KBCGNA#W0
	32-pin plastic LQFP (7 × 7 , 0.8 mm pitch)	Host/Function controller	A	R5F10JBCAFP#V0, R5F10JBCAFP#X0
			G	R5F10JBCGFP#V0, R5F10JBCGFP#X0
		Function controller only	A	R5F10KBCAFP#V0, R5F10KBCAFP#X0
			G	R5F10KBCGFP#V0, R5F10KBCGFP#X0
48 pins	48-pin plastic LFQFP (7 × 7 , 0.5 mm pitch)	Host/Function controller	A	R5F10JGCAFB#V0, R5F10JGCAFB#X0
			G	R5F10JGCGFB#V0, R5F10JGCGFB#X0
		Function controller only	A	R5F10KGCAFB#V0, R5F10KGCAFB#X0s
			G	R5F10JGCANA#U0, R5F10JGCANA#W0
	48-pin plastic HWQFN (7 × 7 , 0.5 mm pitch)	Host/Function controller	A	R5F10JGCANA#U0, R5F10JGCANA#W0
			G	R5F10JGCGNA#U0, R5F10JGCGNA#W0
		Function controller only	A	R5F10KGCANA#U0, R5F10KGCANA#W0
			G	R5F10KGCGNA#U0, R5F10KGCGNA#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G1C**.

Caution The part number above is valid as of when this manual was issued. For the latest part number, see the web page of the target product on the Renesas Electronics website.

Figure 1-1. Part Number, Memory Size, and Package of RL78/G1C

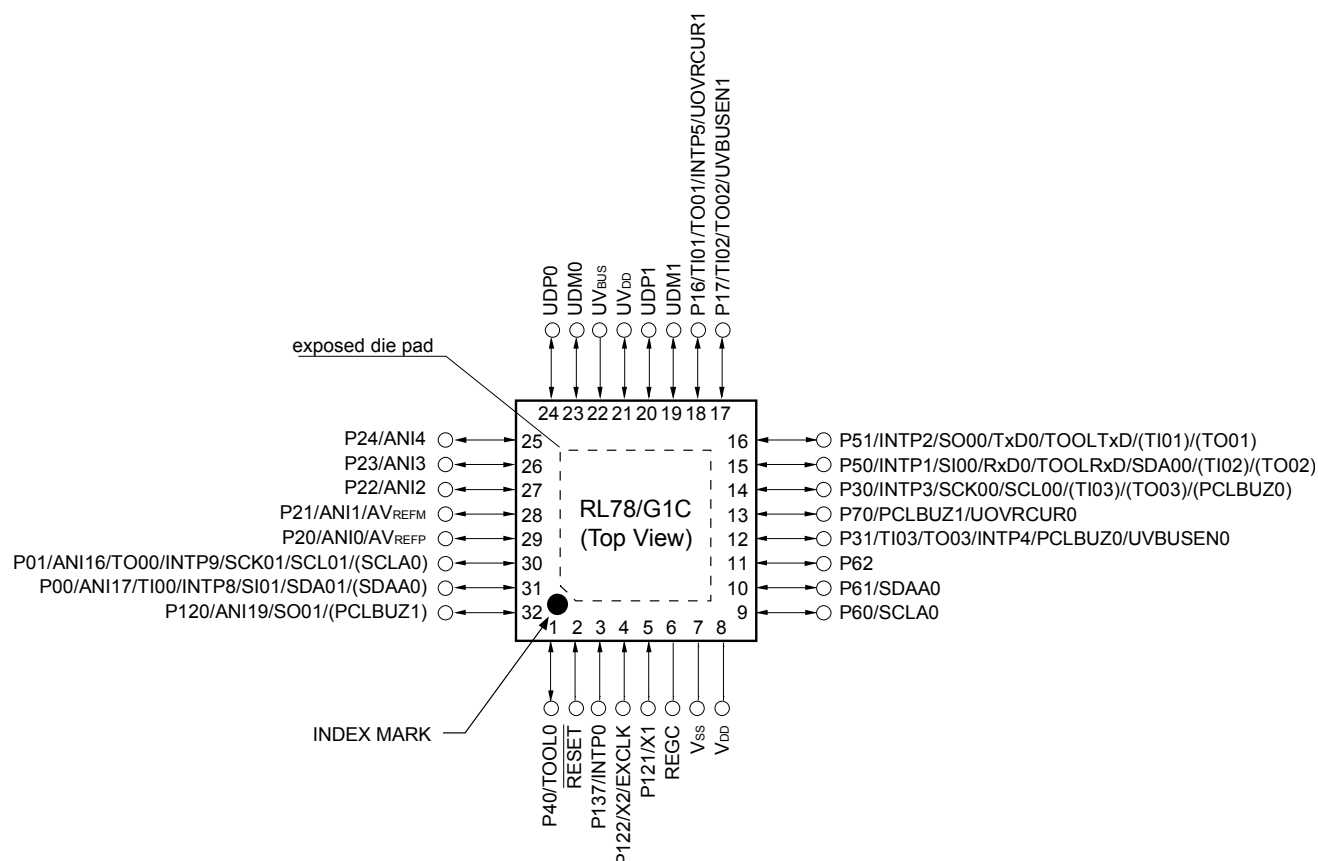
1.3 Pin Configuration (Top View)

1.3.1 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)

(1) USB function: Host/Function controller (R5F10JBC)

<R>



Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

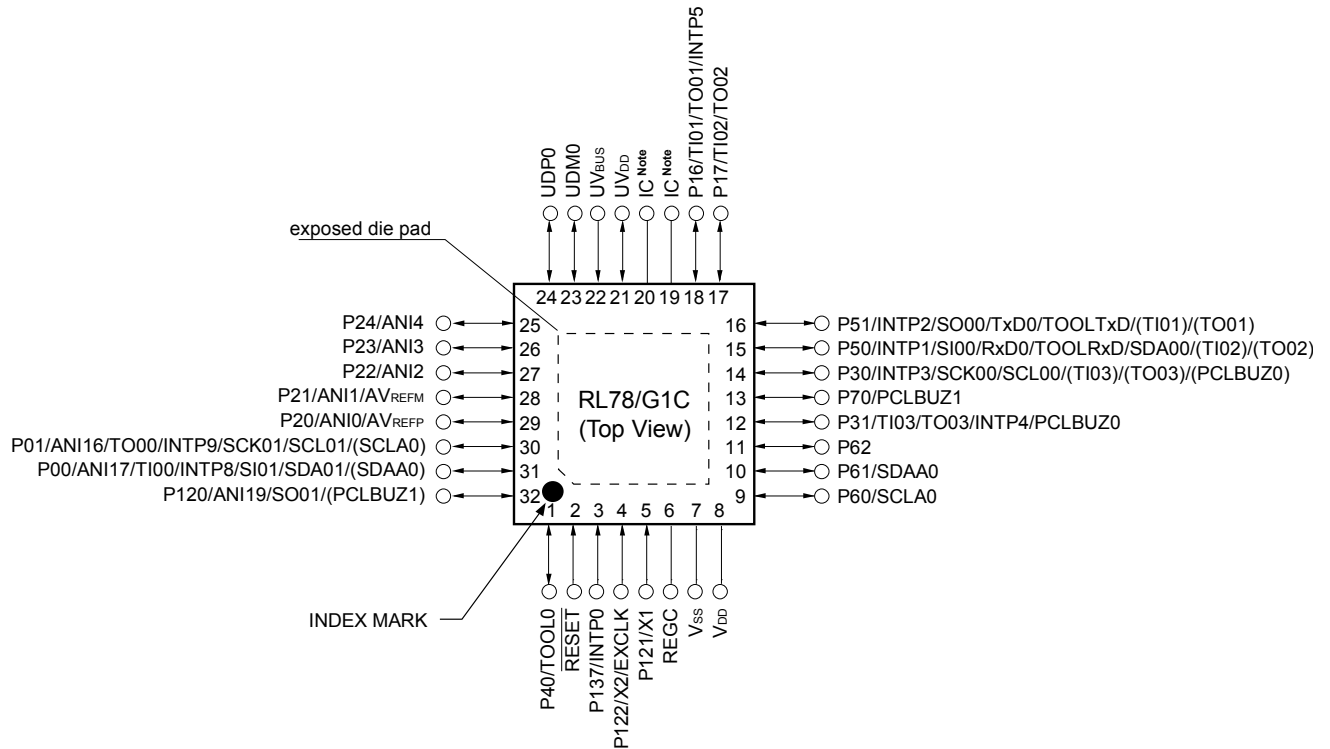
Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

3. It is recommended to connect an exposed die pad to V_{SS}.

(2) USB function: Function controller only (R5F10KBC)

<R>



Note IC: Internal Connection Pin. Leave open.

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

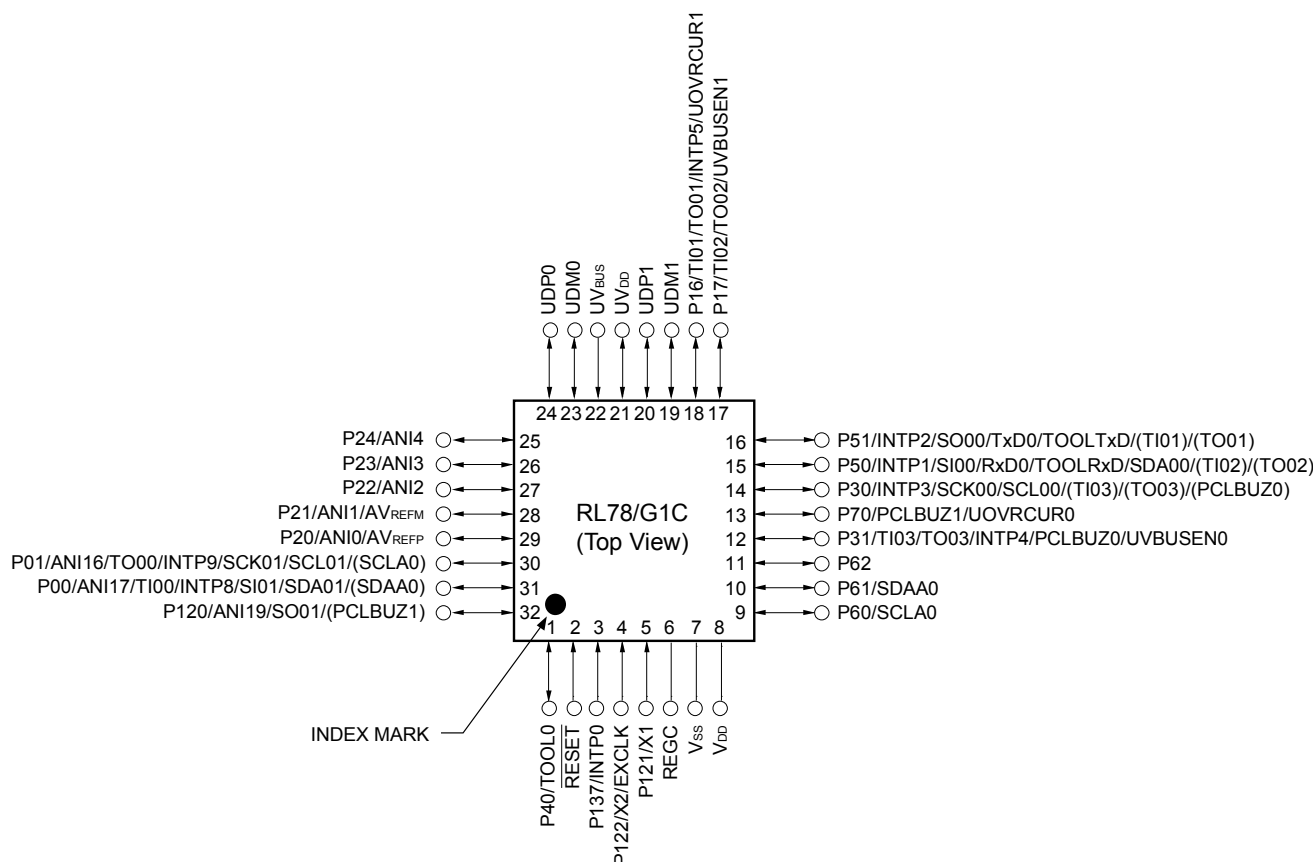
Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).
3. It is recommended to connect an exposed die pad to Vss.

- 32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)

(1) USB function: Host/Function controller (R5F10JBC)

<R>



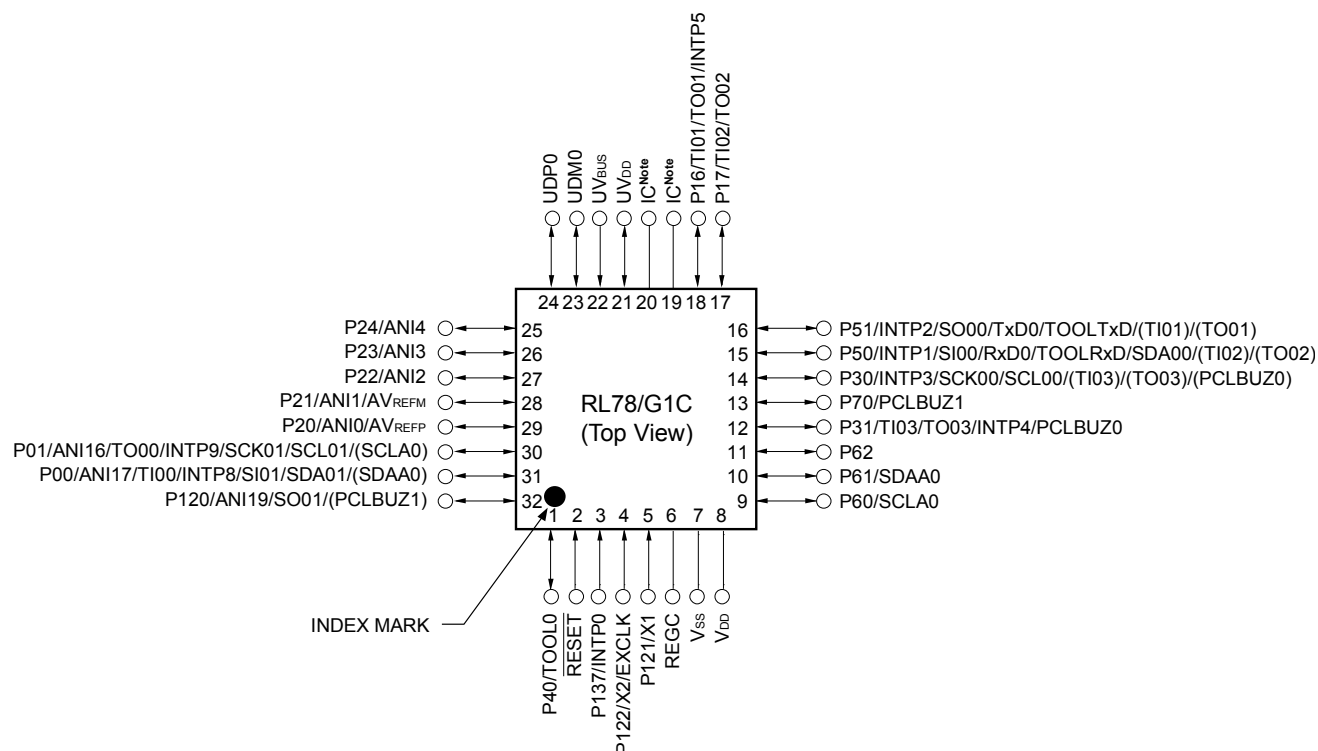
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

(2) USB function: Function controller only (R5F10KBC)

<R>



Note IC: Internal Connection Pin Leave open.

Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

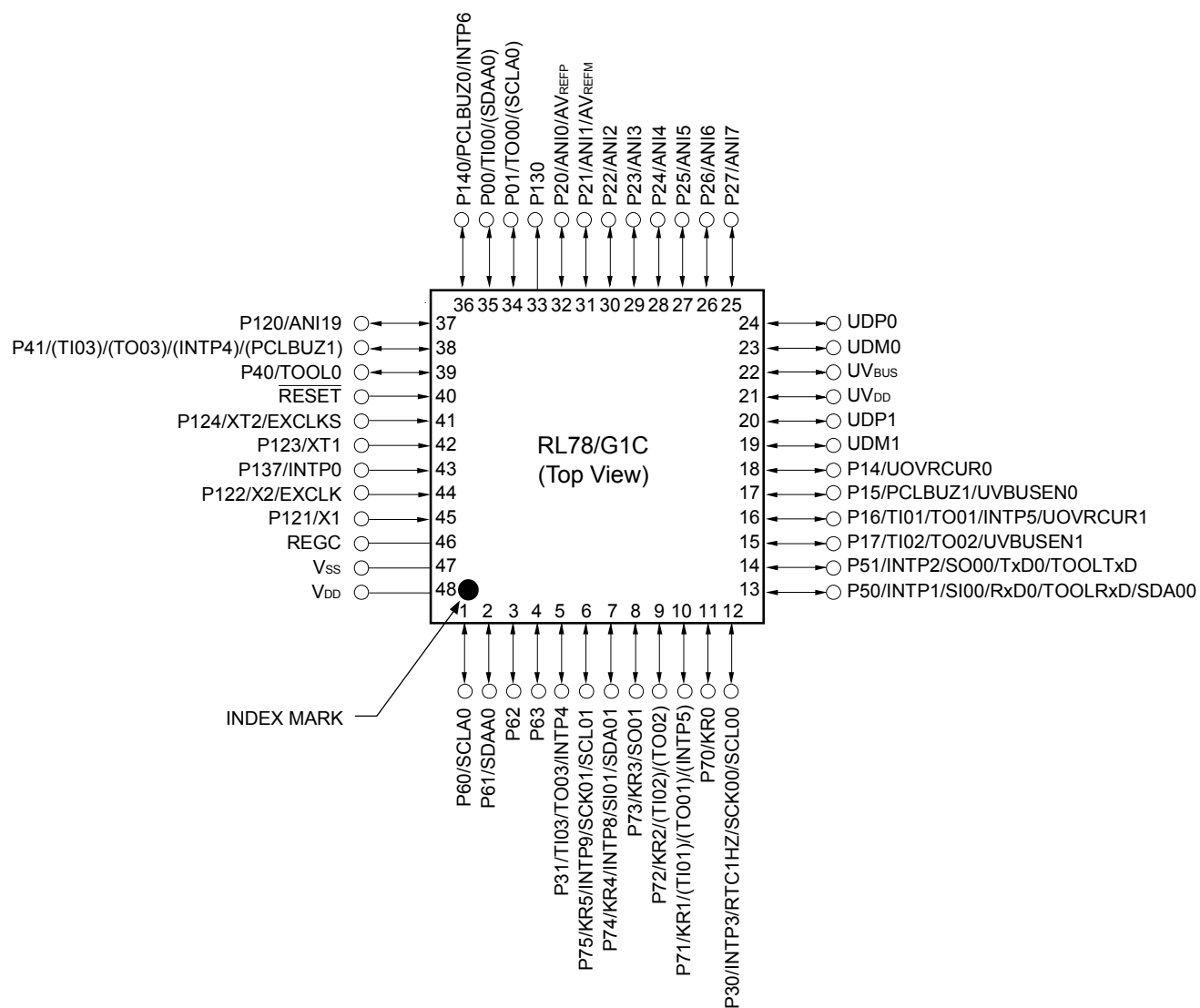
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.2 48-pin products

- 48-pin plastic LFQFP (fine pitch) (7 × 7, 0.5 mm pitch)

(1) USB function: Host/Function controller (R5F10JGC)

<R>



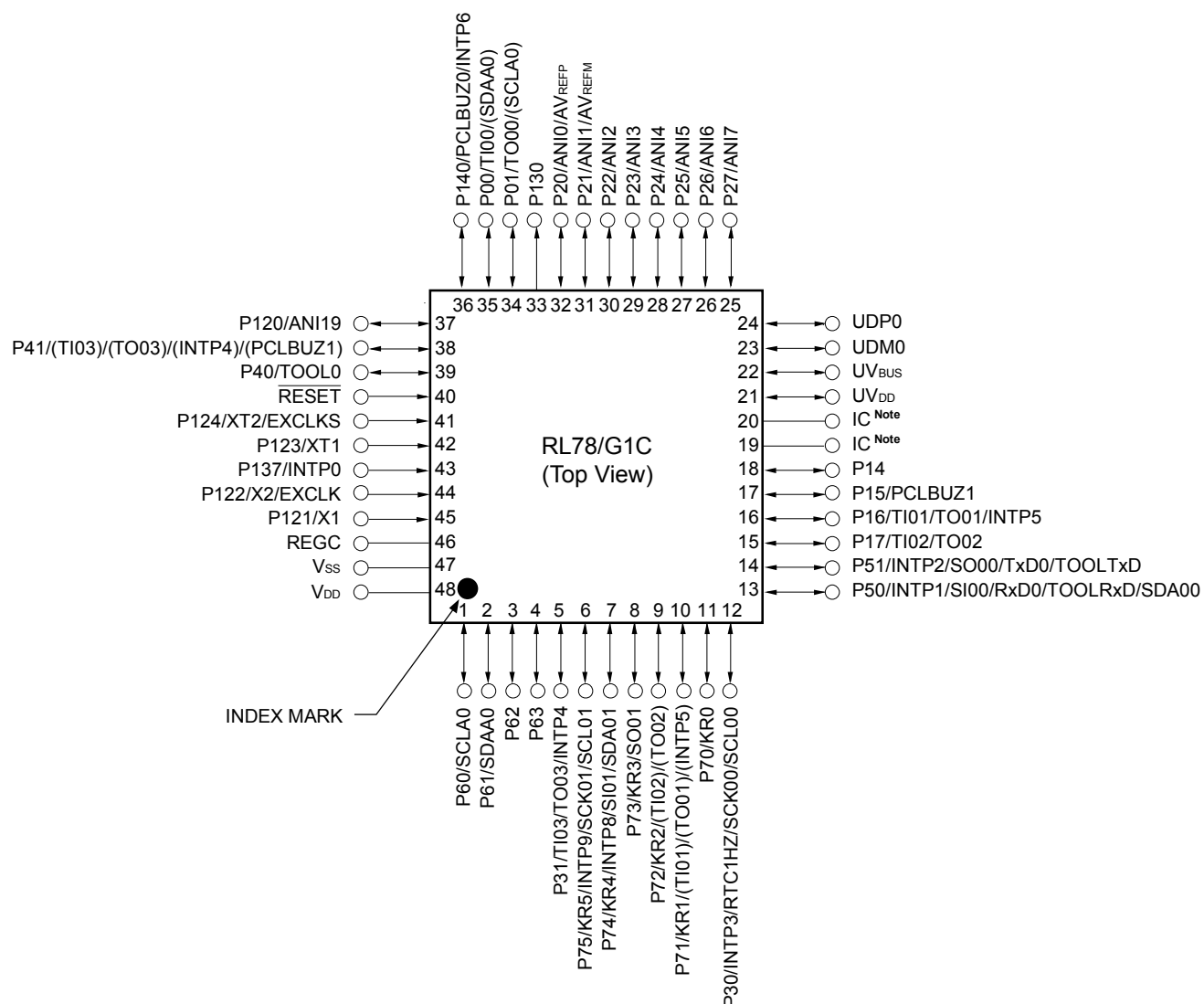
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

(2) USB function: Function controller only (R5F10KGC)

<R>



Note IC: Internal Connection Pin Leave open.

Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

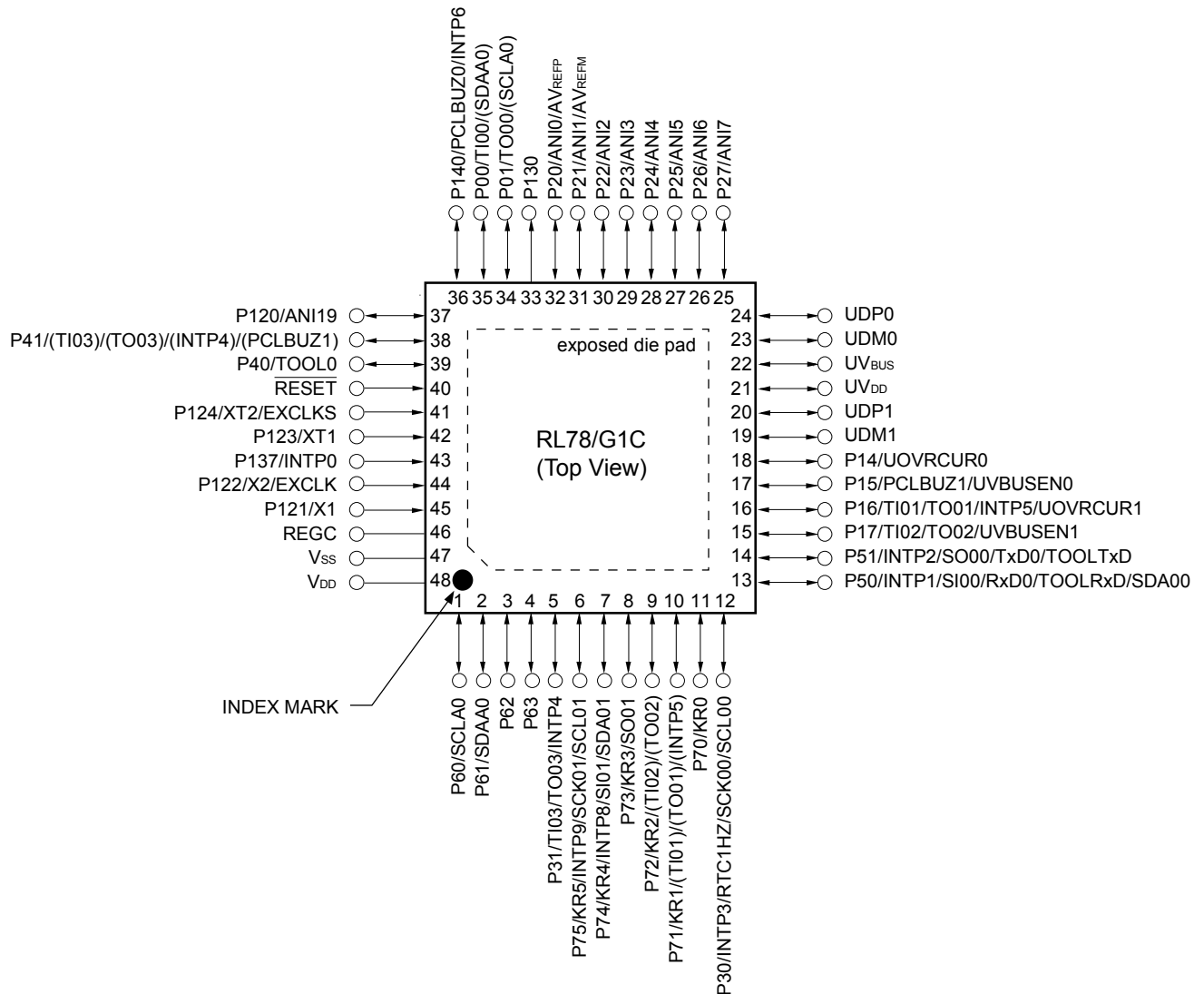
Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 48-pin plastic WHQFN (7 × 7, 0.5 mm pitch)

(1) USB function: Host/Function controller (R5F10JGC)

<R>



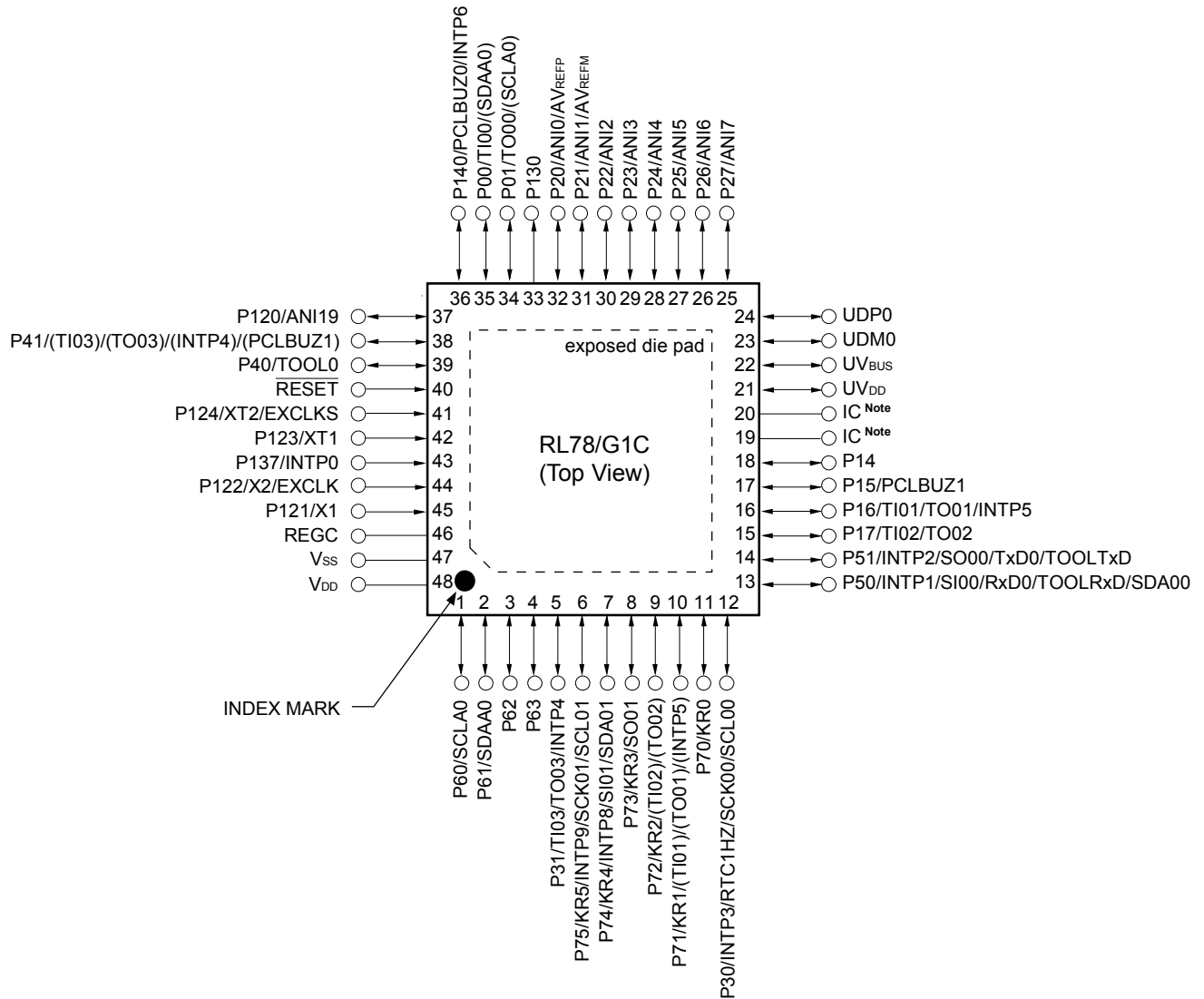
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).
3. It is recommended to connect an exposed die pad to V_{SS}.

(2) USB function: Function controller only (R5F10KGC)

<R>



Note IC: Internal Connection Pin Leave open.

Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

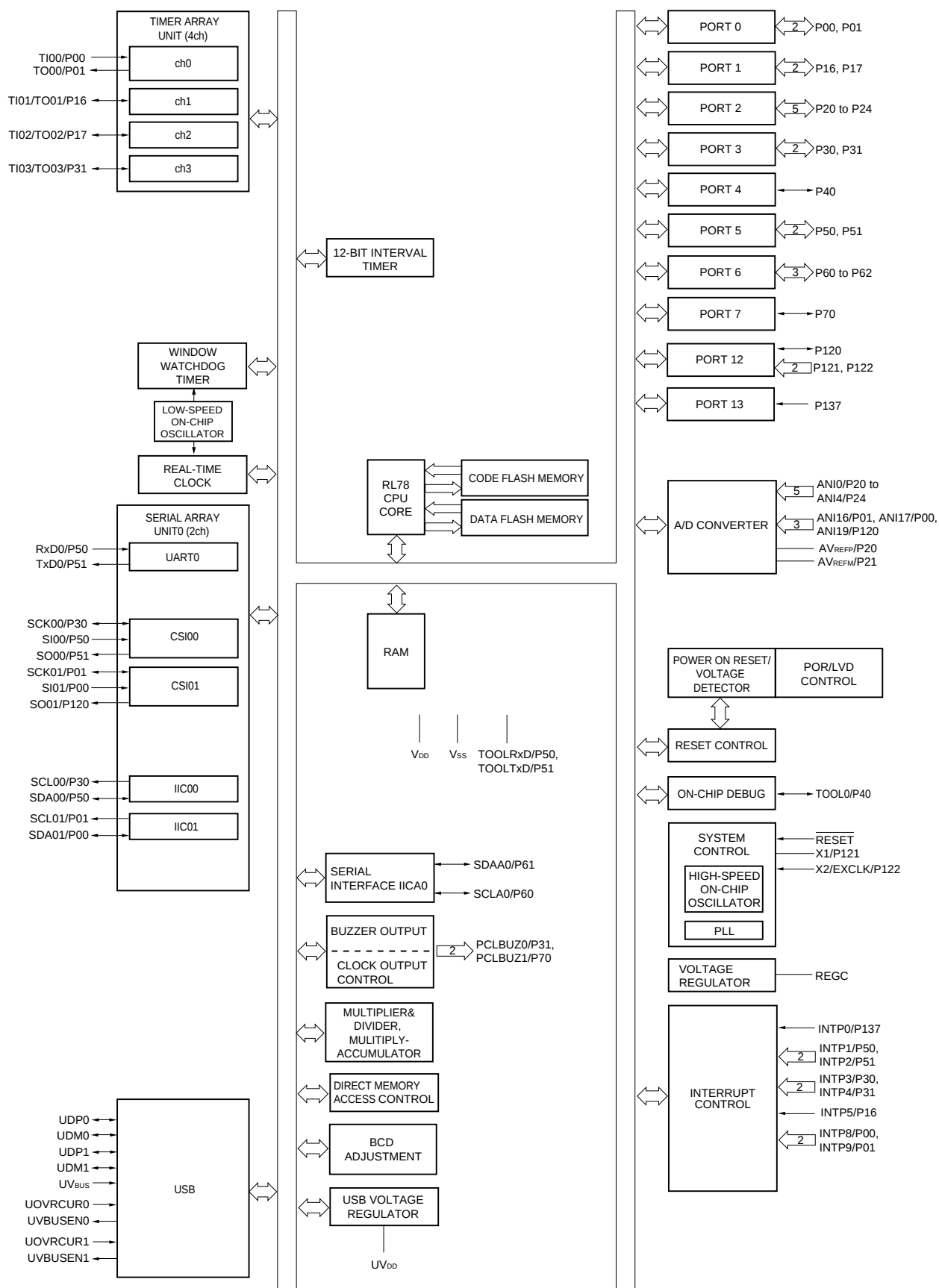
3. It is recommended to connect an exposed die pad to V_{SS}.

1.4 Pin Identification

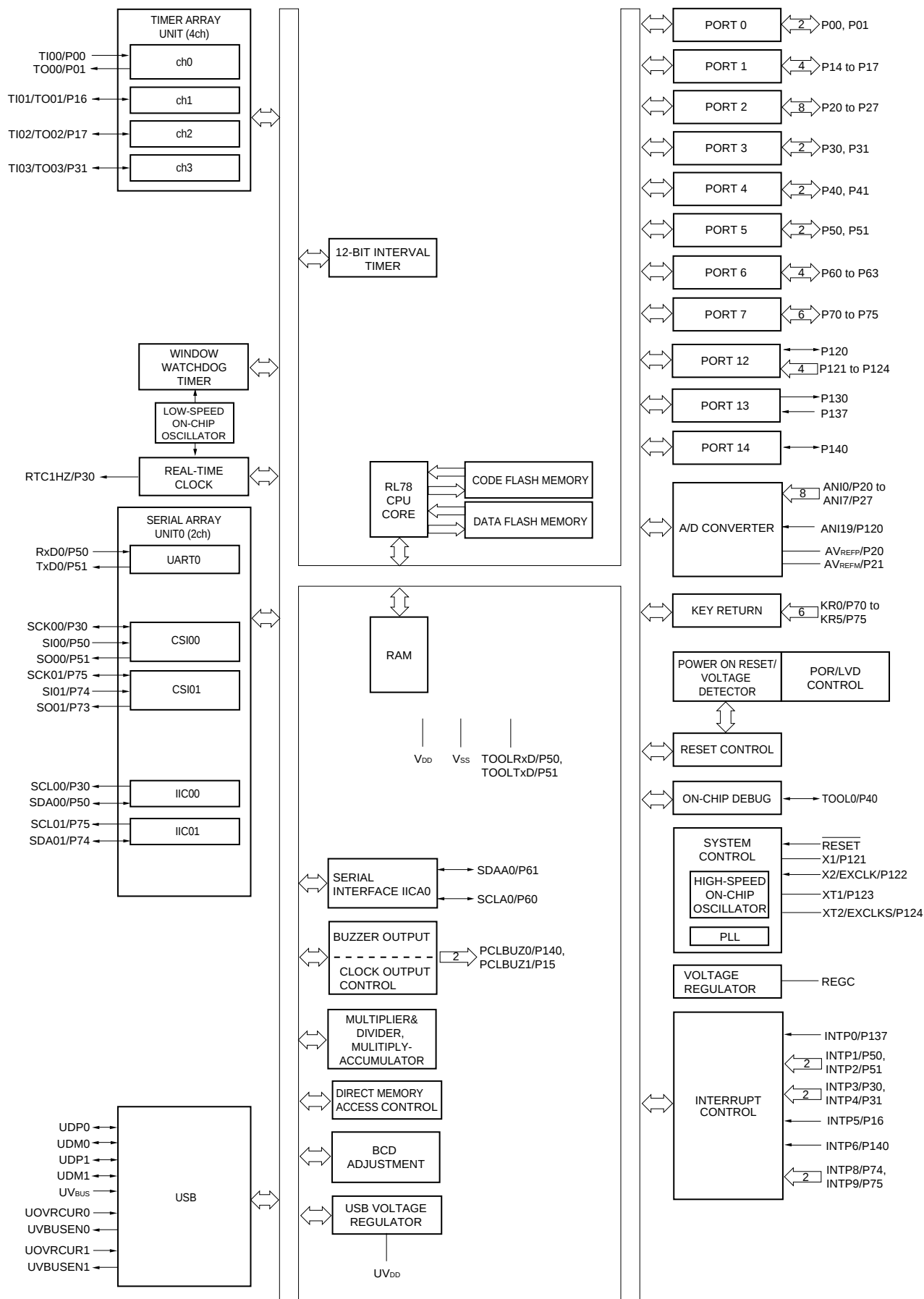
ANI0 to ANI7, ANI16, ANI17, ANI19:	Analog Input
AVREFM:	Analog Reference Voltage Minus
AVREFP:	Analog Reference Voltage Plus
EXCLK:	External Clock Input (Main System Clock)
EXCLKS:	External Clock Input (Sub System Clock)
INTP0 to INTP6, INTP8, INTP9:	External Interrupt Input
KR0 to KR5:	Key Return
P00, P01:	Port 0
P14 to P17:	Port 1
P20 to P27:	Port 2
P30, P31:	Port 3
P40, P41:	Port 4
P50, P51:	Port 5
P60 to P63:	Port 6
P70 to P75:	Port 7
P120 to P124:	Port 12
P130, P137:	Port 13
P140:	Port 14
PCLBUZ0, PCLBUZ1:	Programmable Clock Output/Buzzer Output
REGC:	Regulator Capacitance
RESET:	Reset
RTC1HZ:	Real-time Clock Correction Clock (1 Hz) Output
RxD0:	Receive Data
SCK00, SCK01:	Serial Clock Input/Output
SCLA0, SCL00, SCL01:	Serial Clock Input/Output
SDAA0, SDA00, SDA01:	Serial Data Input/Output
SI00, SI01:	Serial Data Input
SO00, SO01:	Serial Data Output
TI00 to TI03:	Timer Input
TO00 to TO03:	Timer Output
TOOL0:	Data Input/Output for Tool
TOOLRxD, TOOLTxD:	Data Input/Output for External Device
TxD0:	Transmit Data
UDM0, UDM1, UDP0, UDP1:	USB Input/Output
UOVRCUR0, UOVRCUR1:	USB Input
UVBUSEN0, UVBUSEN1:	USB Output
UVDD:	USB Power Supply/USB Regulator Capacitance
UVBUS:	USB Input/USB Power Supply (USB Optional BC)
VDD:	Power Supply
VSS:	Ground
X1, X2:	Crystal Oscillator (Main System Clock)
XT1, XT2:	Crystal Oscillator (Subsystem Clock)

1.5 Block Diagram

1.5.1 32-pin products



1.5.2 48-pin products



1.6 Outline of Functions

[32-pin, 48-pin products]

(1/2)

Item		32-pin		48-pin	
		R5F10JBC	R5F10KBC	R5F10JGC	R5F10KGC
Code flash memory (KB)		32 KB		32 KB	
Data flash memory (KB)		2 KB		2 KB	
RAM (KB)		5.5 KB ^{Note 1}		5.5 KB ^{Note 1}	
Memory space		1 MB			
<R>	Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V)		
		High-speed on-chip oscillator	1 to 24 MHz (V _{DD} = 2.7 to 5.5 V), 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V)		
		PLL clock	6, 12, 24 MHz ^{Note 2} : V _{DD} = 2.4 to 5.5 V		
Subsystem clock		—		XT1 (crystal) oscillation 32.768 kHz (TYP.): V _{DD} = 2.4 to 5.5 V	
Low-speed on-chip oscillator		On-chip oscillation (Watchdog timer/Real-time clock/12-bit interval timer clock) 15 kHz (TYP.): V _{DD} = 2.4 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator: f _{HOCO} = 48 MHz /f _{IH} = 24 MHz operation)			
		0.04167 μs (PLL clock: f _{PLL} = 48 MHz /f _{IH} = 24 MHz ^{Note 2} operation)			
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)			
		—		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	22		38	
	CMOS I/O	16 (N-ch O.D. I/O [V _{DD} withstand voltage]: 5)		28 (N-ch O.D. I/O [V _{DD} withstand voltage]: 6)	
	CMOS input	3		5	
	CMOS output	—		1	
	N-ch open-drain I/O (6 V tolerance)	3		4	
Timer	16-bit timer	4 channel			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel ^{Note 3}			
	12-bit Interval timer (IT)	1 channel			
	Timer output	4 channels (PWM output: 3) ^{Note 4}			
	RTC output	—		1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)	

- Notes**
1. In the case of the 5.5 KB, this is about 4.5 KB when the self-programming function is used.
 2. In the PLL clock 48 MHz operation, the system clock is 2/4/8 dividing ratio.
 3. In 32-pin products, this channel can only be used for the constant-period interrupt function based on the low-speed on-chip oscillator clock (f_{IL}).
 4. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves).

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(2/2)

(2/2)

Item		32-pin		48-pin	
		R5F10JBC	R5F10KBC	R5F10JGC	R5F10KGC
Clock output/buzzer output		2		2	
		2.93 kHz, 5.86 kHz, 11.7 kHz, 1.5 MHz, 3 MHz, 6 MHz, 12 MHz (Main system clock: f_{MAIN} = 24 MHz operation) 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)			
8/10-bit resolution A/D converter		8 channels		9 channels	
Serial interface		CSI: 2 channels/UART: 1 channel/simplified I ² C: 2 channels			
	I ² C bus	1 channel			
USB	Host controller	2 channels	–	2 channels	–
	Function controller	1 channel			
Multiplier and divider/multiply-accumulator		- Multiplier: 16 bits × 16 bits = 32 bits (Unsigned or signed) - Divider: 32 bits ÷ 32 bits = 32 bits (Unsigned) - Multiply-accumulator: 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)			
DMA controller		2 channels			
Vectored interrupt sources	Internal	20		20	
	External	8		10	
Key interrupt		–		6	
Reset		- Reset by RESET pin - Internal reset by watchdog timer - Internal reset by power-on-reset - Internal reset by voltage detector - Internal reset by illegal instruction execution ^{Note} - Internal reset by RAM parity error - Internal reset by illegal-memory access			
Power-on-reset circuit		- Power-on-reset: 1.51 V (TYP.) - Power-down-reset: 1.50 V (TYP.)			
Voltage detector		2.45 V to 4.06 V (9 stages)			
On-chip debug function		Provided			
Power supply voltage		V _{DD} = 2.4 to 5.5 V			
Operating ambient temperature		T _A = –40 to +85 °C (A: Consumer applications), T _A = –40 to +105°C (G: Industrial applications)			

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS (A: T_A = -40 to +85°C)

This chapter describes the electrical specifications for the products "A: Consumer applications (T_A = -40 to +85°C)".

The target products

A: Consumer applications ; T_A = -40 to +85°C

R5F10JBCANA, R5F10JBCAFP, R5F10JGCANA, R5F10JGCAFB,
R5F10KBCANA, R5F10KBCAFP, R5F10KGCANA, R5F10KGCAFB

G: Industrial applications ; when using T_A = -40 to +105°C specification products
at T_A = -40 to +85°C.

R5F10JBCGNA, R5F10JBCGFP, R5F10JGCGNA, R5F10JGCGFB,
R5F10KBCGNA, R5F10KBCGFP, R5F10KGCNA, R5F10KGCGB

Cautions 1. The RL78 microcontrollers has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
REGC pin input voltage	V _{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V _{DD} + 0.3 ^{Note 1}	V
UV _{DD} pin input voltage	V _{IUVDD}	UV _{DD}	-0.3 to V _{DD} + 0.3	V
Input voltage	V _{I1}	P00, P01, P14 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P70 to P75, P120 to P124, P137, P140, EXCLK, EXCLKS, RESET	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V _{I3}	UDP0, UDM0, UDP1, UDM1	-0.3 to +6.5	V
	V _{I4}	UV _{BUS}	-0.3 to +6.5	V
Output voltage	V _{O1}	P00, P01, P14 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P130, P140	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{O2}	UDP0, UDM0, UDP1, UDM1	-0.3 to +6.5	V
Analog input voltage	V _{AI1}	ANI16, ANI17, ANI19	-0.3 to V _{DD} + 0.3 and -0.3 to AV _{REF} (+) + 0.3 Notes 2, 3	V
	V _{AI2}	ANI0 to ANI7	-0.3 to V _{DD} + 0.3 and -0.3 to AV _{REF} (+) + 0.3 Notes 2, 3	V

- Notes 1.** Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
- 2.** Must be 6.5 V or lower.
- 3.** Do not exceed AV_{REF}(+) + 0.3 V in case of A/D conversion target pin

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
- 2.** AV_{REF} (+) : The + side reference voltage of the A/D converter. This can be selected from AV_{REFP}, the internal reference voltage (1.45 V), and V_{DD}.
- 3.** V_{SS} : Reference voltage

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	−40	
		Total of all pins −170 mA	P00, P01, P40, P41, P120, P130, P140	−70	mA
			P14 to P17, P30, P31, P50, P51, P70 to P75	−100	mA
	I _{OH2}	Per pin	P20 to P27	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I _{OL1}	Per pin	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P130, P140	40	mA
		Total of all pins 170 mA	P00, P01, P40, P41, P120, P130, P140	70	mA
			P14 to P17, P30, P31, P50, P51, P60 to P63, P70 to P75	100	mA
	I _{OL2}	Per pin	P20 to P27	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T _A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T _{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f _X) ^{Note}	Ceramic resonator/ crystal resonator	2.7 V ≤ V _{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V	1.0		16.0	MHz
XT1 clock oscillation frequency (f _{XT}) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f _{HOCO}		1		48	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85 °C	-1.0		+1.0	%
		-40 to -20 °C	-1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f _{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

2.2.3 PLL oscillator characteristics

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
PLL input frequency ^{Note}	f _{PLLIN}	High-speed system clock	6.00		16.00	MHz
PLL output frequency ^{Note}	f _{PLL}			48.00		MHz
Lock up time		From PLL output enable to stabilization of the output frequency	40.00			μs
Interval time		From PLL stop to PLL re-operation setting Wait time	4.00			μs
Setting wait time		From after PLL input clock stabilization and PLL setting is fixed to start setting Wait time required	1.00			μs

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	2.4 V ≤ V _{DD} ≤ 5.5 V		-10.0 Note 2	mA
		Total of P00, P01, P40, P41, P120, P130, P140 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V		-55.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		-10.0	mA
			2.4 V ≤ V _{DD} < 2.7 V		-5.0	mA
		Total of P14 to P17, P30, P31, P50, P51, P70 to P75 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V		-80.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		-19.0	mA
			2.4 V ≤ V _{DD} < 2.7 V		-10.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ V _{DD} ≤ 5.5 V		-135.0	mA
	I _{OH2}	Per pin for P20 to P27	2.4 V ≤ V _{DD} ≤ 5.5 V		-0.1 ^{Note 2}	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ V _{DD} ≤ 5.5 V		-1.5	mA

- Notes**
1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.
 2. However, do not exceed the total current value.
 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty ratio to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P01, P30, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	I _{OL1}	Per pin for P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	2.4V ≤ V _{DD} ≤ 5.5 V		20.0 ^{Note 2}	mA
		Per pin for P60 to P63	2.4V ≤ V _{DD} ≤ 5.5 V		20.0 ^{Note 2}	mA
		Total of P00, P01, P40, P41, P120, P130, P140 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V		70.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		15.0	mA
			2.4 V ≤ V _{DD} < 2.7 V		9.0	mA
		Total of P14 to P17, P30, P31, P50, P51, P60 to P63, P70 to P75 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V		80.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		35.0	mA
			2.4 V ≤ V _{DD} < 2.7 V		20.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4V ≤ V _{DD} ≤ 5.5 V		150.0	mA
	I _{OL2}	Per pin for P20 to P27	2.4V ≤ V _{DD} ≤ 5.5 V		0.4 ^{Note 2}	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4V ≤ V _{DD} ≤ 5.5 V		5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty ratio to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \cong 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140	Normal input buffer	0.8V _{DD}		V _{DD}	V
	V _{IH2}	P00, P01, P30, P50	TTL input buffer 4.0 V ≤ V _{DD} ≤ 5.5 V	2.2		V _{DD}	V
			TTL input buffer 3.3 V ≤ V _{DD} < 4.0 V	2.0		V _{DD}	V
			TTL input buffer 2.4 V ≤ V _{DD} < 3.3 V	1.5		V _{DD}	V
	V _{IH3}	P20 to P27		0.7V _{DD}		V _{DD}	V
	V _{IH4}	P60 to P63		0.7V _{DD}		6.0	V
	V _{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V _{DD}		V _{DD}	V
Input voltage, low	V _{IL1}	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140	Normal input buffer	0		0.2V _{DD}	V
	V _{IL2}	P00, P01, P30, P50	TTL input buffer 4.0 V ≤ V _{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V _{DD} < 4.0 V	0		0.5	V
			TTL input buffer 2.4 V ≤ V _{DD} < 3.3 V	0		0.32	V
	V _{IL3}	P20 to P27		0		0.3V _{DD}	V
	V _{IL4}	P60 to P63		0		0.3V _{DD}	V
	V _{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V _{DD}	V

Caution The maximum value of V_{IH} of pins P00, P01, P30, and P74 is V_{DD} , even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to $+85^{\circ}\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V _{OH1}	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -10.0\text{ mA}$	$V_{DD} - 1.5$		V
			$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -3.0\text{ mA}$	$V_{DD} - 0.7$		V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -2.0\text{ mA}$	$V_{DD} - 0.6$		V
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -1.5\text{ mA}$	$V_{DD} - 0.5$		V
	V _{OH2}	P20 to P27	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH2} = -100\text{ }\mu\text{A}$	$V_{DD} - 0.5$		V
Output voltage, low	V _{OL1}	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 20.0\text{ mA}$		1.3	V
			$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 8.5\text{ mA}$		0.7	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 1.5\text{ mA}$		0.4	V
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 0.6\text{ mA}$		0.4	V
	V _{OL2}	P20 to P27	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL2} = 400\text{ }\mu\text{A}$		0.4	V
	V _{OL3}	P60 to P63	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 20.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 3.0\text{ mA}$		0.4	V
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 2.0\text{ mA}$		0.4	V

Caution P00, P01, P30, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	I _{LH1}	P00, P01, P14 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P137, P140, RESET	V _I = V _{DD}		1	μA		
	I _{LH2}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port or external clock input	1	μA		
				In resonator connection	10	μA		
Input leakage current, low	I _{LIL1}	P00, P01, P14 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P137, P140, RESET	V _I = V _{SS}		−1	μA		
	I _{LIL2}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port or external clock input	−1	μA		
				In resonator connection	−10	μA		
On-chip pll-up resistance	R _U	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140	V _I = V _{SS} , In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

(1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I _{DD1}	Operating mode	HS (High-speed main) mode Note 6	f _{HOCO} = 48 MHz f _{IH} = 24 MHz Note 3	Basic operation	V _{DD} = 5.0 V		1.7		mA
						V _{DD} = 3.0 V		1.7		mA
					Normal operation	V _{DD} = 5.0 V		3.7	5.5	mA
						V _{DD} = 3.0 V		3.7	5.5	mA
				f _{HOCO} = 24 MHz f _{IH} = 12 MHz Note 3	Normal operation	V _{DD} = 5.0 V		2.3	3.2	mA
						V _{DD} = 3.0 V		2.3	3.2	mA
				f _{HOCO} = 12 MHz f _{IH} = 6 MHz Note 3	Normal operation	V _{DD} = 5.0 V		1.6	2.0	mA
						V _{DD} = 3.0 V		1.6	2.0	mA
				f _{HOCO} = 6 MHz f _{IH} = 3 MHz Note 3	Normal operation	V _{DD} = 5.0 V		1.2	1.5	mA
						V _{DD} = 3.0 V		1.2	1.5	mA
			HS (High-speed main) mode Note 6	f _{MX} = 20 MHz V _{DD} = 5.0 V Note 2	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	mA
				f _{MX} = 20 MHz V _{DD} = 3.0 V Note 2	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	mA
				f _{MX} = 10 MHz V _{DD} = 5.0 V Note 2	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	mA
				f _{MX} = 10 MHz V _{DD} = 3.0 V Note 2	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	mA
			HS (High-speed main) mode (PLL operation) Note 6	f _{PLL} = 48 MHz, f _{CLK} = 24 MHz Note 2	Normal operation	V _{DD} = 5.0 V		4.0	5.9	mA
						V _{DD} = 3.0 V		4.0	5.9	mA
				f _{PLL} = 48 MHz, f _{CLK} = 12 MHz Note 2	Normal operation	V _{DD} = 5.0 V		2.6	3.6	mA
						V _{DD} = 3.0 V		2.6	3.6	mA
			Subsystem clock operation	f _{SUB} = 32.768 kHz T _A = -40°C Note 4	Normal operation	Resonator connection		4.1	4.9	μA
						Square wave input		4.2	5.0	μA
				f _{SUB} = 32.768 kHz T _A = +25°C Note 4	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f _{SUB} = 32.768 kHz T _A = +50°C Note 4	Normal operation	Square wave input		4.2	5.5	μA
						Resonator connection		4.3	5.6	μA
				f _{SUB} = 32.768 kHz T _A = +70°C Note 4	Normal operation	Square wave input		4.2	6.3	μA
						Resonator connection		4.3	6.4	μA
				f _{SUB} = 32.768 kHz T _A = +85°C Note 4	Normal operation	Square wave input		4.8	7.7	μA
						Resonator connection		4.9	7.8	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 5. When Operating frequency setting of option byte = 48 MHz. When f_{HOCO} is divided by HOCODIV. When RDIV[1:0] = 00 (divided by 2: default).
 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$
	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

- Remarks**
1. f_{HOCO} : High-speed on-chip oscillator clock frequency (Max. 48 MHz)
 2. f_{IH} : Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2, 4, or 8 (Max. 24 MHz)
 3. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 4. f_{PLL} : PLL oscillation frequency
 5. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 6. f_{CLK} : CPU/peripheral hardware clock frequency
 7. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$.

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (High-speed main) mode Note 9	f _{HOCO} = 48 MHz	V _{DD} = 5.0 V		0.67	1.25	mA	
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 3.0 V		0.67	1.25	mA	
				f _{HOCO} = 24 MHz ^{Note 7}	V _{DD} = 5.0 V		0.50	0.86	mA	
				f _{IH} = 12 MHz ^{Note 4}	V _{DD} = 3.0 V		0.50	0.86	mA	
				f _{HOCO} = 12 MHz ^{Note 7}	V _{DD} = 5.0 V		0.41	0.67	mA	
				f _{IH} = 6 MHz ^{Note 4}	V _{DD} = 3.0 V		0.41	0.67	mA	
				f _{HOCO} = 6 MHz ^{Note 7}	V _{DD} = 5.0 V		0.37	0.58	mA	
				f _{IH} = 3 MHz ^{Note 4}	V _{DD} = 3.0 V		0.37	0.58	mA	
			HS (High-speed main) mode Note 9	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.19	0.60	mA	
					Resonator connection		0.26	0.67	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.19	0.60	mA	
					Resonator connection		0.26	0.67	mA	
			HS (High-speed main) mode (PLL operation) Note 9	f _{PLL} = 48 MHz, f _{CLK} = 24 MHz ^{Note 3}	V _{DD} = 5.0 V		0.91	1.52	mA	
					V _{DD} = 3.0 V		0.91	1.52	mA	
				f _{PLL} = 48 MHz, f _{CLK} = 12 MHz ^{Note 3}	V _{DD} = 5.0 V		0.85	1.28	mA	
					V _{DD} = 3.0 V		0.85	1.28	mA	
				f _{PLL} = 48 MHz, f _{CLK} = 6 MHz ^{Note 3}	V _{DD} = 5.0 V		0.82	1.15	mA	
					V _{DD} = 3.0 V		0.82	1.15	mA	
			Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 5} T _A = −40°C	Square wave input		0.25	0.57	μA	
					Resonator connection		0.44	0.76	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +25°C	Square wave input		0.30	0.57	μA	
					Resonator connection		0.49	0.76	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +50°C	Square wave input		0.33	1.17	μA	
					Resonator connection		0.63	1.36	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +70°C	Square wave input		0.46	1.97	μA	
					Resonator connection		0.76	2.16	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +85°C	Square wave input		0.97	3.37	μA	
					Resonator connection		1.16	3.56	μA	
	I _{DD3} ^{Note 6}	STOP mode ^{Note 8}	T _A = −40°C					0.18	0.50	μA
			T _A = +25°C					0.23	0.50	μA
			T _A = +50°C					0.26	1.10	μA
			T _A = +70°C					0.29	1.90	μA
			T _A = +85°C					0.90	3.30	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, USB 2.0 host/function module, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. When Operating frequency setting of option byte = 48 MHz. When f_{HOCO} is divided by HOCODIV. When RDIV[1:0] = 00 (divided by 2: default).
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
 9. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 24 MHz
	2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz

- Remarks**
1. f_{HOCO}: High-speed on-chip oscillator clock frequency (Max. 48 MHz)
 2. f_{IH}: Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2, 4, or 8 (Max. 24 MHz)
 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 4. f_{PLL}: PLL oscillation frequency
 5. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 6. f_{CLK}: CPU/peripheral hardware clock frequency
 7. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C.

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I _{FIL} ^{Note 1}				0.20		μA
RTC operating current	I _{RTC} ^{Notes 1, 2, 3}				0.02		μA
12-bit interval timer operating current	I _{IT} ^{Notes 1, 2, 4}				0.02		μA
Watchdog timer operating current	I _{WDT} ^{Notes 1, 2, 5}	f _{IL} = 15 kHz			0.22		μA
A/D converter operating current	I _{ADC} ^{Notes 1, 6}	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I _{ADREF} ^{Note 1}				75.0		μA
Temperature sensor operating current	I _{TMPS} ^{Note 1}				75.0		μA
LVD operating current	I _{LVD} ^{Notes 1, 7}				0.08		μA
Self-programming operating current	I _{FSP} ^{Notes 1, 9}				2.00	12.20	mA
BGO operating current	I _{BGO} ^{Notes 1, 8}				2.00	12.20	mA
SNOOZE operating current	I _{SNOZ} ^{Note 1}	ADC operation	The mode is performed ^{Note 10}		0.50	1.06	mA
			The A/D conversion operations are performed, Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		1.20	1.62	mA
		CSI operation			0.70	0.84	mA

(Notes and Remarks are listed on the next page.)

(T_A = -40 to $+85^{\circ}\text{C}$, 2.4 V $\leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USB operating current	I _{USBH} Note 11	During USB communication operation under the following settings and conditions ($V_{DD} = 5.0$ V, $T_A = +25^{\circ}\text{C}$): - The internal power supply for the USB is used. - X1 oscillation frequency (f_x) = 12 MHz, PLL oscillation frequency (f_{PLL}) = 48 MHz - The host controller (via two ports) is set to operate in full-speed mode with four pipes (end points) used simultaneously. (PIPE4: Bulk OUT transfer (64 bytes), PIPE5: Bulk IN transfer (64 bytes), PIPE6: Interrupt OUT transfer, PIPE7: Interrupt IN transfer). - The USB ports (two ports) are individually connected to a peripheral function via a 0.5 m USB cable.		9.0		mA
	I _{USBF} Note 11	During USB communication operation under the following settings and conditions ($V_{DD} = 5.0$ V, $T_A = +25^{\circ}\text{C}$): - The internal power supply for the USB is used. - X1 oscillation frequency (f_x) = 12 MHz, PLL oscillation frequency (f_{PLL}) = 48 MHz - The function controller is set to operate in full-speed mode with four pipes (end points) used simultaneously. (PIPE4: Bulk OUT transfer (64 bytes), PIPE5: Bulk IN transfer (64 bytes), PIPE6: Interrupt OUT transfer, PIPE7: Interrupt IN transfer). - The USB port (one port) is connected to the host device via a 0.5 m USB cable.		2.5		mA
	I _{SUSP} Note 12	During suspended state under the following settings and conditions ($V_{DD} = 5.0$ V, $T_A = +25^{\circ}\text{C}$): - The function controller is set to full-speed mode (the UDP0 pin is pulled up). - The internal power supply for the USB is used. - The system is set to STOP mode (When the high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When the watchdog timer is stopped.). - The USB port (one port) is connected to the host device via a 0.5 m USB cable.		240		μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Current flowing to V_{DD} .
 2. When high speed on-chip oscillator and high-speed system clock are stopped.
 3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{RTC} , when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.
 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{IT} , when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.
 6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
 7. Current flowing only to the LVD circuit. The current value of the RL78/G1C is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit operates in the Operating, HALT or STOP mode.
 8. Current flowing only during data flash rewrite.
 9. Current flowing only during self programming.
 10. For shift time to the SNOOZE mode.
 11. Current consumed only by the USB module and the internal power supply for the USB.
 12. Includes the current supplied from the pull-up resistor of the UDP0 pin to the pull-down resistor of the host device, in addition to the current consumed by this MCU during the suspended state.

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

2.4 AC Characteristics

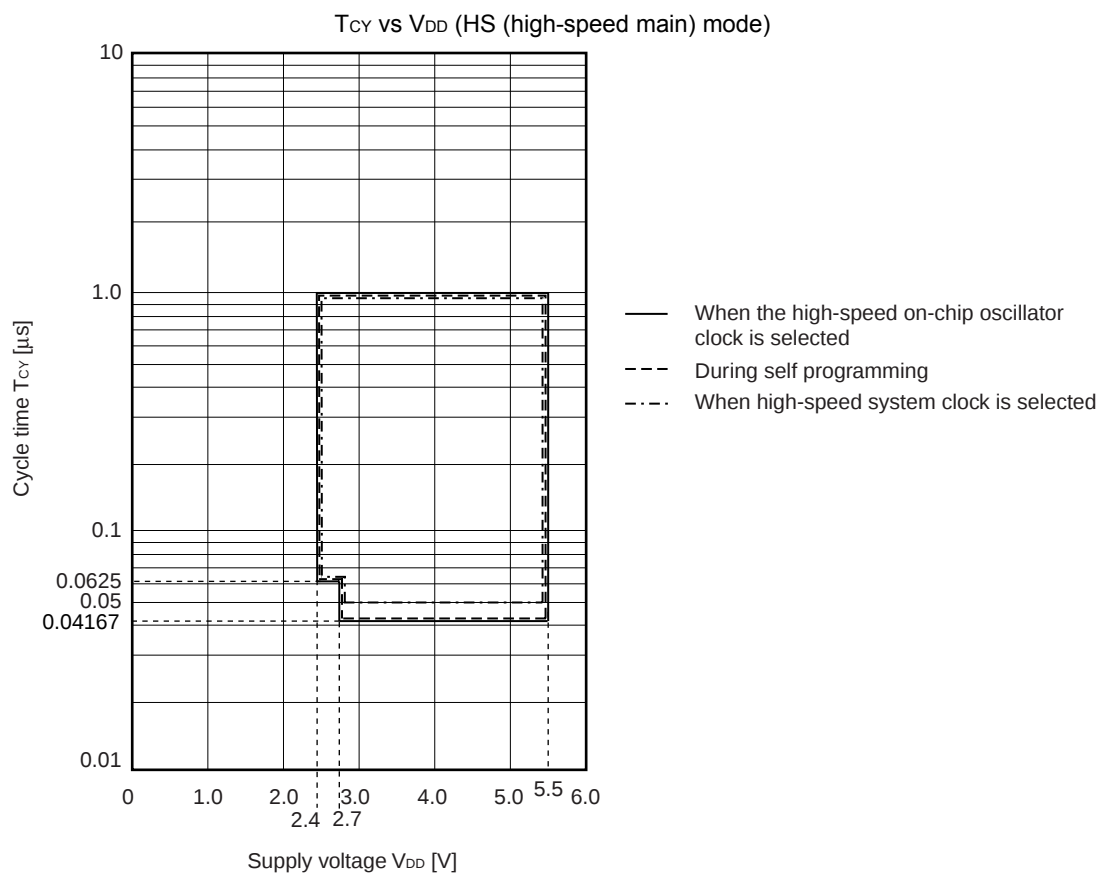
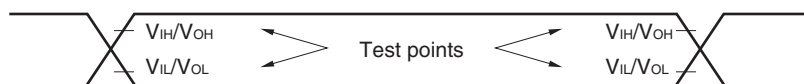
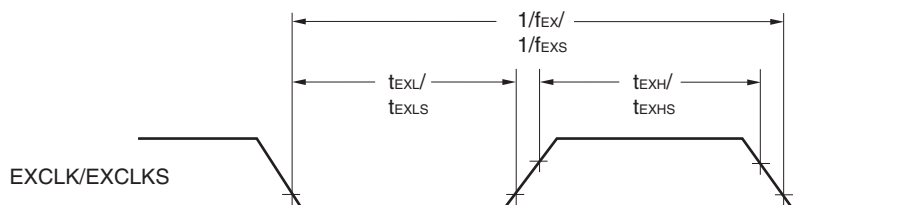
2.4.1 Basic operation

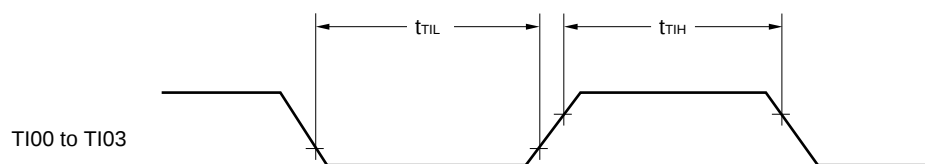
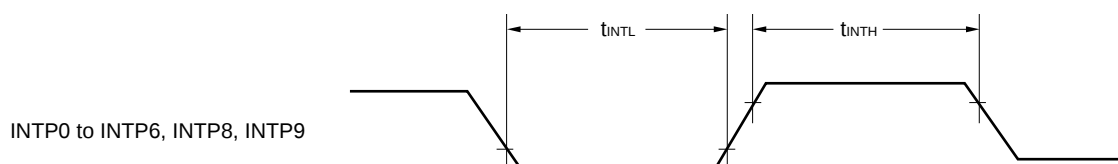
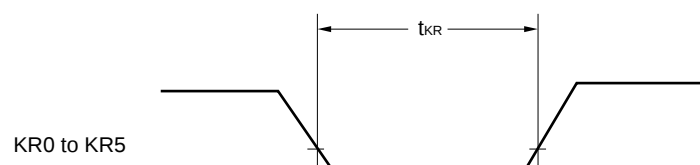
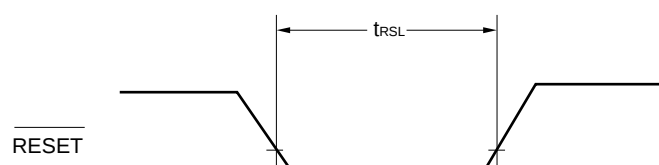
(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (High-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
		Subsystem clock (f _{SUB}) operation		2.4 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (High-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
External system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V			1.0		16.0	MHz
	f _{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V _{DD} < 2.7 V			30			ns
	t _{EXHS} , t _{EXLS}				13.7			μs
TI00 to TI03 input high-level width, low-level width	t _{TIH} , t _{TIL}				1/f _{MCK} +10			ns
TO00 to TO03 output frequency	f _{TO}	High-speed main mode	4.0 V ≤ V _{DD} ≤ 5.5 V				12	MHz
			2.7 V ≤ V _{DD} < 4.0 V				8	MHz
			2.4 V ≤ V _{DD} < 2.7 V				4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	High-speed main mode	4.0 V ≤ V _{DD} ≤ 5.5 V				16	MHz
			2.7 V ≤ V _{DD} < 4.0 V				8	MHz
			2.4 V ≤ V _{DD} < 2.7 V				4	MHz
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0 to INTP6, INTP8, INTP9	2.4 V ≤ V _{DD} ≤ 5.5 V		1			μs
Key interrupt input low-level width	t _{KR}	KR0 to KR5	2.4 V ≤ V _{DD} ≤ 5.5 V		250			ns
RESET low-level width	t _{RSL}				10			μs

Remark f_{MCK}: Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 3))

Minimum Instruction Execution Time during Main System Clock Operation**AC Timing Test Points****External System Clock Timing**

TI/TO Timing**Interrupt Request Input Timing****Key Interrupt Input Timing** **$\overline{\text{RESET}}$ Input Timing**

2.5 Peripheral Functions Characteristics

2.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note			4.0	Mbps

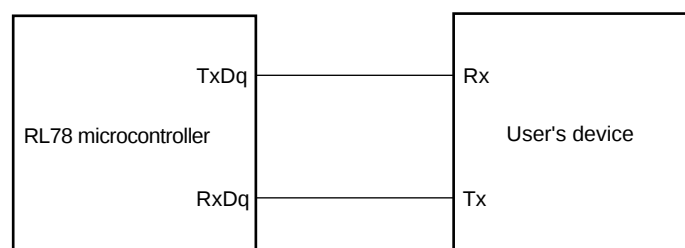
Note The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 24 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

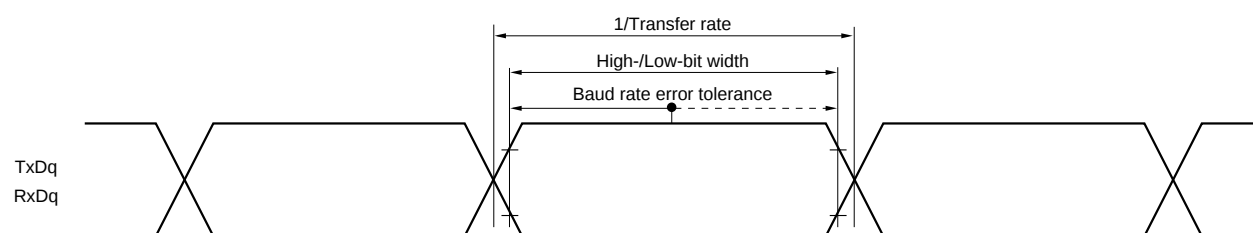
16 MHz ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



- Remarks**
1. q: UART number ($q = 0$), g: PIM and POM number ($g = 5$)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 2/f _{CLK} 2.7 V ≤ V _{DD} ≤ 5.5 V	83.3			ns
SCKp high-/low-level width	t _{KH1} ,	4.0 V ≤ V _{DD} ≤ 5.5 V	t _{KCY1} /2 - 7			ns
	t _{KL1}	2.7 V ≤ V _{DD} ≤ 5.5 V	t _{KCY1} /2 - 10			ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V	23			ns
		2.7 V ≤ V _{DD} ≤ 5.5 V	33			ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{KSH1}	2.7 V ≤ V _{DD} ≤ 5.5 V	10			ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO1}	C = 20 pF ^{Note 3}			10	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. This specification is valid only when CSI00's peripheral I/O redirect function is not used.
 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 3, 5)
 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
($T_A = -40$ to $+85^{\circ}\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$				
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	167			ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	250			ns
SCKp high-/low-level width	t_{KH1} , t_{KL1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 12$			ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 18$			ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 38$			ns
Slp setup time (to SCKp $\uparrow$) ^{Note 1}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	44			ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	44			ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	75			ns
Slp hold time (from SCKp $\uparrow$) ^{Note 2}	t_{SH1}		19			ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 3}	t_{KSO1}	$C = 30\text{ pF}$ ^{Note 4}			25	ns

- Notes**
1. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Slp setup time becomes “to SCKp $\downarrow$ ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 2. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Slp hold time becomes “from SCKp $\downarrow$ ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 3. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The delay time to SOp output becomes “from SCKp $\uparrow$ ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM numbers (g = 0, 3, 5, 7)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKS mn bit of serial mode register mn (SMR mn). m: Unit number,
n: Channel number (mn = 00, 01))

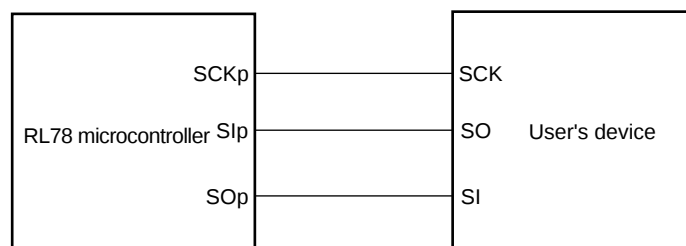
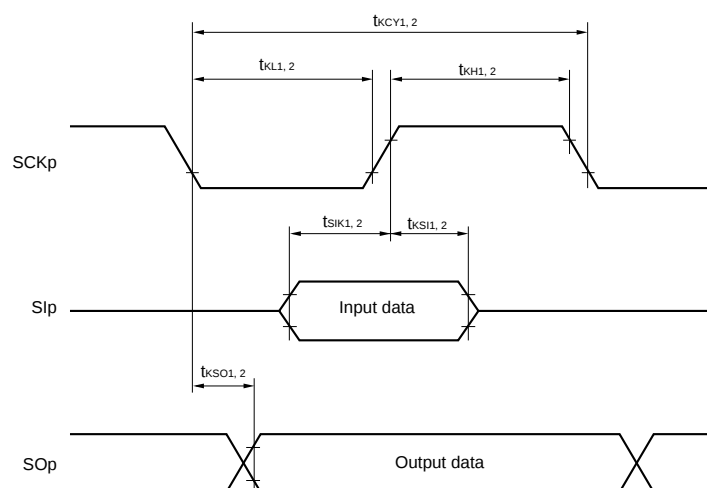
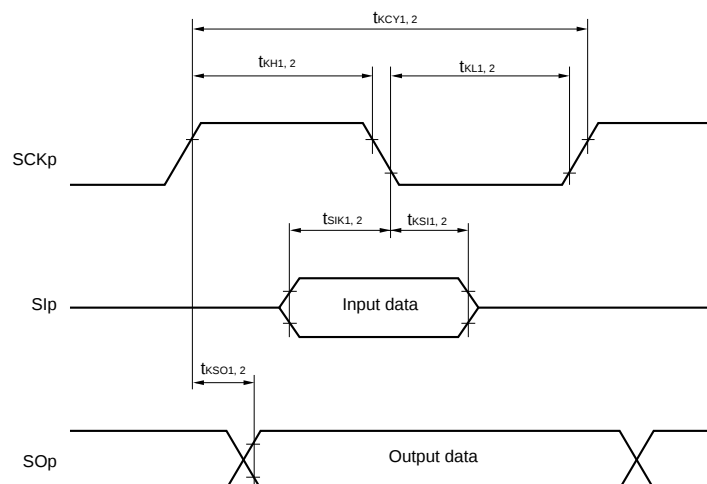
(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time ^{Note 5}	t _{KCY2}	4.0 V ≤ V _{DD} ≤ 5.5 V	20 MHz < f _{MCK}	8/f _{MCK}		ns
			f _{MCK} ≤ 20 MHz	6/f _{MCK}		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V	16 MHz < f _{MCK}	8/f _{MCK}		ns
			f _{MCK} ≤ 16 MHz	6/f _{MCK}		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V		6/f _{MCK} and 500		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ V _{DD} ≤ 5.5 V	t _{KCY2} /2 - 7			ns
		2.7 V ≤ V _{DD} ≤ 5.5 V	t _{KCY2} /2 - 8			ns
		2.4 V ≤ V _{DD} ≤ 5.5 V	t _{KCY2} /2 - 18			ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK2}	2.7 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} +20			ns
		2.4 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} +30			ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{KSI2}	2.7 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} +31			ns
		2.4 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} +31			ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO2}	C = 30 pF ^{Note 4}	2.7 V ≤ V _{DD} ≤ 5.5 V		2/f _{MCK} +44	ns
			2.4 V ≤ V _{DD} ≤ 5.5 V		2/f _{MCK} +75	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01), m: Unit number (m = 0),
n: Channel number (n = 0, 1), g: PIM number (g = 0, 3, 5, 7)
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 01))

CSI mode connection diagram (during communication at same potential)**CSI mode serial transfer timing (during communication at same potential)**(When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$.)**CSI mode serial transfer timing (during communication at same potential)**(When $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.)

- Remarks**
1. p: CSI number (p = 00, 01)
 2. m: Unit number, n: Channel number (mn = 00, 01)

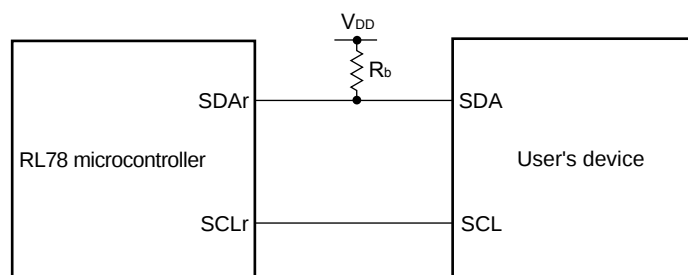
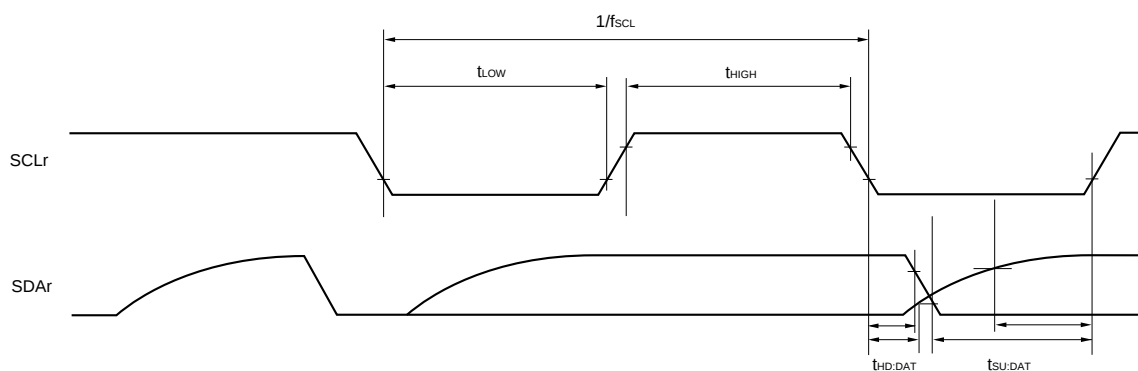
(5) During communication at same potential (simplified I²C mode)**(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f _{SCL}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 ^{Note 1}	kHz
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ		400 ^{Note 1}	kHz
		2.4 V ≤ V _{DD} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ		300 ^{Note 1}	kHz
Hold time when SCLr = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	475		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		ns
		2.4 V ≤ V _{DD} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1550		ns
Hold time when SCLr = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	475		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		ns
		2.4 V ≤ V _{DD} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1550		ns
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 85 ^{Note 2}		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 145 ^{Note 2}		ns
		2.4 V ≤ V _{DD} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 230 ^{Note 2}		ns
Data hold time (transmission)	t _{HD:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	ns
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	0	355	ns
		2.4 V ≤ V _{DD} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	0	405	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Caution and Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
 2. r: IIC number (r = 00, 01), g: PIM number (g = 5), h: POM number (h = 3, 5)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01)

(6) Communication at different potential (2.5 V, 3 V) (UART mode) (1/2)**(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate		reception	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			f _{MCK} /6 ^{Note 1}	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}			4.0	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			f _{MCK} /6 ^{Note 1}	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}			4.0	Mbps
			2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			f _{MCK} /6 ^{Note 1}	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}			4.0	Mbps

Notes 1. Use it with V_{DD} ≥ V_b.**2.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage**2.** q: UART number (q = 0), g: PIM and POM number (g = 5)**3.** f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

(6) Communication at different potential (2.5 V, 3 V) (UART mode) (2/2)**(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate		transmission	4.0 V ≤ V _{DD} ≤ 5.5 V,			Note 1	bps
			2.7 V ≤ V _b ≤ 4.0 V	Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V		2.8 ^{Note 2}	Mbps
			2.7 V ≤ V _{DD} < 4.0 V			Note 3	bps
			2.3 V ≤ V _b ≤ 2.7 V	Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V		1.2 ^{Note 4}	Mbps
			2.4 V ≤ V _{DD} < 3.3 V			Notes 5, 6	bps
			1.6 V ≤ V _b ≤ 2.0 V	Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V		0.43 ^{Note 7}	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

5. Use it with V_{DD} ≥ V_b.

Notes 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

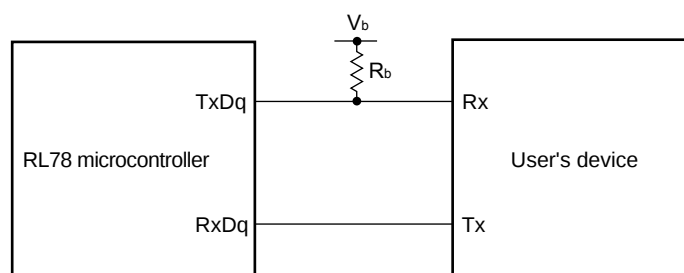
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

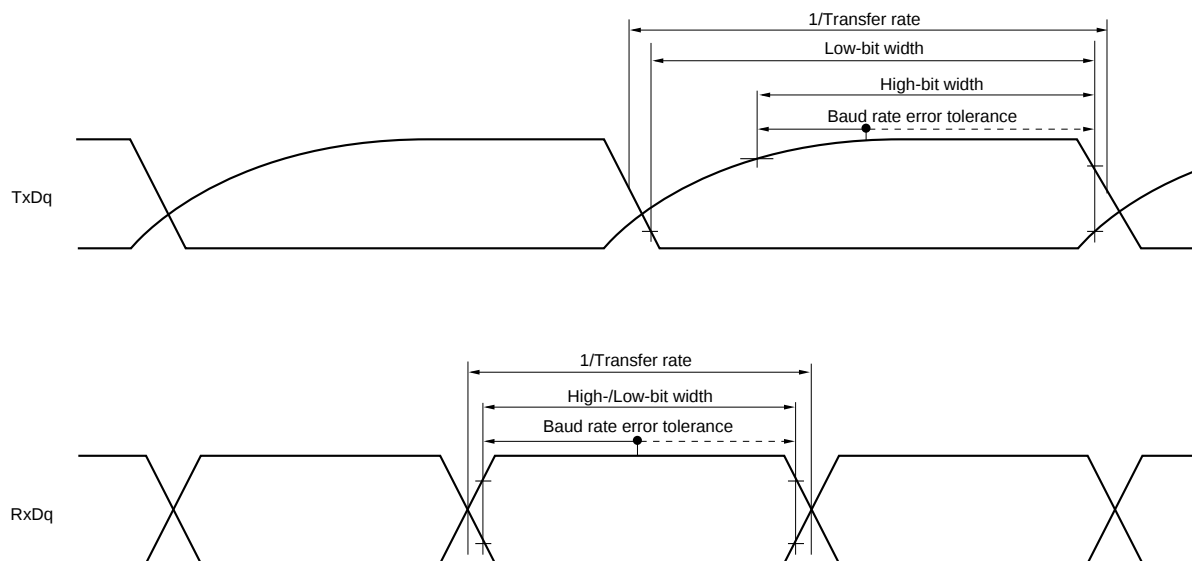
* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the Rx_{Dq} pin and the N-ch open drain output (V_{DD} tolerance) mode for the Tx_{Dq} pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $C_b[\text{F}]$: Communication line (TxDq) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. q: UART number ($q = 0$), g: PIM and POM number ($g = 5$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number ($mn = 00$))

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = -40 to $+85^\circ\text{C}$, 2.4 V $\leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t _{KCY1}	t _{KCY1} $\geq 2/f_{CLK}$ 4.0 V $\leq V_{DD} \leq 5.5$ V, 2.7 V $\leq V_b \leq 4.0$ V, C _b = 20 pF, R _b = 1.4 k Ω	200			ns
		2.7 V $\leq V_{DD} < 4.0$ V, 2.3 V $\leq V_b \leq 2.7$ V, C _b = 20 pF, R _b = 2.7 k Ω	300			ns
SCKp high-level width	t _{KH1}	4.0 V $\leq V_{DD} \leq 5.5$ V, 2.7 V $\leq V_b \leq 4.0$ V, C _b = 20 pF, R _b = 1.4 k Ω	t _{KCY1} /2 – 50			ns
		2.7 V $\leq V_{DD} < 4.0$ V, 2.3 V $\leq V_b \leq 2.7$ V, C _b = 20 pF, R _b = 2.7 k Ω	t _{KCY1} /2 – 120			ns
SCKp low-level width	t _{KL1}	4.0 V $\leq V_{DD} \leq 5.5$ V, 2.7 V $\leq V_b \leq 4.0$ V, C _b = 20 pF, R _b = 1.4 k Ω	t _{KCY1} /2 – 7			ns
		2.7 V $\leq V_{DD} < 4.0$ V, 2.3 V $\leq V_b \leq 2.7$ V, C _b = 20 pF, R _b = 2.7 k Ω	t _{KCY1} /2 – 10			ns
Slp setup time (to SCKp $\uparrow$) ^{Note 1}	t _{SIK1}	4.0 V $\leq V_{DD} \leq 5.5$ V, 2.7 V $\leq V_b \leq 4.0$ V, C _b = 20 pF, R _b = 1.4 k Ω	58			ns
		2.7 V $\leq V_{DD} < 4.0$ V, 2.3 V $\leq V_b \leq 2.7$ V, C _b = 20 pF, R _b = 2.7 k Ω	121			ns
Slp hold time (from SCKp $\uparrow$) ^{Note 1}	t _{KSI1}	4.0 V $\leq V_{DD} \leq 5.5$ V, 2.7 V $\leq V_b \leq 4.0$ V, C _b = 20 pF, R _b = 1.4 k Ω	10			ns
		2.7 V $\leq V_{DD} < 4.0$ V, 2.3 V $\leq V_b \leq 2.7$ V, C _b = 20 pF, R _b = 2.7 k Ω	10			ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 1}	t _{KSO1}	4.0 V $\leq V_{DD} \leq 5.5$ V, 2.7 V $\leq V_b \leq 4.0$ V, C _b = 20 pF, R _b = 1.4 k Ω			60	ns
		2.7 V $\leq V_{DD} < 4.0$ V, 2.3 V $\leq V_b \leq 2.7$ V, C _b = 20 pF, R _b = 2.7 k Ω			130	ns
Slp setup time (to SCKp $\downarrow$) ^{Note 2}	t _{SIK1}	4.0 V $\leq V_{DD} \leq 5.5$ V, 2.7 V $\leq V_b \leq 4.0$ V, C _b = 20 pF, R _b = 1.4 k Ω	23			ns
		2.7 V $\leq V_{DD} < 4.0$ V, 2.3 V $\leq V_b \leq 2.7$ V, C _b = 20 pF, R _b = 2.7 k Ω	33			ns
Slp hold time (from SCKp $\downarrow$) ^{Note 2}	t _{KSI1}	4.0 V $\leq V_{DD} \leq 5.5$ V, 2.7 V $\leq V_b \leq 4.0$ V, C _b = 20 pF, R _b = 1.4 k Ω	10			ns
		2.7 V $\leq V_{DD} < 4.0$ V, 2.3 V $\leq V_b \leq 2.7$ V, C _b = 20 pF, R _b = 2.7 k Ω	10			ns
Delay time from SCKp $\uparrow$ to SOp output ^{Note 2}	t _{KSO1}	4.0 V $\leq V_{DD} \leq 5.5$ V, 2.7 V $\leq V_b \leq 4.0$ V, C _b = 20 pF, R _b = 1.4 k Ω			10	ns
		2.7 V $\leq V_{DD} < 4.0$ V, 2.3 V $\leq V_b \leq 2.7$ V, C _b = 20 pF, R _b = 2.7 k Ω			10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(Caution and Remark are listed on the next page.)

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

- Remarks**
1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage
 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM number (g = 3, 5)
 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))
 4. This value is valid only when CSI00's peripheral I/O redirect function is not used.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)
(1/2)
(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK} 4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	300			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	500			ns
		2.4 V ≤ V _{DD} < 3.3 V, 2.4 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	1150			ns
SCKp high-level width	t _{KH1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 75			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 170			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 - 458			ns
SCKp low-level width	t _{KL1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 12			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 18			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 - 50			ns

- Cautions**
1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.
 2. Use it with V_{DD} ≥ V_b.

(Remarks are listed two pages after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)
(2/2)(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

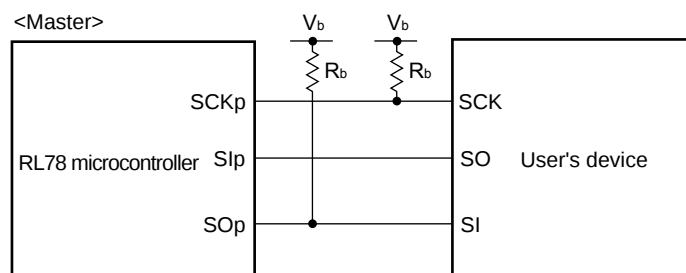
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	81			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	177			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ	479			ns
Slp hold time (from SCKp↑) ^{Note 1}	t _{KSI1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ	19			ns
Delay time from SCKp↓ to SOP output ^{Note 1}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			100	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			195	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ			483	ns
Slp setup time (to SCKp↓) ^{Note 2}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	44			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	44			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ	110			ns
Slp hold time (from SCKp↓) ^{Note 2}	t _{KSI1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ	19			ns
Delay time from SCKp↑ to SOP output ^{Note 2}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			25	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			25	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ			25	ns

(Notes, Cautions and Remarks are listed on the next page.)

- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$.
 2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 3. Use it with $V_{DD} \geq V_b$.

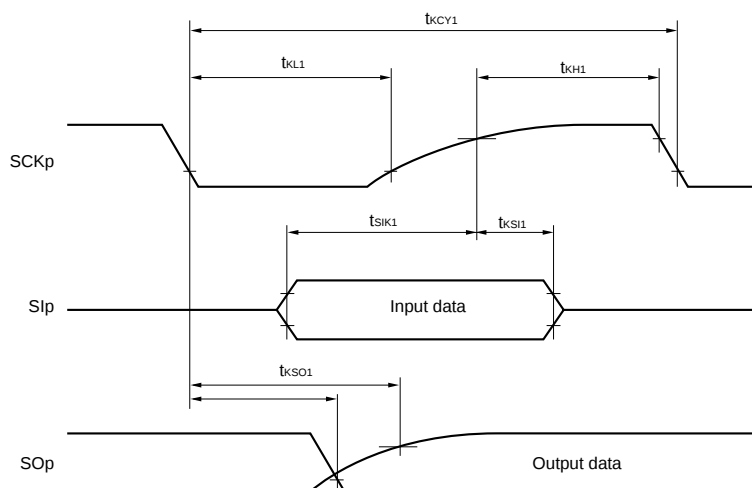
Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

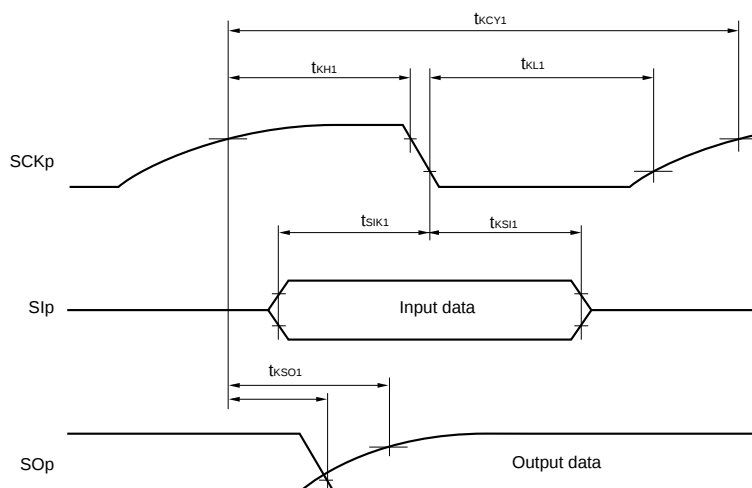


- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SCKp, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. p: CSI number ($p = 00$), m: Unit number, n: Channel number ($mn = 00$), g: PIM and POM number ($g = 0, 3, 5, 7$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number ($mn = 00$))
 4. CSI01 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00), m: Unit number, n: Channel number (mn = 00), g: PIM and POM number (g = 0, 3, 5, 7)
 2. CSI01 cannot communicate at different potential. Use other CSI for communication at different potential.

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	20 MHz < f _{MCK} ≤ 24 MHz	12/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 20 MHz	10/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	20 MHz < f _{MCK} ≤ 24 MHz	16/f _{MCK}		ns
			16 MHz < f _{MCK} ≤ 20 MHz	14/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 16 MHz	12/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	20 MHz < f _{MCK} ≤ 24 MHz	36/f _{MCK}		ns
			16 MHz < f _{MCK} ≤ 20 MHz	32/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 16 MHz	26/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	10/f _{MCK}		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	t _{KCY2} /2 – 12			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	t _{KCY2} /2 – 18			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	t _{KCY2} /2 – 50			ns
Slp setup time (to SCKp↑) ^{Note 3}	t _{SIK2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	1/f _{MCK} + 20			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	1/f _{MCK} + 20			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	1/f _{MCK} + 30			ns
Slp hold time (from SCKp↑) ^{Note 4}	t _{KS12}		1/f _{MCK} + 31			ns
Delay time from SCKp↓ to SOp output ^{Note 5}	t _{KSO2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			2/f _{MCK} + 120	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			2/f _{MCK} + 214	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ			2/f _{MCK} + 573	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps2. Use it with V_{DD} ≥ V_b.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

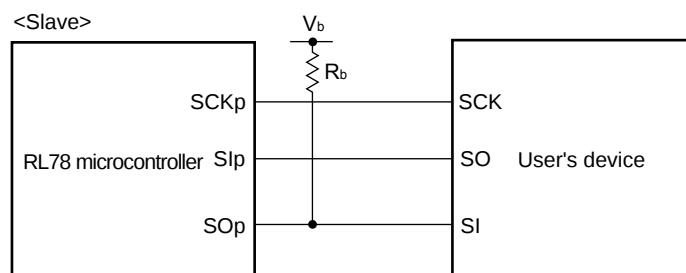
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(Caution and Remarks are listed on the next page.)

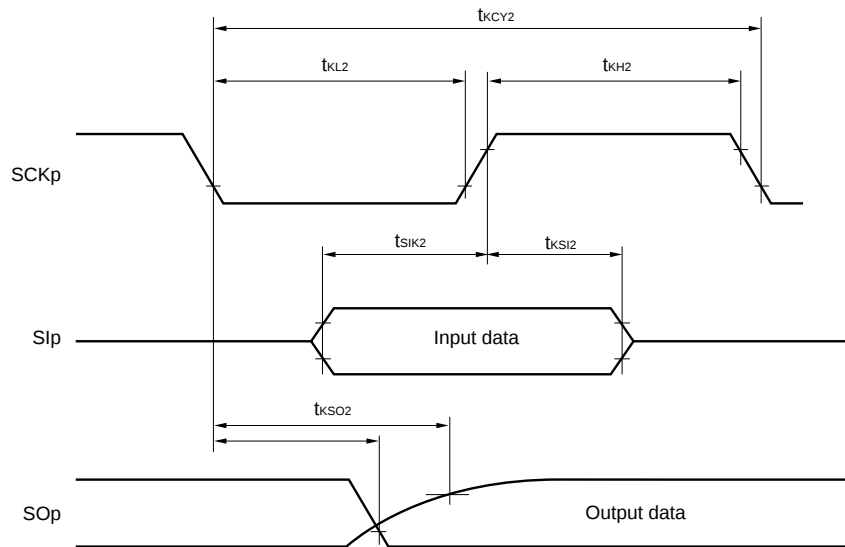
Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

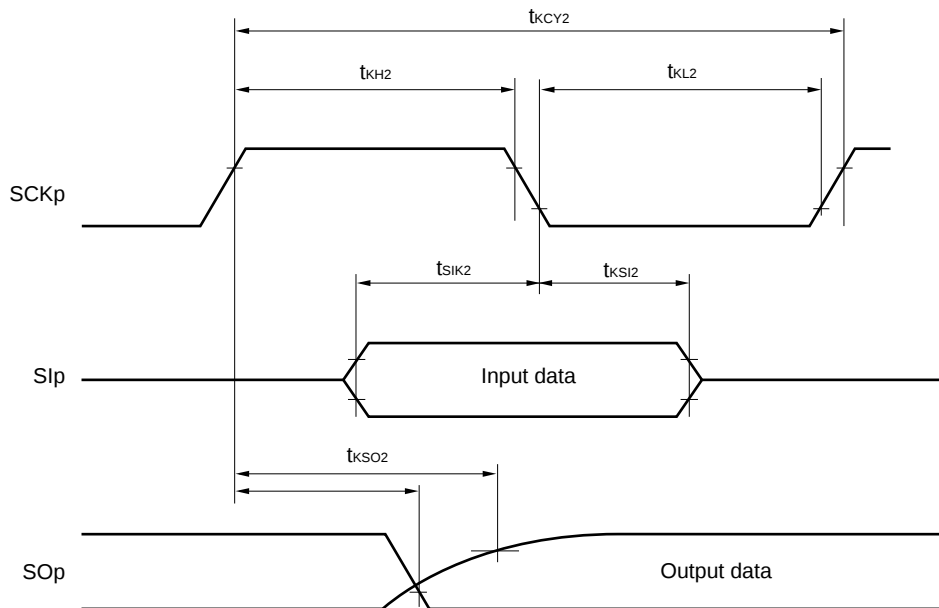


- Remarks**
1. $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number ($p = 00$), m: Unit number, n: Channel number ($mn = 00$), g: PIM and POM number ($g = 0, 3, 5, 7$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number ($mn = 00$))
 4. CSI01 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number ($p = 00$), m: Unit number, n: Channel number ($mn = 00$),
g: PIM and POM number ($g = 0, 3, 5, 7$)
 2. CSI01 cannot communicate at different potential. Use other CSI for communication at different potential.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)**(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f _{SCL}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 ^{Note 1}	kHz
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 ^{Note 1}	kHz
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		400 ^{Note 1}	kHz
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		400 ^{Note 1}	kHz
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ		300 ^{Note 1}	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	475		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	475		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1150		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1150		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	1550		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	245		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	200		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	675		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	600		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	610		ns

(Notes, Caution and Remarks are listed on the next page.)

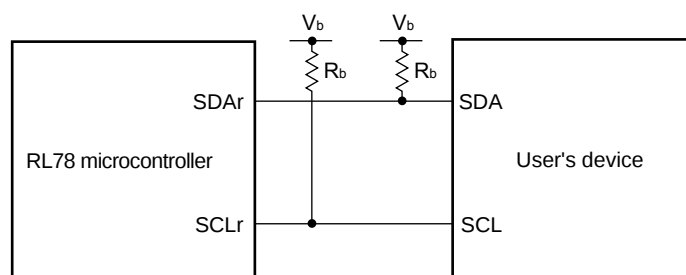
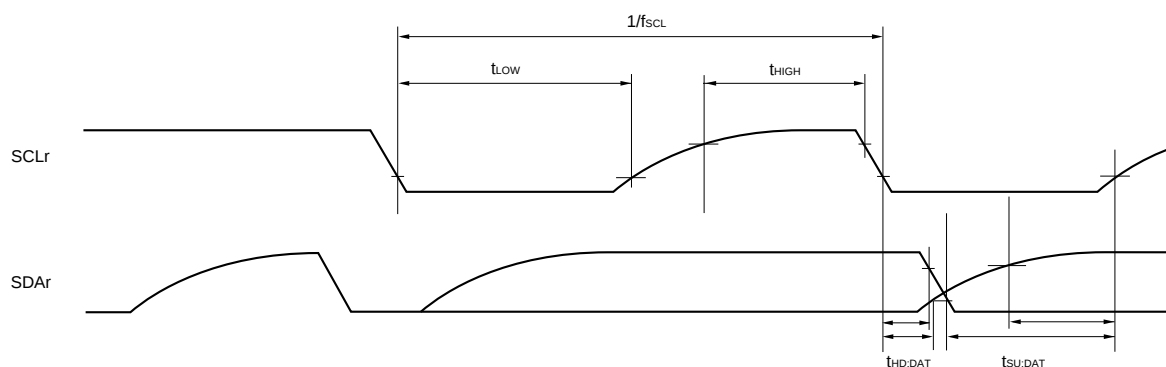
(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data setup time (reception)	t _{SU:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 Note 3		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 Note 3		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 190 Note 3		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 190 Note 3		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 190 Note 3		ns
Data hold time (transmission)	t _{HD:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	355	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	355	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	0	405	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.2. Use it with V_{DD} ≥ V_b.3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 2. r: IIC number (r = 00), g: PIM, POM number (g = 0, 3, 5, 7)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

2.5.2 Serial interface IICA

(1) I²C standard mode(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Standard mode: f _{CLK} ≥ 1 MHz	2.7 V ≤ V _{DD} ≤ 5.5 V	0	100	kHz
			2.4 V ≤ V _{DD} ≤ 5.5 V	0	100	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		4.7		μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		4.0		μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		4.7		μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		4.0		μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V		250		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		250		μs
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V		0	3.45	μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		0	3.45	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		4.0		μs
Bus-free time	t _{BUF}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		4.7		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the $\overline{\text{ACK}}$ (acknowledge) timing.

Caution The values in the above table are applied even when bit 1 (PIOR1) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I²C fast mode(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz	2.7 V ≤ V _{DD} ≤ 5.5 V	0	400	kHz
			2.4 V ≤ V _{DD} ≤ 5.5 V	0	400	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		0.6		μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 5.5 V		1.3		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		1.3		μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		0.6		μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V		100		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V		0	0.9	μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		0	0.9	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		0.6		μs
Bus-free time	t _{BUF}	2.7 V ≤ V _{DD} ≤ 5.5 V		1.3		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 1 (PIOR1) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

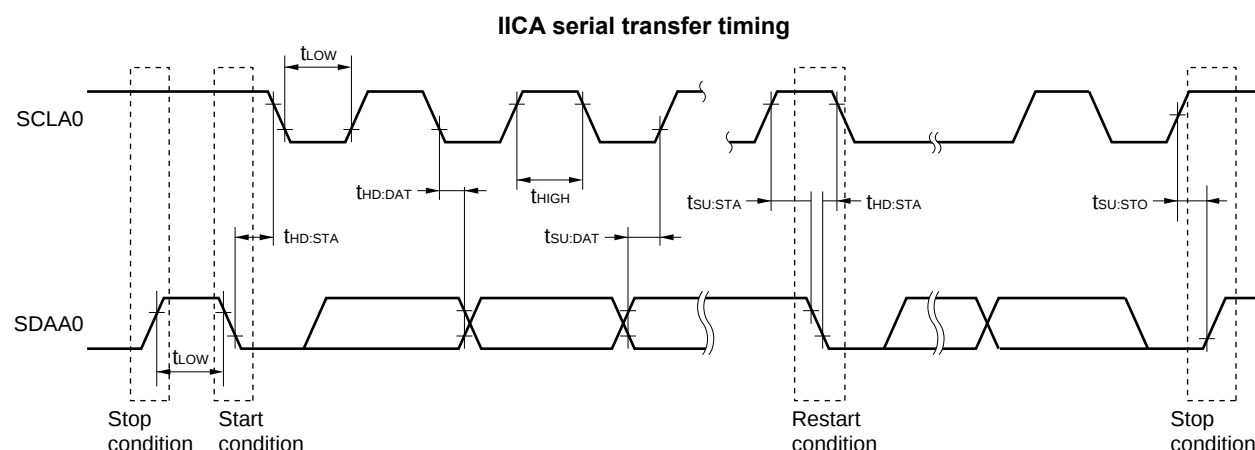
(3) I²C fast mode plus(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode plus: f _{CLK} ≥ 10 MHz	2.7 V ≤ V _{DD} ≤ 5.5 V	0	1000	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.26		μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.26		μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.5		μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.26		μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V		50		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V		0	0.45	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.26		μs
Bus-free time	t _{BUF}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.5		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 1 (PIOR1) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

2.5.3 USB

(1) Electrical specifications

(T_A = -40 to +85°C, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

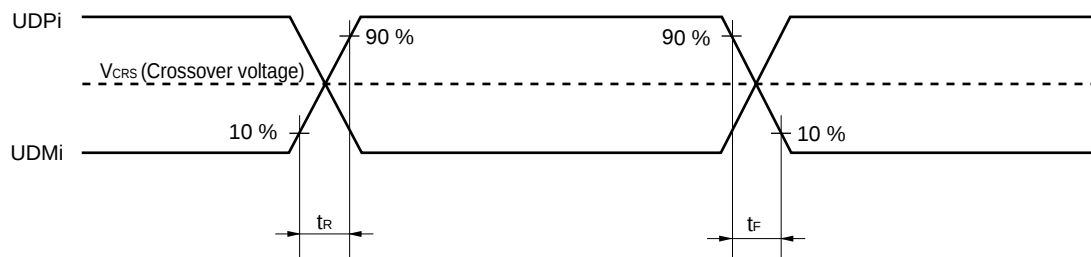
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UV _{DD}	UV _{DD} input voltage characteristic	UV _{DD}	V _{DD} = 3.0 to 5.5 V, PXXCON = 1, VDDUSEB = 0 (UV _{DD} ≤ V _{DD})	3.0	3.3	3.6	V
	UV _{DD} output voltage characteristic	UV _{DD}	V _{DD} = 4.0 to 5.5 V, PXXCON = VDDUSEB = 1	3.0	3.3	3.6	V
UV _{BUS}	UV _{BUS} input voltage characteristic	UV _{BUS}	Function	4.35 (4.02 ^{Note})	5.00	5.25	V
			Host	4.75	5.00	5.25	V

Note Value of instantaneous voltage(T_A = -40 to +85°C, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDPi/UDMi pins input characteristic (FS/LS receiver)	Input voltage	V _{IH}		2.0			V
		V _{IL}				0.8	V
	Difference input sensitivity	V _{DI}	UDP voltage – UDM voltage	0.2			V
	Difference common mode range	V _{CM}		0.8		2.5	V
UDPi/UDMi pins output characteristic (FS driver)	Output voltage	V _{OH}	I _{OH} = -200 μA	2.8		3.6	V
		V _{OL}	I _{OL} = 2.4 mA	0		0.3	V
	Transi-ti on time	t _{FR}	Rising: From 10% to 90 % of amplitude,	4		20	ns
		t _{FF}	Falling: From 90% to 10 % of amplitude,	4		20	ns
	Matching (TFR/TFF)	V _{FRFM}	CL = 50 pF	90		111.1	%
	Crossover voltage	V _{FCRS}		1.3		2.0	V
	Output Impedance	Z _{DRV}	UV _{DD} voltage = 3.3 V, Pin voltage = 1.65 V	28		44	Ω
UDPi/UDMi pins output characteristic (LS driver)	Output voltage	V _{OH}		2.8		3.6	V
		V _{OL}		0		0.3	V
	Transi-ti on time	t _{LR}	Rising: From 10% to 90 % of amplitude,	75		300	ns
		t _{LF}	Falling: From 90% to 10 % of amplitude,	75		300	ns
	Matching (TFR/TFF) Note	V _{LTFM}	CL = 200 to 600 pF	80		125	%
	Crossover voltage Note	V _{LCRS}	When the host controller function is selected: The UDMi pin (i = 0, 1) is pulled up via 1.5 kΩ. When the function controller function is selected: The UDP0 and UDM0 pins are individually pulled down via 15 kΩ	1.3		2.0	V
UDPi/UDMi pins pull-up, pull-down	Pull-down resistor	R _{PD}		14.25		24.80	kΩ
	Pull-up resistor (i = 0 only)	R _{PUI}	Idle	0.9		1.575	kΩ
		R _{PUA}	Recep-t ion	1.425		3.09	kΩ
UV _{BUS}	UV _{BUS} pull-down resistor	R _{VBUS}	UV _{BUS} voltage = 5.5 V		1000		kΩ
	UV _{BUS} input voltage	V _{IH}		3.20			V
		V _{IL}				0.8	V

Note Excludes the first signal transition from the idle state.**Remark** i = 0, 1

Timing of UDPI and UDMI



(2) BC standard

(
 $T_A = -40$ to $+85^\circ\text{C}$, $3.0\text{ V} \leq UV_{DD} \leq 3.6\text{ V}$, $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USB standard BC1.2	UDPi sink current	I_{DP_SINK}		25		175	μA
	UDMi sink current	I_{DM_SINK}		25		175	μA
	DCD source current	I_{DP_SRC}		7		13	μA
	Dedicated charging port resistor	R_{DCP_DAT}	$0\text{ V} < \text{UDP/UDM voltage} < 1.0\text{ V}$			200	Ω
	Data detection voltage	V_{DAT_REF}		0.25		0.4	V
	UDPi source voltage	V_{DP_SRC}	Output current $250\text{ }\mu\text{A}$	0.5		0.7	V
	UDMi source voltage	V_{DM_SRC}	Output current $250\text{ }\mu\text{A}$	0.5		0.7	V

Remark $i = 0, 1$

(3) BC option standard (Host)

(T_A = -40 to +85°C, 4.75 V ≤ UV_{BUS} ≤ 5.25 V, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDPi output voltage (UV _{BUS} divider ratio) • VDOUEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V _{P20}		38	40	42	% UV _{BUS}
		1001	V _{P27}		51.6	53.6	55.6	% UV _{BUS}
		1010	V _{P20}		38	40	42	% UV _{BUS}
		1100	V _{P33}		60	66	72	% UV _{BUS}
UDMi output voltage (UV _{BUS} divider ratio) • VDOUEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V _{M20}		38	40	42	% UV _{BUS}
		1001	V _{M20}		38	40	42	% UV _{BUS}
		1010	V _{M27}		51.6	53.6	55.6	% UV _{BUS}
		1100	V _{M33}		60	66	72	% UV _{BUS}
UDPi comparing voltage Note 1 (UV _{BUS} divider ratio) • VDOUEi = 1 • CUSDETEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V _{HDETP_UP0}	The rise of pin voltage detection voltage	56.2			% UV _{BUS}
			V _{HDETP_DWN0}	The fall of pin voltage detection voltage			29.4	% UV _{BUS}
		1001	V _{HDETP_UP1}	The rise of pin voltage detection voltage	60.5			% UV _{BUS}
			V _{HDETP_DWN1}	The fall of pin voltage detection voltage			45.0	% UV _{BUS}
		1010	V _{HDETP_UP2}	The rise of pin voltage detection voltage	56.2			% UV _{BUS}
			V _{HDETP_DWN2}	The fall of pin voltage detection voltage			29.4	% UV _{BUS}
UDMi comparing voltage Note 1 (UV _{BUS} divider ratio) • VDOUEi = 1 • CUSDETEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V _{HDETM_UP0}	The rise of pin voltage detection voltage	56.2			% UV _{BUS}
			V _{HDETM_DWN0}	The fall of pin voltage detection voltage			29.4	% UV _{BUS}
		1001	V _{HDETM_UP1}	The rise of pin voltage detection voltage	56.2			% UV _{BUS}
			V _{HDETM_DWN1}	The fall of pin voltage detection voltage			29.4	% UV _{BUS}
		1010	V _{HDETM_UP2}	The rise of pin voltage detection voltage	60.5			% UV _{BUS}
			V _{HDETM_DWN2}	The fall of pin voltage detection voltage			45.0	% UV _{BUS}
UDPi pull-up detection Note 2 Connect detection with the full speed function (pull-up resistor)		1000	R _{HDET_PULL}	In full-speed mode, the power supply voltage range of pull-up resistors connected to the USB function module is between 3.0 V and 3.6 V.			1.575	kΩ
		1001						
		1010						
UDMi pull-up detection Note 2 Connect detection with the low-speed (pull-up resistor)		1000	R _{HDET_PULL}	In low-speed mode, the power supply voltage range of pull-up resistors connected to the USB function module is between 3.0 V and 3.6 V.			1.575	kΩ
		1001						
		1010						
UDMi sink current detection Note 2 Connect detection with the BC1.2 portable device (sink resistor)		1000	I _{HDET_SINK}		25			μA
		1001						
		1010						

Notes 1. If the voltage output from UDPi or UDMi (i = 0, 1) exceeds the range of the MAX and MIN values prescribed in this specification, DPCUSDETi (bit 8) and DMCUSDETi (bit 9) of the USBBCOPTi register are set to 1.

2. If the pull-up resistance or sink current prescribed in this specification is applied to UDPi or UDMi (i = 0, 1), DPCUSDETi (bit 8) and DMCUSDETi (bit 9) of the USBBCOPTi register are set to 1.

Remark i = 0, 1

(4) BC option standard (Function)

(T_A = -40 to $+85^{\circ}\text{C}$, $4.35\text{ V} \leq \text{UV}_{\text{BUS}} \leq 5.25\text{ V}$, $3.0\text{ V} \leq \text{UV}_{\text{DD}} \leq 3.6\text{ V}$, $2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = 0\text{ V}$)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDPi/UDMi input reference voltage (UV _{BUS} divider ratio) • VDOUEi = 0 (i = 0))	VDSELi [3:0] (i = 0)	0000	V _{DDDET0}		27	32	37	% UV _{BUS}
		0001	V _{DDDET1}		29	34	39	% UV _{BUS}
		0010	V _{DDDET2}		32	37	42	% UV _{BUS}
		0011	V _{DDDET3}		35	40	45	% UV _{BUS}
		0100	V _{DDDET4}		38	43	48	% UV _{BUS}
		0101	V _{DDDET5}		41	46	51	% UV _{BUS}
		0110	V _{DDDET6}		44	49	54	% UV _{BUS}
		0111	V _{DDDET7}		47	52	57	% UV _{BUS}
		1000	V _{DDDET8}		51	56	61	% UV _{BUS}
		1001	V _{DDDET9}		55	60	65	% UV _{BUS}
		1010	V _{DDDET10}		59	64	69	% UV _{BUS}
		1011	V _{DDDET11}		63	68	73	% UV _{BUS}
		1100	V _{DDDET12}		67	72	77	% UV _{BUS}
		1101	V _{DDDET13}		71	76	81	% UV _{BUS}
		1110	V _{DDDET14}		75	80	85	% UV _{BUS}
		1111	V _{DDDET15}		79	84	89	% UV _{BUS}

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (–) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (–) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (–) = AV_{REFM}
ANI0 to ANI7	Refer to 2.6.1 (1).	Refer to 2.6.1 (3).	Refer to 2.6.1 (4).
ANI16, ANI17, ANI19	Refer to 2.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 2.6.1 (1).		–

(1) When $AV_{REF (+)} = AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (–) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin : ANI2 to ANI7, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^{\circ}\text{C}$, $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (–) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 3.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2 to ANI7 $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.25	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.25	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 1.5	LSB
Analog input voltage	V_{AIN}	ANI2 to ANI7	0		AV_{REFP}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)	V_{BGR} ^{Note 4}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)	V_{TMPS25} ^{Note 4}			V

(Notes are listed on the next page.)

- Notes**
1. Excludes quantization error ($\pm 1/2$ LSB).
 2. This value is indicated as a ratio (%FSR) to the full-scale value.
 3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 4. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin : ANI16, ANI17, ANI19

(T_A = -40 to +85°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	2.4 V ≤ V _{DD} ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	t _{CONV}	10-bit resolution Target ANI pin : ANI16, ANI17, ANI19	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.35	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.35	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	2.4 V ≤ V _{DD} ≤ 5.5 V			±3.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	2.4 V ≤ V _{DD} ≤ 5.5 V			±2.00	LSB
Analog input voltage	V _{AIN}	ANI16, ANI17, ANI19		0		AV_{REFP} and V _{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

- (3) Reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), Reference voltage (–) = V_{SS} (ADREFM = 0), target ANI pin : ANI0 to ANI7, ANI16, ANI17, ANI19, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^{\circ}\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error ^{Notes 1, 2}	A_{INL}	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin : ANI0 to ANI7, ANI16, ANI17, ANI19	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
		10-bit resolution Target ANI pin : Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Full-scale error ^{Notes 1, 2}	E_{FS}	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	I_{LE}	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 4.0	LSB
Differential linearity error ^{Note 1}	D_{LE}	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI7, ANI16, ANI17, ANI19		0		V_{DD}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{BGR} ^{Note 3}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{TMPS25} ^{Note 3}			V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

(4) When Reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), Reference voltage (–) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin : ANI0 to ANI7, ANI16, ANI17, ANI19

($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{BGR} ^{Note 3}, Reference voltage (–) = AV_{REFM} ^{Note 4} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			Bit
Conversion time	t_{CONV}	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS} , the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the MAX. value when reference voltage (–) = AV_{REFM} .

Integral linearity error: Add ± 0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM} .

Differential linearity error: Add ± 0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM} .

2.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = -40 to $+85^{\circ}\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

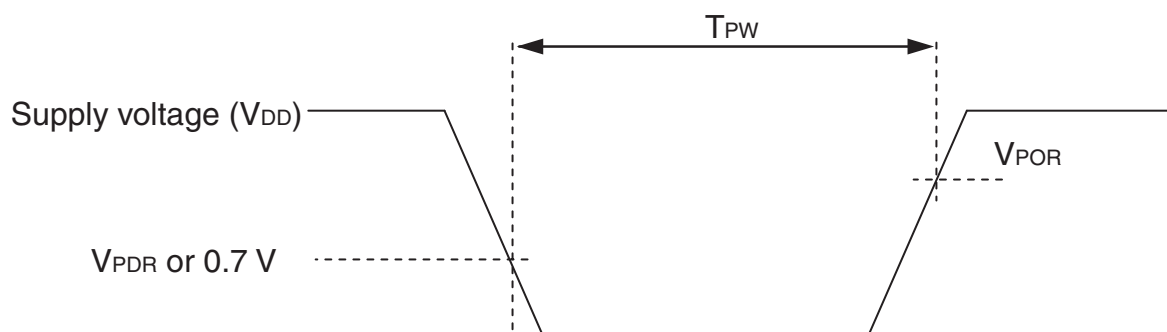
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V _{TMP25}	Setting ADS register = 80H, T _A = $+25^{\circ}\text{C}$		1.05		V
Internal reference voltage	V _{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F _{VTMP25}	Temperature sensor that depends on the temperature		-3.6		mV/ $^{\circ}\text{C}$
Operation stabilization wait time	t _{AMP}		5			μs

2.6.3 POR circuit characteristics

(T_A = -40 to $+85^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{POR}	Power supply rise time	1.47	1.51	1.55	V
	V _{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width ^{Note}	T _{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock (f_{MAIN}) is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode(T_A = -40 to +85°C, V_{PDR} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Detection voltage	Supply voltage level	VLVD0	Power supply rise time	3.98	4.06	4.14	V		
			Power supply fall time	3.90	3.98	4.06	V		
		VLVD1	Power supply rise time	3.68	3.75	3.82	V		
			Power supply fall time	3.60	3.67	3.74	V		
		VLVD2	Power supply rise time	3.07	3.13	3.19	V		
			Power supply fall time	3.00	3.06	3.12	V		
		VLVD3	Power supply rise time	2.96	3.02	3.08	V		
			Power supply fall time	2.90	2.96	3.02	V		
		VLVD4	Power supply rise time	2.86	2.92	2.97	V		
			Power supply fall time	2.80	2.86	2.91	V		
		VLVD5	Power supply rise time	2.76	2.81	2.87	V		
			Power supply fall time	2.70	2.75	2.81	V		
		VLVD6	Power supply rise time	2.66	2.71	2.76	V		
			Power supply fall time	2.60	2.65	2.70	V		
		VLVD7	Power supply rise time	2.56	2.61	2.66	V		
			Power supply fall time	2.50	2.55	2.60	V		
		VLVD8	Power supply rise time	2.45	2.50	2.55	V		
			Power supply fall time	2.40	2.45	2.50	V		
		Minimum pulse width		tLW		300			μs
		Detection delay time		tLD				300	μs

LVD Detection Voltage of Interrupt & Reset Mode**($T_A = -40$ to $+85^{\circ}\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V _{LVDC0}	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	V _{LVDC1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V _{LVDC2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V _{LVDC3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	V _{LVDD0}	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V _{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	V _{LVDD3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

2.6.5 Power supply voltage rising slope characteristics**($T_A = -40$ to $+85^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

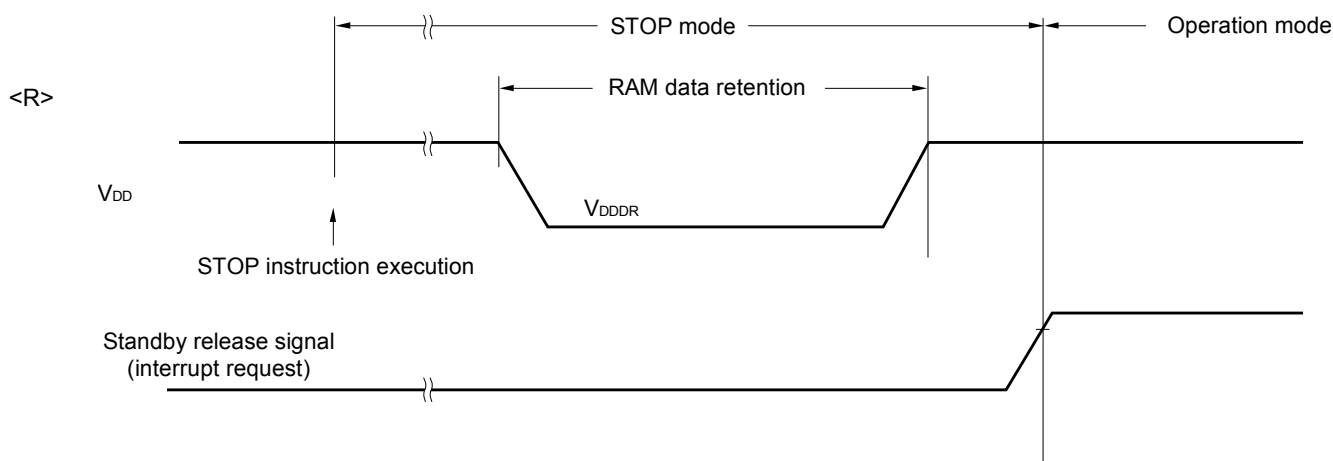
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 30.4 AC Characteristics.

<R> 2.7 RAM Data Retention Characteristics

 $(T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 ^{Note}		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



2.8 Flash Memory Programming Characteristics

 $(T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		24	MHz
<R> Number of code flash rewrites	C_{erwr}	Retaining years: 20 years $T_A = +85^\circ\text{C}$	1,000			Times
<R> Number of data flash rewrites Notes 1, 2, 3		Retaining years: 1 year $T_A = +25^\circ\text{C}$		1,000,000		
<R>		Retaining years: 5 years $T_A = +85^\circ\text{C}$	100,000			
<R>		Retaining years: 20 years $T_A = +85^\circ\text{C}$	10,000			

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
 2. When using flash memory programmer and Renesas Electronics self programming library.
 3. These specifications show the characteristics of the flash memory and the results obtained from Renesas Electronics reliability testing.

2.9 Dedicated Flash Memory Programmer Communication (UART)

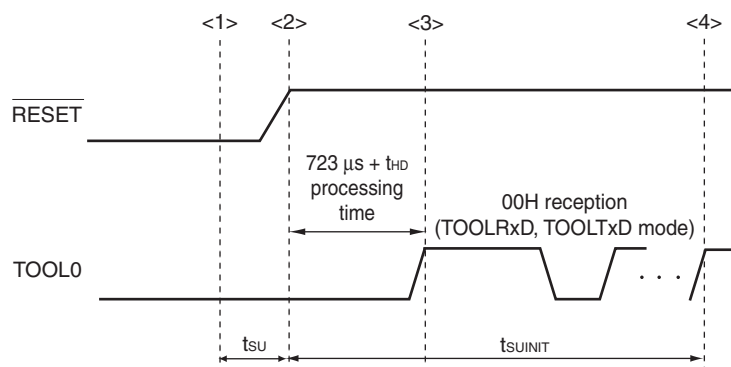
 $(T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing Specs for Switching Flash Memory Programming Modes

(T_A = -40 to $+85^{\circ}\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t _{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t _{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t _{HD}	POR and LVD reset must end before the external reset ends.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset ends (POR and LVD reset must end before the external reset ends.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until an external reset ends

t_{HD}: How long to keep the TOOL0 pin at the low level from when the external and internal resets end (excluding the processing time of the firmware to control the flash memory)

3. ELECTRICAL SPECIFICATIONS (G: T_A = -40 to +105°C)

This chapter describes the electrical specifications for the products "G: Industrial applications (T_A = -40 to +105°C)".

The target products

G: Industrial applications ; T_A = -40 to +105°C

R5F10JBCGNA, R5F10JBCGFP, R5F10JGCGNA, R5F10JGCGFB,

R5F10KBCGNA, R5F10KBCGFP, R5F10KGCGNA, R5F10KGCGFB

Cautions 1. The RL78 microcontrollers has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product.

3. Please contact Renesas Electronics sales office for derating of operation under T_A = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

There are following differences between the products "G: Industrial applications (T_A = -40 to +105°C)" and the products "A: Consumer applications".

Parameter	Application	
	A: Consumer applications	G: Industrial applications
Operating ambient temperature	T _A = -40 to +85°C	T _A = -40 to +105°C
High-speed on-chip oscillator clock accuracy	2.4 V ≤ V _{DD} ≤ 5.5 V ±1.0% @ T _A = -20 to +85°C ±1.5% @ T _A = -40 to -20°C	2.4 V ≤ V _{DD} ≤ 5.5 V ±2.0% @ T _A = +85 to +105°C ±1.0% @ T _A = -20 to +85°C ±1.5% @ T _A = -40 to -20°C
Serial array unit	UART CSI: f _{CLK} /2 (supporting 16 Mbps), f _{CLK} /4 Simplified I ² C communication	UART CSI: f _{CLK} /4 Simplified I ² C communication
IICA	Normal mode Fast mode Fast mode plus	Normal mode Fast mode

Remark The electrical characteristics of the products G: Industrial applications (T_A = -40 to +105°C) are different from those of the products "A: Consumer applications". For details, refer to 3.1 to 3.10.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
REGC pin input voltage	V _{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V _{DD} +0.3 ^{Note 1}	V
UV _{DD} pin input voltage	V _{IUVDD}	UV _{DD}	-0.3 to V _{DD} +0.3	V
Input voltage	V _{I1}	P00, P01, P14 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P70 to P75, P120 to P124, P137, P140, EXCLK, EXCLKS, RESET	-0.3 to V _{DD} +0.3 ^{Note 2}	V
	V _{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V _{I3}	UDP0, UDM0, UDP1, UDM1	-0.3 to +6.5	V
	V _{I4}	UV _{BUS}	-0.3 to +6.5	V
Output voltage	V _{O1}	P00, P01, P14 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P130, P140	-0.3 to V _{DD} +0.3 ^{Note 2}	V
	V _{O2}	UDP0, UDM0, UDP1, UDM1	-0.3 to +6.5	V
Analog input voltage	V _{AI1}	ANI16, ANI17, ANI19	-0.3 to V _{DD} +0.3 and -0.3 to AV _{REF} (+) +0.3 Notes 2, 3	V
	V _{AI2}	ANI0 to ANI7	-0.3 to V _{DD} +0.3 and -0.3 to AV _{REF} (+) +0.3 Notes 2, 3	V

- Notes 1.** Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
- 2.** Must be 6.5 V or lower.
- 3.** Do not exceed AV_{REF}(+) + 0.3 V in case of A/D conversion target pin

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
- 2.** AV_{REF} (+) : The + side reference voltage of the A/D converter. This can be selected from AV_{REFP}, the internal reference voltage (1.45 V), and V_{DD}.
- 3.** V_{SS} : Reference voltage

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	−40	mA
		Total of all pins −170 mA	P00, P01, P40, P41, P120, P130, P140	−70	mA
			P14 to P17, P30, P31, P50, P51, P70 to P75	−100	mA
	I _{OH2}	Per pin	P20 to P27	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I _{OL1}	Per pin	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P130, P140	40	mA
		Total of all pins 170 mA	P00, P01, P40, P41, P120, P130, P140	70	mA
			P14 to P17, P30, P31, P50, P51, P60 to P63, P70 to P75	100	mA
	I _{OL2}	Per pin	P20 to P27	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T _A	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	T _{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.2 Oscillator Characteristics

3.2.1 X1, XT1 oscillator characteristics

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f _X) ^{Note}	Ceramic resonator/ crystal resonator	2.7 V ≤ V _{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V	1.0		16.0	MHz
XT1 clock oscillation frequency (f _{XT}) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

3.2.2 On-chip oscillator characteristics

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f _{HOCO}		1		48	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85 °C	-1.0		+1.0	%
		-40 to -20 °C	-1.5		+1.5	%
		+85 to +105 °C	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f _{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

3.2.3 PLL oscillator characteristics

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
PLL input frequency ^{Note}	f _{PLLIN}	High-speed system clock	6.00		16.00	MHz
PLL output frequency ^{Note}	f _{PLL}			48.00		MHz
Lock up time		From PLL output enable to stabilization of the output frequency	40.00			μs
Interval time		From PLL stop to PLL re-operation setting Wait time	4.00			μs
Setting wait time		From after PLL input clock stabilization and PLL setting is fixed to start setting Wait time required	1.00			μs

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

3.3 DC Characteristics

3.3.1 Pin characteristics

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	2.4 V ≤ V _{DD} ≤ 5.5 V		-3.0 ^{Note 2}	mA
		Total of P00, P01, P40, P41, P120, P130, P140 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V		-30.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		-10.0	mA
			2.4 V ≤ V _{DD} < 2.7 V		-5.0	mA
		Total of P14 to P17, P30, P31, P50, P51, P70 to P75 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V		-30.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		-19.0	mA
			2.4 V ≤ V _{DD} < 2.7 V		-10.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ V _{DD} ≤ 5.5 V		-60.0	mA
	I _{OH2}	Per pin for P20 to P27	2.4 V ≤ V _{DD} ≤ 5.5 V		-0.1 ^{Note 2}	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ V _{DD} ≤ 5.5 V		-1.5	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty ratio to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7) / (80 \times 0.01) \cong -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P01, P30, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	I _{OL1}	Per pin for P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	2.4V ≤ V _{DD} ≤ 5.5 V		8.5 ^{Note 2}	mA
		Per pin for P60 to P63	2.4V ≤ V _{DD} ≤ 5.5 V		15.0 ^{Note 2}	mA
		Total of P00, P01, P40, P41, P120, P130, P140 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V		40.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		15.0	mA
			2.4 V ≤ V _{DD} < 2.7 V		9.0	mA
		Total of P14 to P17, P30, P31, P50, P51, P60 to P63, P70 to P75 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V		40.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		35.0	mA
			2.4 V ≤ V _{DD} < 2.7 V		20.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4V ≤ V _{DD} ≤ 5.5 V		80.0	mA
	I _{OL2}	Per pin for P20 to P27	2.4V ≤ V _{DD} ≤ 5.5 V		0.4 ^{Note 2}	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4V ≤ V _{DD} ≤ 5.5 V		5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty ratio to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \cong 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140	Normal input buffer	0.8V _{DD}	V _{DD}	V
	V _{IH2}	P00, P01, P30, P50	TTL input buffer 4.0 V ≤ V _{DD} ≤ 5.5 V	2.2	V _{DD}	V
			TTL input buffer 3.3 V ≤ V _{DD} < 4.0 V	2.0	V _{DD}	V
			TTL input buffer 2.4 V ≤ V _{DD} < 3.3 V	1.5	V _{DD}	V
	V _{IH3}	P20 to P27	0.7V _{DD}		V _{DD}	V
	V _{IH4}	P60 to P63	0.7V _{DD}		6.0	V
	V _{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	0.8V _{DD}		V _{DD}	V
Input voltage, low	V _{IL1}	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140	Normal input buffer	0	0.2V _{DD}	V
	V _{IL2}	P00, P01, P30, P50	TTL input buffer 4.0 V ≤ V _{DD} ≤ 5.5 V	0	0.8	V
			TTL input buffer 3.3 V ≤ V _{DD} < 4.0 V	0	0.5	V
			TTL input buffer 2.4 V ≤ V _{DD} < 3.3 V	0	0.32	V
	V _{IL3}	P20 to P27	0		0.3V _{DD}	V
	V _{IL4}	P60 to P63	0		0.3V _{DD}	V
	V _{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	0		0.2V _{DD}	V

Caution The maximum value of V_{IH} of pins P00, P01, P30, and P74 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V _{OH1}	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -3.0\text{ mA}$	$V_{DD} - 0.7$		V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -2.0\text{ mA}$	$V_{DD} - 0.6$		V
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -1.5\text{ mA}$	$V_{DD} - 0.5$		V
	V _{OH2}	P20 to P27	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH2} = -100\text{ }\mu\text{A}$	$V_{DD} - 0.5$		V
Output voltage, low	V _{OL1}	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 8.5\text{ mA}$		0.7	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 1.5\text{ mA}$		0.4	V
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 0.6\text{ mA}$		0.4	V
	V _{OL2}	P20 to P27	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL2} = 400\text{ }\mu\text{A}$		0.4	V
	V _{OL3}	P60 to P63	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 15.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 3.0\text{ mA}$		0.4	V
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 2.0\text{ mA}$		0.4	V

Caution P00, P01, P30, and P74 do not output high level in N-ch open-drain mode.**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	I _{LIH1}	P00, P01, P14 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P137, P140, RESET	V _I = V _{DD}		1	μA		
	I _{LIH2}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port or external clock input	1	μA		
				In resonator connection	10	μA		
Input leakage current, low	I _{LIL1}	P00, P01, P14 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P137, P140, RESET	V _I = V _{SS}		−1	μA		
	I _{LIL2}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port or external clock input	−1	μA		
				In resonator connection	−10	μA		
On-chip pll-up resistance	R _U	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140	V _I = V _{SS} , In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

(1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current Note 1	I _{DD1}	Operating mode	HS (High-speed main) mode Note 6	f _{HOCO} = 48 MHz f _{IH} = 24 MHz Note 3	Basic operation	V _{DD} = 5.0 V		1.7		mA	
						V _{DD} = 3.0 V		1.7		mA	
					Normal operation	V _{DD} = 5.0 V		3.7	5.8	mA	
						V _{DD} = 3.0 V		3.7	5.8	mA	
				f _{HOCO} = 24 MHz f _{IH} = 12 MHz Note 3	Normal operation	V _{DD} = 5.0 V		2.3	3.4	mA	
						V _{DD} = 3.0 V		2.3	3.4	mA	
				f _{HOCO} = 12 MHz f _{IH} = 6 MHz Note 3	Normal operation	V _{DD} = 5.0 V		1.6	2.2	mA	
						V _{DD} = 3.0 V		1.6	2.2	mA	
				f _{HOCO} = 6 MHz f _{IH} = 3 MHz Note 3	Normal operation	V _{DD} = 5.0 V		1.2	1.6	mA	
						V _{DD} = 3.0 V		1.2	1.6	mA	
				HS (High-speed main) mode Note 6	f _{MX} = 20 MHz V _{DD} = 5.0 V Note 2	Normal operation	Square wave input		3.0	4.9	mA
							Resonator connection		3.2	5.0	mA
					f _{MX} = 20 MHz V _{DD} = 3.0 V Note 2	Normal operation	Square wave input		3.0	4.9	mA
							Resonator connection		3.2	5.0	mA
			f _{MX} = 10 MHz V _{DD} = 5.0 V Note 2		Normal operation	Square wave input		1.9	2.9	mA	
						Resonator connection		1.9	2.9	mA	
			f _{MX} = 10 MHz V _{DD} = 3.0 V Note 2		Normal operation	Square wave input		1.9	2.9	mA	
						Resonator connection		1.9	2.9	mA	
			HS (High-speed main) mode (PLL operation) Note 6	f _{PLL} = 48 MHz, f _{CLK} = 24 MHz Note 2	Normal operation	V _{DD} = 5.0 V		4.0	6.3	mA	
						V _{DD} = 3.0 V		4.0	6.3	mA	
				f _{PLL} = 48 MHz, f _{CLK} = 12 MHz Note 2	Normal operation	V _{DD} = 5.0 V		2.6	3.9	mA	
						V _{DD} = 3.0 V		2.6	3.9	mA	
				f _{PLL} = 48 MHz, f _{CLK} = 6 MHz Note 2	Normal operation	V _{DD} = 5.0 V		1.9	2.7	mA	
						V _{DD} = 3.0 V		1.9	2.7	mA	
			Subsystem clock operation	f _{SUB} = 32.768 kHz T _A = −40°C Note 4	Normal operation	Resonator connection		4.1	4.9	μA	
						Square wave input		4.2	5.0	μA	
				f _{SUB} = 32.768 kHz T _A = +25°C Note 4	Normal operation	Square wave input		4.1	4.9	μA	
						Resonator connection		4.2	5.0	μA	
				f _{SUB} = 32.768 kHz T _A = +50°C Note 4	Normal operation	Square wave input		4.2	5.5	μA	
						Resonator connection		4.3	5.6	μA	
				f _{SUB} = 32.768 kHz T _A = +70°C Note 4	Normal operation	Square wave input		4.2	6.3	μA	
						Resonator connection		4.3	6.4	μA	
				f _{SUB} = 32.768 kHz T _A = +85°C Note 4	Normal operation	Square wave input		4.8	7.7	μA	
						Resonator connection		4.9	7.8	μA	
f _{SUB} = 32.768 kHz T _A = +105°C Note 4	Normal operation	Square wave input			6.9	19.7	μA				
		Resonator connection			7.0	19.8	μA				

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 5. When Operating frequency setting of option byte = 48 MHz. When f_{HOCO} is divided by HOCODIV. When RDIV[1:0] = 00 (divided by 2: default).
 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 24 MHz
	2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz

- Remarks**
1. f_{HOCO}: High-speed on-chip oscillator clock frequency (Max. 48 MHz)
 2. f_{IH}: Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2, 4, or 8 (Max. 24 MHz)
 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 4. f_{PLL}: PLL oscillation frequency
 5. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 6. f_{CLK}: CPU/peripheral hardware clock frequency
 7. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C.

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (High-speed main) mode Note 9	f _{HOCO} = 48 MHz	V _{DD} = 5.0 V		0.67	2.25	mA	
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 3.0 V		0.67	2.25	mA	
				f _{HOCO} = 24 MHz ^{Note 7}	V _{DD} = 5.0 V		0.50	1.55	mA	
				f _{IH} = 12 MHz ^{Note 4}	V _{DD} = 3.0 V		0.50	1.55	mA	
				f _{HOCO} = 12 MHz ^{Note 7}	V _{DD} = 5.0 V		0.41	1.21	mA	
				f _{IH} = 6 MHz ^{Note 4}	V _{DD} = 3.0 V		0.41	1.21	mA	
				f _{HOCO} = 6 MHz ^{Note 7}	V _{DD} = 5.0 V		0.37	1.05	mA	
				f _{IH} = 3 MHz ^{Note 4}	V _{DD} = 3.0 V		0.37	1.05	mA	
				HS (High-speed main) mode Note 9	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.28	1.90	mA
						Resonator connection		0.45	2.00	mA
					f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.28	1.90	mA
						Resonator connection		0.45	2.00	mA
					f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.19	1.02	mA
						Resonator connection		0.26	1.10	mA
			f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V		Square wave input		0.19	1.02	mA	
					Resonator connection		0.26	1.10	mA	
			HS (High-speed main) mode (PLL operation) Note 9	f _{PLL} = 48 MHz, f _{CLK} = 24 MHz ^{Note 3}	V _{DD} = 5.0 V		0.91	2.74	mA	
					V _{DD} = 3.0 V		0.91	2.74	mA	
				f _{PLL} = 48 MHz, f _{CLK} = 12 MHz ^{Note 3}	V _{DD} = 5.0 V		0.85	2.31	mA	
					V _{DD} = 3.0 V		0.85	2.31	mA	
				f _{PLL} = 48 MHz, f _{CLK} = 6 MHz ^{Note 3}	V _{DD} = 5.0 V		0.82	2.07	mA	
					V _{DD} = 3.0 V		0.82	2.07	mA	
			Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 5} T _A = −40°C	Square wave input		0.25	0.57	μA	
					Resonator connection		0.44	0.76	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +25°C	Square wave input		0.30	0.57	μA	
					Resonator connection		0.49	0.76	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +50°C	Square wave input		0.33	1.17	μA	
					Resonator connection		0.63	1.36	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +70°C	Square wave input		0.46	1.97	μA	
					Resonator connection		0.76	2.16	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +85°C	Square wave input		0.97	3.37	μA	
					Resonator connection		1.16	3.56	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +105°C	Square wave input		3.01	15.37	μA	
					Resonator connection		3.20	15.56	μA	
	I _{DD3} ^{Note 6}	STOP mode Note 8	T _A = −40°C					0.18	0.50	μA
			T _A = +25°C					0.23	0.50	μA
			T _A = +50°C					0.26	1.10	μA
			T _A = +70°C					0.29	1.90	μA
			T _A = +85°C					0.90	3.30	μA
			T _A = +105°C					2.94	15.30	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, USB2.0 host/function module, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. When Operating frequency setting of option byte = 48 MHz. When f_{HOCO} is divided by HOCODIV. When RDIV[1:0] = 00 (divided by 2: default).
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
 9. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- | | |
|----------------------------|---|
| HS (high-speed main) mode: | 2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 24 MHz |
| | 2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz |

- Remarks**
1. f_{HOCO}: High-speed on-chip oscillator clock frequency (Max. 48 MHz)
 2. f_{IH}: Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2, 4, or 8 (Max. 24 MHz)
 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 4. f_{PLL}: PLL oscillation frequency
 5. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 6. f_{CLK}: CPU/peripheral hardware clock frequency
 7. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C.

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I _{FIL} ^{Note 1}				0.20		μA
RTC operating current	I _{RTC} ^{Notes 1, 2, 3}				0.02		μA
12-bit interval timer operating current	I _{IT} ^{Notes 1, 2, 4}				0.02		μA
Watchdog timer operating current	I _{WDT} ^{Notes 1, 2, 5}	f _{IL} = 15 kHz			0.22		μA
A/D converter operating current	I _{ADC} ^{Notes 1, 6}	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V		1.3	1.8	mA
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		0.5	0.8	mA
A/D converter reference voltage current	I _{ADREF} ^{Note 1}				75.0		μA
Temperature sensor operating current	I _{TMPS} ^{Note 1}				75.0		μA
LVD operating current	I _{LVD} ^{Notes 1, 7}				0.08		μA
Self-programming operating current	I _{FSP} ^{Notes 1, 9}				2.00	12.30	mA
BGO operating current	I _{BGO} ^{Notes 1, 8}				2.00	12.30	mA
SNOOZE operating current	I _{SNOZ} ^{Note 1}	ADC operation	The mode is performed ^{Note 10}		0.80	1.97	mA
			The A/D conversion operations are performed, Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		1.20	3.00	mA
		CSI operation			0.70	1.56	mA

(Notes and Remarks are listed on the next page.)

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USB operating current	I _{USBH} Note 11	During USB communication operation under the following settings and conditions (V _{DD} = 5.0 V, T _A = +25°C): - The internal power supply for the USB is used. - X1 oscillation frequency (f_x) = 12 MHz, PLL oscillation frequency (f_{PLL}) = 48 MHz - The host controller (via two ports) is set to operate in full-speed mode with four pipes (end points) used simultaneously. (PIPE4: Bulk OUT transfer (64 bytes), PIPE5: Bulk IN transfer (64 bytes), PIPE6: Interrupt OUT transfer, PIPE7: Interrupt IN transfer). - The USB ports (two ports) are individually connected to a peripheral function via a 0.5 m USB cable.		9.0		mA
	I _{USBF} Note 11	During USB communication operation under the following settings and conditions (V _{DD} = 5.0 V, T _A = +25°C): - The internal power supply for the USB is used. - X1 oscillation frequency (f_x) = 12 MHz, PLL oscillation frequency (f_{PLL}) = 48 MHz - The function controller is set to operate in full-speed mode with four pipes (end points) used simultaneously. (PIPE4: Bulk OUT transfer (64 bytes), PIPE5: Bulk IN transfer (64 bytes), PIPE6: Interrupt OUT transfer, PIPE7: Interrupt IN transfer). - The USB port (one port) is connected to the host device via a 0.5 m USB cable.		2.5		mA
	I _{SUSP} Note 12	During suspended state under the following settings and conditions (V _{DD} = 5.0 V, T _A = +25°C): - The function controller is set to full-speed mode (the UDP0 pin is pulled up). - The internal power supply for the USB is used. - The system is set to STOP mode (When the high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When the watchdog timer is stopped.). - The USB port (one port) is connected to the host device via a 0.5 m USB cable.		240		μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Current flowing to V_{DD} .
 2. When high speed on-chip oscillator and high-speed system clock are stopped.
 3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{RTC} , when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.
 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{IT} , when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.
 6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
 7. Current flowing only to the LVD circuit. The current value of the RL78/G1C is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit operates in the Operating, HALT or STOP mode.
 8. Current flowing only during data flash rewrite.
 9. Current flowing only during self programming.
 10. For shift time to the SNOOZE mode.
 11. Current consumed only by the USB module and the internal power supply for the USB.
 12. Includes the current supplied from the pull-up resistor of the UDP0 pin to the pull-down resistor of the host device, in addition to the current consumed by this MCU during the suspended state.

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

3.4 AC Characteristics

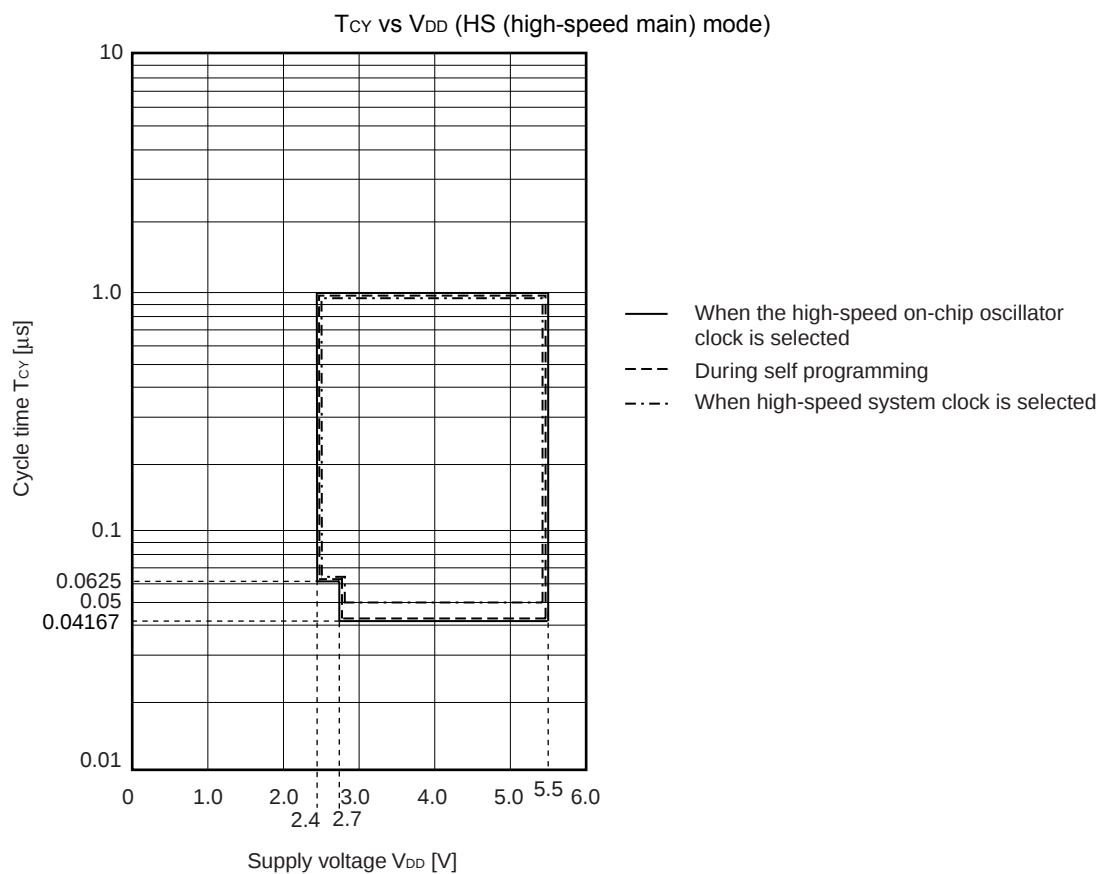
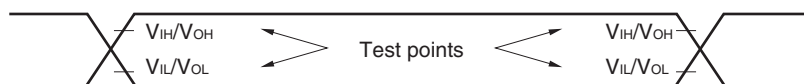
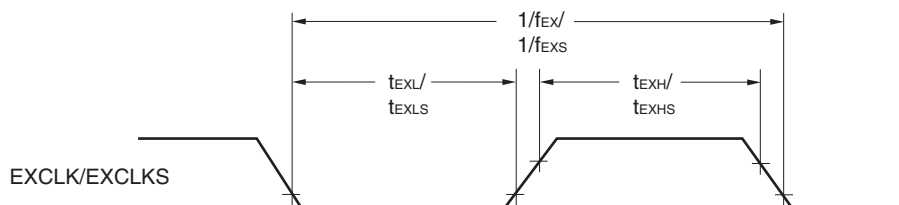
3.4.1 Basic operation

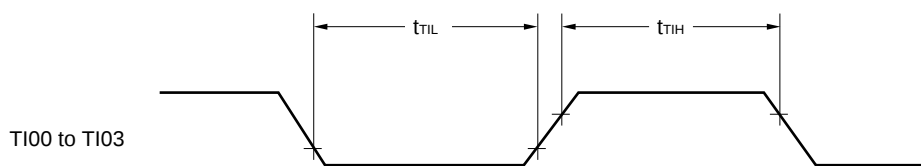
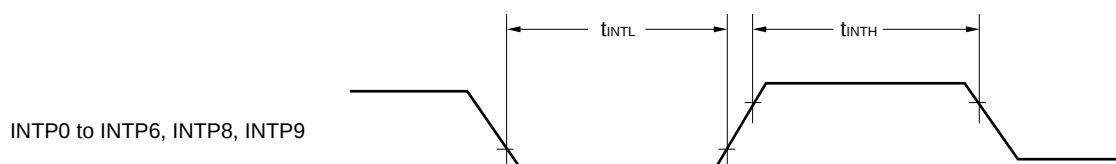
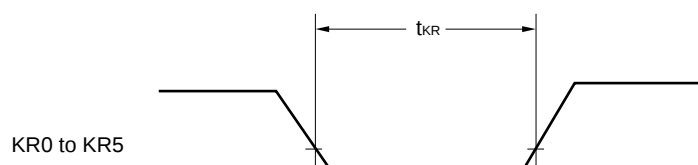
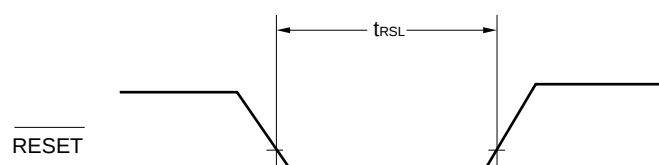
(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (High-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
		Subsystem clock (f _{SUB}) operation		2.4 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (High-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
External system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V			1.0		16.0	MHz
	f _{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V _{DD} < 2.7 V			30			ns
	t _{EXHS} , t _{EXLS}				13.7			μs
TI00 to TI03 input high-level width, low-level width	t _{TIH} , t _{TIL}				1/f _{MCK} +10			ns
TO00 to TO03 output frequency	f _{TO}	High-speed main mode	4.0 V ≤ V _{DD} ≤ 5.5 V				12	MHz
			2.7 V ≤ V _{DD} < 4.0 V				8	MHz
			2.4 V ≤ V _{DD} < 2.7 V				4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	High-speed main mode	4.0 V ≤ V _{DD} ≤ 5.5 V				16	MHz
			2.7 V ≤ V _{DD} < 4.0 V				8	MHz
			2.4 V ≤ V _{DD} < 2.7 V				4	MHz
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0 to INTP6, INTP8, INTP9	2.4 V ≤ V _{DD} ≤ 5.5 V		1			μs
Key interrupt input low-level width	t _{KR}	KR0 to KR5	2.4 V ≤ V _{DD} ≤ 5.5 V		250			ns
RESET low-level width	t _{RSL}				10			μs

Remark f_{MCK}: Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 3))

Minimum Instruction Execution Time during Main System Clock Operation**AC Timing Test Points****External System Clock Timing**

TI/TO Timing**Interrupt Request Input Timing****Key Interrupt Input Timing** **$\overline{\text{RESET}}$ Input Timing**

3.5 Peripheral Functions Characteristics

3.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					f _{MCK} /12	bps
		Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note			2.0	Mbps

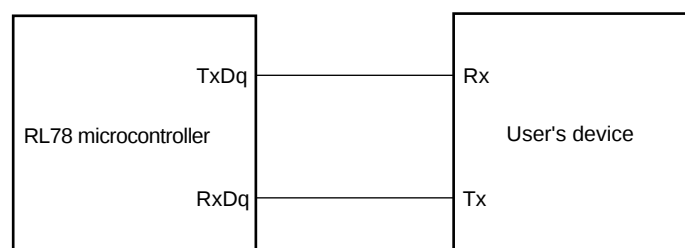
Note The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

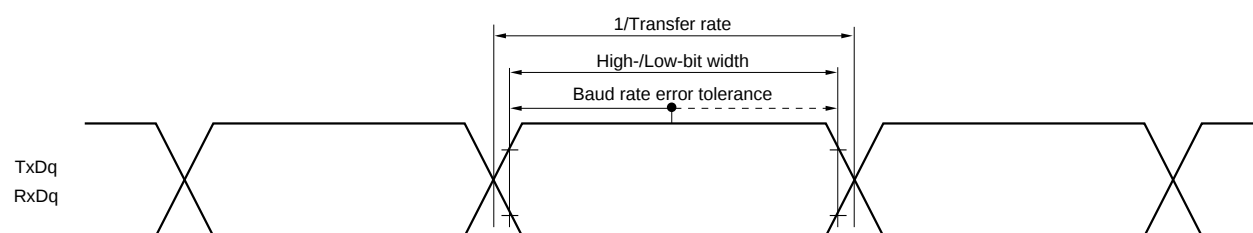
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0), g: PIM and POM number (g = 5)

2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
($T_A = -40$ to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$				
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	250			ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	500			ns
SCKp high-/low-level width	t_{KH1} , t_{KL1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{\text{KCY1}}/2 - 24$			ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{\text{KCY1}}/2 - 36$			ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{\text{KCY1}}/2 - 76$			ns
Slp setup time (to SCKp $\uparrow$) ^{Note 1}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	66			ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	66			ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	113			ns
Slp hold time (from SCKp $\uparrow$) ^{Note 2}	t_{SH1}		38			ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 3}	t_{KSO1}	$C = 30\text{ pF}$ ^{Note 4}			50	ns

- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes “to SCKp $\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp hold time becomes “from SCKp $\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 3. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from SCKp $\uparrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM numbers (g = 0, 3, 5, 7)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKS mn bit of serial mode register mn (SMR mn). m: Unit number,
n: Channel number (mn = 00, 01))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

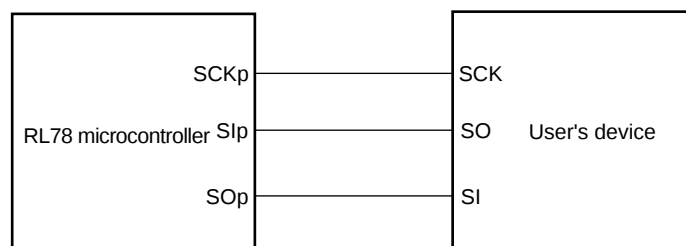
(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time ^{Note 5}	t _{KCY2}	4.0 V ≤ V _{DD} ≤ 5.5 V	20 MHz < f _{MCK}	16/f _{MCK}		ns
			f _{MCK} ≤ 20 MHz	12/f _{MCK}		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V	16 MHz < f _{MCK}	16/f _{MCK}		ns
			f _{MCK} ≤ 16 MHz	12/f _{MCK}		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V	12/f _{MCK} and 1000			ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V	t _{KCY2} /2 – 14			ns
		2.7 V ≤ EV _{DD0} ≤ 5.5 V	t _{KCY2} /2 – 16			ns
		2.4 V ≤ V _{DD} ≤ 5.5 V	t _{KCY2} /2 – 36			ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK2}	2.7 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} +40			ns
		2.4 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} +60			ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{KSI2}	2.7 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} +62			ns
		2.4 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} +62			ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO2}	C = 30 pF ^{Note 4}	2.7 V ≤ V _{DD} ≤ 5.5 V		2/f _{MCK} +66	ns
			2.4 V ≤ V _{DD} ≤ 5.5 V		2/f _{MCK} +113	ns

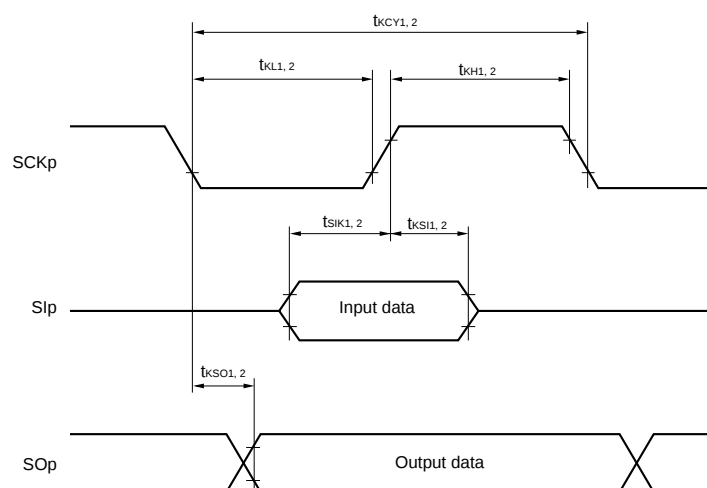
- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

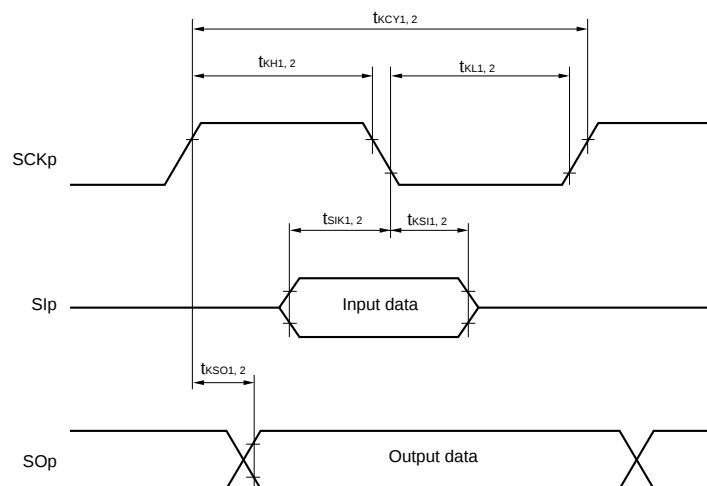
- Remarks**
1. p: CSI number (p = 00, 01), m: Unit number (m = 0),
n: Channel number (n = 0, 1), g: PIM number (g = 0, 3, 5, 7)
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 01))

CSI mode connection diagram (during communication at same potential)**CSI mode serial transfer timing (during communication at same potential)**

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

**CSI mode serial transfer timing (during communication at same potential)**

(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00, 01)
 2. m: Unit number, n: Channel number (mn = 00, 01)

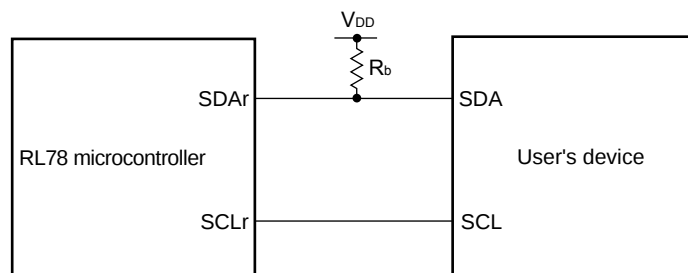
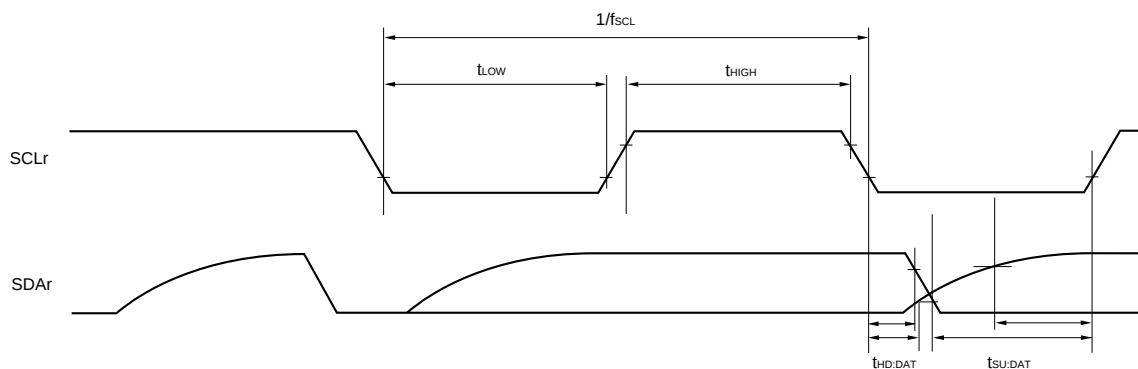
(4) During communication at same potential (simplified I²C mode)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		400 ^{Note 1}	kHz
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$		100 ^{Note 1}	kHz
Hold time when SCLr = "L"	t_{LOW}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		ns
Hold time when SCLr = "H"	t_{HIGH}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		ns
Data setup time (reception)	$t_{\text{SU:DAT}}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 220$ ^{Note 2}		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	$1/f_{\text{MCK}} + 580$ ^{Note 2}		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	0	1420	ns

Notes 1. The value must also be equal to or less than $f_{\text{MCK}}/4$.2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Caution and Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
 2. r: IIC number (r = 00, 01), g: PIM number (g = 5), h: POM number (h = 3, 5)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01)

(5) Communication at different potential (2.5 V, 3 V) (UART mode) (1/2)**(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate		reception	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			f _{MCK} /12 Note 1	bps
			Theoretical value of the maximum transfer rate f _{CLK} = 24 MHz, f _{MCK} = f _{CLK} Note 2			2.0	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			f _{MCK} /12 Note 1	bps
			Theoretical value of the maximum transfer rate f _{CLK} = 24 MHz, f _{MCK} = f _{CLK} Note 2			2.0	Mbps
			2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			f _{MCK} /12 Note 1	bps
			Theoretical value of the maximum transfer rate f _{CLK} = 24 MHz, f _{MCK} = f _{CLK} Note 2			2.0	Mbps

Notes 1. Use it with V_{DD} ≥ V_b.**2.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected

Remarks 1. V_b[V]: Communication line voltage**2.** q: UART number (q = 0), g: PIM and POM number (g = 5)**3.** f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00)

(5) Communication at different potential (2.5 V, 3 V) (UART mode) (2/2)**(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		transmission	4.0 V ≤ V _{DD} ≤ 5.5 V,				Note 1	bps
			2.7 V ≤ V _b ≤ 4.0 V	Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V			2.6 ^{Note 2}	Mbps
			2.7 V ≤ V _{DD} < 4.0 V,				Note 3	bps
			2.3 V ≤ V _b ≤ 2.7 V	Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V			1.2 ^{Note 4}	Mbps
			2.4 V ≤ V _{DD} < 3.3 V,				Notes 5, 6	bps
			1.6 V ≤ V _b ≤ 2.0 V	Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V			0.43 ^{Note 7}	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

5. Use it with V_{DD} ≥ V_b.

Notes 6. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

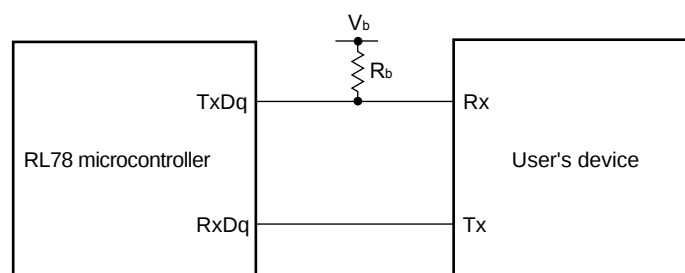
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

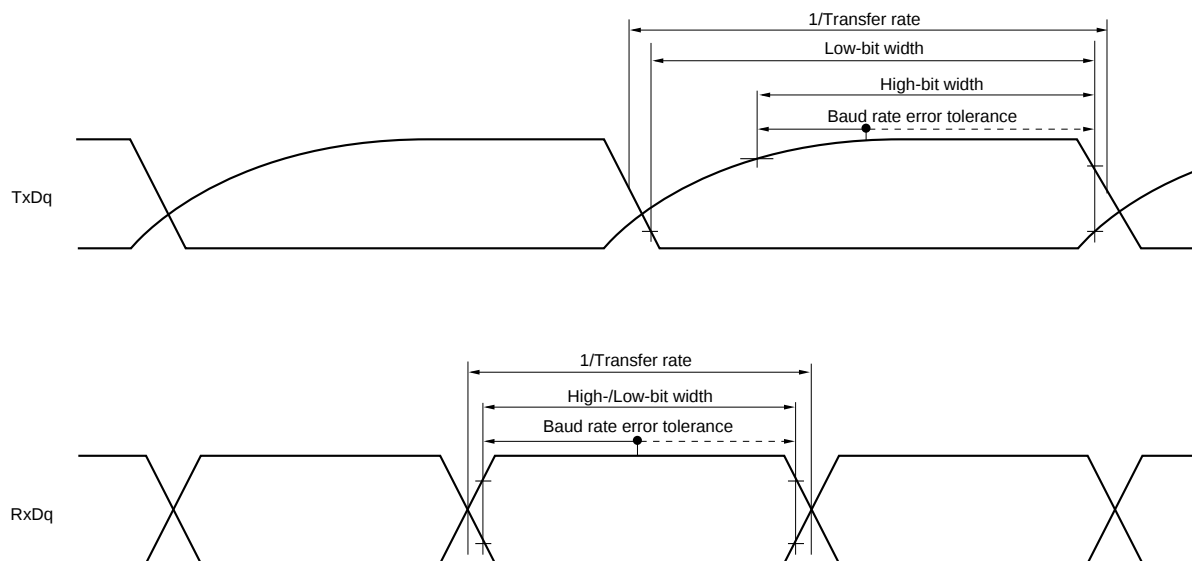
* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $C_b[\text{F}]$: Communication line (TxDq) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. q: UART number ($q = 0$), g: PIM and POM number ($g = 5$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number ($mn = 00$))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)**(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK} 4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	600			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	1000			ns
		2.4 V ≤ V _{DD} < 3.3 V, 2.4 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	2300			ns
SCKp high-level width	t _{KH1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 – 150			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 – 340			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 – 916			ns
SCKp low-level width	t _{KL1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 – 24			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 – 36			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 – 100			ns

Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

2. Use it with V_{DD} ≥ V_b.

(Remarks are listed two pages after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)
(2/2)(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

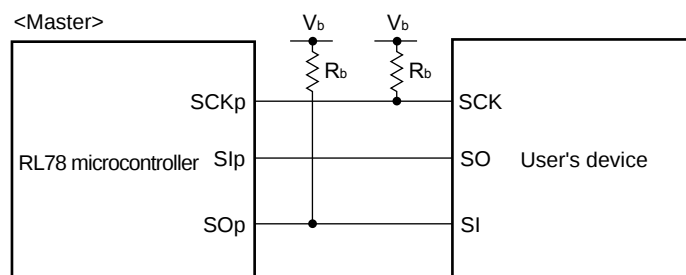
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	162			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	354			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ	958			ns
Slp hold time (from SCKp↑) ^{Note 1}	t _{KSI1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	38			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	38			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ	38			ns
Delay time from SCKp↓ to SOP output ^{Note 1}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			200	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			390	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ			966	ns
Slp setup time (to SCKp↓) ^{Note 2}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	88			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	88			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ	220			ns
Slp hold time (from SCKp↓) ^{Note 2}	t _{KSI1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	38			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	38			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ	38			ns
Delay time from SCKp↑ to SOP output ^{Note 2}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			50	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			50	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ			50	ns

(Notes, Cautions and Remarks are listed on the next page.)

- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$.
 2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 3. Use it with $V_{DD} \geq V_b$.

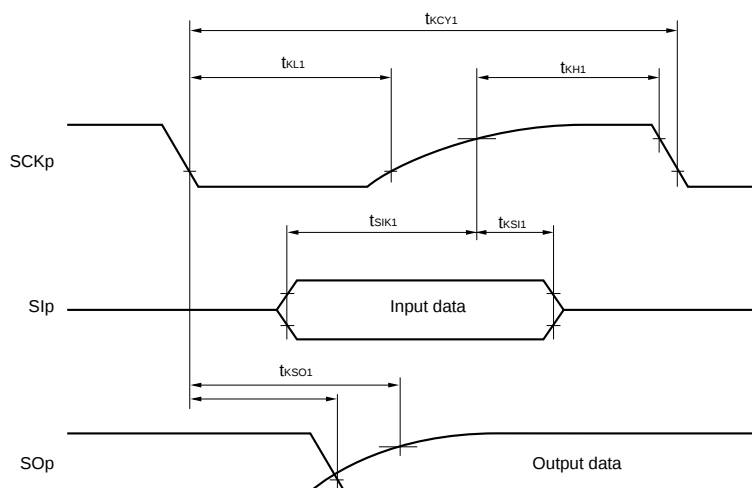
Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

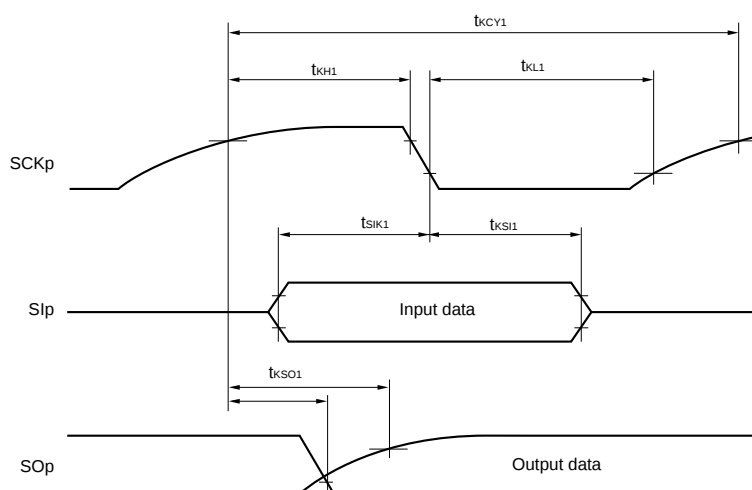


- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SCKp, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. p: CSI number ($p = 00$), m: Unit number, n: Channel number ($mn = 00$), g: PIM and POM number ($g = 0, 3, 5, 7$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number ($mn = 00$))
 4. CSI01 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00), m: Unit number, n: Channel number (mn = 00), g: PIM and POM number (g = 0, 3, 5, 7)
 2. CSI01 cannot communicate at different potential. Use other CSI for communication at different potential.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	20 MHz < f _{MCK} ≤ 24 MHz	24/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 20 MHz	20/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	12/f _{MCK}		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	20 MHz < f _{MCK} ≤ 24 MHz	32/f _{MCK}		ns
			16 MHz < f _{MCK} ≤ 20 MHz	28/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 16 MHz	24/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	12/f _{MCK}		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	20 MHz < f _{MCK} ≤ 24 MHz	72/f _{MCK}		ns
			16 MHz < f _{MCK} ≤ 20 MHz	64/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 16 MHz	52/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	32/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	20/f _{MCK}		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	t _{KCY2} /2 – 24			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	t _{KCY2} /2 – 36			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	t _{KCY2} /2 – 100			ns
Slp setup time (to SCKp↑) ^{Note 3}	t _{SIK2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	1/f _{MCK} + 40			ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	1/f _{MCK} + 40			ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	1/f _{MCK} + 60			ns
Slp hold time (from SCKp↑) ^{Note 4}	t _{KS12}		1/f _{MCK} + 62			ns
Delay time from SCKp↓ to SOp output ^{Note 5}	t _{KSO2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			2/f _{MCK} + 240	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			2/f _{MCK} + 428	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ			2/f _{MCK} + 1146	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps2. Use it with V_{DD} ≥ V_b.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

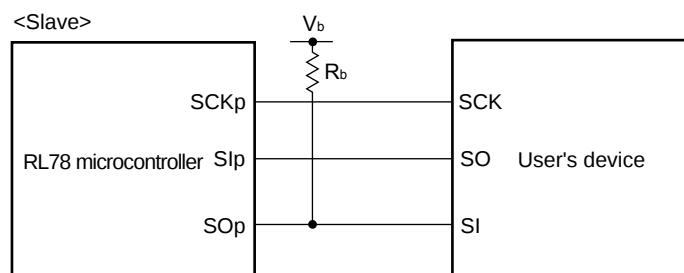
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(Caution and Remarks are listed on the next page.)

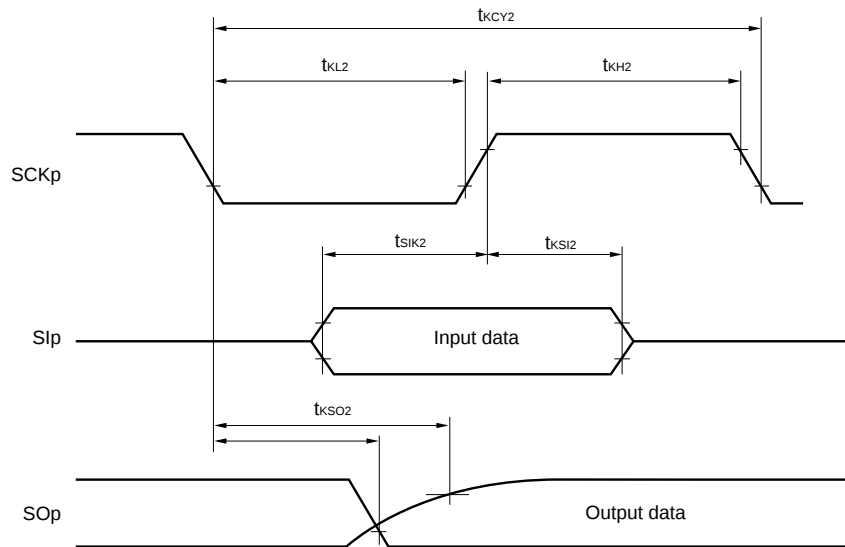
Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

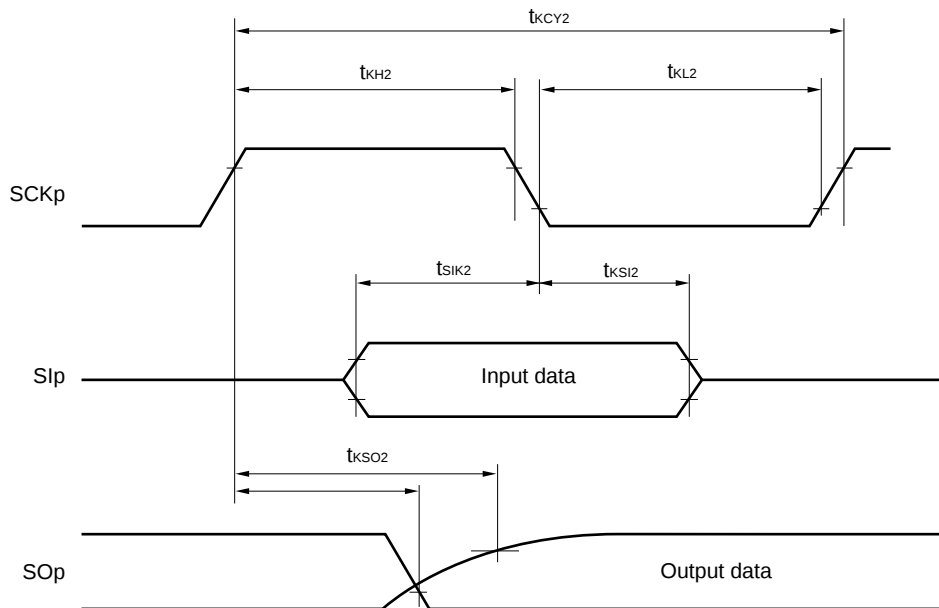


- Remarks**
1. $R_b[\Omega]$: Communication line (SO_p) pull-up resistance, $C_b[F]$: Communication line (SO_p) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number (p = 00), m: Unit number, n: Channel number (mn = 00), g: PIM and POM number (g = 0, 3, 5, 7)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))
 4. CSI01 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00), m: Unit number, n: Channel number (mn = 00),
g: PIM and POM number (g = 0, 3, 5, 7)
 2. CSI01 cannot communicate at different potential. Use other CSI for communication at different potential.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)**(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f _{SCL}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ		400 ^{Note 1}	kHz
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ		400 ^{Note 1}	kHz
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		100 ^{Note 1}	kHz
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		100 ^{Note 1}	kHz
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ		100 ^{Note 1}	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1200		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1200		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	4600		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	4600		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	620		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	500		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	2700		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	2400		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	1830		ns

(Notes, Caution and Remarks are listed on the next page.)

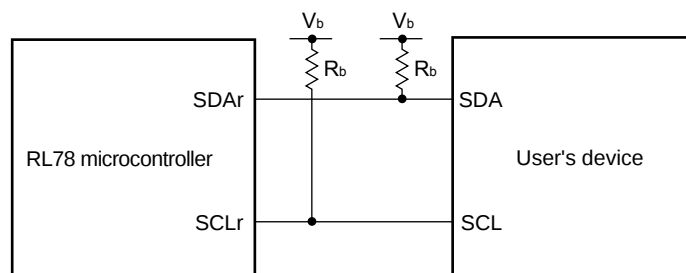
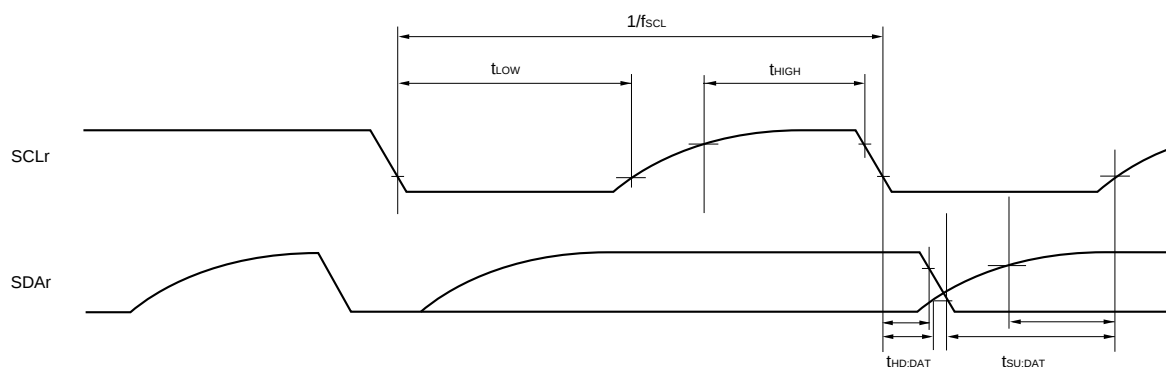
(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data setup time (reception)	t _{SU:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 340 Note 3		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 340 Note 3		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 760 Note 3		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 760 Note 3		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 570 Note 3		ns
Data hold time (transmission)	t _{HD:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	0	770	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	770	ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	1420	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	1420	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	0	1215	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.2. Use it with V_{DD} ≥ V_b.3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 2. r: IIC number (r = 00), g: PIM, POM number (g = 0, 3, 5, 7)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

3.5.2 Serial interface IICA

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz	–	–	0	400	kHz
		Standard mode: f _{CLK} ≥ 1 MHz	0	100	–	–	kHz
Setup time of restart condition	t _{SU:STA}		4.7		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}		4.0		0.6		μs
Hold time when SCLA0 = “L”	t _{LOW}		4.7		1.3		μs
Hold time when SCLA0 = “H”	t _{HIGH}		4.0		0.6		μs
Data setup time (reception)	t _{SU:DAT}		250		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}		0	3.45	0	0.9	μs
Setup time of stop condition	t _{SU:STO}		4.0		0.6		μs
Bus-free time	t _{BUF}		4.7		1.3		μs

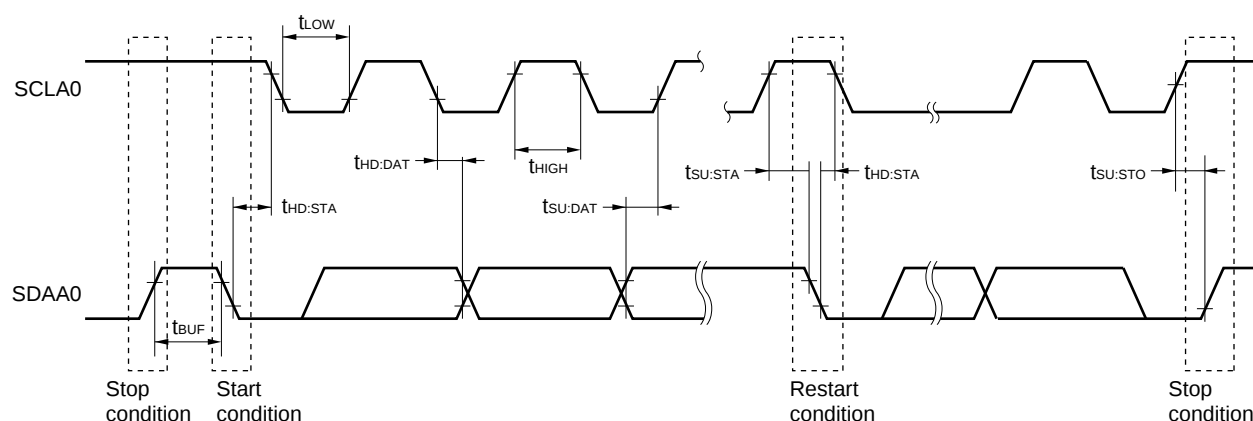
Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the $\overline{\text{ACK}}$ (acknowledge) timing.

Caution The values in the above table are applied even when bit 1 (PIOR1) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩFast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



3.5.3 USB

(1) Electrical specifications

(T_A = -40 to +105°C, 3.0 V ≤ V_{DD} ≤ 3.6 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

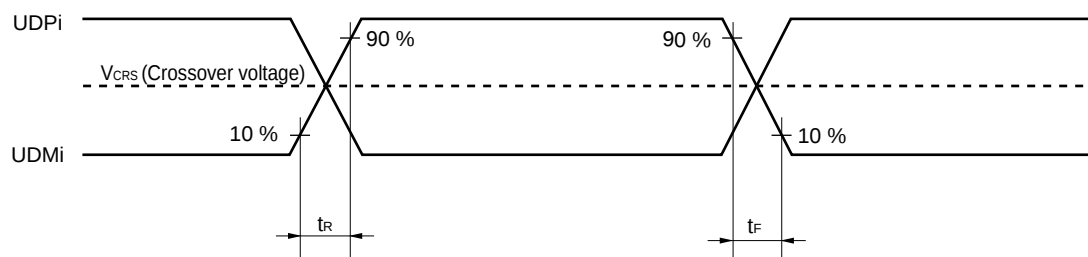
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UV _{DD}	UV _{DD} input voltage characteristic	UV _{DD}	V _{DD} = 3.0 to 5.5 V, PXXCON = 1, VDDUSEB = 0 (UV _{DD} ≤ V _{DD})	3.0	3.3	3.6	V
	UV _{DD} output voltage characteristic	UV _{DD}	V _{DD} = 4.0 to 5.5 V, PXXCON = VDDUSEB = 1	3.0	3.3	3.6	V
UV _{BUS}	UV _{BUS} input voltage characteristic	UV _{BUS}	Function	4.35 (4.02 ^{Note})	5.00	5.25	V
			Host	4.75	5.00	5.25	V

Note Value of instantaneous voltage(T_A = -40 to +105°C, 3.0 V ≤ V_{DD} ≤ 3.6 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDPi/UDMi pins input characteristic (FS/LS receiver)	Input voltage	V _{IH}		2.0			V
		V _{IL}				0.8	V
	Difference input sensitivity	V _{DI}	UDP voltage – UDM voltage	0.2			V
	Difference common mode range	V _{CM}		0.8		2.5	V
UDPi/UDMi pins output characteristic (FS driver)	Output voltage	V _{OH}	I _{OH} = -200 μA	2.8		3.6	V
		V _{OL}	I _{OL} = 2.4 mA	0		0.3	V
	Transi-ti on time	t _{FR}	Rising: From 10% to 90 % of amplitude,	4		20	ns
		t _{FF}	Falling: From 90% to 10 % of amplitude,	4		20	ns
	Matching (TFR/TFF)	V _{FRFM}	CL = 50 pF	90		111.1	%
	Crossover voltage	V _{FCRS}		1.3		2.0	V
	Output Impedance	Z _{DRV}	UV _{DD} voltage = 3.3 V, Pin voltage = 1.65 V	28		44	Ω
UDPi/UDMi pins output characteristic (LS driver)	Output voltage	V _{OH}		2.8		3.6	V
		V _{OL}		0		0.3	V
	Transi-ti on time	t _{LR}	Rising: From 10% to 90 % of amplitude,	75		300	ns
		t _{LF}	Falling: From 90% to 10 % of amplitude,	75		300	ns
	Matching (TFR/TFF) Note	V _{LTFM}	CL = 200 to 600 pF	80		125	%
	Crossover voltage Note	V _{LCRS}	When the host controller function is selected: The UDMi pin (i = 0, 1) is pulled up via 1.5 kΩ. When the function controller function is selected: The UDP0 and UDM0 pins are individually pulled down via 15 kΩ	1.3		2.0	V
UDPi/UDMi pins pull-up, pull-down	Pull-down resistor	R _{PD}		14.25		24.80	kΩ
	Pull-up resistor (i = 0 only)	R _{PUI}	Idle	0.9		1.575	kΩ
		R _{PUA}	Recep-t ion	1.425		3.09	kΩ
UV _{BUS}	UV _{BUS} pull-down resistor	R _{VBUS}	UV _{BUS} voltage = 5.5 V		1000		kΩ
	UV _{BUS} input voltage	V _{IH}		3.20			V
		V _{IL}				0.8	V

Note Excludes the first signal transition from the idle state.**Remark** i = 0, 1

Timing of UDPI and UDMi



(2) BC standard

(T_A = -40 to $+105^\circ\text{C}$, $3.0\text{ V} \leq UV_{DD} \leq 3.6\text{ V}$, $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USB standard BC1.2	UDPi sink current	I _{DP_SINK}		25		175	μA
	UDMi sink current	I _{DM_SINK}		25		175	μA
	DCD source current	I _{DP_SRC}		7		13	μA
	Dedicated charging port resistor	R _{DCP_DAT}	$0\text{ V} < \text{UDP/UDM voltage} < 1.0\text{ V}$			200	Ω
	Data detection voltage	V _{DAT_REF}		0.25		0.4	V
	UDPi source voltage	V _{DP_SRC}	Output current $250\text{ }\mu\text{A}$	0.5		0.7	V
	UDMi source voltage	V _{DM_SRC}	Output current $250\text{ }\mu\text{A}$	0.5		0.7	V

Remark i = 0, 1

(3) BC option standard (Host)

(T_A = -40 to +105°C, 4.75 V ≤ UV_{BUS} ≤ 5.25 V, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDPi output voltage (UV _{BUS} divider ratio) • VDOUEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V _{P20}		38	40	42	% UV _{BUS}
		1001	V _{P27}		51.6	53.6	55.6	% UV _{BUS}
		1010	V _{P20}		38	40	42	% UV _{BUS}
		1100	V _{P33}		60	66	72	% UV _{BUS}
UDMi output voltage (UV _{BUS} divider ratio) • VDOUEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V _{M20}		38	40	42	% UV _{BUS}
		1001	V _{M20}		38	40	42	% UV _{BUS}
		1010	V _{M27}		51.6	53.6	55.6	% UV _{BUS}
		1100	V _{M33}		60	66	72	% UV _{BUS}
UDPi comparing voltage Note 1 (UV _{BUS} divider ratio) • VDOUEi = 1 • CUSDETEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V _{HDETP_UP0}	The rise of pin voltage detection voltage	56.2			% UV _{BUS}
			V _{HDETP_DWN0}	The fall of pin voltage detection voltage			29.4	% UV _{BUS}
		1001	V _{HDETP_UP1}	The rise of pin voltage detection voltage	60.5			% UV _{BUS}
			V _{HDETP_DWN1}	The fall of pin voltage detection voltage			45.0	% UV _{BUS}
		1010	V _{HDETP_UP2}	The rise of pin voltage detection voltage	56.2			% UV _{BUS}
			V _{HDETP_DWN2}	The fall of pin voltage detection voltage			29.4	% UV _{BUS}
UDMi comparing voltage Note 1 (UV _{BUS} divider ratio) • VDOUEi = 1 • CUSDETEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V _{HDETM_UP0}	The rise of pin voltage detection voltage	56.2			% UV _{BUS}
			V _{HDETM_DWN0}	The fall of pin voltage detection voltage			29.4	% UV _{BUS}
		1001	V _{HDETM_UP1}	The rise of pin voltage detection voltage	56.2			% UV _{BUS}
			V _{HDETM_DWN1}	The fall of pin voltage detection voltage			29.4	% UV _{BUS}
		1010	V _{HDETM_UP2}	The rise of pin voltage detection voltage	60.5			% UV _{BUS}
			V _{HDETM_DWN2}	The fall of pin voltage detection voltage			45.0	% UV _{BUS}
UDPi pull-up detection Note 2 Connect detection with the full speed function (pull-up resistor)		1000	R _{HDET_PULL}	In full-speed mode, the power supply voltage range of pull-up resistors connected to the USB function module is between 3.0 V and 3.6 V.			1.575	kΩ
		1001						
		1010						
UDMi pull-up detection Note 2 Connect detection with the low-speed (pull-up resistor)		1000	R _{HDET_PULL}	In low-speed mode, the power supply voltage range of pull-up resistors connected to the USB function module is between 3.0 V and 3.6 V.			1.575	kΩ
		1001						
		1010						
UDMi sink current detection Note 2 Connect detection with the BC1.2 portable device (sink resistor)		1000	I _{HDET_SINK}		25			μA
		1001						
		1010						

Notes 1. If the voltage output from UDPi or UDMi (i = 0, 1) exceeds the range of the MAX and MIN values prescribed in this specification, DPCUSDETi (bit 8) and DMCUSDETi (bit 9) of the USBBCOPTi register are set to 1.

2. If the pull-up resistance or sink current prescribed in this specification is applied to UDPi or UDMi (i = 0, 1), DPCUSDETi (bit 8) and DMCUSDETi (bit 9) of the USBBCOPTi register are set to 1.

Remark i = 0, 1

(4) BC option standard (Function)**($T_A = -40$ to $+105^\circ\text{C}$, $4.35\text{ V} \leq UV_{BUS} \leq 5.25\text{ V}$, $3.0\text{ V} \leq UV_{DD} \leq 3.6\text{ V}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDPi/UDMi input reference voltage (UV_{BUS} divider ratio) • $VDOUE_i = 0$ ($i = 0$)	VDSELi [3:0] ($i = 0$)	0000	V_{DDET0}		27	32	37	% UV_{BUS}
		0001	V_{DDET1}		29	34	39	% UV_{BUS}
		0010	V_{DDET2}		32	37	42	% UV_{BUS}
		0011	V_{DDET3}		35	40	45	% UV_{BUS}
		0100	V_{DDET4}		38	43	48	% UV_{BUS}
		0101	V_{DDET5}		41	46	51	% UV_{BUS}
		0110	V_{DDET6}		44	49	54	% UV_{BUS}
		0111	V_{DDET7}		47	52	57	% UV_{BUS}
		1000	V_{DDET8}		51	56	61	% UV_{BUS}
		1001	V_{DDET9}		55	60	65	% UV_{BUS}
		1010	V_{DDET10}		59	64	69	% UV_{BUS}
		1011	V_{DDET11}		63	68	73	% UV_{BUS}
		1100	V_{DDET12}		67	72	77	% UV_{BUS}
		1101	V_{DDET13}		71	76	81	% UV_{BUS}
		1110	V_{DDET14}		75	80	85	% UV_{BUS}
		1111	V_{DDET15}		79	84	89	% UV_{BUS}

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV _{REFP} Reference voltage (-) = AV _{REFM}	Reference voltage (+) = V _{DD} Reference voltage (-) = V _{SS}	Reference voltage (+) = V _{BGR} Reference voltage (-) = AV _{REFM}
ANI0 to ANI7	Refer to 3.6.1 (1).	Refer to 3.6.1 (3).	Refer to 3.6.1 (4).
ANI16, ANI17, ANI19	Refer to 3.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 3.6.1 (1).		—

(1) When AV_{REF} (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI2 to ANI7, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	2.4 V ≤ AV _{REFP} ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI2 to ANI7	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	2.4 V ≤ AV _{REFP} ≤ 5.5 V			±0.25	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	2.4 V ≤ AV _{REFP} ≤ 5.5 V			±0.25	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	2.4 V ≤ AV _{REFP} ≤ 5.5 V			±2.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	2.4 V ≤ AV _{REFP} ≤ 5.5 V			±1.5	LSB
Analog input voltage	V _{AIN}	ANI2 to ANI7		0		AV _{REFP}	V
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{BGR} ^{Note 4}			V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{TMPS25} ^{Note 4}			V

(Notes are listed on the next page.)

- Notes**
1. Excludes quantization error ($\pm 1/2$ LSB).
 2. This value is indicated as a ratio (%FSR) to the full-scale value.
 3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 4. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin : ANI16, ANI17, ANI19

(T_A = -40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	2.4 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	t _{CONV}	10-bit resolution Target ANI pin : ANI16, ANI17, ANI19	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±3.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V _{AIN}	ANI16, ANI17, ANI19		0		AV_{REFP} and V _{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

- (3) Reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), Reference voltage (-) = V_{SS} (ADREFM = 0), target ANI pin : ANI0 to ANI7, ANI16, ANI17, ANI19, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R _{ES}			8		10	bit
Overall error ^{Notes 1, 2}	AINL	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t _{CONV}	10-bit resolution Target ANI pin : ANI0 to ANI7, ANI16, ANI17, ANI19	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target ANI pin : Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V _{AIN}	ANI0 to ANI7, ANI16, ANI17, ANI19		0		V _{DD}	V
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{BGR} ^{Note 3}			V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{TMPS25} ^{Note 3}			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

(4) When Reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), Reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI0 to ANI7, ANI16, ANI17, ANI19

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{BGR}^{Note 3}, Reference voltage (-) = AV_{REFM}^{Note 4} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R _{ES}			8			Bit
Conversion time	t _{CONV}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V _{AIN}			0		V _{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV_{REFM}.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

3.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = -40 to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

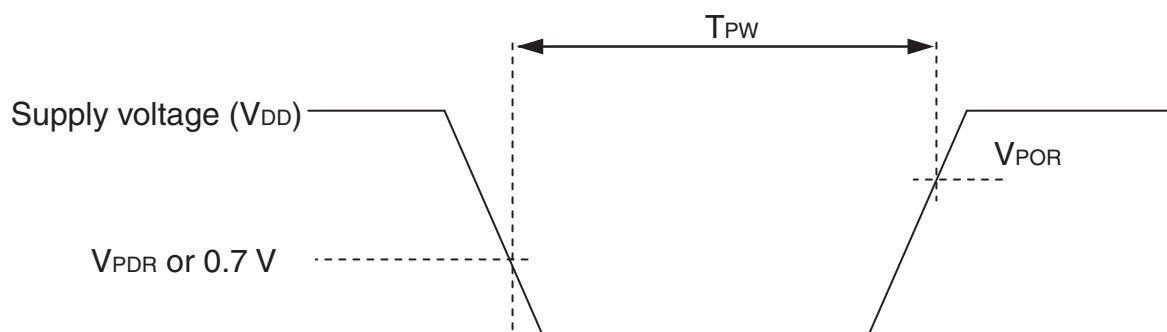
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V _{TMP25}	Setting ADS register = 80H, T _A = $+25^{\circ}\text{C}$		1.05		V
Internal reference voltage	V _{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F _{VTMP25}	Temperature sensor that depends on the temperature		-3.6		mV/ $^{\circ}\text{C}$
Operation stabilization wait time	t _{AMP}		5			μs

3.6.3 POR circuit characteristics

(T_A = -40 to $+105^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{POR}	Power supply rise time	1.45	1.51	1.57	V
	V _{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width ^{Note}	T _{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock (f_{MAIN}) is stopped through setting bit 0 (HISTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode(T_A = -40 to +105°C, V_{PDR} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	VLVD0	Power supply rise time	3.90	4.06	4.22	V
			Power supply fall time	3.83	3.98	4.13	V
		VLVD1	Power supply rise time	3.60	3.75	3.90	V
			Power supply fall time	3.53	3.67	3.81	V
		VLVD2	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		VLVD3	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		VLVD4	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		VLVD5	Power supply rise time	2.70	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		VLVD6	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		VLVD7	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		tLW		300			μs
Detection delay time		tLD				300	μs

LVD Detection Voltage of Interrupt & Reset Mode(T_A = -40 to +105°C, V_{PDR} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V _{LVDD0}	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	V _{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	V _{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	V _{LVDD3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

3.6.5 Power supply voltage rising slope characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S _{VDD}				54	V/ms

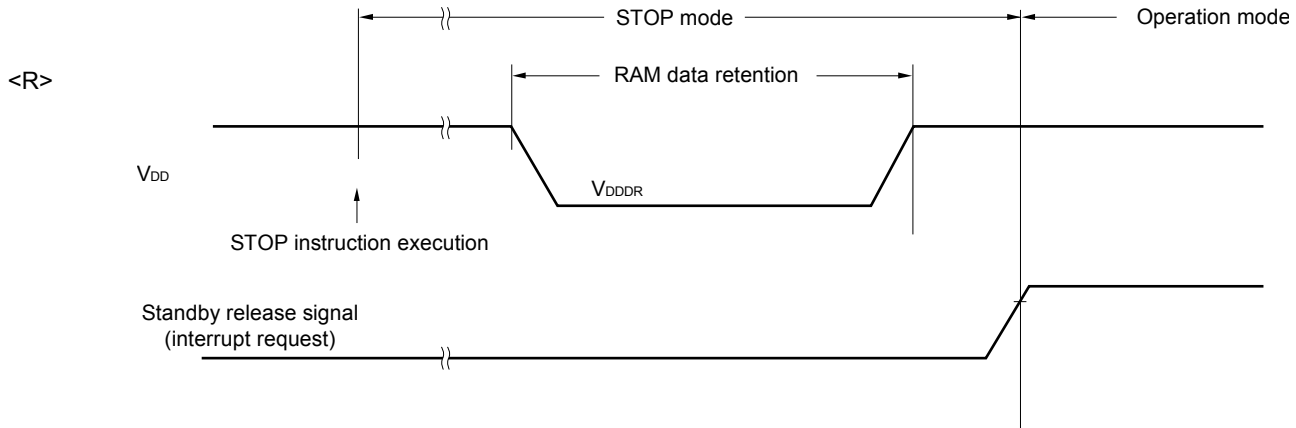
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

<R> 3.7 RAM Data Retention Characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{DDDR}		1.44 ^{Note}		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



3.8 Flash Memory Programming Characteristics

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f _{CLK}	2.4 V ≤ V _{DD} ≤ 5.5 V	1		24	MHz
<R> Number of code flash rewrites	C _{erwr}	Retaining years: 20 years T _A = +85°C ^{Note 4}	1,000			Times
<R> Number of data flash rewrites Notes 1, 2, 3		Retaining years: 1 year T _A = +25°C ^{Note 4}		1,000,000		
<R>		Retaining years: 5 years T _A = +85°C ^{Note 4}	100,000			
<R>		Retaining years: 20 years T _A = +85°C ^{Note 4}	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library.

3. These specifications show the characteristics of the flash memory and the results obtained from Renesas Electronics reliability testing.

<R> 4. This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

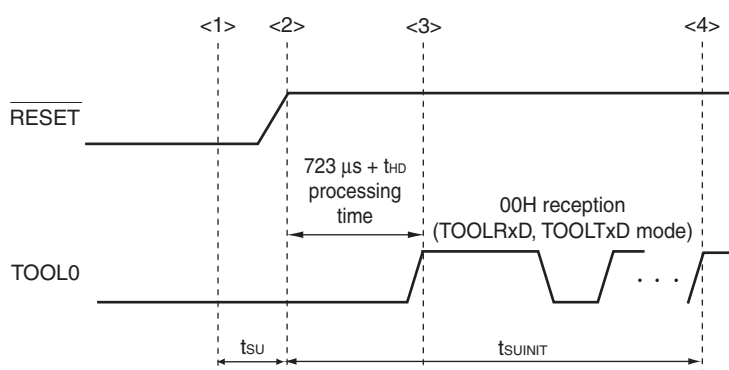
(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.10 Timing Specs for Switching Flash Memory Programming Modes

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t _{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t _{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t _{HD}	POR and LVD reset must end before the external reset ends.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset ends (POR and LVD reset must end before the external reset ends.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until an external reset ends

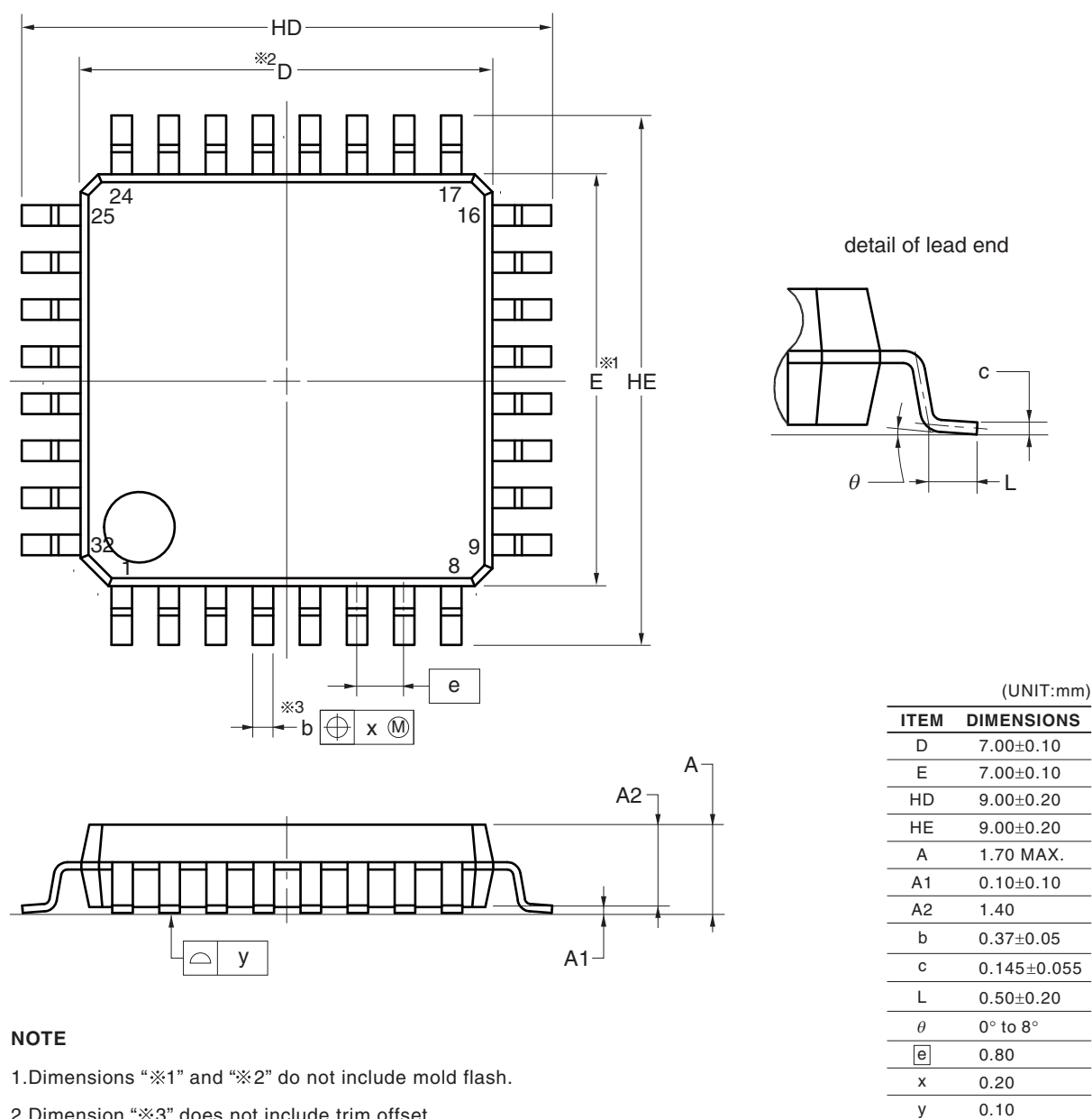
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external and internal resets end (excluding the processing time of the firmware to control the flash memory)

4. PACKAGE DRAWINGS

4.1 32-pin Products

R5F10JBCAFP, R5F10KBCAFP
R5F10JBCGFP, R5F10KBCGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2

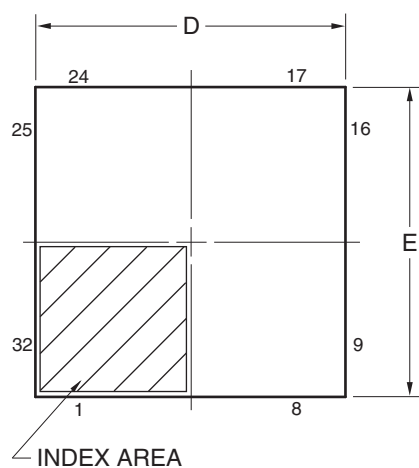


R5F10JBCANA, R5F10KBCANA

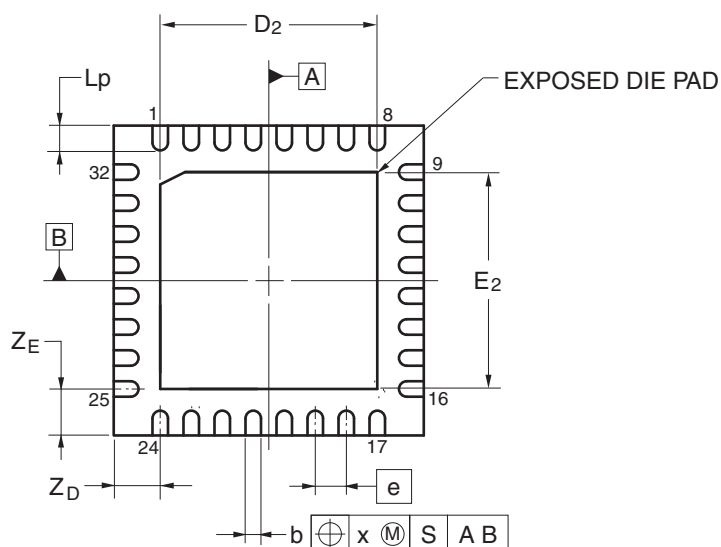
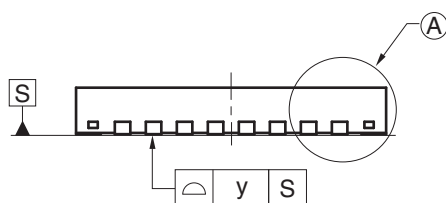
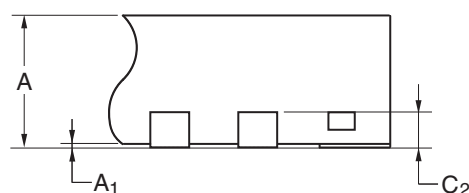
R5F10JBCGNA, R5F10KBCGNA

<R>

JEITA Package code	RENESAS code	Previous code	MASS (TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06



DETAIL OF (A) PART



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.95	5.00	5.05
E	4.95	5.00	5.05
A	—	—	0.80
A ₁	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
L _p	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z _D	—	0.75	—
Z _E	—	0.75	—
c ₂	0.15	0.20	0.25
D ₂	—	3.50	—
E ₂	—	3.50	—

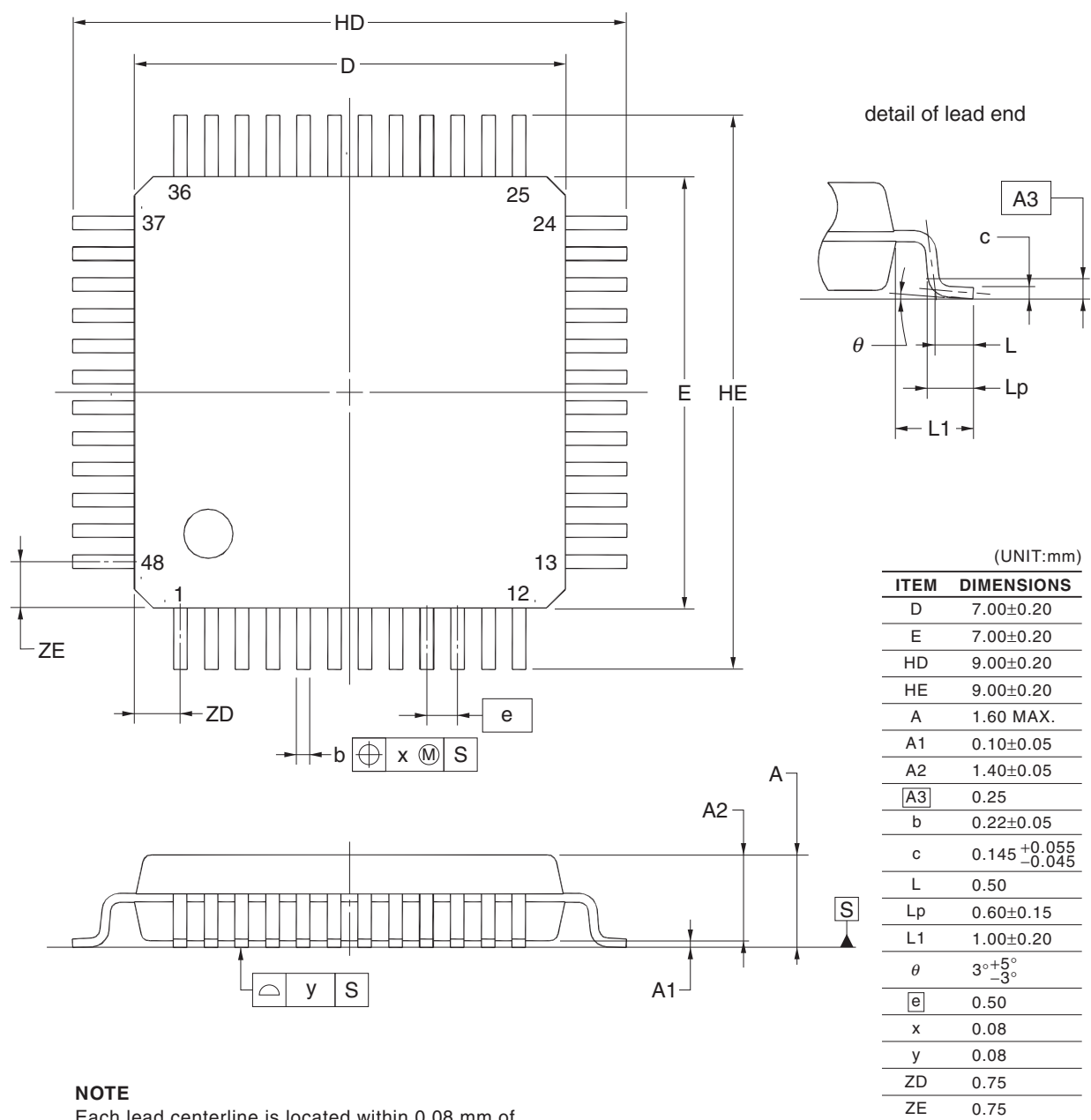
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4.2 48-pin Products

R5F10JGCAFB, R5F10KGCAFB

R5F10JGCGFB, R5F10KGCGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16

**NOTE**

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

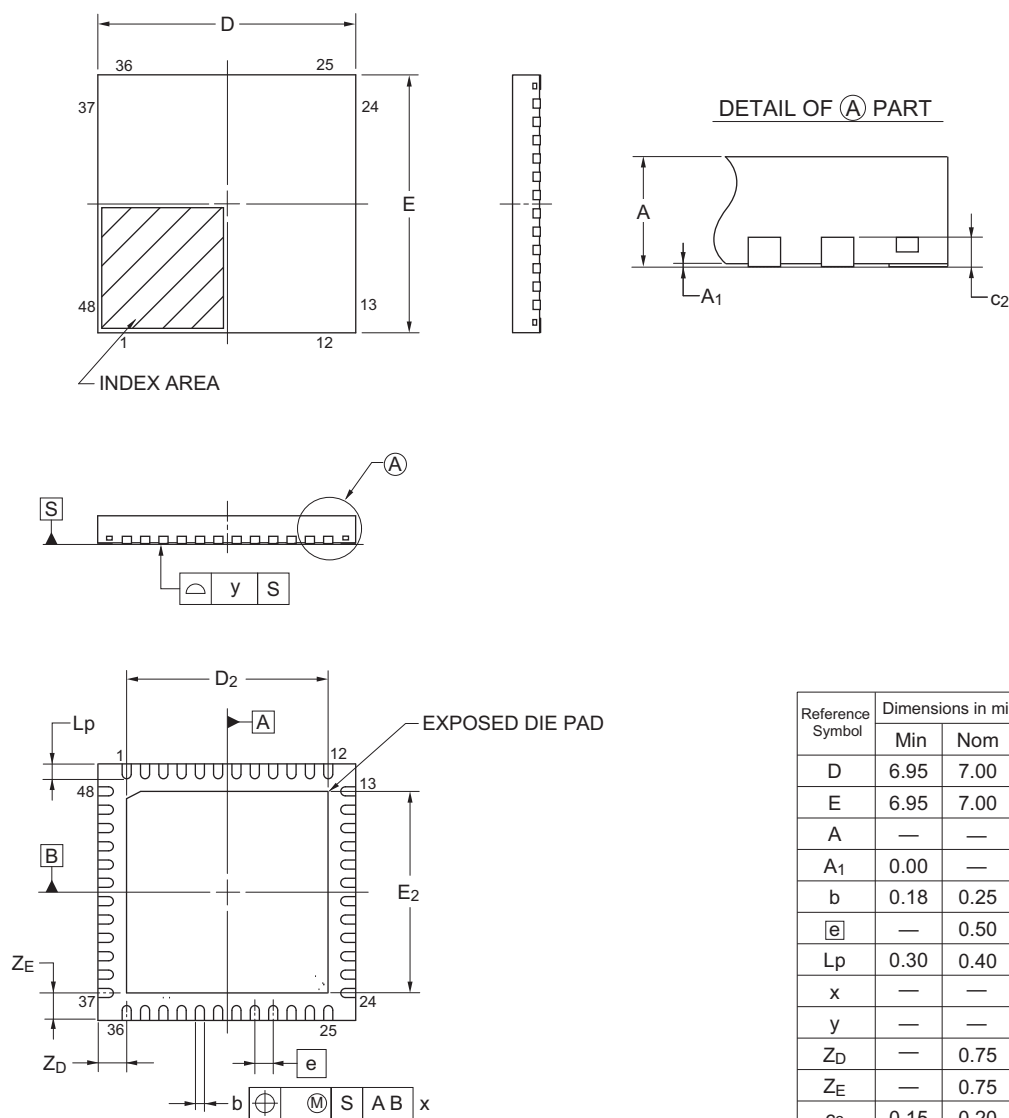
R5F10JGCANA, R5F10KGCANA

R5F10JGCGNA, R5F10KGCNA

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-7	0.13

Unit: mm



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Revision History	RL78/G1A Data Sheet
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Rev.	Date	Description	
		Page	Summary
0.01	Sep 20, 2012	-	First Edition issued
1.00	Aug 08, 2013	Throughout	Deletion of the bar over SCK and SCKxx
			Renaming of f _{EXT} to f _{EXS}
			Renaming of interval timer (unit) to 12-bit interval timer
			Addition of products for G: Industrial applications (T _A = -40 to +105 °C)
		1	Change of 1.1 Features
		2	Change of 1.2 List of Part Numbers
		3	Modification of Figure 1-1. Part Number, Memory Size, and Package of RL78/G1C
		4, 5	Addition of remark to 1.3 Pin Configuration (Top View)
		15, 16	Change of 1.6 Outline of Functions
		17 to 76	Addition of a whole chapter
		77 to 131	Addition of a whole chapter
		132	Addition of products for G: Industrial applications (T _A = -40 to +105 °C)
1.10	Nov 15, 2013	77	Caution 3 added.
		79	Note for operating ambient temperature in 3.1 Absolute Maximum Ratings deleted.
1.20	Sep 30, 2016	4 to 7	Modification of pin configuration in 1.3.1 32-pin products
		8 to 11	Modification of pin configuration in 1.3.2 48-pin products
		15	Modification of description of main system clock in 1.6 Outline of Functions
		74	Modification of title of 2.7 RAM Data Retention Characteristics and figure
		74	Modification of table of 2.8 Flash Memory Programming Characteristics
		129	Modification of title of 3.7 RAM Data Retention Characteristics and figure
		129	Modification of table of 3.8 Flash Memory Programming Characteristics and addition of Note 4
		132	Change of figure in 4.1 32-pin Products
		134	Change of figure in 4.2 48-pin Products

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NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
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