High Efficiency 3-Channel Buck Converter with dual LDO

General Description

PV88090 is a power management unit (PMU) optimized for supplying systems with central processing units (CPU), input/output (I/O), and dual data rate (DDR) memory. The target application range covers television, set-up box, wifi routers, and enterprise access point and network addressable servers.

PV88090 features a two-phase buck converter providing up to 9.5 A current, and two one-phase buck converters for dual date rate (DDR) memory and auxiliary power. High efficiency is achieved over a wide load range by using automatic pulse frequency modulation (PFM). All power switches are integrated, eliminating the need for external Schottky diodes are not needed. This optimizes power efficiency and reduces the external component count. Two LDO regulators with programmable output voltage are integrated and provide up to 400 mA. PV88090 provides dynamic voltage control (DVC) via I²C command to support adaptive adjustment of the supply voltage based on the processor loading. All power blocks have over-current circuit protection and the start-up timing can be controlled through the I²C interface. The supply voltages of PV88090 control can be realized via direct register writes through the I²C interface to the operating point of the system.

PV88090 includes over-temperature and over-current protection for increased system reliability, without external sensing components. A soft-start mechanism limits the inrush current from the input node and secures a slope-controlled rail activation. A standby mode provides reduced power consumption. Optional standby operation for DDR memory, auxiliary buck, and analog core LDO are configurable in PV88090 for optimizing the power rails. The PV88090is available in a 30-pin QFN package and is specified from -40 °C to 85 °C ambient temperature.

Key Features

- Input voltage 4.75 V to 5.25 V
- Three synchronous buck converters with integrated low R_{ON} FET
  - Buck1: Programmable output voltage from 0.9 V to 1.3 V with 9.5 A continuous output current, 11 A peak current if standalone
  - Buck2: Programmable output voltage from 1 V to 2.5 V with 2 A continuous output current
  - Buck3: Programmable output voltage 1.3 V to 3.4 V with 2 A continuous output current
  - 93 % efficiency
  - Auto mode on all three buck converters
- Integrated power switches
- DVC for buck converters
- 2 LDO regulators
  - LDO1: 1.05 V to 1.23 V, 400 mA
    LDO2: 1.8 V to 3.3 V, 250 mA
- Adjustable soft-start
- I²C compatible interface
- -40 ºC to +85 ºC ambient temperature range
- Custom 30-pin FC-MQFN package with thermal pad, 0.5 mm pin pitch

Applications

- Supply for digital television processor
- Power supply for digital set top box (STB)
- Networking home terminal

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System Diagram

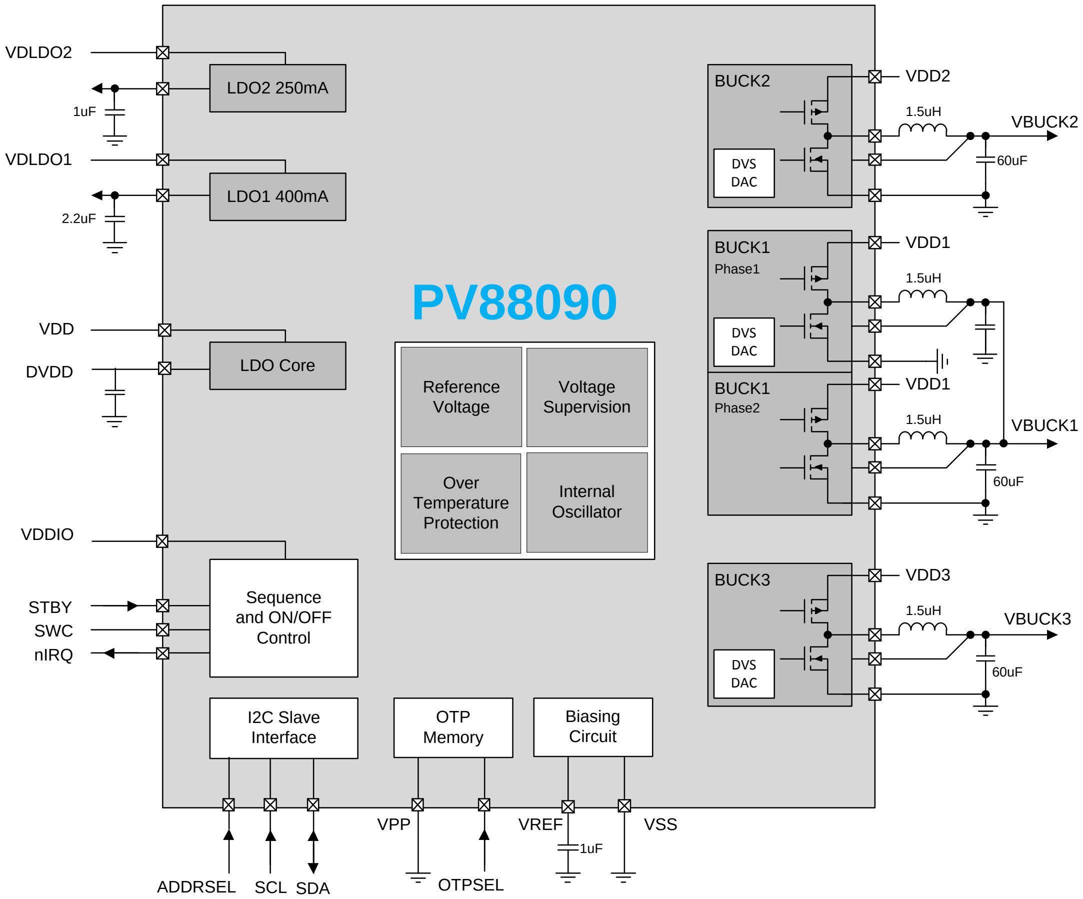

Figure 1: System Diagram

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1 Terms and definitions

CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
HBM	Human Body Model
OTP	One Time Programmable
PCB	Printed Circuit Board
PG	Power Good
PMIC	Power Management Integrated Circuit
POR	Power On Reset
PVC	Power Voltage Converter
PWC	Power Cycle

2 References

[1] UM10204 I²C bus specification and user manual

[2] PV88080 High Efficiency Advanced Feature 4-Channel PMIC datasheet

3 Block Diagram

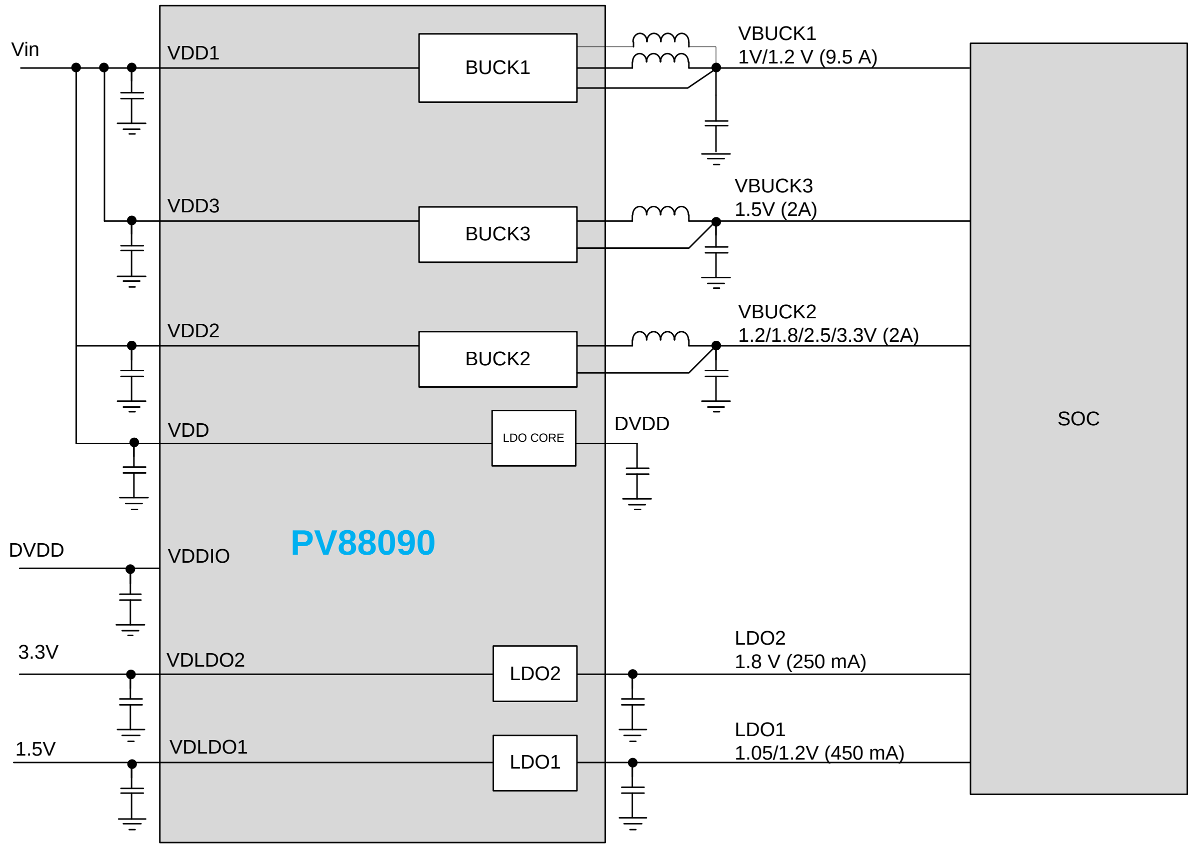


Figure 2: Block Diagram

4 Pinout

Table 1: Pin Description

Pin No.	Pin Name	Type (Table 2)	Description
1	VDD2	PWR	Supply voltage for Buck2 To be connected to VDD after input capacitor
2	VSS12	GND	Ground voltage for Buck2 and Buck1 phase1
3	VDD1	PWR	Supply voltage Buck1 To be connected to VDD after input capacitor
4	VSS13	GND	Ground voltage for Buck3 and Buck1 phase2
5	VDD3	PWR	Supply voltage for Buck3 To be connected to VDD after input capacitor
6	ADDRSEL	DI	I^2C alternate address select
7	OTPSEL	DI	OTP page select (high end / low end)
8	VDLDO1	PWR	Supply voltage for LDO1
9	VDLDO1	PWR	Supply voltage for LDO1
10	LDO1	AO	LDO1 output
11	VDLDO2	PWR	Supply voltage for LDO2

Pin No.	Pin Name	Type (Table 2)	Description
12	LDO2	AO	LDO2 output
13	FB3	AI	Feedback node Buck3
14	VPP	PWR	OTP programming voltage input Connect to VSS in application
15	nIRQ	DO	Interrupt line towards the host
16	VDDIO	PWR	Supply voltage for I/O rail
17	STBY	DI	System standby signal
18	SWC	DIO	Connect to VSS for normal application
19	LX3	AO	Switching node for Buck3
20	LX1B	AO	Switching node for Buck1 phase 2
21	LX1A	AO	Switching node for Buck1 phase 1
22	LX2	AO	Switching node for Buck2
23	DVDD	AIO	Core digital supply voltage
24	FB2	AI	Feedback node Buck2
25	VDD	PWR	Supply voltage
26	FB1	AI	Feedback node Buck1
27	VREF	AO	Voltage reference decouple
28	VSS	GND	Quiet ground
29	SDA	DIO	I2C data
30	SCL	DI	I2C clock

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
DIOD	Digital input/output open drain	BP	Back drive protection
PU	Pull-up resistor (fixed)	SPU	Switchable pull-up resistor
PD	Pull-down resistor (fixed)	SPD	Switchable pull-down resistor
PWR	Power	GND	Ground

5 Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
T_{STG}	Storage temperature		-60	+165	°C
T_J	Junction temperature		-40	+125	°C
V_{VDD}	Power supply input VDD, VDD1, VDD2, VDD3	STBY =0 and VIN ramp < 1 V/µs	-0.3	5.5	V
V_{VLDO2}	Power supply input VLDO2		-0.3	5.5	V
V_{VDLDO1}	Power supply input VDLDO1		-0.3	2.75	V
V_{DVDD}	Power supply input DVDD		-0.3	5.5	V
V_{LX}	Power supply input LX1A, Lx1B, LX2, LX3		-0.3	5.5	V
V_{VREF}	Power supply input VREF		-0.3	2.75	V
V_{IN_MAX}	Maximum input voltage ADRSEL, OTPSEL, SCL, SDA, SWC, STBY		-0.3	V_{VDD} + 0.3	V

5.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Ambient temperature		-40		+85	°C
V_{VDD}	Power supply input VDD, VDD1, VDD2, VDD3		4.75		5.25	V
V_{VLDO2}	Power supply input VDLDO2			3.5	3.6	V
V_{DDIO}	Power supply input VDDIO				3.4	V
V_{VDLDO1}	Power supply input VDLDO1				1.7	V
V_{IN_MAX}	Maximum input voltage ADRSEL, OTPSEL, SCL, SDA, SWC, STBY				V_{DDIO}+ 0.3	V
I/O pins					V_{VDD} + 0.3	V

5.3 ESD Ratings

Table 5: ESD Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{ESD_HBM}	ESD protection	Human Body Model (HBM)			2	kV
V_{ESD_CDM}	ESD protection	Charge Device Model (CDM)			500	V

5.4 Electrical Characteristics

5.4.1 Digital I/O

Unless otherwise noted, the following is valid for Ta = 25ºC, VDD = 5V.**Table 6: Digital I/O Electrical Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high voltage ADRSEL, OTPSEL, SWC, STBY, SCL, SDA	VDDCORE mode	0.7*V_{DVDD}		V_{DDIO}	V
		VDDIO mode	0.7*V_{DDIO}			
V_{IL}	Input low voltage ADRSEL, OTPSEL, SWC, STBY, SCL, SDA	VDDCORE mode	-0.3		0.3*V_{DVDD}	V
		VDDIO mode			0.3*V_{DDIO}	
V_{OH}	Output high voltage nIRQ, SWC	@ 1 mA	0.8*V_{DDIO}		V_{DDIO}	V
V_{OL}	Output low voltage nIRQ, SWC, SDA	@ 1 mA	0		0.2*V_{DDIO}	V
R_{PU}	Pull-up resistor ADRSEL, OTPSEL			10		kΩ

5.4.2 I²C Interface

Unless otherwise noted, the following is valid for Ta = 25ºC, VDD = 5V.

Table 7: I²C Interface Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{BUF}	Bus free time from STOP to START condition		0.5			µs
C_B	Bus line capacitive load				150	pF
Standard/Fast/Fast+ Mode						
f_{CLK}	Clock frequency at pin CLK		1		1000	kHz
t_{SU_STA}	START condition set-up time		0.26			µs
t_{H_STA}	START condition hold time		0.26			µs

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{W_CL}	Clock LOW duration		0.5			µs
t_{W_CH}	Clock HIGH duration		0.26			µs
t_R	Rise time at pin clk and data	Input requirement			1000	ns
t_F	Fall time at pin clk and data	Input requirement			300	ns
t_{SU_D}	Data set-up time		50			ns
t_{H_D}	Data hold time		0			ns
High Speed Mode						
f_{CLK_HS}	Clock frequency at pin CLK		1		3400	kHz
$t_{SU\_STA\_HS}$	START condition set-up time		160			ns
$t_{H\_STA\_HS}$	START condition hold time		160			ns
$t_{W\_CL\_HS}$	Clock LOW duration		160			ns
$t_{W\_CH\_HS}$	Clock HIGH duration		60			ns
t_{R_HS}	Rise time at pin clk and data	Input requirement			160	ns
t_{F_HS}	Fall time at pin clk and data	Input requirement			160	ns
$t_{SU\_D\_HS}$	Data set-up time		10			ns
$t_{H\_D\_HS}$	Data hold time		0			ns
$t_{SU\_STO\_HS}$	STOP condition set-up time		160			ns

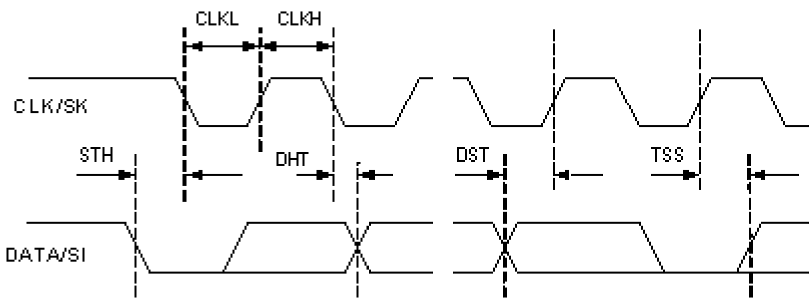


Figure 3: I2C Interface Timing

5.4.3 Buck Converter Electrical Characteristics

5.4.3.1 Buck1 Electrical Characteristics

Unless otherwise noted, the following is valid for Ta = 25ºC, VDD = 5V, C_{OUT} = 2x47µF, local sensing

Parameter	Description	Conditions	Min	Typ	Max	Unit
VDD	Input voltage		4.75		5.25	V
COUT	Output Capacitance	(including voltage and temperature coefficient)	60	100 (2x47)	400	µF
L_{BUCK1}	Inductor value	Including current & temperature dependence	-30%	1.5	+30%	µH
VBUCK1	Output Voltage	IOUT = IMAX Step = 6.25mV	0.9		1.3	V
V_{BUCK1_ACC}	Output Voltage Accuracy	VOUT = 1V IOUT = ½IMAX	-3		3	%
V_{BUCK1_RPL}	Output Voltage Ripple	IOUT = IMAX			30	mVpp
VTR_{LOAD}	Load regulation transient	IOUT = ¼Imax to Imax Tr=tf=25uSec VOUT=1V, L=1.5µH		25		mV
VTR_{LINE}	Line regulation transient	VDD = 4.75 to 5.25V Tr=Tf=10uSec IOUT = 8500mA (Dual) IOUT = 5000mA (Single)		10		mV
I_{MAX}	Output Current	Single Phase Dual Phase	5000 9500			mA
I_{LIM}	Peak Inductor Current Limit (programmable)	BUCK1_SYNC_ILIM=1111	-20%	7040	+20%	mA/ phase
IQFF	Quiescent current in OFF mode				15	µA
F	Switching frequency			1.0		MHz
D	Switching duty cycle		10		95	%
R_{PD}	Output Pull Down Resistor	Can be switched off via BUCK1_PD_DIS			200	Ω
RpMOS	On resistance pMOS	Per phase include pin and routing			0.062	Ω
RnMOS	On resistance nMOS	Per phase include pin and routing			0.025	Ω

5.4.3.2 Buck2 Electrical Characteristics

Unless otherwise noted, the following is valid for T_A = 25 ºC, V_{DD} = 5 V, C_{OUT} = 2 x 47 µF, local sensing.

Table 8: Buck2 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage		4.75		5.25	V
C_{OUT}	Output capacitance	Including voltage and temperature coefficient	60	100 (2 x 47)	400	µF

Parameter	Description	Conditions	Min	Typ	Max	Unit
L_{BUCK2}	Inductor value	Including current and temperature dependence	-30 %	1.5	+30 %	µH
V_{BUCK2}	Output voltage	$I_{OUT} = I_{MAX}$ Step = 6.25 mV	1.0		2.19	V
		$I_{OUT} = I_{MAX}$ Step 12.5 mV	2.2		2.5	V
V_{BUCK2_ACC}	Output voltage accuracy	I_{OUT} = ½ I_{MAX}	-3		3	%
V_{BUCK2_RPL}	Output voltage ripple	$I_{OUT} = I_{MAX}$ V_{OUT} = 1.0 V			30	mVpp
V_{TRLOAD}	Load regulation transient	I_{OUT} = ¼ I_{MAX} to I_{MAX} tr = tf = 10 µs V_{OUT} = 1 V L = 1.5 µH		25		mV
V_{TRLINE}	Line regulation transient	V_{DD} = 4.75 V to 5.25 V tr = tf = 10 µs I_{OUT} = 2000 mA		10		mV
I_{MAX}	Output current		2000			mA
I_{LIM}	Peak Inductor Current Limit (programmable)	Buck2_sync_ilim = 11	-20 %	4189	+20 %	mA
I_{QFF}	Quiescent current in OFF mode				2	µA
F	Switching frequency			1		MHz
D	Switching duty cycle		10		95	%
R_{PD}	Output pull-down resistor	Can be switched off via BUCK2_PD_DIS			200	Ω
R_{PMOS}	On resistance PMOS	Include pin and routing			0.125	Ω
R_{NMOS}	On resistance NMOS	Include pin and routing			0.050	Ω

5.4.3.3 Buck3 Electrical Characteristics

Unless otherwise noted, the following is valid for T_A = 25 ºC, V_{DD} = 5 V, C_{OUT} = 2 x47 µF, local sensing.

Table 9: Buck3 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage		4.75		5.25	V
C_{OUT}	Output capacitance	Including voltage and temperature coefficient	60	100 (2 x 47)	400	µF
L_{BUCK3}	Inductor value	Including current and temperature dependence	-30 %	1.5	+30 %	µH
V_{BUCK3}	Output voltage	$I_{OUT} = I_{MAX}$ Step 6.25 mV	1.3		2.19	V
		$I_{OUT} = I_{MAX}$ Step 12.5 mV	2.2		3.4	V
V_{BUCK3_ACC}	Output voltage accuracy	I_{OUT} = ½ I_{MAX}, note: V_{BUCK3} =< 2.5V	-3		3	%

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{BUCK1_RPL}	Output voltage ripple	$I_{OUT} = I_{MAX}$ V_{OUT} = 1.0 V			30	mV
V_{TRLOAD}	Load regulation transient	I_{OUT} = ¼ I_{MAX} to I_{MAX} tr = tf = 10 µs V_{OUT} = 1 V L = 1.5 µh		10		mV
V_{TRLINE}	Line regulation transient	V_{DD} = 4.75 V to 5.25 V tr = tf = 10 µs I_{OUT} = 2000 mA	2000			mA
I_{MAX}	Output current		250			mA
I_{LIM}	Peak Inductor Current Limit (programmable)	Buck2_sync_ilim = 11	-20 %	4189	+20 %	mA
I_{QFF}	Quiescent current in OFF mode				2	µA
F	Switching frequency			1		MHz
D	Switching duty cycle		10		95	%
R_{PD}	Output pull-down resistor	Can be switched off via BUCK2_PD_DIS			200	Ω
R_{PMOS}	On resistance PMOS	Include pin and routing			0.125	Ω
R_{NMOS}	On resistance NMOS	Include pin and routing			0.05	Ω

5.5 LDO Electrical Characteristics

5.5.1 LDO1

Unless otherwise noted, the following is valid for T_A = 25 ºC, VDLDO1 = 1.5 V, C_{OUT} = 2.2 µF, local sensing.

Table 10: LDO1 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
VDLDO1	Input voltage Note 1			1.5	2.2	V
V_{LDO1}	Output voltage	$I_{OUT} = I_{MAX}$	1		1.25	V
V_{LDO1_ACC}	Output voltage accuracy	I_{OUT} = ½ I_{MAX}	-3		+3	%
C_{OUT}	Output capacitance	Including voltage and temperature coefficients		2.2		µF
I_{MAX}	Maximum output current	V_{OUT} = 1.05 V V_{OUT} = 1.2 V			400 300	mA
I_{SHORT}	Short circuit current		500			mA
$V_{DROPOUT}$	Dropout voltage	$I_{OUT} = I_{MAX}$			200	mV
V_{SLINE}	Static line regulation	VDLDO1 = 1.4 V to 1.6 V $I_{OUT} = I_{MAX}$		5	20	mV
V_{SLOAD}	Static load regulation	I_{OUT} = 1 mA to I_{MAX}		5	20	mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{TRLINE}	Line transient response	VDLDO1 = 1.4 V to 1.6 V tr = tf = 10 µs I_{OUT} = I_{MAX}		5		mV
V_{TRLOAD}	Load transient response	VDLDO1 = 1.5 V tr = tf = 1 µs I_{OUT} = 1 mA to I_{MAX}		25		mV
PSRR		f = 10 Hz to 10 kHz V_{DD} = 1.5 V I_{OUT} = ½ I_{MAX}	50	60		dB
N	Output noise	f = 10 Hz to 100 kHz VDLDO1 = 1.5 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
R_{OFF}	Output Pull down resistor	Can be switched off via LDO1a_PD_DIS		100		Ω

Note 1 1.2 V output voltage is not supported below VDLDO1=1.4 V due to drop out voltage limitation.

5.5.2 LDO2

Unless otherwise noted, the following is valid for T_A = 25 ºC, V_{DLDO2} = 3.5 V, C_{OUT} = 1 µF, local sensing.

Table 11: LDO2 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DLDO2}	Input voltage			3.5	3.6	V
V_{LDO2}	Output voltage	I_{OUT} = I_{MAX}		1.8	3.3	V
V_{LDO2_ACC}	Output voltage accuracy	I_{OUT} = ½ I_{MAX}	-3		+3	%
C_{OUT}	Output capacitance	Including voltage and temperature coefficients		1		µF
I_{MAX}	Maximum output current				250	mA
I_{SHORT}	Short circuit current		300			mA
$V_{DROPOUT}$	Dropout voltage	I_{OUT} = I_{MAX}			1.2	V
V_{SLINE}	Static line regulation	V_{DLDO2} = 3.4 V to 3.6 V I_{OUT} = I_{MAX}		5	20	mV
V_{SLOAD}	Static load regulation	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
V_{TRLINE}	Line transient response	VDLDO1 = 1.4 V to 1.6 V tr = tf = 10 µs I_{OUT} = I_{MAX}		5	20	mV
V_{TRLOAD}	Load transient response	VDLDO1 = 1.5 V tr = tf = 1 µs I_{OUT} = 1 mA to I_{MAX}		25	50	mV
PSRR		f = 10 Hz to 10 kHz V_{DD} = 3.5 V I_{OUT} = ½ I_{MAX}	50	60		dB

Parameter	Description	Conditions	Min	Typ	Max	Unit
N	Output noise	f = 10 Hz to 100 kHz V_{LDO2} = 3.5 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
R_{OFF}	Output pull-down resistor	Can be switched off via LDO2_PD_DIS		100		Ω

5.5.3 Core LDO Electrical Characteristics

Unless otherwise noted, the following is valid for T_A = 25 ºC, V_{DD} = 5 V, C_{OUT} = 1 µF, local sensing.

Table 12: Core LDO Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Input voltage	I_{OUT} = 0 mA to I_{MAX}	2.45	2.5	2.55	V
C_{OUT}	Output capacitance	Including voltage and temperature coefficients		1		µF
I_{MAX}	Maximum output current				4	mA

5.6 Reference Voltage and Bias Current Generation

Unless otherwise noted, the following is valid for T_A = 25 ºC, V_{DD} = 5 V, C_{OUT} = 0.1 µF, local sensing.

Table 13: Reference Voltage and Bias Current Generation Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{REF}	Reference Voltage		-1 %	1.2	+1 %	V
T_{REF}	Reference Temperature Coefficient				100	ppm/ºC
	Decoupling Capacitor			0.1		µF

5.7 Supply Monitoring Electrical Characteristics

Table 14: Supply Monitoring Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD_FAULT}	V_{DD} fault			4.5		V
V_{DDIO_FAULT}	V_{DDIO} fault			2.4		V
T_{OVR}	Critical temperature			140	155	°C
	Temperature hysteresis			25		°C

5.8 Current Consumption

The 2-layer PCB layout was secured with 2 oz copper on the bottom layer of the PCB. The top layer only consisted of traces for signal routing.

The 4-layer PCB layout was also secured with 2 oz copper in the middle (ground) layer. The top layer only consisted of traces for signal routing.

The table below shows the results of several thermal experiments conducted with the PV88090. The best thermal performance can be achieved with more copper area for heat dissipation and increased thermal vias.

5.8.1 Power Use Case

Package	30-pin FC-MQFN 4.5x7mm
Board technology	PCB FR4 with 2 Oz Copper Thickness
High power	4-layer 240 mm * 200 mm
Low power	2-layer 240 mm * 200 mm
Ambient temperature	65 °C

Table 15: Power Dissipation

			High Power Dissipation		Low Power Dissipation	
Block	**Function**	**Voltage (V)**	**TYPE1**	**TYPE2**	**TYPE 1**	**TYPE 2**
Buck1	CORE	1, 1.2	8500 (mA) (2-phase)	9500 (mA) (2-phase)	5000 (mA) (1-phase)	5000 (mA) (1-phase)
Buck2	AUX	1.0, 1.2, 1.8, 2.5	2000 (mA)	1600 (mA)	0	2000 (mA)
Buck3	MEMORY	1.5	2000 + LDO1 (mA)	1600 + LDO1 (mA)**Note 2**	1000 (mA)	1000 (mA)
LDO2	EMMC	1.8	0	0	250(mA)	250(mA)
LDO1	ANA1V05	1.2, 1.05	400 ((mA))	400 ((mA))	0	0

Note 2 Increased Buck3 current from 1600 to 2000 (+ LDO1) in use case High Power Dissipation B exceeds the power budget based on the existing power estimate and package thermal data. To be reviewed based on thermal performance of revised package.

6 Functional Description

6.1 Control Signals

6.1.1 OTP Bank Select - OTPSEL

The OTPSEL pin is an input with pull-up which allows selection between two OTP start-up conditions. With this configurable start-up condition, the PV88090 is compatible with two generations of system on a chip (SOC) with different and mutually exclusive start-up conditions.

After the initial boot with the selected OTP settings, the SOC can customize the PV88090 configuration as required.

The OTPSEL input and pull-up are enabled and latched before each OTP read. The input and pull-up are then disabled to save power.

The OTPSEL pin should be tied to VSS to select start-up state 0, and leave no connection to select start-up state 1.

6.1.2 Address Select - ADRSEL

The ADRSEL pin is an input with pull-up which modifies the I^2C address. Bit 2 of the I^2C address takes the value of the ADRSEL pin.

6.1.3 Standby Pin - STBY

The STBY pin controls the power-up sequence of a system containing PV88090. If STBY is set to low, the system follows through the power-up sequence to active mode. If STBY is set to high, the system follows through the power-down sequence to standby mode. STBY should be low at power-up so that the system boots when power is applied.

6.1.4 Programming Voltage Input - VPP

The VPP pin must be connected to VSS on the application board.

6.1.5 Single Wire Communication I/O - SWC

The SWC I/O pin is a single wire communication interface used by the PV88090 to communicate the timing of the power-up and power-down sequences and to handle fault conditions.

Normal communication on the interface is a short low pulse. An error condition is indicated by a long pulse. Pulse widths are selectable.

The single wire interface can be disabled (swi_en=0). In this case the sequencing will not wait for a response from the other chip.

6.1.6 Interrupt Request - nIRQ

The nIRQ is an active low output signal which indicates that an interrupt causing event has occurred and status information is available in the related registers. Such information can be temperature, voltage, and over-current fault conditions.

When an event bit is set, the nIRQ signal is asserted (unless masked by a bit in the IRQ mask register). The nIRQ will not be released until the event registers have been cleared by writing a 1 to the related register for the bit to be cleared. The event registers should be written in page/repeated mode because the nIRQ will not be cleared until all registers with an asserted event have been reset. New events that occur during register writing will be held until all the event registers have been written. Then they are passed to the event register, ensuring the SOC does not miss them.

6.1.7 I²C Interface

The I²C interface provides access to control and status registers. The interface supports operations compatible to standard, fast, fast-plus, and high-speed mode of the I²C bus specification.

Communication on the I²C bus is always between two devices, one acting as the master and the other as the slave. PV88090 will only operate as a slave. The I²C interface has direct access to two pages of the PV88090 register map (up to 256 addresses).

SCL carries the I²C clock and SDA carries the bi-directional data. The I²C interface is open drain supporting multiple devices on a single line. The bus lines have to be pulled high by external pull-up resistors (2 kΩ to 20 kΩ). The attached devices only drive the bus lines low by connecting them to ground. As a result, two devices cannot conflict if they drive the bus simultaneously. In standard/fast mode the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and it does not have any relation to the PV88090 internal clock signals. PV88090 will synchronize with the host clock speed within the described limitations and will not initiate any clock arbitration or slow down.

If SDA is stuck the bus clears after receiving 9 clock pulses. Operation in high speed mode at 3.4 MHz requires a minimum 1.8 V interface supply voltage and a mode change in order to enable spike suppression and slope control characteristics compatible to the I²C specification.

6.1.8 I²CProtocol

All data is transmitted across the I²C bus in 8 bit groups. To send a bit the SDA line is driven to the intended state while the SCL is low. Once the SDA has settled, the SCL line is brought high and then low. This pulse on SCL clocks the SDA bit into the receiver’s shift register.

A two-byte serial protocol is used containing one byte for address and one byte data. Data and address transfer is transmitted MSB first for both read and write operations. All transmission begins with the START condition from the master during which the bus is in IDLE state (the bus is free). It is initiated by a high-to-low transition on the SDA line while the SCL is in the high state. A STOP condition is indicated by a low-to-high transition on the SDA line while the SCL is in the high state. The START and STOP conditions are illustrated in Figure 4.

Figure 4: Timing of the START and STOP conditions

The I²C bus is monitored by PV88090 for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. The acknowledge is achieved by pulling the SDA line low during the following clock cycle: white blocks marked with A in the following figures.

The protocol for a register write from master to slave consists of a START condition, a slave address, a read/write-bit, 8-bit address, 8-bit data, and a STOP condition. PV88090 responds to all bytes with an ACK.

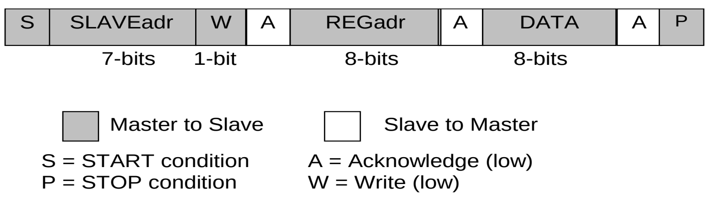


Figure 5: Byte Write Operation

When the host reads data from a register it first has to write access PV88090 with the target register address and then read access PV88090 with a repeated START, or alternatively a second START condition. After receiving the data the host sends NACK and terminates the transmission with a STOP condition.

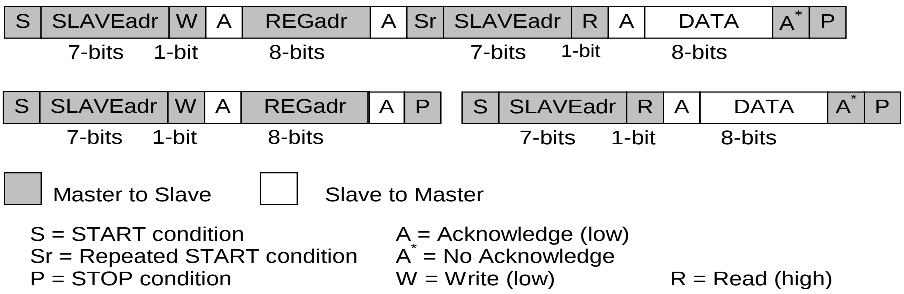


Figure 6: Examples of Byte Read Operations

Consecutive (page) read-out mode is initiated from the master by sending an ACK instead of NACK after receiving a byte, see Figure 7. The I²C control block then increments the address pointer to the next register address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a NACK directly after receiving the data, followed by a subsequent STOP condition. If a non-existent I²C address is read-out then the PV88090 will return code zero.

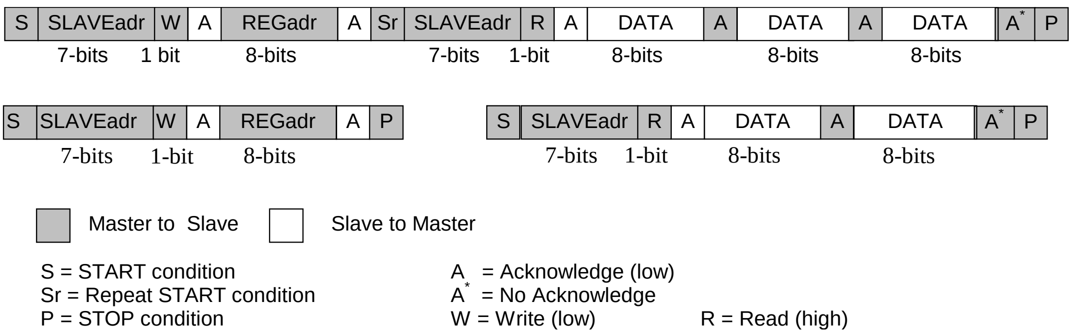


Figure 7: I²C Page Read

The slave address after the repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the master sends several data bytes following a slave register address. The I²C control block then increments the address pointer to the next I²C address, stores the received data, and sends an ACK until the master sends a STOP condition. The page write mode is illustrated in Figure 8.

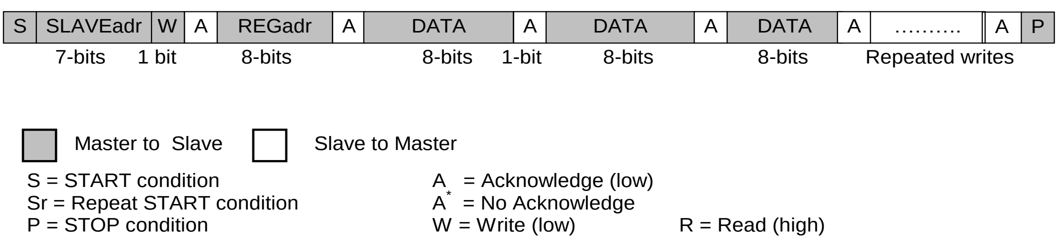


Figure 8: I²C Page Write

Via control WRITE_MODE a repeated write mode can be enabled. In this mode, the master can execute back-to-back write operations to non-consecutive addresses. This is achieved by transmitting register address and data pairs. The data will be stored in the address specified by preceding byte. The repeated write mode is illustrated in Figure 9.

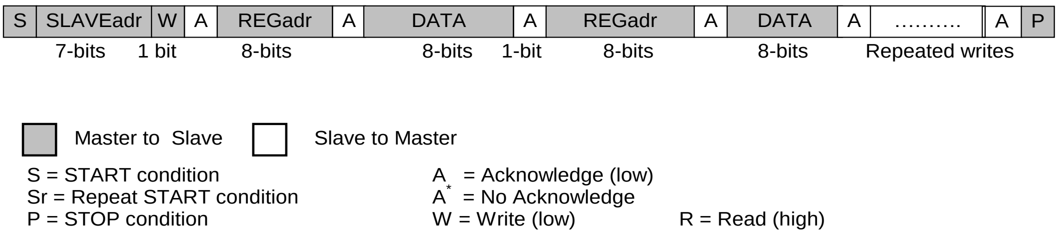


Figure 9: I²C Repeated Write

If a new START or STOP condition occurs within a message, the bus will return to IDLE-mode.

6.1.9 Dynamic Voltage Control

All buck converters can be controlled by DVC. The buck converters feature a voltage ramping feature that enables smooth transition from one voltage setting to another.

All output voltages can be controlled with SW via the I²C interface (VBUCK<x>). The I²C interface is operational when the device is in active mode.

6.2 LDOs

All LDOs employ Dialog Semiconductor's Smart Mirror dynamic biasing technology, see Figure 10, the illustrator which maintains high performance over a wide range of operating conditions and a power saving mode (sleep mode) to minimize the quiescent current during very low output current. The circuit technique offers significantly higher gain bandwidth performance than conventional designs, enabling higher power supply rejection performance at higher frequencies. PSRR is maintained across the full operating current range however quiescent current consumption is scaled to demand providing improved efficiency when current demand is low.

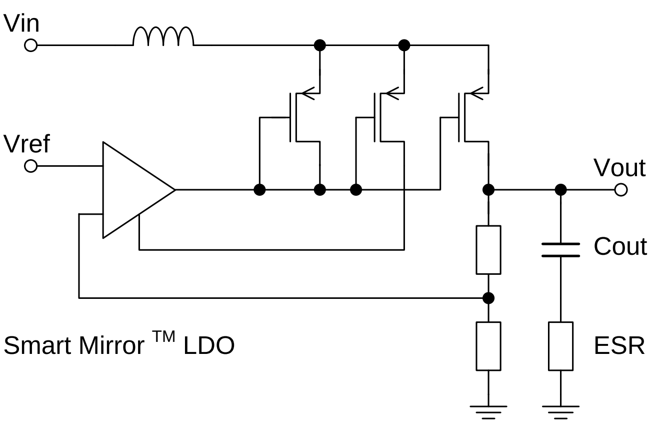


Figure 10: Smart Mirror™ Voltage Regulator

LDO1 provides the analog 1.05 V supply voltage (or 1.2 V depending on the system).To limit power dissipation the input voltage to LDO1 is the DDR voltage, typically 1.5 V.In standby mode the DDR voltage availability is not guaranteed. Therefore, the input voltage to the LDO switches to VDLDO2 during standby. The current in standby mode is reduced to 100 mA. During standby mode the output stage from VDLDO1 must be disabled such that reverse current does not flow from VDLDO2 to VDLDO1 (requires bulk switch on P-channel).

6.3 Buck Converters

DC-DC converters Buck1 to Buck3 are high efficiency synchronous step-down regulators operating at 1 MHz frequency and providing individual output voltages with ±3 % accuracy. The default output voltages of these regulators are loaded from OTP and can be programmed in 6.25 mV or 12.5 mV steps.The selectable switching frequency is high enough to allow the use of a 1.5 µH inductor. The operating mode of the buck converter is selected in the buck control register bits. The Buck3 converter can be forced to operate in either synchronous mode (PWM) or sleep mode (PFM). Additionally, the Buck3 converter has an automatic mode where it will switch between PWM and PFM modes depending on the load current. In PFM mode an internal zero crossing comparator is used to time the NFET turn-off, so an external Schottky diode is not needed. The quiescent current for all these DC-DC converters in PFM mode is 25 µA. The DC-DC single-phase converters feature a programmable pull-down resistors, which can be either enabled or disabled when the buck converted is powered down.Bucks 1 and 2 operate in PWM only. Buck3 operates in PWM in active mode, in PFM, if enabled, in standby mode, and also supports auto mode.

Table 16: Buck Converter Summary

Block	V_{OUT} (V)	I_{OUT} (mA)	External Components	Control
Buck1 Dual Phase Single Phase	0.9 to 1.3	PWM: 9500 PWM: 5000	L = 1.5 µH C_{OUT} > 60 µF	I^2C
Buck2	1.0 to 2.5	PWM: 2000	L = 1.5 µH C_{OUT} > 60 µF	I^2C
Buck3	1.3 to 3.4	PWM: 2000	L = 1.5 µH C_{OUT} > 60 µF	I^2C

6.3.1 Buck1

Buck1 has two switch banks. It can be configured as a one-phase buck using one of the switch banks (requires one external inductor), or as a two-phase buck using both switch banks (requires two external inductors, one driven by each switch bank).

The operating mode selection is determined by the system power calculation and the bill of materials (BOM). The power dissipation of the two-phase buck is reduced compared to the one-phase as the on resistance of the pass switches is halved.

For a high-end product (for example 9.5 A) it is expected to operate in two-phase.

For a low-end product (for example 5 A) there are two options:

- operate in one-phase mode and require only one inductor dissipating more power in Buck1
- operate in two-phase mode and require an extra inductor but save on power in Buck1, use the saved power enhance Buck2’s bandwidth

6.3.2 Buck2

Buck2 is a single-phase buck converter with a configurable output voltage (1.0 V to 2.5 V), 2 A maximum current (typically). The maximum current is dependent on the system power dissipation calculation.

Buck2 operates in forced PWM mode when enabled.

6.3.3 Buck3

Buck3 supplies the power to the DDR memory and to the LDO1. During normal mode it is always enabled and will run in forced PWM mode. During standby mode Buck3 may be enabled to supply the DDR memory standby current. In this mode it should operate in a low power discontinuous mode.

The Buck3 converter has an automatic mode where it will switch between PWM and PFM modes depending on the load current.

6.4 Power Modes

The power modes are illustrated in Table 17.

6.4.1 Normal Mode - Default Power-Up State

PV88090 enters the default power-up state at start-up when VDD exceeds the POR threshold.

In normal mode Bucks 1 and 3 (Core, Memory) and LDOs 1 and 2 (ANACORE, EMMC) are enabled.

Buck2 is disabled by default but can be enabled by I^2C control.

After start-up the SoC will either enable standby mode, or configure the normal operation mode with the I^2C interface.

6.4.2 Normal Mode

After the first start-up the SOC can configure which blocks are active in normal mode with the I^2C interface.

6.4.3 Standby Mode

Standby mode is entered when the STBY input pin is driven to the LDO1 voltage. In standby mode the device enters a low power state.

The memory supply from Buck3 is optionally maintained depending on OTP/I^2C setting.

When the STBY pin is driven to low the system will restart in normal mode.

Table 17: Function Block of Mode Operation

Block	Function	Normal Mode	Standby Mode
Buck1	CORE	Enabled OTP configurable: ● Two-phase (high end), one-phase (low end) ● Voltage = 1.0 V (high end)/1.2 V (low end)	Off
Buck2	I/O 3.3V	I^2C (default off) Voltage I^2C (default 1.0 V)	
Buck3	MEMORY	Enabled Voltage I^2C (default 1.5 V)	I^2C (default off) Voltage I^2C (default 1.5 V)
LDO1	1.5V	Enabled (high end)/off (low end) Voltage OTP/I^2C (default 1.05 V)	I^2C enabled (high end)/off (low end) (default) Voltage OTP/I^2C (default 1.05 V)
LDO2	EMMC	OTP/I^2C enabled (high end)/off (low end)	Off
Serial Control	I^2C	Enabled	Enabled
Enable Control	STBY PIN	Enabled	Enabled

Block	Function	Normal Mode	Standby Mode
Interrupt	nIRQ PIN	Enabled	Enabled
Reference		Enabled	Enabled
Trimmed OSC		Enabled	Enabled
Int Dig Supply		Enabled	Enabled

6.4.4 Power Supply Sequencer

The PV88090 start-up is supplied controlled by a sequencer that contains a programmable step timer, a variable ID array of time slot pointers, and three predefined pointers (SYSTEM_END, POWER_END, and MAX_COUNT). The sequencer is able to control up to six IDs (three buck converters, three LDOs), which can be grouped in three power domains. The power domains are configurable and their limits are defined by the location pointers SYSTEM_END, POWER_END, and MAX_COUNT.

The lowest level power domain SYSTEM starts at step 1 and ends at the step that is defined by the location pointer SYSTEM_END. The second level domain POWER starts at the successive step and ends at POWER_END. The values of pointer SYSTEM_END, POWER_END, and MAX_COUNT are predefined in OTP registers and must be configured as
SYSTEM_END < POWER_END < MAX_COUNT.

The SYSTEM domain can be viewed as a basic set of supplies that are mandatory to power up the application. The second (POWER) domain includes additional supplies that are required to wake the application and put PV88090 into active mode.

Up to three buck converters and three LDOs can be assigned unique sequencer IDs. The power-up sequence is then defined by an OTP register bank that contains a series of supplies (and other features), which are pointing to a sequencer time slot. Several supplies can point to the same time slot, and thereby enable them in parallel. Time slots that have no IDs pointing towards them are dummy steps that do nothing but insert a configurable time delay. Supplies that are not pointing towards a sequencer time slot (with a step number greater than zero and less than MAX_COUNT) will not be enabled by the power sequencer and have to be controlled individually by the host (via the power manager interface).

The delay between the sequencer steps is controlled via a 4-bit, OTP-programmable, timer unit (SEQ_TIME) with a default delay of 128 µs per step (minimum 32 µs and maximum 8 ms).

Asserting control register bit SHUTDOWN forces PV88090 to power down to step 0 and then enter reset mode.

6.4.5 Boot Sequence

The SOC power-on-reset (POR) at switch on is timed from standby 3.3 V and is 100 ms. The PV88090 start-up sequence must complete within the POR.

Table 18: The Start-Up Sequence at POR

	Event	Action
	Reset mode	
1	VDD > POR Threshold and STBY = 0	VREF START to PV88090
2	VDDIO good on PV88090 Detects START	PV88090 loads OTP settings PV88090 starts Buck1 PV88090 starts Buck2 PV88090 starts Buck3 PV88090 starts LDO1 (Analog 1.05/1.2) PV88090 starts LDO2 (EMMC)

	Event	Action
3		Default normal mode
4	I^2C write	Enable/disable block with I^2C control

The SOC initiates wake-up from standby mode by taking STBY low. The start-up time before boot is timed by the SOC and is 100 ms. The PV88090start-up sequence must complete this time.

Table 19: Start-Up Sequence Example from Standby

	Event	Action
	Standby mode	
1	STBY = 0	detects START signal
2	STBY = 0	1. starts Buck1 2. starts Buck2 3. starts Buck3 or switches Buck3 to PWM mode if already active 4. PV88090starts LDO1 (analog 1.05 V/1.2 V) or switches supply from VDDLDO to Buck3 if LDO1 was active in standby. PV88090 starts LDO2 (EMMC)
3		**Normal mode**
4	I^2C write	Enable/disable block under I^2C control

Blocks can be set to active in normal mode by setting the appropriate BLOCK_EN register bit via I^2C.

Table 20: Shutdown Sequence Example to Standby

	Event	Action
	Normal mode	
1	STBY = 1	1. detects START signal
3	PV88090	PV880902. enters disable mode 3. disables LDO2 (EMMC) PV880904. disables LDO1 (analog 1.05 V/1.2 V) 5. PV88090disables Buck3 or switches Buck3 to low power mode if enabled in standby. 6. PV88090disables Buck2 7. PV88090disables Buck1
		Standby mode

Blocks may be set to remain active in standby mode by setting the appropriate BLOCK_STBY register bit via I^2C.

If the STBY bit is flipped during a power-up/-down sequence the sequence should be reversed safely. If STBY = 0 the delay time before SOC boot must still be met.

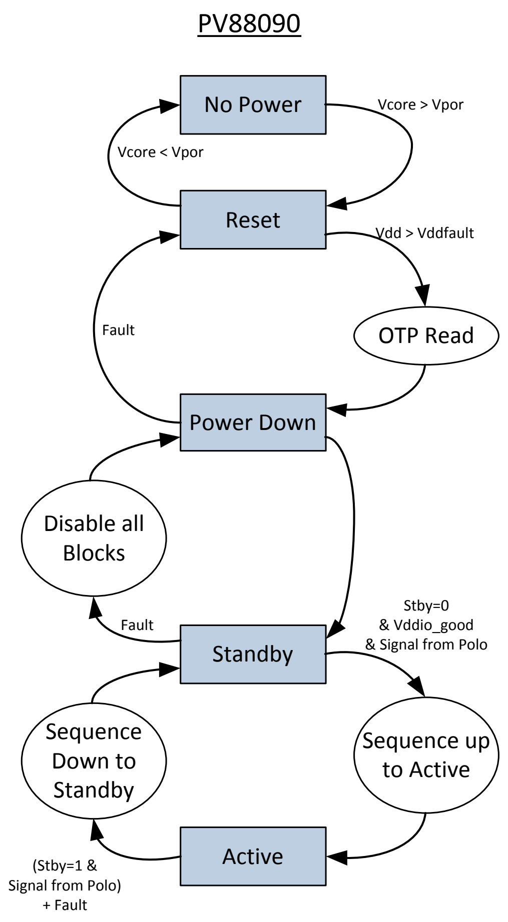


Figure 11: PV88090 Boot Sequence

6.5 Monitoring and Interrupts

An interrupt is generated if the chip detects an over-current on an LDO, or a SWITCH, or an over-temperature condition, and if the interrupt mask is set for that bit.

Table 21: Functional Block Mode of Monitoring and Interrupts

	Voltage Good	Over-Current
V_{REF}	Start sequence status bit	N/A
DVDD Supply	Start sequence status bit	N/A
Bucks	Start sequence status bit	N/A
VDDIO	Start sequence	N/A
LDOs	Start sequence status bit	Interrupt after start-up
Over-temperature	N/A	Interrupt

6.6 Power-On-Reset

The main POR signal is directly dependent on DVDD voltage. The logic generating the POR signal is controlled by two comparators – one monitoring the upper 2.35 V (nominal) POR threshold and the other the lower 2.0 V threshold. Both comparators use node VREF as input reference which means the upper threshold is affected by the untrimmed bandgap variation.

The internal LDO is only enabled after the VREF voltage has been ramped up after a VDD supply connection. A dedicated VDD comparator monitors the VDD voltage and gates all start-up activities if it is below 2.5 V. This comparator is only active during the start-up sequence.

6.7 Reference Voltage and Bias Current Generation

The VREF voltage reference, bias current, and internally regulated DVDD (2.5 V) supply are permanently enabled after the VDD supply reaches 2.5 V. The internal bandgap circuit and the VREF buffer provide 1.2 V reference with a low (<100 ppm) temperature coefficient. The current bias is derived from the VREF voltage across an internal trimmed resistor to provide a reference current which is scaled appropriately to provide the bias current for the blocks. The internal resistor is made up of a combination of resistor types with different temperature coefficients to keep the current flat over temperature for setting current limits.

6.8 Over-Temperature

The over-temperature circuit monitors the junction temperature. A fault condition is generated if the junction temperature exceeds the critical temperature (T_{OVR}). The fault condition remains asserted until the temperature drops below a safe threshold.

6.9 Supply Monitoring

The 5 V V_{DD} supply is monitored by the V_{DD} fault comparator. The circuits remain in the reset state until 5 V has been established ($V_{DDFAULT}$ low). If the 5 V V_{DD} supply falls below the $V_{DDFAULT}$ threshold the input supply is too low, and a fault condition is generated. The V_{DDIO} voltage is monitored and if it is below $V_{DDIOFAULT}$ the I^2C interface and the single wire communications is disabled.

6.10 Fault Condition

A fault condition is generated by:

- An over-temperature event
- An LDO over-current event
- An under-voltage of the 5 V supply

If a fault condition is detected the chip will signal to the other chip, then follow its power-down sequence without waiting for the other chip to complete its part. At the end of the power-down sequence the chip will move to the reset state.

In the reset state the registers, apart from the fault log, will be reset and the OTP will be reloaded at start-up.

7 Register Definitions

7.1 Register Page Control

Status / Configuration									
Register	**Address**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
STATUS_A	0x0001	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OVER_TMP	VDD_FLT
STATUS_B	0x0002	Reserved	Reserved	Reserved	Reserved	Reserved	LDO1a_OK	LDO2_OK	Reserved
EVENT_A	0x0003	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	E_OVER_TMP	E_VDD_FLT
EVENT_B	0x0004	Reserved	Reserved	Reserved	Reserved	Reserved	E_LDO1a_FAIL	E_LDO2_FAIL	Reserved
FAULT_LOG	0x0005	Reserved	Reserved	Reserved	Reserved	Reserved	VDDIO_FAULT	OVER_TEMP	VDD_FAULT
IRQ_MASK_A	0x0006	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	M_OVER_TMP	M_VDD_FLT
IRQ_MASK_B	0x0007	Reserved	Reserved	Reserved	Reserved	M_LDO1a_FAIL	M_LDO1a_FAIL	M_LDO2_FAIL	Reserved
CONTROL_B	0x0009	SHUTDOWN	Reserved (Set to 0)	Reserved	I2C_SPEED	Reserved	Reserved (Set in OTP)	Reserved	Reserved
INTERFACE	0x000C	I^{2}C Slave address set by OTP			Reserved	Reserved	Reserved	Reserved	Reserved

Supplies									
Register	**Address**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
BUCK1_CONF0	0x0018	BUCK1_EN	VBUCK1						
BUCK1_CONF1	0x0019	BUCK1_PD_DIS	BUCK1_SYNC_ILIM					Reserved (Set to 0x2)	
BUCK2_CONF0	0x001B	BUCK2_EN	VBUCK2						
BUCK2_CONF1	0x001C	Reserved	Reserved (Set in OTP)		Reserved	BUCK2_SYNC_ILIM		Reserved	
BUCK3_CONF0	0x001D	BUCK3_EN	VBUCK3						
BUCK3_CONF1	0x001E	Reserved	Reserved (Set in OTP)		Reserved	BUCK3_SYNC_ILIM		Reserved	
LDO2	0x001F	LDO2_PD_DIS	LDO2_EN	VLDO2					
LDO1a	0x0020	LDO1a_PD_DIS	LDO1a_EN	VLDO1a					

7.2 Status and Events

7.2.1 Register STATUS_A

Address	Name	POR value	Status
0x0001	STATUS_A	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OVER_TMP	VDD_FLT

Field name	Bits	Type	POR	Description
OVER_TMP	[1]	RO	0x0	Indicates Over Temperature Status Over Temperature Detected **Value** / **Description** 0x0: 0:Normal 0x1: 1:Over Temperature Fault
VDD_FLT	[0]	RO	0x0	Indicates VDD below VDD_FAULT Threshold **Value** / **Description** 0x0: 0:Normal 0x1: 1:Low VDD Fault

7.2.2 Register STATUS_B

Address	Name	POR value	Status
0x0002	STATUS_B	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	LDO1A_OK	LDO2_OK	Reserved

Field name	Bits	Type	POR	Description
LDO1A_OK	[2]	RO	0x0	Indicates LDO1 (VDLDO1) Fault Status **Value** / **Description** 0x0: 0:Normal 0x1: 1:LDO2 (VDLDO1) Fault
LDO2_OK	[1]	RO	0x0	Indicates LDO2 Fault Status **Value** / **Description** 0x0: 0:Normal 0x1: 1:LDO2 Fault

7.2.3 Register EVENT_A

Address	Name	POR value	IRQ event
0x0003	EVENT_A	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	E_OVER_TMP	E_VDD_FLT

Field name	Bits	Type	POR	Description
E_OVER_TMP	[1]	RW W1CL	0x0	Event caused by Over Temperature Status (Write 1 to clear) **Value** / **Description** 0x0: 0:Normal 0x1: 1:Event Over Temperature
E_VDD_FLT	[0]	RW	0x0	Event caused by VDD below VDD_FAULT Threshold

		W1CL		Value / Description: 0x0 — 0:Normal 0x1 — 1:Event Low VDD

7.2.4 Register EVENT_B

Address	Name	POR value	
0x0004	EVENT_B	0x00	IRQ event

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	E_LDO1A_FAIL	E_LDO2_FAIL	Reserved

Field name	Bits	Type	POR	Description
E_LDO1A_FAIL	[2]	RW W1CL	0x0	Event caused by LDO1 (VDLDO1) Fault Status (Write 1 to clear) Value / Description: 0x0 — 0:Normal 0x1 — 1:Event LDO1 (VDLDO1) Fault
E_LDO2_FAIL	[1]	RW W1CL	0x0	Event caused by LDO2 Fault Status (Write 1 to clear) Value / Description: 0x0 — 0:Normal 0x1 — 1:Event LDO2 (VDLDO2) Fault

7.2.5 Register FAULT_LOG

Address	Name	POR value	
0x0005	FAULT_LOG	0x01	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	VDDIO_FAULT	OVER_TEMP	VDD_FAULT

Field name	Bits	Type	POR	Description
VDDIO_FAULT	[2]	RW W1CL	0x0	Power Down by VDDIO_FAULT (Write 1 to clear) Value / Description: 0x0 — 0:Normal 0x1 — 1:Fault
OVER_TEMP	[1]	RW W1CL	0x0	Power Down by Junction Over Temperature Detection (Write 1 to clear) Value / Description: 0x0 — 0:Normal 0x1 — 1:Fault
VDD_FAULT	[0]	RW W1CL	0x1	Power Down by VDD Under Voltage Detection (Write 1 to clear) Value / Description: 0x0 — 0:Normal 0x1 — 1:Fault

7.2.6 Register IRQ_MASK_A

Address	Name	POR value	
0x0006	IRQ_MASK_A	0x00	Typical OTP value : OTP 0x04

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	M_OVER_TMP	M_VDD_FLT

Field name	Bits	Type	POR	Description
M_OVER_TMP	[1]	RW OTP	0x0	nIRQ Mask - Over Temperature Fault **Value** / **Description** 0x0: 0:nIRQ from Over Temp Event 0x1: 1:Mask nIRQ from Over Temp Event
M_VDD_FLT	[0]	RW OTP	0x0	nIRQ_Mask - VDD below VDD_FAULT Threshold **Value** / **Description** 0x0: 0:nIRQ from VDD_FAULT Event 0x1: 1:Mask nIRQ from VDD_FAULT Event

7.2.7 Register IRQ_MASK_B

Address	Name	POR value	
0x0007	IRQ_MASK_B	0x00	Typical OTP value : OTP 0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	M_LDO1A_FAIL	M_LDO2_FAIL	Reserved

Field name	Bits	Type	POR	Description
M_LDO1A_FAIL	[2]	RW OTP	0x0	nIRQ Mask - LDO1 (VDLDO1) Fail **Value** / **Description** 0x0: 0:nIRQ from LDO1 (VDLDO1) Fault Event 0x1: 1:Mask nIRQ from LDO1 (VDLDO1) Fault Event
M_LDO2_FAIL	[1]	RW OTP	0x0	nIRQ Mask - LDO2 Fail **Value** / **Description** 0x0: 0:nIRQ from LDO2 Fault Event 0x1: 1:Mask nIRQ from LDO2 Fault Event

7.2.8 Register CONTROL_B

Address	Name	POR value	
0x0009	CONTROL_B	0x24	Typical OTP value : 0x20

7	6	5	4	3	2	1	0
SHUTDOWN	Reserved	Reserved	I2C_SPEED	Reserved	Reserved	Reserved	Reserved

Field name	Bits	Type	POR	Description
SHUTDOWN	[7]	RW RT0	0x0	If written to '1' the Sequencer powers down to RESET Mode. Automatically cleared (back to 0) before leaving RESET mode
I2C_SPEED	[4]	RW OTP	0x0	I2C DATA READ Speed **Value** / **Description** 0x0 (POR): 0: 400 kHz 0x1: 1: 1.1 MHz

7.2.9 Register INTERFACE

Address	Name	POR value	Typical OTP value : 0x40
0x000C	INTERFACE	0x80	

7	6	5	4	3	2	1	0
IF_BASE_ADDR			Reserved	Reserved	Reserved	Reserved	Reserved

Field name	Bits	Type	POR	Description
IF_BASE_ADDR	[7:5]	RW OTP	0x4	3 MSB of the I2C Interfaces Base Address XXX10000 10010010 = 0x92 write address of HS (I2C) IF 10010011 = 0x93 read address of HS (I2C) IF

Value	Description
0x0	Slave Address 0x12
0x1	Slave Address 0x32
0x2	Slave Address 0x52
0x3	Slave Address 0x72
0x4	Slave Address 0x92 (Default)
0x5	Slave Address 0xB2
0x6	Slave Address 0xD2
0x7	Slave Address 0xF2

7.3 Supplies (Bucks and LDOs)

7.3.1 Register BUCK1_CONF0

Address	Name	POR value	Typical OTP value (High End) 0x40 (Low End) 0x60
0x0018	BUCK1_CONF0	0x50	

7	6	5	4	3	2	1	0
BUCK1_EN	VBUCK1						

Field name	Bits	Type	POR	Description
BUCK1_EN	[7]	RW OTP	0x0	

Value	Description
0x0	0: BUCK1 Disabled
0x1	1: BUCK1 Enabled

Field name	Bits	Type	POR	Description
VBUCK1	[6:0]	RW OTP	0x50	Buck1 Target Voltage.

Value	Description
0x30	0.9V
...	...
0x40	1V
0x60	1.2V
...	...
0x70	1.3V

7.3.2 Register BUCK1_CONF1

Address	Name	POR value	Typical OTP value (High End) 0x7E (Low End) 0x7E
0x0019	BUCK1_CONF1	0x09	

7	6	5	4	3	2	1	0
BUCK1_PD_DIS	BUCK1_SYNC_ILIM					Reserved (Set to 0x2)	

Field name	Bits	Type	POR	Description
BUCK1_PD_DIS	[7]	RW	0x0	Pull down disable

		OTP		Value: 0x0 — 0: Enable Pull Down Resistor 0x1 — 1: No Pull Down Resistor in OFF Mode
BUCK1_SYNC_ILIM	[6:2]	RW OTP	0x2	BUCK1 Peak Current Limit Peak current is DC current + Inductor Ripple Value — Description 0x0 — 00000: 220mA 0x1 — 00001: 440mA & — ... 0x30 — 11110: 6820mA 0x31 — 11111: 7040mA

7.3.3 Register BUCK2_CONF0

Address	Name	POR value	Typical OTP value : 0x40
0x001B	**BUCK2_CONF0**	**0x50**	

7	6	5	4	3	2	1	0
BUCK2_EN	VBUCK2						

Field name	Bits	Type	POR	Description
BUCK2_EN	[7]	RW OTP	0x0	Value — Description 0x0 — 0: BUCK2 Disabled 0x1 — 1: BUCK2 Enabled
VBUCK2	[6:0]	RW OTP	0x50	Buck Target Voltage. Value — Description (BUCK2_VDAC_RANGE=0,BUCK2_VRANGE_GAIN=0) **0x40** — **1000000: 1.0V** … — … **0x60** — **1100000: 1.2V** … — … 0x7E — 1111110: 1.3875V 0x7F — 1111111:1.39375V Value — Description (BUCK2_VDAC_RANGE=1,BUCK2_VRANGE_GAIN=0) 0x0 — 0000000: 1.4V 0x1 — 0000001: 1.40625V … — … **0x40** — **1000000: 1.8V** … — … 0x7E — 1111110: 2.1875V 0x7F — 1111111: 2.19375V Value — Description (BUCK2_VDAC_RANGE=0,BUCK2_VRANGE_GAIN=1) … — … 0x67 — 1010011: 2.4875V **0x68** — **1010100: 2.5V**

7.3.4 Register BUCK2_CONF1

Address	Name	POR value	Typical OTP value : 0x29

0x001C	BUCK2_CONF1	0x29					
7	6	5	4	3	2	1	0
Reserved	Reserved		Reserved	BUCK2_SYNC_ILIM		Reserved	

Field name	Bits	Type	POR	Description
BUCK2_SYNC_ILIM	[3:2]	RW OTP	0x2	BUCK2 Peak Current Limit Peak current is DC current + Inductor Ripple **Value** / **Description** 0x0: 00: 1496mA 0x1: 01: 2393mA 0x2: 10: 3291mA 0x3: 11: 4189mA

7.3.5 Register BUCK3_CONF0

Address	Name	POR value	
0x001D	BUCK3_CONF0	0x50	Typical OTP value : 0x10

7	6	5	4	3	2	1	0
BUCK3_EN	VBUCK3						

Field name	Bits	Type	POR	Description
BUCK3_EN	[7]	RW OTP	0x0	**Value** / **Description** 0x0: 0: BUCK3 Disabled 0x1: 1: BUCK3 Enabled
VBUCK3	[6:0]	RW OTP	0x50	Buck Target Voltage. **Value** / **Description (BUCK3_VDAC_RANGE=0,BUCK3_VRANGE_GAIN=0)** **0x70: 1110000: 1.3V** … … 0x7E: 1111110: 1.3875V 0x7F: 1111111:1.39375V **Value** / **Description (BUCK3_VDAC_RANGE=1,BUCK3_VRANGE_GAIN=0)** 0x0: 0000000: 1.4V 0x1: 0000001: 1.40625V … … **0x10: 0010000: 1.5V** … … **0x30: 0110000: 1.7V**

7.3.6 Register BUCK3_CONF1

Address	Name	POR value	
0x001E	BUCK3_CONF1	0x29	Typical OTP value : 0x29

7	6	5	4	3	2	1	0
Reserved	Reserved		Reserved	BUCK3_SYNC_ILIM		Reserved	

Field name	Bits	Type	POR	Description
BUCK3_SYNC_ILIM	[3:2]	RW OTP	0x2	BUCK3 Current Limit: **Value** / **Description** 0x0: 00: 1496mA 0x1: 01: 2393mA

				&	10: 3291mA
				0x30	11: 4189mA

7.3.7 Register LDO2

Address	Name	POR value	Typical OTP value : 0x0C
0x001F	LDO2	**0x00**	

7	6	5	4	3	2	1	0
LDO2_PD_DIS	LDO2_EN	VLDO2					

Field name	Bits	Type	POR	Description
LDO2_PD_DIS	[7]	RW OTP	0x0	LDO2 Pull down disable. **Value** / **Description** 0x0: 0: Enable Pull Down Resistor 0x1: 1: No Pull Down Resistor in OFF Mode
LDO2_EN	[6]	RW OTP	0x0	LDO2 Enable **Value** / **Description** 0x0: 0: LDO2 Disabled 0x1: 1: LDO2 Enabled
VLDO2	[5:0]	RW OTP	0x0	LDO2 voltage select **Value** / **Description** 0x0: 000000: 1.20V 0x1: 000001: 1.25V 0x2: 000010: 1.30V ...: ... 0x28: 101000: 3.20V 0x29: 101001: 3.25V 0x2A: 101010: 3.30V 0x2B: 101011: 3.35V

7.3.8 Register LDO1a [1.5V Supply]

Address	Name	POR value	Typical OTP value (High End) 0x90 (Low End) 0x96
0x0020	**LDO1A**	**0x20**	

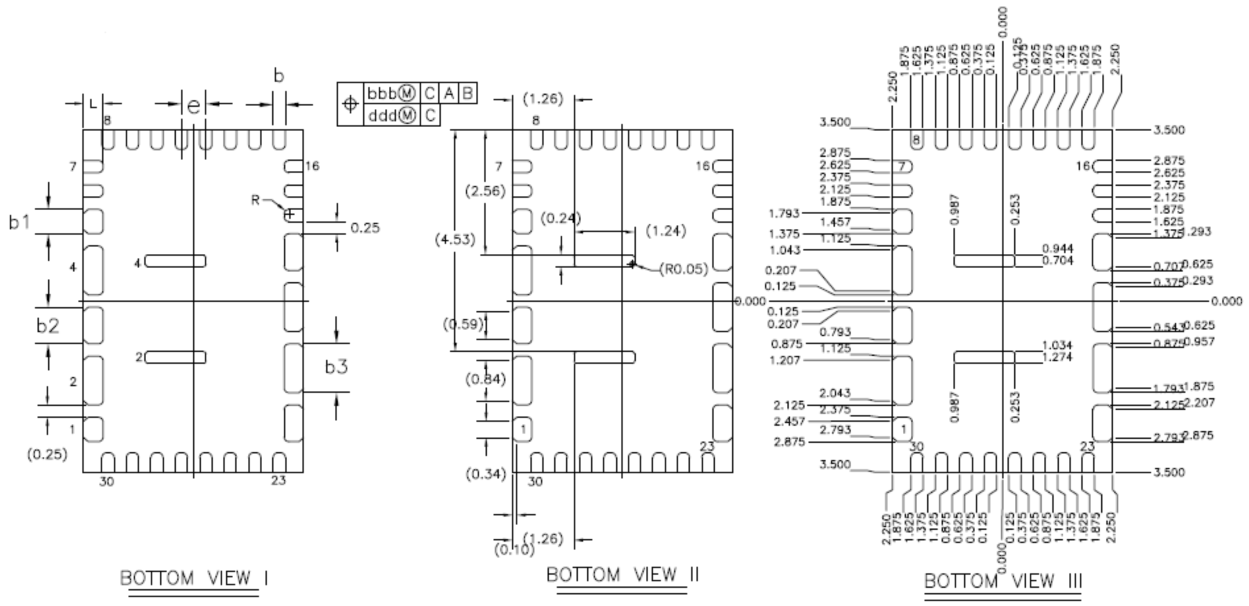
7	6	5	4	3	2	1	0
LDO1a_PD_DIS	LDO1a_EN	VLDO1A					

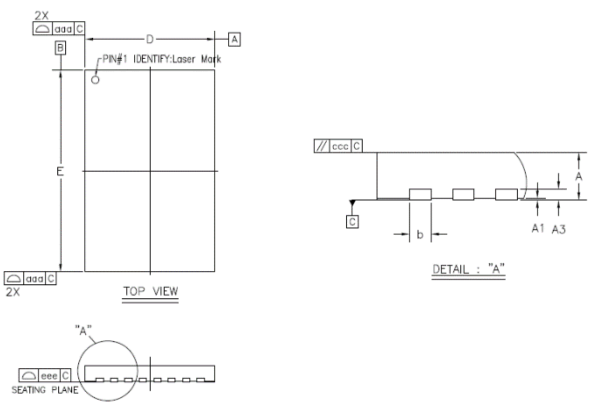
Field name	Bits	Type	POR	Description
LDO1a_PD_DIS	[7]	RW OTP	0x0	LDO1a (VDLDO1) Pull down disable. *** Must set to 1 if LDO1a is enabled or in overlap mode **Value** / **Description** 0x0: 0: Enable Pull Down Resistor 0x1: 1: No Pull Down Resistor in OFF Mode
LDO1a_EN	[6]	RW OTP	0x0	LDO1a [1.5V Supply] Enable. **Value** / **Description** 0x0: 0: LDO1a (VDLDO1) Disabled 0x1: 1: LDO1a (VDLDO1) Enabled
VLDO1a	[5:0]	RW OTP	0x20	LDO voltage select. **Value** / **Description** 0x10: 001111: 1.050V

				0x11	001111: 1.075V
				0x12	001111: 1.100V
				0x13	001111: 1.125V
				0x14	001111: 1.150V
				0x15	001111: 1.175V
				0x16	001111: 1.200V
				0x17	001111: 1.225V

8 Package Information

8.1 Package Outlines





Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.577	0.60	0.020	0.023	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.127 REF			0.005 REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.45	0.50	0.55	0.018	0.020	0.022
b2	0.70	0.75	0.80	0.028	0.030	0.031
b3	0.95	1.00	1.05	0.037	0.039	0.041
D	4.43	4.50	4.57	0.174	0.177	0.180
E	6.93	7.00	7.07	0.273	0.276	0.278
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
R	0.10	---	0.15	0.004	---	0.006
aaa	0.15			0.006		
bbb	0.10			0.004		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 12: PV88090 Package Outline Drawing

9 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. The xx represents a placeholder for the specific OTP variant. For details and availability, please consult Dialog Semiconductor's customer support portal or your local sales representative.

Table 22: Ordering Information

Part Number (Note 3)	Package Information	Package Description	Pack Outline
PV88090-xxFQ1	30-pin FC-MQFN	Waffle tray	Figure 12
PV88090-xxFQ2	30-pin FC-MQFN	Tape and Reel	Figure 12

Note 3 xx is the OTP variant. Please refer the detail information in OTP variant application note AN-PV-07.

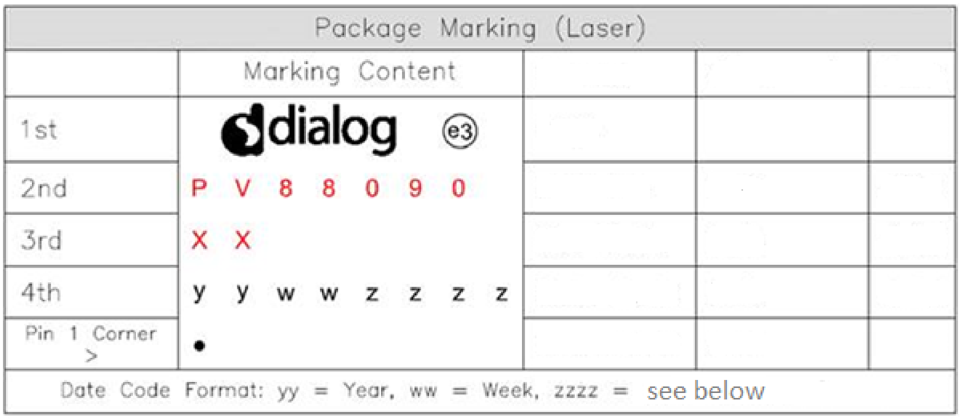


Figure 13: PV88090 Package Markings

Where zzzz = first z is wafer fab, second z is assembly supplier, third and fourth z are unique lot identifiers.

10 Application Information

10.1 Capacitors Selection

Ref	Value	Tol.	Size (mm)	Height (mm)	Temp. Char.	Rating (V)	Part
VLDO2	2 x 1 µF	±10 %	0603	0.9	X5R	10	GRM188R61A105KA61D
VLDO1	1 µF	±10 %	0603	0.9	X5R	10	GRM188R61A105KA61D
VDLDO1	2.2 µF	±10 %	0603	0.9	X5R	10	GRM188R61A225KE34
VBuck1	2 × 100 nF	±10 %	0402	0.55	X7R	16	GRM155R71C104KA88D
	2 × 10 µF	±10 %	0805	1.35	X5R	16	GRM21BR61C106KE15L
	2 × 47 µF	±20 %	0805	1.45	X5R	10	GRM21BR61A476ME15
VBuck2 VBuck3	100 nF	±10 %	0402	0.55	X7R	16	GRM155R71C104KA88D
	10 µF	±10 %	0805	1.35	X5R	16	GRM21BR61C106KE15L
	2 × 47 µF	±20 %	0805	1.45	X5R	10	GRM21BR61A476ME15

VREF VDDIO	100 nF	±10 %	0402	0.55	X5R	10	GRM155R61A104KA01D
VDD VDVDD	1 µF	±10 %	0603	0.9	X5R	10	GRM188R61A105KA61D

10.2 Inductor Selection

Ref	Value	ISAT (A)	IRMS (A)	DCR (Typ) (mΩ)	Size (W×L×H) (mm)	Part
Buck1 Buck2 Buck3	1.5 µH	11.5 10	11 8.5	9.7 12	7.1×6.5×3	TDK SPM6530T -1R5M Sunlord WPL6530H1R5MT
		11.5 10	11 8.5	9.7 12	7.1×6.5×3	TDK SPM6530T -1R5M Sunlord WPL6530H1R5MT
		11.5 10	11 8.5	9.7 12	7.1×6.5×3	TDK SPM6530T -1R5M Sunlord WPL6530H1R5MT

11 Layout Guidelines

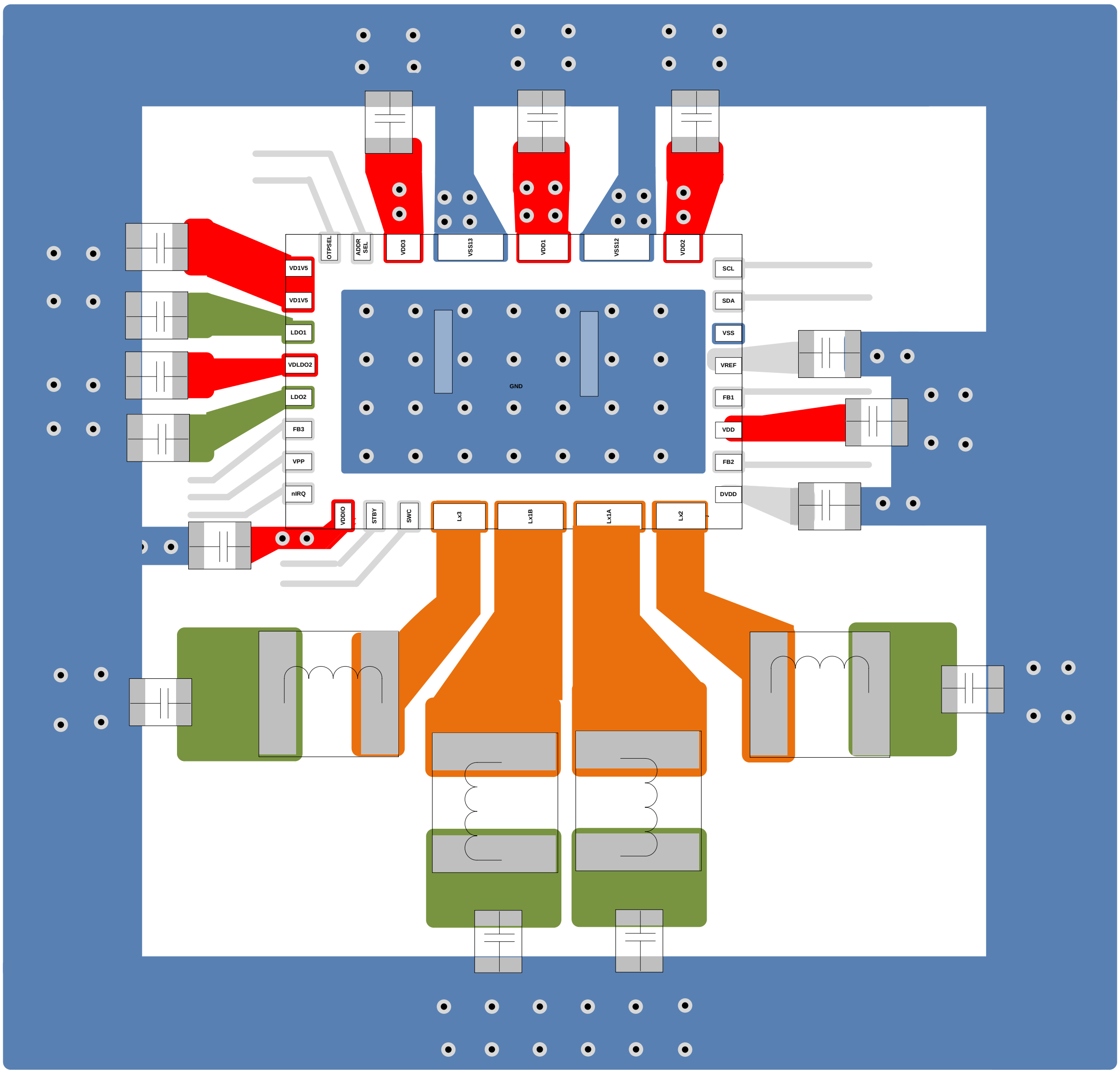


Figure 14: PCB Layout for PV88090

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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