User's Manual

A Renesas Company

ISL854102DEMO2Z

User's Manual: Demonstration Board

Industrial Analog and Power

Rev 0.00 Aug 2017

ISL854102DEMO2Z

Demonstration Board

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1. Overview

The ISL854102DEMO2Z board uses the ISL854102 in an isolated buck configuration. The primary output is configured to be 12V and the dual secondary outputs are +12V and -12V, respectively. The board is used to demonstrate the performance of the ISL854102, wide V_{IN} synchronous buck regulator configured to support a primary output, and a dual inverting and non-inverting secondary output.

The ISL854102 is the higher current version of the family of ISL85410 (1A), ISL854102 (1.2A), and ISL85418 (0.8A), which are offered in a 4mmx3mm 12 Ld DFN package with 1mm maximum height.

1.1 Key Features

- Wide input voltage range up to 40V
- Synchronous operation for high efficiency
- Integrated high-side and low-side NMOS devices
- Internal fixed (500kHz) or adjustable (300kHz to 2MHz) switching frequency
- Continuous output current up to 0.8A at primary output and ±150mA at secondary outputs
- Internal or external soft-start
- Minimal external components required
- Power-good and enable functions available

1.2 Specifications

These boards have been configured and optimized for the following operating conditions:

- V_{IN} = 24V
- V_{OUT_PR} = +12V, V_{OUT_SC} = -12V
- I_{MAX_PR} = 0.8A, I_{MAX_SC} = 150mA
- f_{SW} = 500kHz

1.3 Ordering Information

Part Number	Description
ISL854102DEMO2Z	Demonstration board

1.4 Related Literature

- For a full list of related documents, visit our website
    - ISL854102 product page

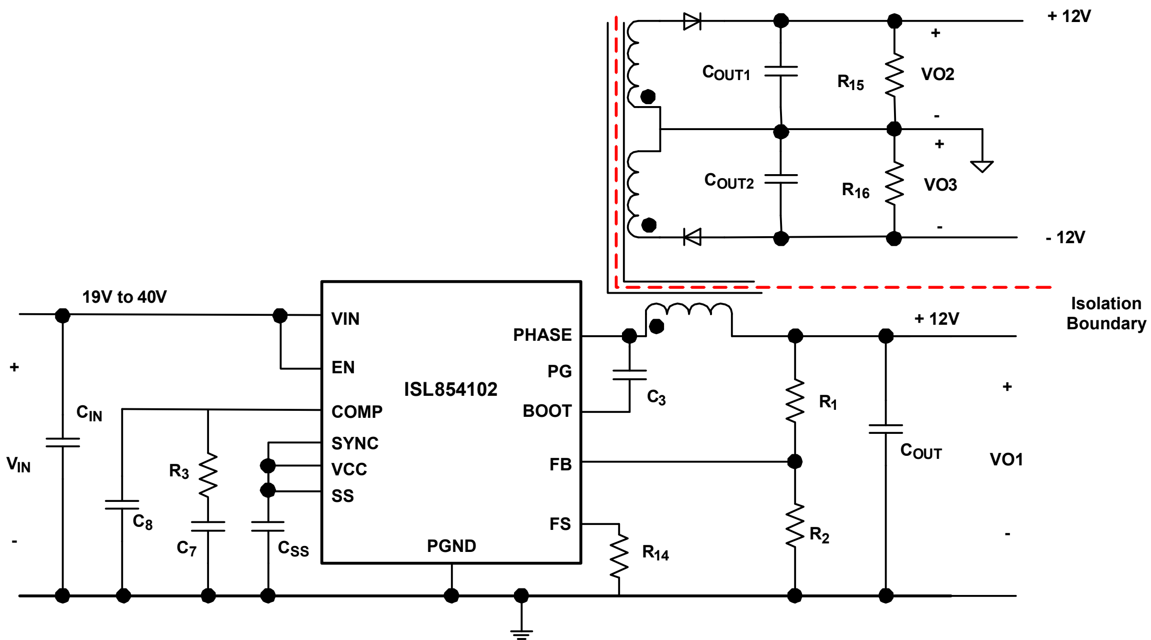

Figure 1. Block Diagram

2. Functional Description

2.1 Recommended Equipment

The following materials are recommended for testing:

- 0V to 50V power supply with at least 2A source current capability
- Electronic loads capable of sinking current up to 2A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope
- Signal generator

2.2 Quick Setup Guide

(1) Ensure that the circuit is correctly connected to the supply and loads before applying any power.

(2) Connect the bias supply to VIN, the plus terminal to VIN (P4), and the negative return to GND (P5).

(3) Verify that SW1 is in the ON position.

(4) Turn on the power supply.

(5) Verify the output voltage is 12V for $V_{OUT\_PR.}$

2.3 Frequency Control

The ISL854102 has an FS pin that controls the frequency of operation. Programmable frequency allows for optimization between efficiency and external component size. It also allows low frequency operation for low V_{OUTs} when minimum on-time would otherwise limit the operation. The default switching frequency is 500kHz when FS is tied to V_{CC} (R_{13} = 0). By removing R_{13}, the switching frequency can be changed from 300kHz (R_{14} = 340k) to 2MHz (R_{14} = 32.4k). Refer to the ISL854102 datasheet for information about calculating the value of R_{14}. Do not leave this pin floating.

2.4 Switch Control

The ISL854102DEMO2Z board contains an SW1 switch that enables or disables the part, thus allowing low quiescent current state. Table 1 details this function.

TABLE 1. Switch Settings

SW1	On/Off Control
ON	Enable V_{OUT}
OFF	Disable V_{OUT}

2.5 SYNC Control

The ISL854102DEMO2Z board has a SYNC pin that allows an external synchronization frequency to be applied. The default board configuration has R_9 = 200k to V_{CC}, which defaults to PWM operation mode and also to the preselected switching frequency set by R_{14}. Refer to the ISL854102 datasheet and previous section "Frequency Control" for details. If this pin is tied to GND, the IC will operate in PFM mode. This is not recommended for this board since the purpose of this board is to demonstrate generating multiple secondary outputs, which does not work well in PFM mode.

2.6 Soft-Start/Comp Control

R_{11} selects between internal (R_{11} = 0) and external soft-start. R_8 selects between internal (R_8 = 0) and external compensation. For applications in which repetitive restarts of the IC are required, it is recommended to add a 350kΩ resistor in parallel to C_{SS} to allow its fast discharge. Refer to the pin description table of the ISL854102 datasheet.

2.7 Secondary Isolation

The R_{12} resistor, which shorts the PGND and the ISOGND on the ISL854102DEMO2Z board, can be replaced with a 2200pF ceramic capacitor (C2012X5R2E222K085AA) to isolate the secondary output from the primary output.

3. PCB Layout Guidelines

The ISL854102DEMO2Z PCB layout has been optimized for electrical and thermal performance. Proper layout of the power converter will minimize EMI and noise while ensuring first pass success of the design.

A multilayer printed circuit board with GND plane is recommended. The most critical connections are to tie the PGND pin to the package GND pad and then use vias to directly connect the GND pad to the system GND plane. This connection of the GND pad to system plane insures a low impedance path for all return current, as well as an excellent thermal path to dissipate heat.

With this connection made, place the high frequency MLCC input capacitors C_1, C_2 near the VIN pin and use vias directly at the capacitor pads to tie the capacitors to the system GND plane. Also, use vias directly at the C_5 and C_6 output capacitor pads to tie the capacitors to the system GND plane and C_{11} to C_{14} to the ISOGND plane. These measures will minimize the high dV/dt and dI/dt loops. Minimize the PHASE connection by placing L_1 very close to the IC. Place a 1µF MLCC near the VCC pin and directly connect its return with a via to the system GND plane. Keep the power components path (L_1, C_1, C_2, C_3, C_5, C_6, C_{11} to C_{14}) separated from the small signal node (FB) by placing the feedback divider close to the FB pin and do not route any feedback components near PHASE or BOOT. Keep the FB trace as short as possible.

Figure 2. Top of Board

Figure 3. Bottom of Board

3.1 Schematic

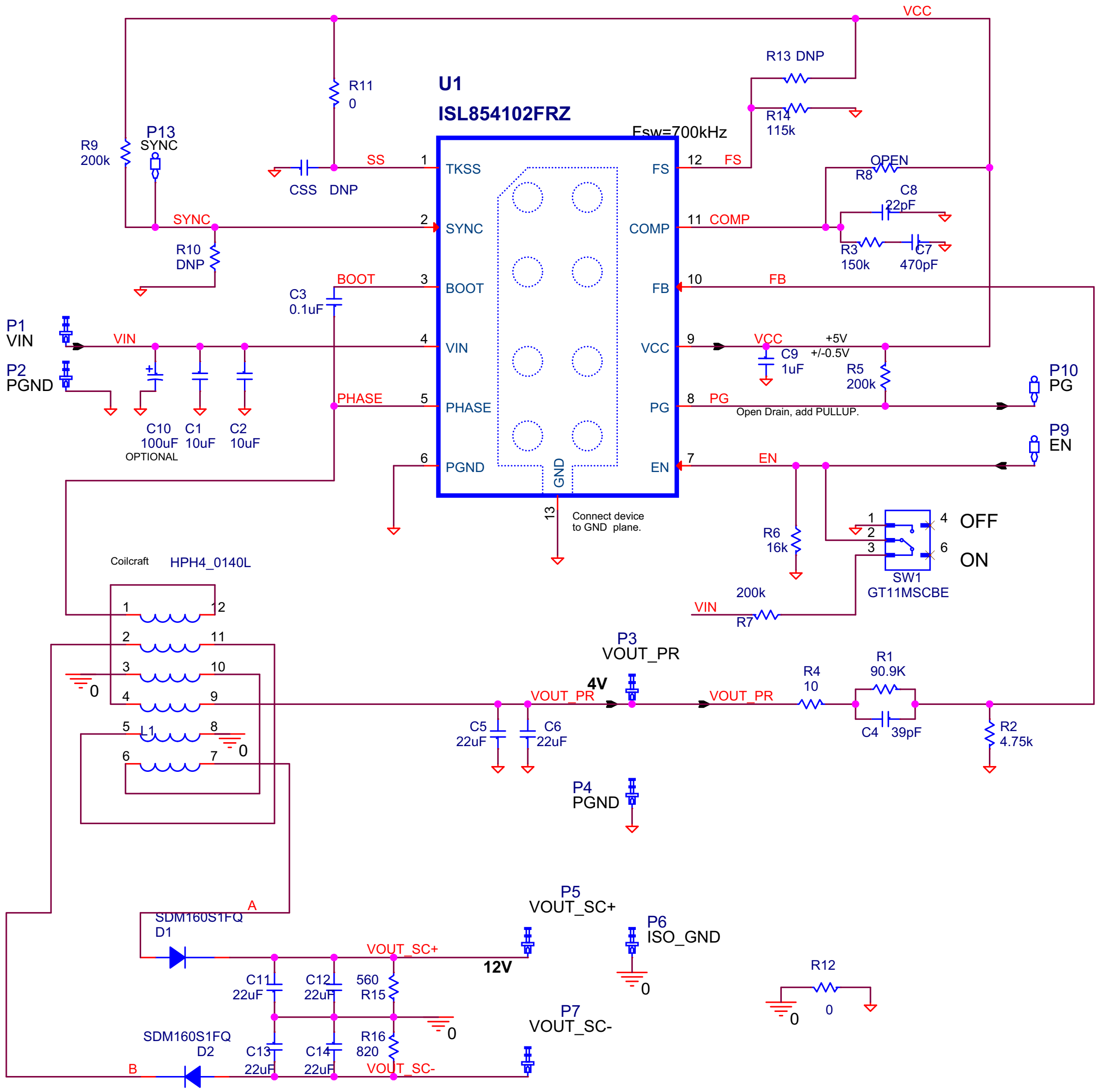

Figure 4. ISL854102DEMO2Z Schematic

3.2 Bill of Materials

Qty	Reference Designator	Description	Manufacturer Part	Manufacturer
1	C10 (OPTIONAL)	CAP ALUM 100µF 20% 50V SMD	EEE-FTH101XAP	PANASONIC
2	C1, C2	CAP, SMD, 1206, 10µF, 50V, 10%, X5R, ROHS	C3216X5R1H106K	TDK
1	C3	CAP, SMD, 0603, 0.1µF, 50V, 10%, X7R, ROHS	06035C104KAT2A	AVX
1	C4	CAP, SMD, 0402, 39pF, 50V, 1%, NP0, ROHS	04025A390FAT2A	AVX
6	C5, C6, C11-C14	CAP, SMD, 1206, 22µF, 16V, 20%, X5R, ROHS	CGA5L1X5R1C226M160AC	TDK
1	C7	CAP, SMD, 0402, 470pF, 50V, 5%, NP0, ROHS	04025A471JAT2A	AVX
1	C8	CAP, SMD, 0402, 22pF, 50V, 1%, NP0, ROHS	04025U220FAT2A	AVX

Qty	Reference Designator	Description	Manufacturer Part	Manufacturer
1	C9	CAP, SMD, 0603, 1µF, 16V, 10%, X5R, ROHS	GRM188R61C105KA12D	MURATA
7	P1-P7	CONN-TURRET, TERMINAL POST, TH, ROHS	1514-2	KEYSTONE
3	P9, P10, P13	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	5002	KEYSTONE
2	D1, D2	SCHOTTKY DIODE, SMD, 2P, SOD-123F, 60V, 1A, ROHS	SDM160S1FQ	DIODES, INC.
1	U1	IC 40V BUCK REGULATOR, 12P, DFN, 3x4, ROHS	ISL854102FRZ for ISL854102DEMO2Z	INTERSIL
1	L1	CONFIGURABLE TRANSFORMER, SMD, 12P, 23.7µH, ROHS	HPH4_0140L	COILCRAFT
1	R1	RES, SMD, 0402, 90.9k, 1/16W, 1%, TF, ROHS	CRCW040290K9FKED	VISHAY/DALE
1	R2	RES, SMD, 0402, 4.75k, 1/16W, 1%, TF, ROHS	CRCW04024K75FKED	VISHAY/DALE
1	R3	RES, SMD, 0402, 150k, 1/16W, 1%, TF, ROHS	CR0402-16W-1503FT	VENKEL
1	R4	RES, SMD, 0402, 10Ω, 1/10W, 1%, TF, ROHS	ERJ-2RKF10R0X	PANASONIC
3	R5, R7, R9	RES, SMD, 0402, 200k, 1/16W, 1%, TF, ROHS	MCR01MZPF2003	ROHM
1	R6	RES, SMD, 0402, 16kΩ, 1/16W, 1%, TF, ROHS	CRCW040216K0FKED	VISHAY/DALE
0	R8, R10, R13	RES, SMD, 0402, DNP-PLACE HOLDER, ROHS		
1	R11	RES, SMD, 0402, 0Ω, 1/16W, TF, ROHS	CR0402-16W-000T	VENKEL
1	R12	RES, SMD, 0805, 0Ω, 1/8W, TF, ROHS	CR0805-10W-000T	VENKEL
1	R14	RES, SMD, 0402, 115k, 1/16W, 1%, TF, ROHS	CRCW0402115KFKED	VISHAY/DALE
1	R15	RES, SMD, 0805, 560Ω, 1/2W, 1%, TF, ROHS	ERJ-P6WF5600V	PANASONIC
1	R16	RES, SMD, 0805, 820Ω, 1/2W, 1%, TF, ROHS	ERJ-P6WF8200V	PANASONIC
1	SW1	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 2POS, ON-NONE-ON, ROHS	GT11MSCBE	ITT INDUSTRIES/C&K DIVISION

3.3 Board Layout

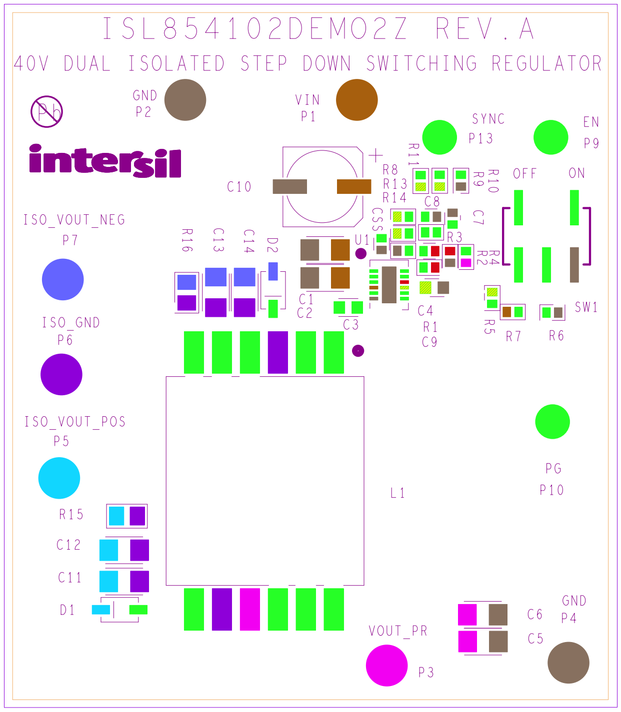

Figure 5. Silk Screen Top

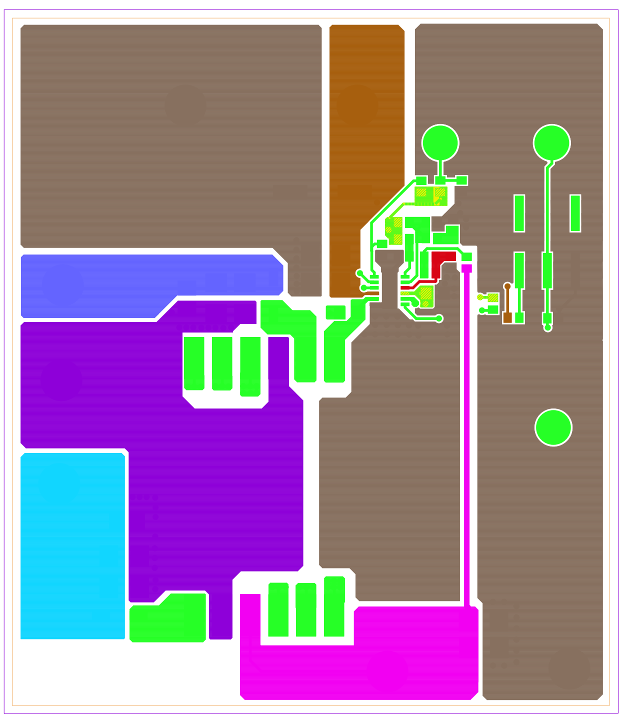

Figure 6. Layer 1

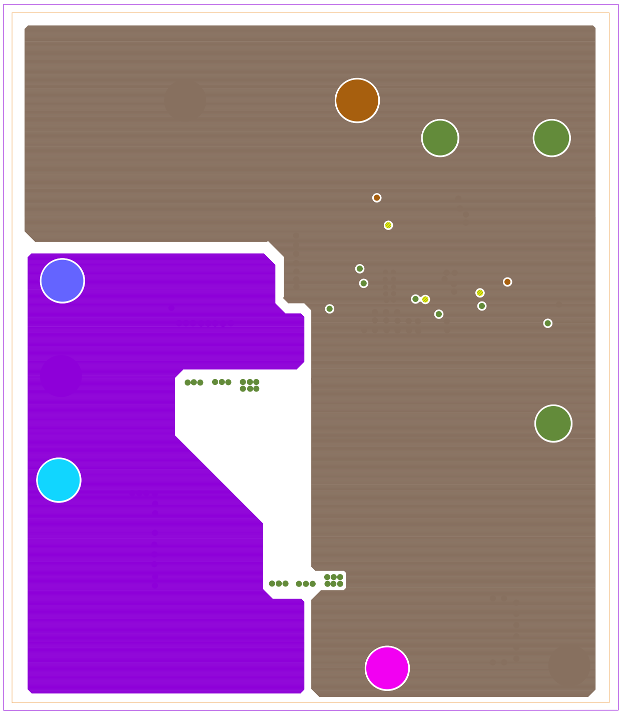

Figure 7. Layer 2

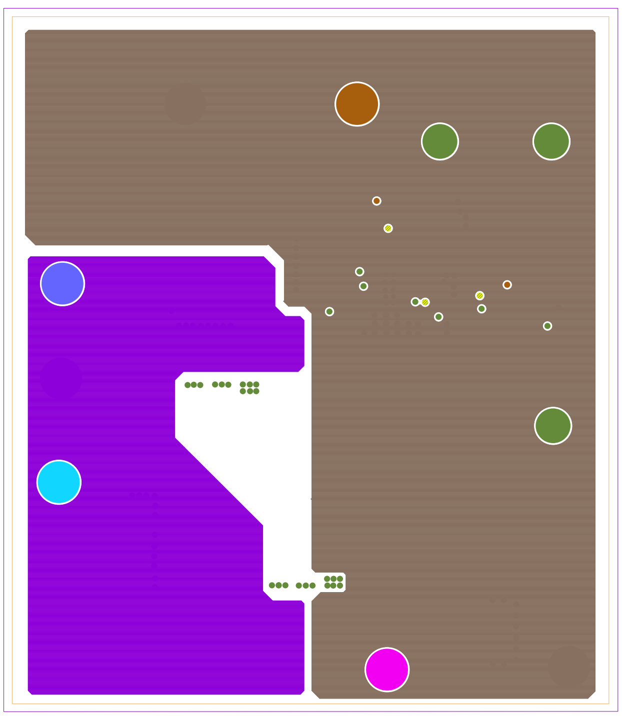

Figure 8. Layer 3

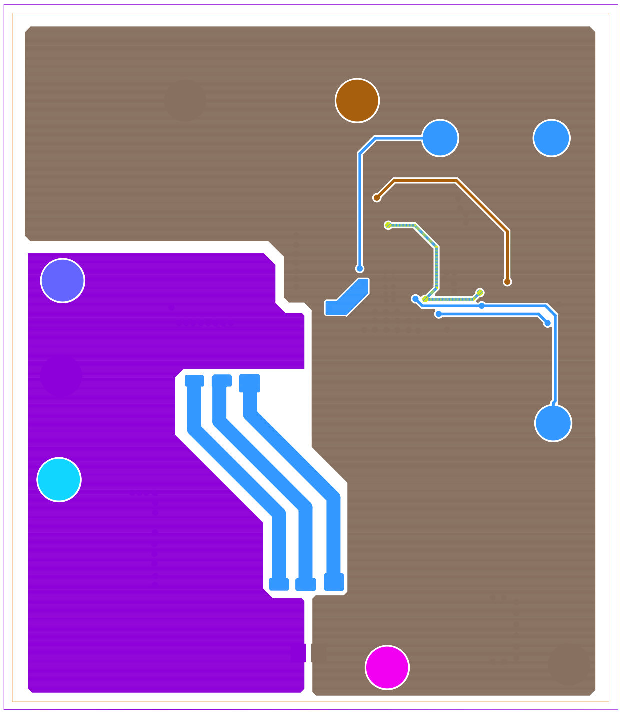

Figure 9. Layer 4

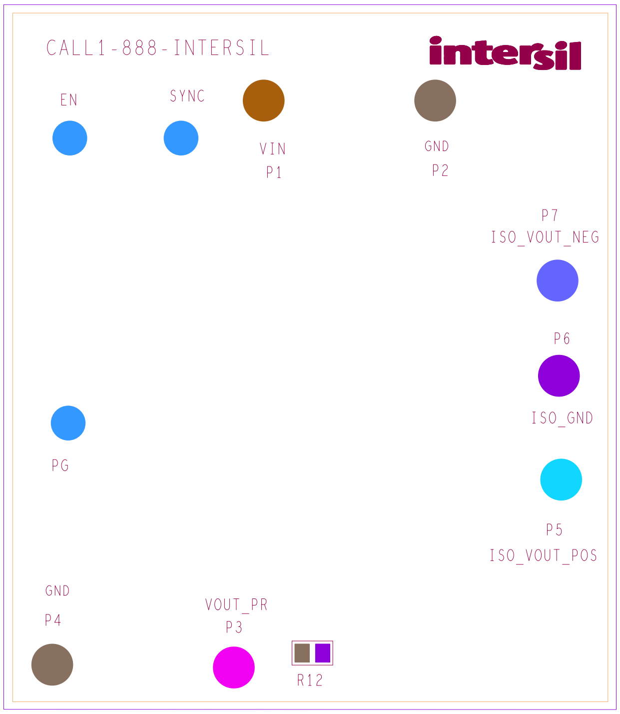

Figure 10. Silk Screen Bottom

4. Typical Performance Curves

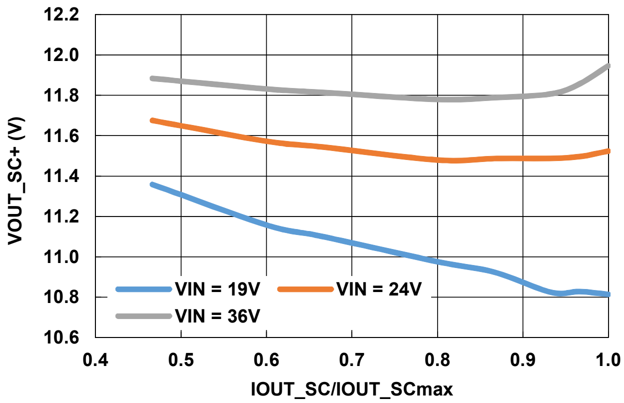

Figure 11. VOUT_SC+ Regulation vs IOUT_SC/IOUT_SCmax (V_{OUT} = ±12V)

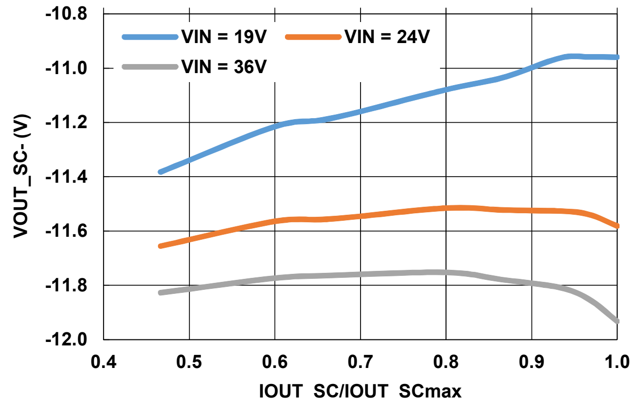

Figure 12. VOUT_SC- Regulation vs IOUT_SC/IOUT_SCmax (V_{OUT} = ±12V)

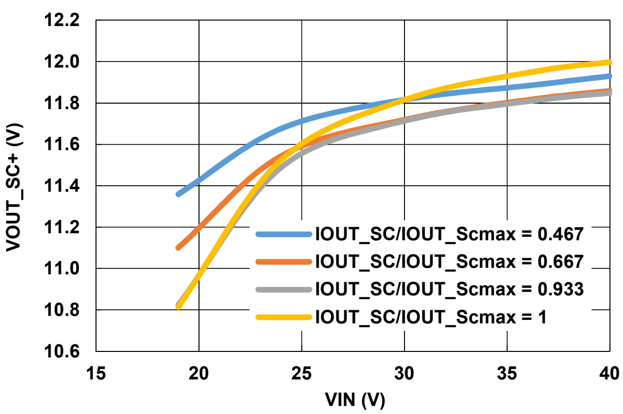

Figure 13. VOUT_SC+ Regulation vs V_{IN} (V_{OUT} = ±12V)

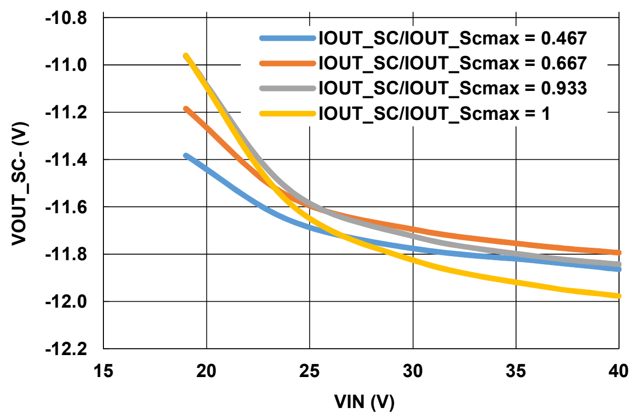

Figure 14. VOUT_SC- Regulation vs V_{IN} (V_{OUT} = ±12V)

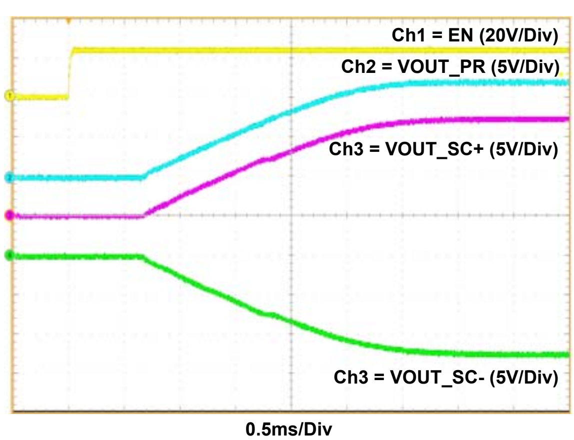

Figure 15. Start-Up by Enable (V_{IN} = 24V, VOUT_PR = +12V, VOUT_SC± = ±12V, IOUT_PR = 0.8A, IOUT_SC± = 150mA, FCCM)

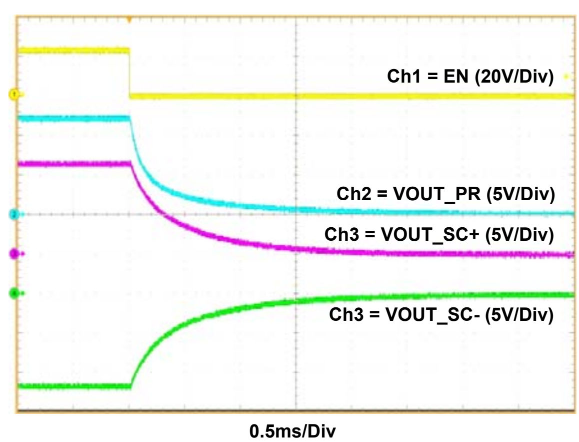

Figure 16. Shutdown by Enable (V_{IN} = 24V, VOUT_PR = +12V, VOUT_SC± = ±12V, IOUT_PR = 0.8A, IOUT_SC± = 150mA, FCCM)

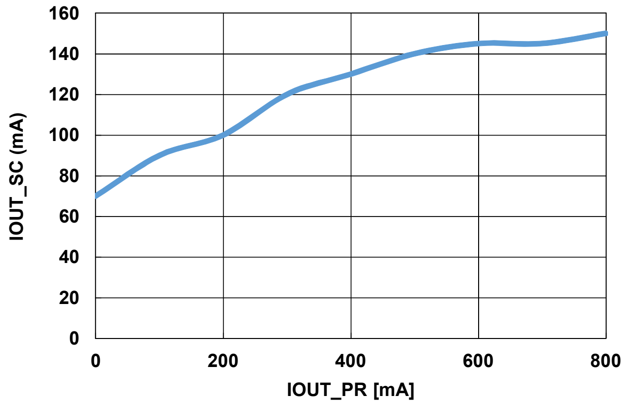

Figure 17. IOUT_SC± vs Corresponding IOUT_PR (V_{OUT} = 12V)

5. Revision History

Rev.	Date	Description
0.00	Aug 16, 2017	Initial release

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