ISL4485E

±15kV ESD Protected, 20Mbps, 5V, Low Power, RS-485/RS-422 Transceiver

FN6049
Rev 4.00
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The ISL4485E is a high speed, BiCMOS 5V powered, single transceiver that meets both the RS-485 and RS-422 standards for balanced communication. Each driver output/receiver input is protected against ±15kV ESD strikes without latch-up. Unlike competitive devices, this device is specified for 10% tolerance supplies (4.5V to 5.5V).

The excellent differential output voltage coupled with high drive-current output stages allow 20Mbps operation over twisted pair networks up to 450ft in length. The 25kΩ receiver input resistance presents a single unit load to the RS-485 bus, allowing up to 32 transceivers on the network.

The receiver (Rx) inputs feature a “fail-safe if open” design, which ensures a logic high Rx output if the Rx inputs are floating.

The driver (Tx) outputs are short-circuit protected, even for voltages exceeding the power supply voltage. Additionally, on-chip thermal shutdown circuitry disables the Tx outputs to prevent damage if power dissipation becomes excessive.

The half duplex configuration multiplexes the Rx inputs and Tx outputs to allow transceivers with Rx and Tx disable functions in 8 Ld packages.

Related Literature

For a full list of related documents, visit our website:

- ISL4485E product page

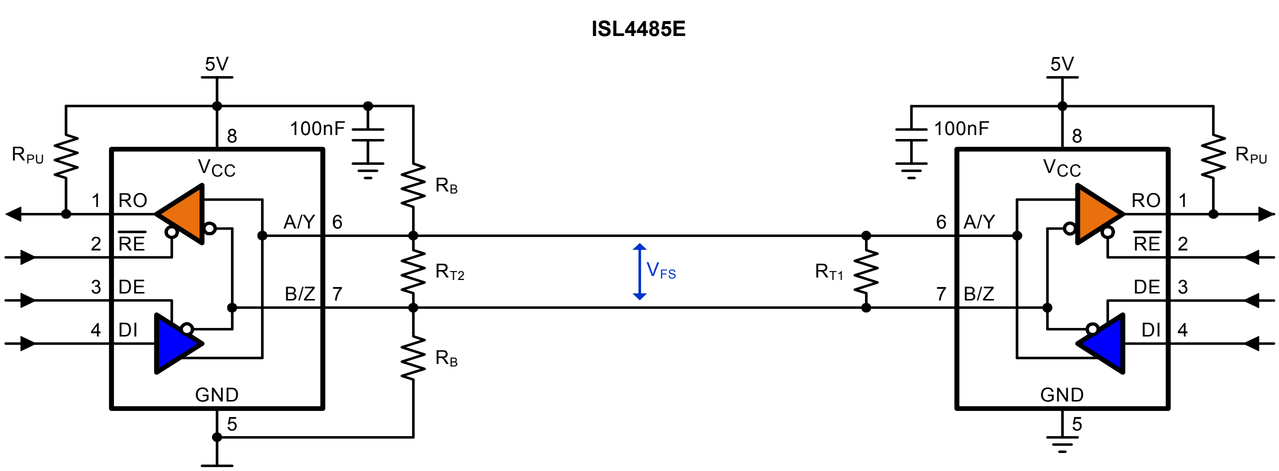
Features

- Pb-free available (RoHS compliant)
- High data rates. . . . . up to 20Mbps
- RS-485 I/O pin ESD protection . . . . ±15kV HBM
  - Class 3 ESD level on all other pins . . . . >7kV HBM
- Operates from a single +5V supply (10% tolerance)
- 1 unit load allows up to 32 devices on the bus
- Low quiescent current 700µA
- -7V to +12V common-mode input voltage range
- Three state Rx and Tx outputs
- 30ns propagation delays, 2ns skew
- Current limiting and thermal shutdown for driver overload protection

Applications

- SCSI “fast 20” drivers and receivers
- Data loggers
- Security networks
- Building environmental control systems
- Industrial/process control networks
- Level translators

Typical Operating Circuit



To calculate the resistor values, refer to TB509.

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL4485EIBZ	4485EIBZ	-40 to +85	-	8 Ld SOIC (Pb-free)	M8.15
ISL4485EIBZ-T	4485EIBZ	-40 to +85	2.5k	8 Ld SOIC Tape & Reel (Pb-free)	M8.15

NOTE:

1. Refer to TB347 for details about reel specifications.
2. These Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL4485E product information page. For more information, refer to TB363.

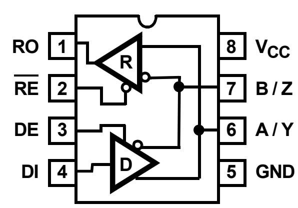
Truth Tables

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B/Z	A/Y
X	1	1	0	1
X	1	0	1	0
X	0	X	High-Z	High-Z

RECEIVING			
INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2V	1
0	0	≤ -0.2V	0
0	0	Inputs Open	1
1	X	X	High-Z

Pinout

TOP VIEW



Pin Descriptions

PIN	FUNCTION
RO	Receiver output: RO is high if A > B by at least 0.2V; RO is low if A < B by 0.2V or more; RO = high if A and B are unconnected (floating).
$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low.
DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	Ground connection.
A/Y	±15kV HBM ESD protected, noninverting receiver input and noninverting driver output. Pin is an input (A) if DE = 0; pin is an output (Y) if DE = 1.
B/Z	±15kV HBM ESD protected, inverting receiver input and inverting driver output. Pin is an input (B) if DE = 0; pin is an output (Z) if DE = 1.
V_{CC}	System power supply input (4.5V to 5.5V).

Absolute Maximum Ratings

V_{CC} to Ground 7V
Input Voltages
DI, DE, $\overline{RE}$ . . . . -0.5V to (V_{CC} +0.5V)
Input / Output Voltages
A / Y, B / Z . . . . -8V to +12.5V
RO . . . . -0.5V to (V_{CC} +0.5V)
Short-Circuit Duration
Y, Z . . . . Continuous
ESD Rating . . . . See "Electrical Specifications"

Operating Conditions

Temperature Range
ISL4485EIBZ . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
8 Ld SOIC Package 170
Maximum Junction Temperature (Plastic Package) 150
Maximum Storage Temperature Range . . . . -65°C to +150
Maximum Lead Temperature (Soldering 10s) 300
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" can permanently damage the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See TB379 for details.

Electrical Specifications

Test Conditions: V_{CC} = 4.5V to 5.5V; unless otherwise specified. Typicals are at V_{CC} = 5V, T_A = +25°C, Note 5

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS								
Driver Differential V_{OUT} (no load)	V_{OD1}			Full	-	-	V_{CC}	V
Driver Differential V_{OUT} (with load)	V_{OD2}	R = 50Ω (RS-422), (Figure 1)		Full	2	3	-	V
		R = 27Ω (RS-485), (Figure 1)		Full	1.5	2.3	5	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, (Figure 1)		Full	-	0.01	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R = 27Ω or 50Ω, (Figure 1)		Full	-	-	3	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R = 27Ω or 50Ω, (Figure 1)		Full	-	0.01	0.2	V
Logic Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		Full	2	-	-	V
Logic Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$		Full	-	-	0.8	V
Logic Input Current	I_{IN1}	DE, DI, $\overline{RE}$		Full	-25	-	25	µA
Input Current (A, B), (Note 8)	I_{IN2}	DE = 0V, V_{CC} = 0V or 4.5V to 5.5V	V_{IN} = 12V	Full	-	-	1	mA
			V_{IN} = -7V	Full	-	-	-0.8	mA
Receiver Differential Threshold Voltage	V_{TH}	$-7V \le V_{CM} \le 12V$		Full	-0.2	-	0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		25	-	70	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		Full	3.5	4	-	V
Receiver Output Low Voltage	V_{OL}	I_O = -4mA, V_{ID} = 200mV		Full	-	0.1	0.4	V
Three-State (High Impedance) Receiver Output Current	I_{OZR}	$0.4V \le V_O \le 2.4V$		Full	-	-	±1	µA
Receiver Input Resistance	R_{IN}	$-7V \le V_{CM} \le 12V$		Full	12	25	-	kΩ
No-Load Supply Current, (Note 6)	I_{CC}	DI, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}	Full	-	700	900	µA
			DE = 0V	Full	-	500	565	µA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	DE = V_{CC}, $-7V \le V_Y$ or $V_Z \le 12V$, (Note 7)		Full	35	-	250	mA

Electrical Specifications

Test Conditions: V_{CC} = 4.5V to 5.5V; unless otherwise specified. Typicals are at V_{CC} = 5V, T_A = +25°C, Note 5 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNIT
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}	Full	7	-	85	mA
SWITCHING CHARACTERISTICS							
Driver Input to Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2)	Full	15	30	50	ns
Driver Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2)	Full	-	1.3	5	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2)	Full	3	11	25	ns
Driver Enable to Output High	t_{ZH}	C_L = 100pF, SW = GND, (Figure 3)	Full	-	17	30	ns
Driver Enable to Output Low	t_{ZL}	C_L = 100pF, SW = V_{CC}, (Figure 3)	Full	-	14	30	ns
Driver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND, (Figure 3)	Full	-	19	30	ns
Driver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC}, (Figure 3)	Full	-	13	30	ns
Driver Maximum Data Rate	f_{MAXD}	$\|V_{OD}\|$ ≥ 1.5V, (Figure 4, Note 9)	Full	20	-	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	Figure 5	Full	20	40	70	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	Figure 5	Full	-	3	10	ns
Receiver Enable to Output High	t_{ZH}	C_L = 15pF, SW = GND, (Figure 6)	Full	-	9	25	ns
Receiver Enable to Output Low	t_{ZL}	C_L = 15pF, SW = V_{CC}, (Figure 6)	Full	-	9	25	ns
Receiver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND, (Figure 6)	Full	-	9	25	ns
Receiver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC}, (Figure 6)	Full	-	9	25	ns
Receiver Maximum Data Rate	f_{MAXR}	C_L = 15pF, V_{ID} ≥ 1.5V (Note 9)	Full	20	-	-	Mbps
ESD PERFORMANCE							
RS-485 Pins (A/Y, B/Z)		Human Body Model	25	-	±15	-	kV
All Other Pins			25	-	>±7	-	kV

NOTE:

5. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
6. Supply current specification is valid for loaded drivers when DE = 0V.
7. Applies to peak current. See "Typical Performance Curves" for more information.
8. Devices meeting these limits are denoted as "single unit load (1 UL)" transceivers. The RS-485 standard allows up to 32 unit loads on the bus.
9. Guaranteed by characterization, but not tested.

Test Circuits and Waveforms

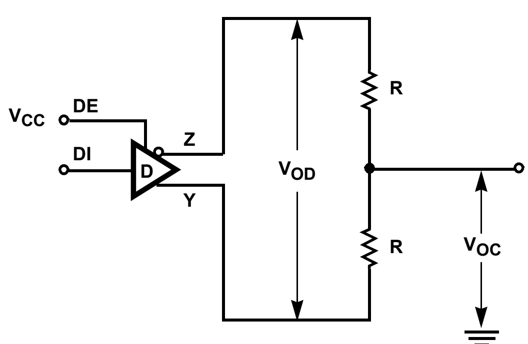


FIGURE 1. DRIVER V_{OD} AND V_{OC}

Test Circuits and Waveforms *(Continued)*

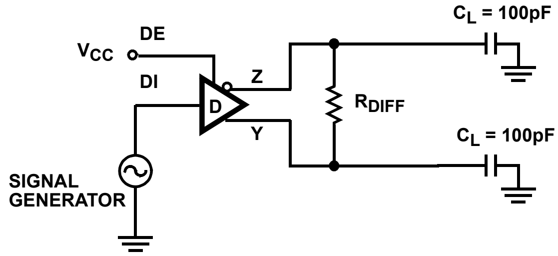


FIGURE 2A. TEST CIRCUIT

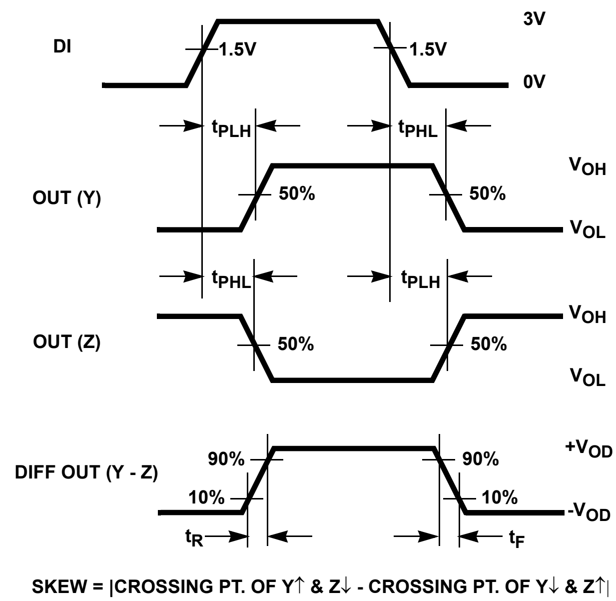
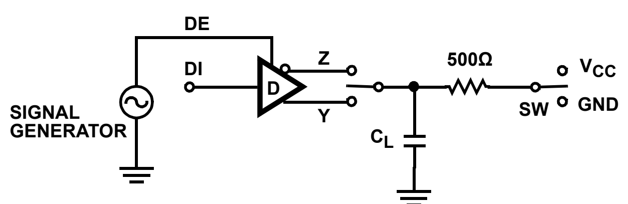


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



PARAMETER	OUTPUT	$\overline{RE}$	DI	SW	C_L (pF)
t_{HZ}	Y/Z	X	1/0	GND	15
t_{LZ}	Y/Z	X	0/1	V_{CC}	15
t_{ZH}	Y/Z	X	1/0	GND	100
t_{ZL}	Y/Z	X	0/1	V_{CC}	100

FIGURE 3A. TEST CIRCUIT

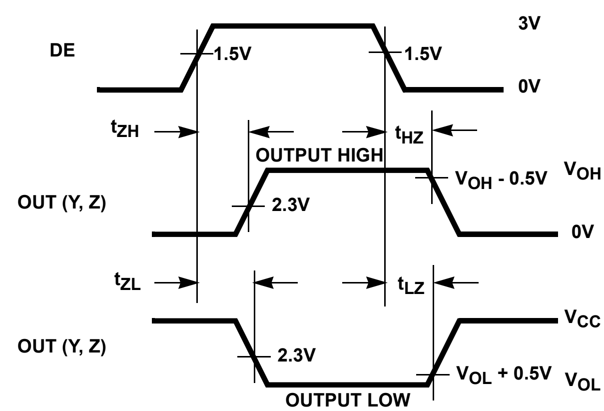


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

Test Circuits and Waveforms (Continued)

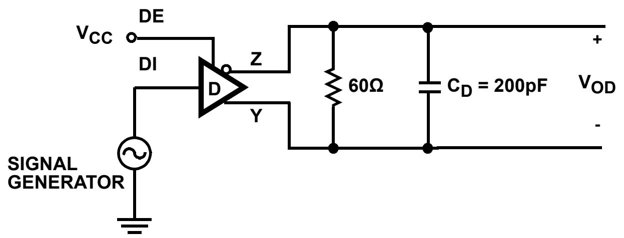


FIGURE 4A. TEST CIRCUIT

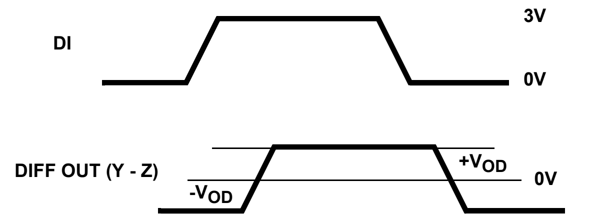


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. DRIVER DATA RATE

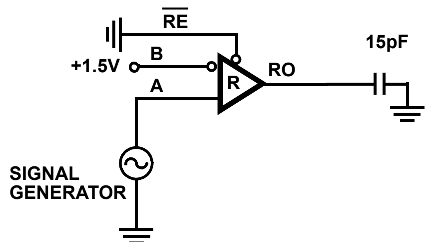


FIGURE 5A. TEST CIRCUIT

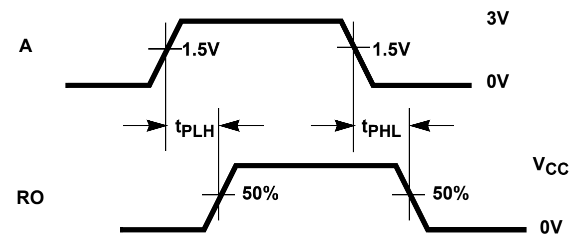
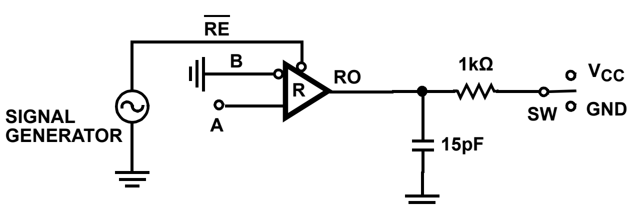


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER PROPAGATION DELAY



PARAMETER	DE	A	SW
t_{HZ}	0	+1.5V	GND
t_{LZ}	0	-1.5V	V_{CC}
t_{ZH}	0	+1.5V	GND
t_{ZL}	0	-1.5V	V_{CC}

FIGURE 6A. TEST CIRCUIT

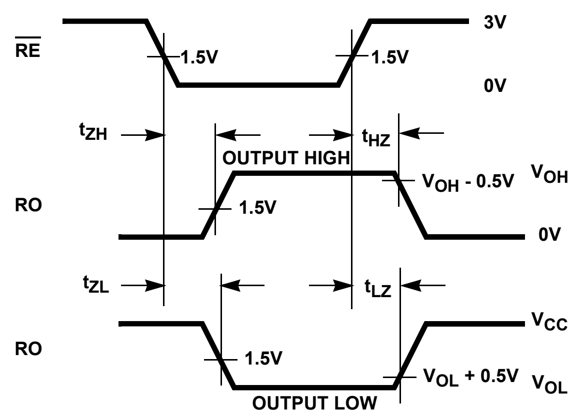


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. RECEIVER ENABLE AND DISABLE TIMES

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard that allows only one driver and up to 10 receivers on each bus (assuming one unit load devices). RS-485 is a true multipoint standard that allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

An important advantage of RS-485 is the extended Common-Mode Range (CMR). The CMR specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000ft, so the wide CMR is necessary to handle ground potential differences and voltages induced in the cable by external fields.

Receiver Features

The ISL4485E uses a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is ±200mV, as required by the RS-422 and RS-485 specifications.

Receiver input impedance surpasses the RS-422 specification of 4kΩ and meets the RS-485 unit load requirement of 12kΩ minimum.

Receiver inputs function with common-mode voltages as great as ±7V outside the power supplies (+12V and -7V), making them ideal for long networks in which induced voltages are a realistic concern.

The receiver includes a “fail-safe if open” function that guarantees a high level receiver output if the receiver inputs are unconnected (floating). The output is three-statable using the active low $\overline{RE}$ input, and the receiver meets the 20Mbps data rate.

Driver Features

The RS-485/422 driver is a differential output device that delivers at least 1.5V across a 54Ω load (RS-485) and at least 2V across a 100Ω load (RS-422). The ISL4485E driver features low propagation delay skew to maximize bit width and to minimize EMI, and the outputs are three-statable using the active high DE input.

The ISL4485E driver outputs are not slew rate limited, so faster output transition times allow data rates up to 20Mbps.

Data Rate, Cables, and Terminations

Twisted pair cable is the cable of choice for RS-485/422 networks. Twisted pair cables pick up noise and other electromagnetically induced voltages as common-mode signals that are effectively rejected by the differential receivers in these ICs.

RS-485/422 are intended for network lengths up to 4000ft, but the maximum transmission length decreases as the data rate increases. According to guidelines in the RS-422 specification, a 20Mbps network should be limited to less than 50ft of 24 AWG twisted pair. However, the ISL4485E's large differential voltage swing, fast transition times, and high drive-current output stages allow operation at 20Mbps in RS-485/422 networks as long as 450ft. Figure 7 on page 8 details ISL4485E operation at 20Mbps driving 300ft of CAT 5 cable terminated in 120Ω at the driver and the receiver (that is, double terminated). The acceptance criteria for this test was the ability of the driver to deliver a 1.5V differential signal to the receiver at the end of the cable (|A-B| ≥ 1.5V). If a more liberal acceptance criteria is used, the distance can be further extended. For example, Figure 8 on page 8 illustrates the performance in the same configuration but with a cable length of 450ft and an acceptance criteria of no more than 6dB attenuation across the cable (|A-B| = |Y-Z|/2).

Driver differential output voltage decreases with increasing differential load capacitance, so maintaining a 1.5V differential output requires a data rate reduction as shown in Figure 9 on page 8.

To minimize reflections, proper termination is imperative when using this 20Mbps device. In point-to-point or point-to-multipoint (single driver on bus) networks, terminate the main cable in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, keep stubs connecting receivers to the main cable as short as possible (preferably less than 12in). Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Keep stubs connecting a transceiver to the main cable as short as possible.

Built-In Driver Overload Protection

The RS-485 specification requires that drivers survive worst case bus contentions undamaged. The ISL4485E device meets this requirement with driver output short-circuit current limits and on-chip thermal shutdown circuitry.

The driver output stages incorporate short-circuit current limiting circuitry, ensuring that the output current never exceeds the RS-485 specification even at the common-mode voltage range extremes. These devices also use a foldback circuit that reduces the short-circuit current (and the power dissipation) when the contending voltage exceeds either supply.

In the event of a major short-circuit condition, this device’s thermal shutdown feature disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically reenable after the die temperature drops about 15°C. If the condition persists, the thermal shutdown/reenable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

ESD Protection

All pins on these interface devices include class 3 Human Body Model (HBM) ESD protection structures, but the RS-485 pins (driver outputs and receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of ±15kV HBM. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins or connecting a cable can cause an ESD event that destroys unprotected ICs. The ISL4485E ESD structures protect the device whether or not it is powered up, protect without allowing any latchup mechanism to activate, and without degrading the RS-485 CMR of -7V to +12V. This built-in ESD protection eliminates the need for board level protection structures (for example, transient suppression diodes) and the associated undesirable capacitive load that they cause.

Human Body Model Testing

This test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge stored on a 100pF capacitor through a 1.5kΩ current limiting resistor into the pin under test. The HBM method determines an IC's ability to withstand the ESD events typically present during handling and manufacturing.

The RS-485 pin survivability on this high ESD device has been characterized to be in excess of ±15kV, for discharges to GND.

Typical Performance Curves V_{CC} = 5V, T_A = 25°C, Unless Otherwise Specified

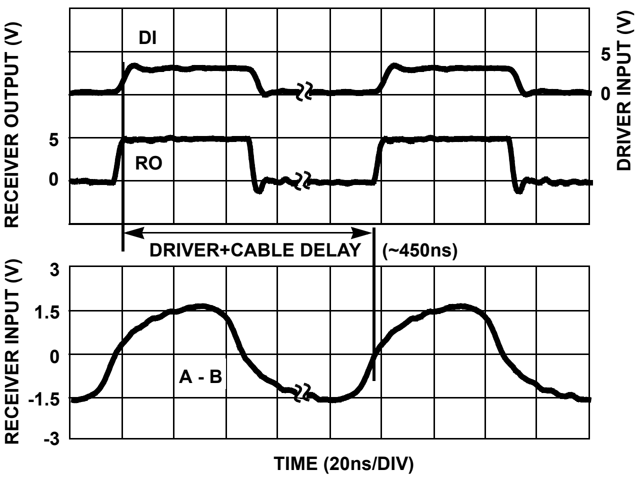


FIGURE 7. DRIVER AND RECEIVER WAVEFORMS DRIVING 300FT OF CABLE (DOUBLE TERMINATED)

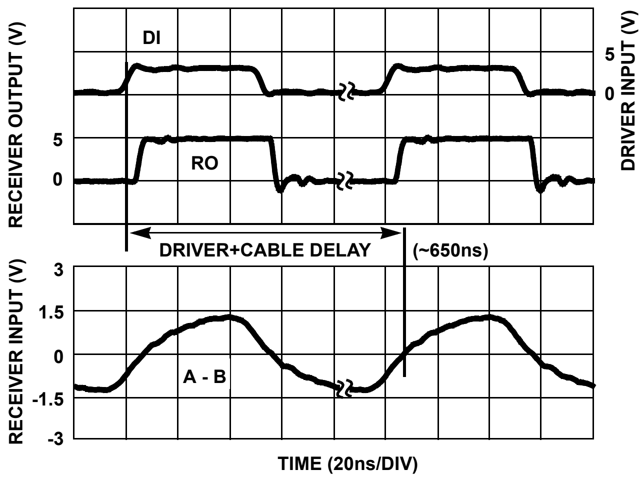


FIGURE 8. DRIVER AND RECEIVER WAVEFORMS DRIVING 450FT OF CABLE (DOUBLE TERMINATED)

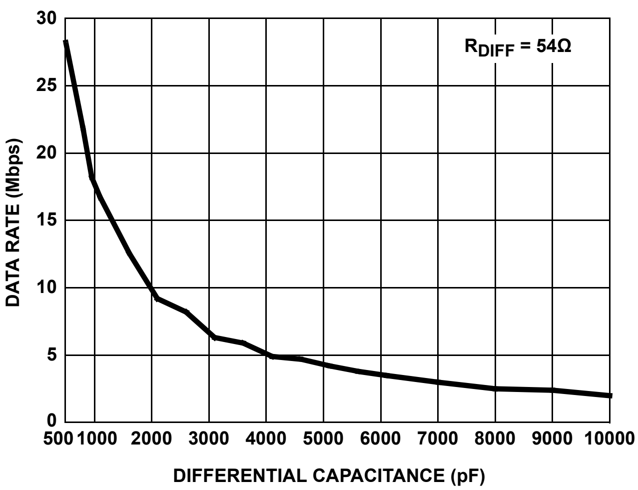


FIGURE 9. DATA RATE vs DIFFERENTIAL CAPACITANCE

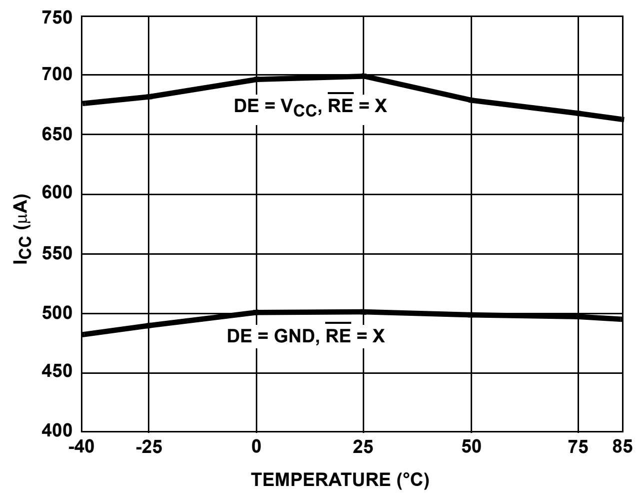


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued) V_{CC} = 5V, T_A = 25°C, Unless Otherwise Specified

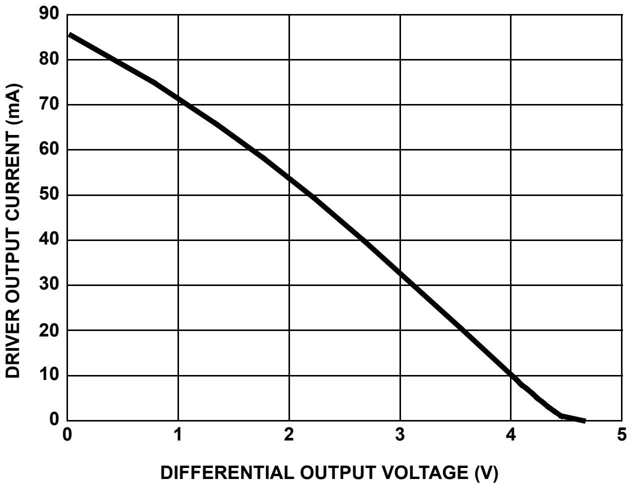


FIGURE 11. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

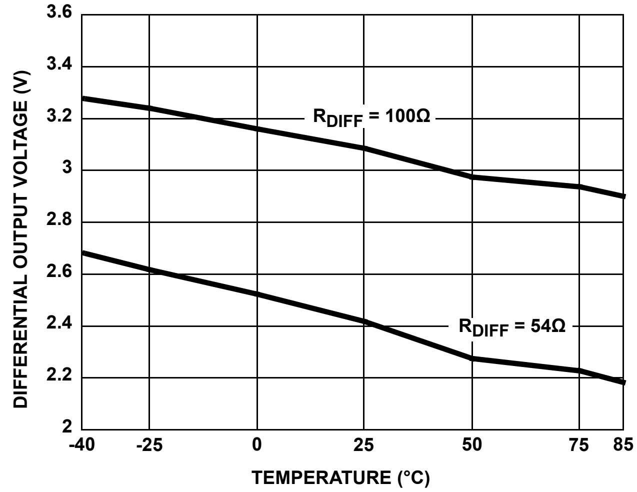


FIGURE 12. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

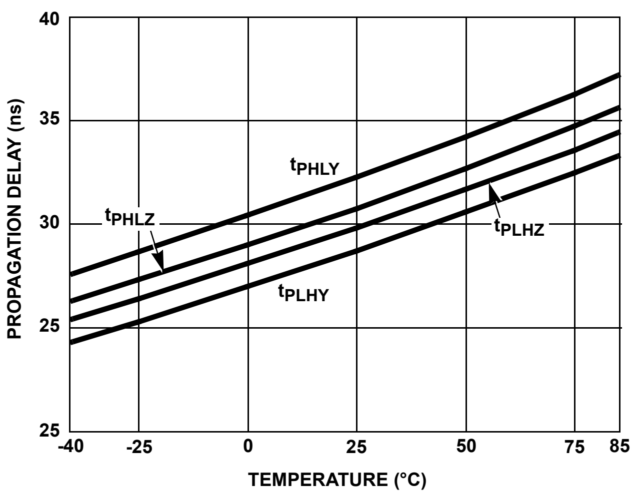


FIGURE 13. DRIVER PROPAGATION DELAY vs TEMPERATURE

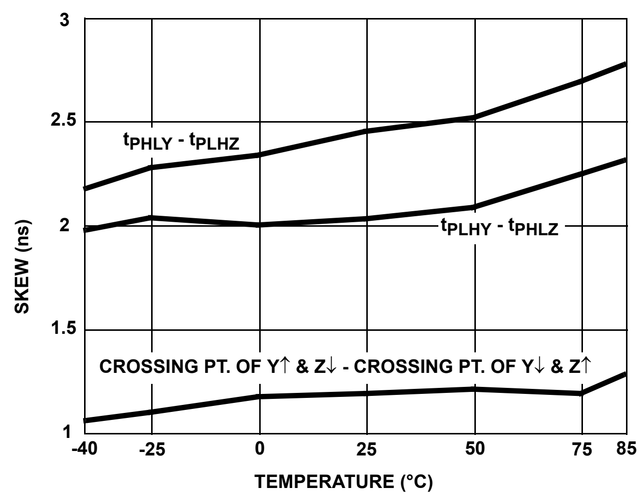


FIGURE 14. DRIVER SKEW vs TEMPERATURE

Typical Performance Curves **(Continued)** V_{CC} = 5V, T_A = 25°C, Unless Otherwise Specified

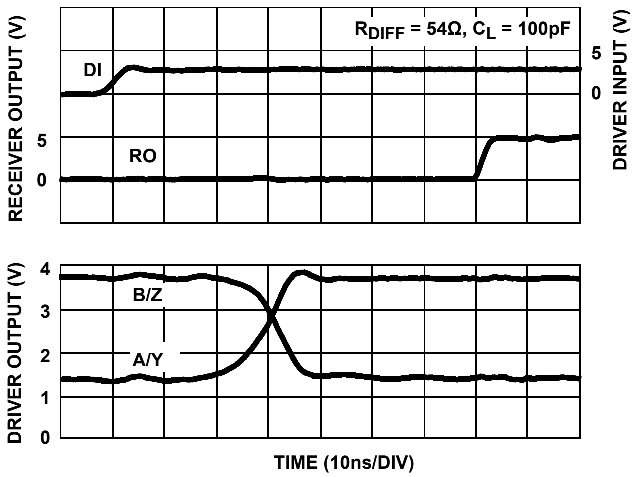


FIGURE 15. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH

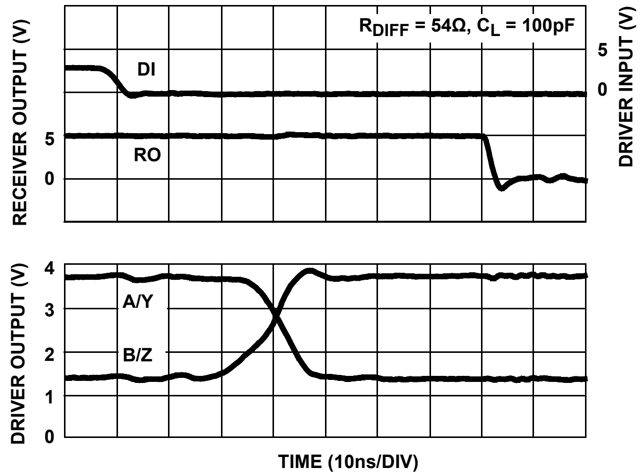


FIGURE 16. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW

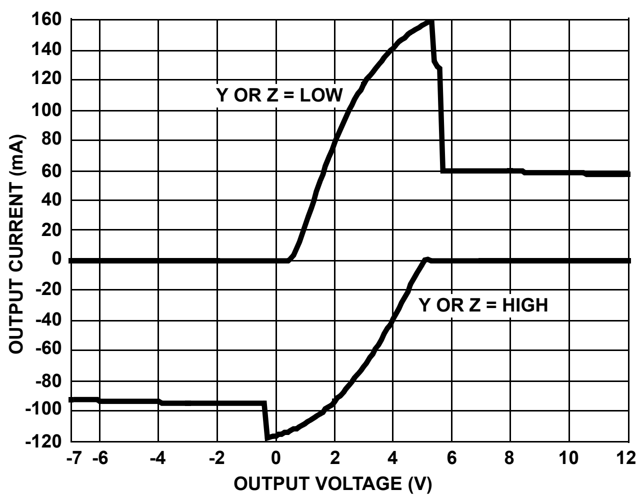


FIGURE 17. DRIVER OUTPUT CURRENT vs SHORT-CIRCUIT VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

518

PROCESS:

Si Gate CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Oct 8, 2018	FN6049.4	Updated typical operating circuit on page 1. Added Related Literature section to page 1. Removed ISL4485EIB and ISL4485EIB-T from ordering information table on page 2. Added Tape and Reel column and Notes 1, 2, and 3 to ordering information table on page 2. Removed Intersil copyright information and added Renesas disclaimer. Added Revision History to page 11. Updated package outline drawing from revision 0 to revision 4. Changes between revisions: -Revision 1: Initial revision -Revision 1 to revision 2: Updated to new package outline drawing format by removing table, moving dimensions onto drawing, and adding land pattern -Revision 2 to revision 3: Changed the following values in Typical Recommended Landing Pattern: 2.41(0.095) to 2.20 (0.087) 0.76(0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Revision 3 to revision 4: Changed text in Note 1 from “1982” to “1994”

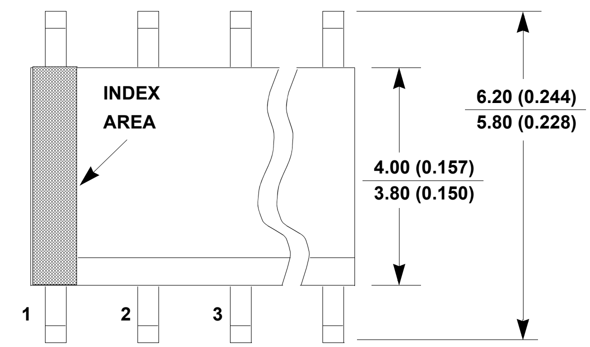
Package Outline Drawing

For the most recent package outline drawing, see M8.15.

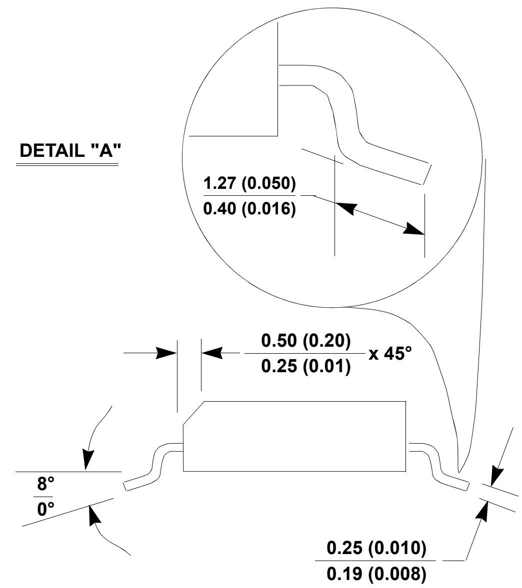
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

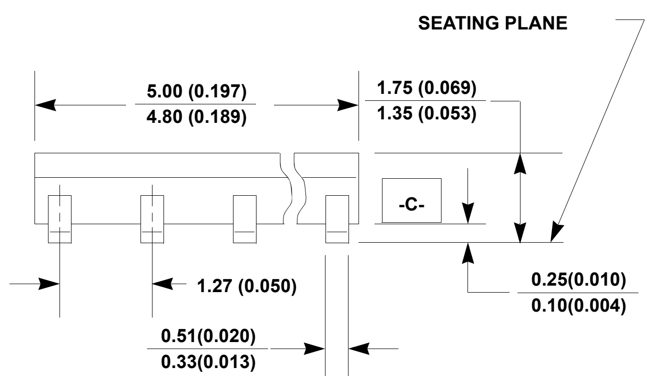
Rev 4, 1/12



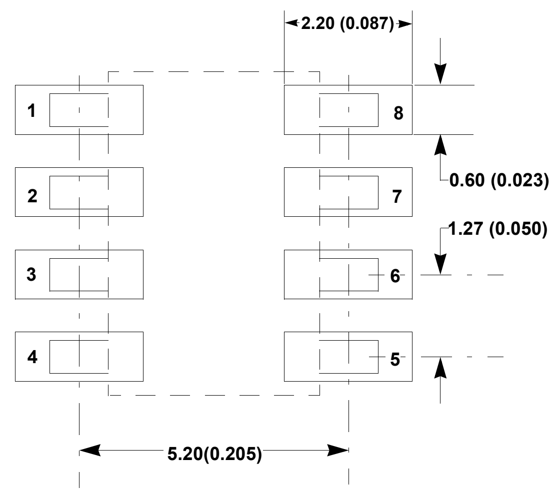
TOP VIEW



SIDE VIEW “B”



SIDE VIEW “A



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

10. Dimensioning and tolerancing per ANSI Y14.5M-1994.
11. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
12. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
13. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
14. Terminal numbers are shown for reference only.
15. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
16. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
17. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

RENESAS

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Colophon 7.2