GreenPAK Macro Circuit Design: Single Wire Interface / GPIO Expander

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Introduction

A Single Wire Interface (SWI) system is designed to reduce the number of wires in serial data communication. It is particularly useful in mobile devices because it increases the reliability of the product (fewer contact points) while reducing its size and cost. The design objective is to transfer digital data using a one wire protocol. Other possible uses are GPIO expander, serial 1 to 6 line decoder for status indicators, etc.

This SWI works by counting how many rising edges on the serial input occurred, up to 64 (6-bits). The binary equivalent from a counter is then presented to latched outputs 40mS after the last serial input.

Digital Single Wire circuit design

As shown in Figure 1, we start with a configurable SLG46722 chip and arrange toggle cells as a binary ripple counter. The FIRST_TOGGLE through SIXTH_TOGGLE are implemented using D flip-flops DFF5, DFF3, DFF2, DFF1, DFF0 and Pipe Delay. Then the digital latches LATCH1 ─ LATCH6 are implemented using six look up tables (3-bit LUT5 through 3-bit LUT0, see truth table in Figure 2). The one shot generator is implemented using a falling edge detector (PDLY cell), and CNT0/DLY0 configured as falling edge delay cell is connected to the 6 holding LATCH's IN2 inputs.

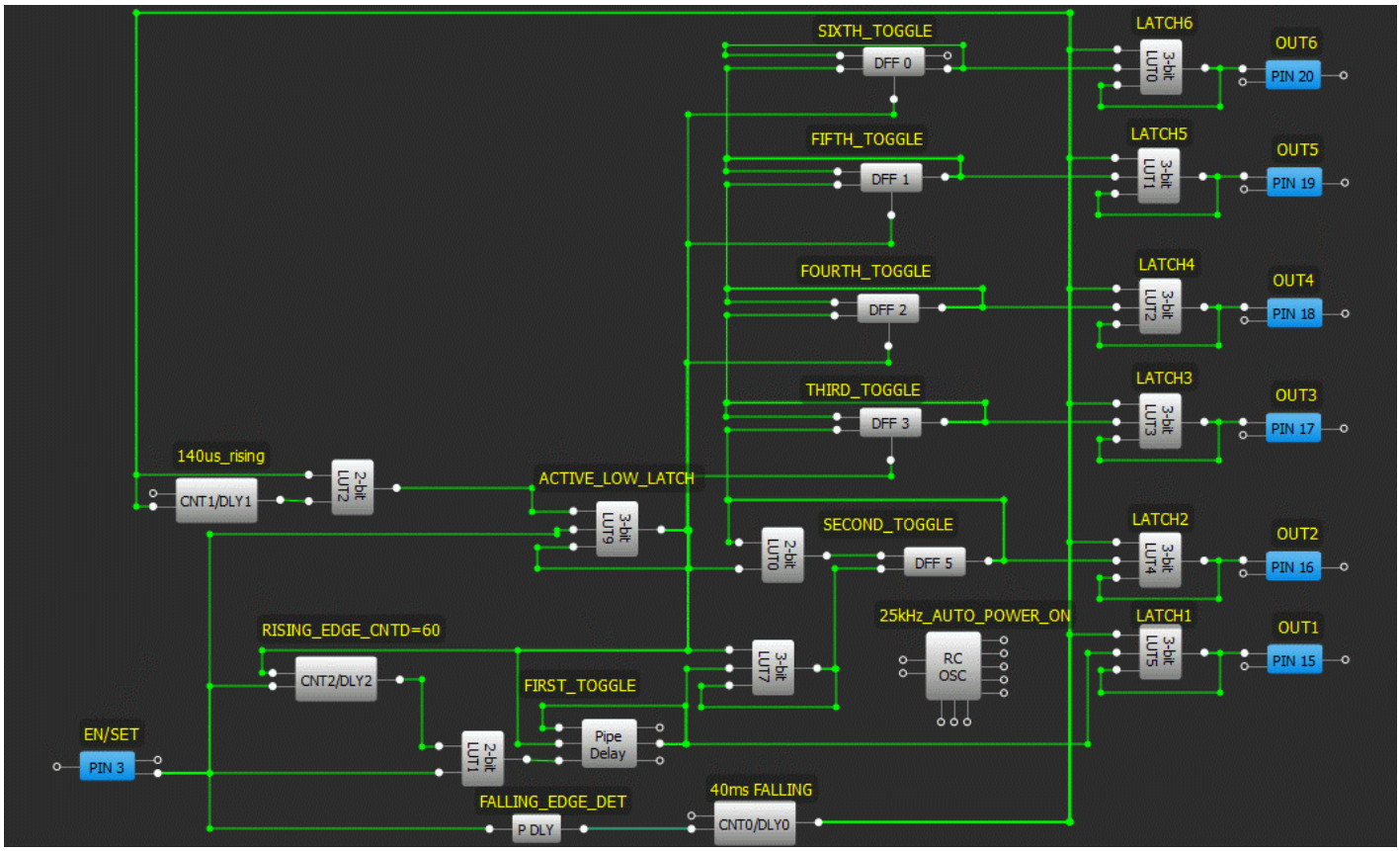

Figure 1. Single Wire circuit schematic

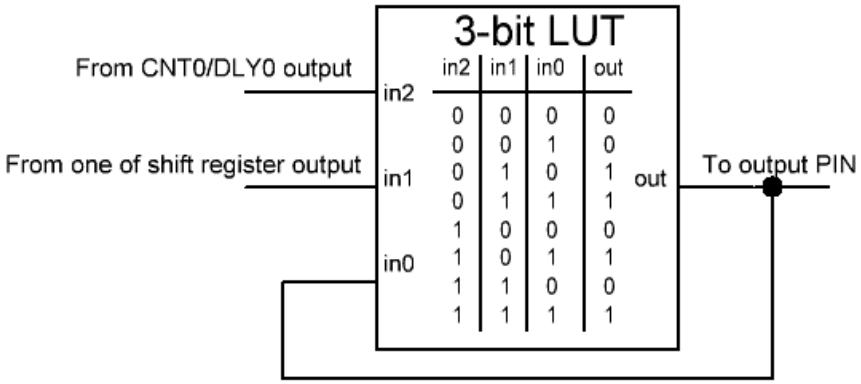

Figure 2. Latch truth table

Digital Single Wire circuit analysis

When PIN3 (EN/SET) goes LOW, the falling edge detector implemented on PDLY cell will produce a short HIGH pulse, but it's the falling edge that will be delayed by CNT0/DLY0 delay cell. This signal will hold data on LATCH1 ─ LATCH6 for approximately 40ms if no new falling edges on PIN3 (EN/SET) are detected.

Meanwhile during that CNT0/DLY0 operation (for 40ms), a HIGH signal goes to the rising edge detector implemented using CNT1/DLY1 and 2-bit LUT2 which in its turn produces HIGH pulse on active LOW latch input implemented on 3-bit LUT9 (see truth table in Figure 3).

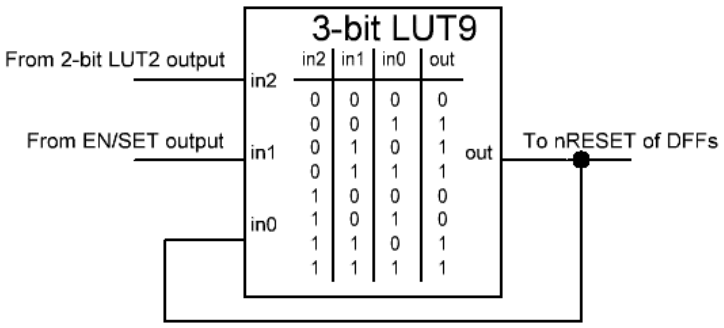

Figure 3. Active LOW latch truth table

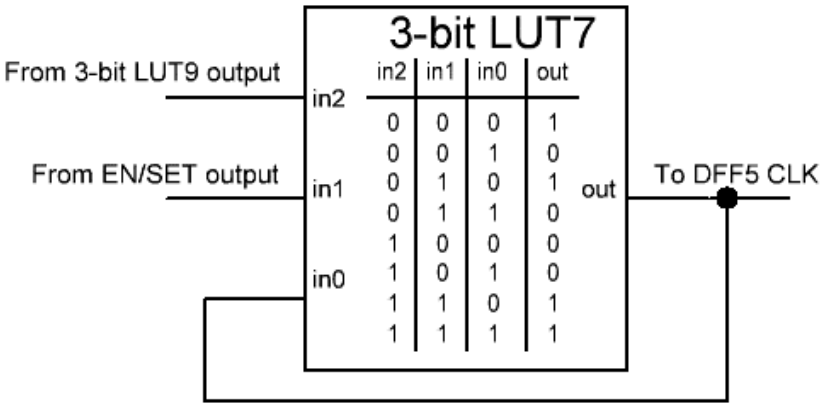

Figure 4. 3-bit LUT7 truth table

The enabled latch will set nRESET inputs of FIRST_TOGGLE – SIXTH_TOGGLE cells into a LOW state, which is how they are initialized. However, notice that in Figure 1, SECOND_TOGGLE (DFF5) has no nRESET input and this function must be added.

This is why additional look up tables are connected to its data and clock inputs. Further description of adding nSET/nRESET to DFF's can be found in AN-1029, but it can be summarized as follows:

2-bit LUT0, which produces a LOW state when nRESET is active, and 3-bit LUT7 configured to generate high frequency pulses (to guarantee switching of DFF5 to reset state) during LOW state from 2-bit LUT2. Truth table of 3-bit LUT7 can be found in Figure 4. When PIN3 (EN/SET) returns to its HIGH state, the RESET of 3-bit LUT9 active LOW latch output goes HIGH (RESET signal is LOW). The resulting oscillator pulses on 4-bit LUT0 will stop, and system will be ready to count rising edges from PIN3 (EN/SET). At that time, CNT0/DLY0 delay cell has not yet counted up to 40ms. An example waveform screenshot can be seen in Figure 5. There are 6 rising edges after the first time PIN3 goes LOW.

Where: D0 (top line) – PIN3 (EN/SET), D1 (2nd line) – PIN15 (OUT1), D2 (3rd line) – PIN16 (OUT2), D3 (4th line) – PIN17 (OUT3), D4 (5th line) – PIN18 (OUT4), D5 (6th line) – PIN19 (OUT5) and D6 (7th line) – PIN20 (OUT6).

This means that each falling edge from PIN3 (EN/SET) will reset CNT0/DLY0, and it will start counting up from its initial position.

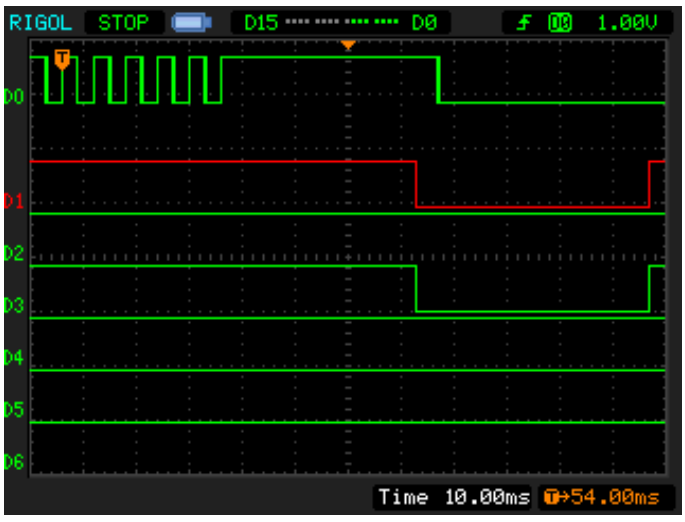

Figure 5. Single Wire functionality waveform

Meanwhile, each rising edge will count successively to the new truth table state (see Figure 6).

After six switches on DFF5 input clock, implemented on DFF5, DFF3, DFF2, DFF1, DFF0 and Pipe Delay cell (operating as six dividers by two connected from inverted output to clock of each other), will produce binary code on its outputs according to the truth table that can be found in Table 1.

This data will be transferred to LATCH1 ─ LATCH6 which will block it from propagating to OUT1 ─ OUT6 outputs, until final, HIGH (greater than duration of CNT0/DLY0 = 40ms) state comes from PIN3 (EN/SET) and CNT0/DLY0 will count up to 40ms settled delay time and produce LOW state on its output.

After CNT0/DLY0 output sets LOW, data from FIRST_TOGGLE to SIXTH_TOGGLE outputs will pass through LATCH1 ─ LATCH6 to OUT1 ─ OUT6 outputs. If after data is output, PIN3 (EN/SET) will go LOW, all DFFs and Pipe Delay from FIRST_ TOGGLE─ SIXTH_TOGGLE will go to their initial state.

This basic design works so far, but it lacks overflow protection and can lead to data errors. To improve this design, let's add delay cell (CNT2/DLY2) with external clock connected to PIN3 (EN/SET) and input connected with 3-bit LUT9 output in order to ignore more than sixty four clocks from EN/SET (see Figure 6).

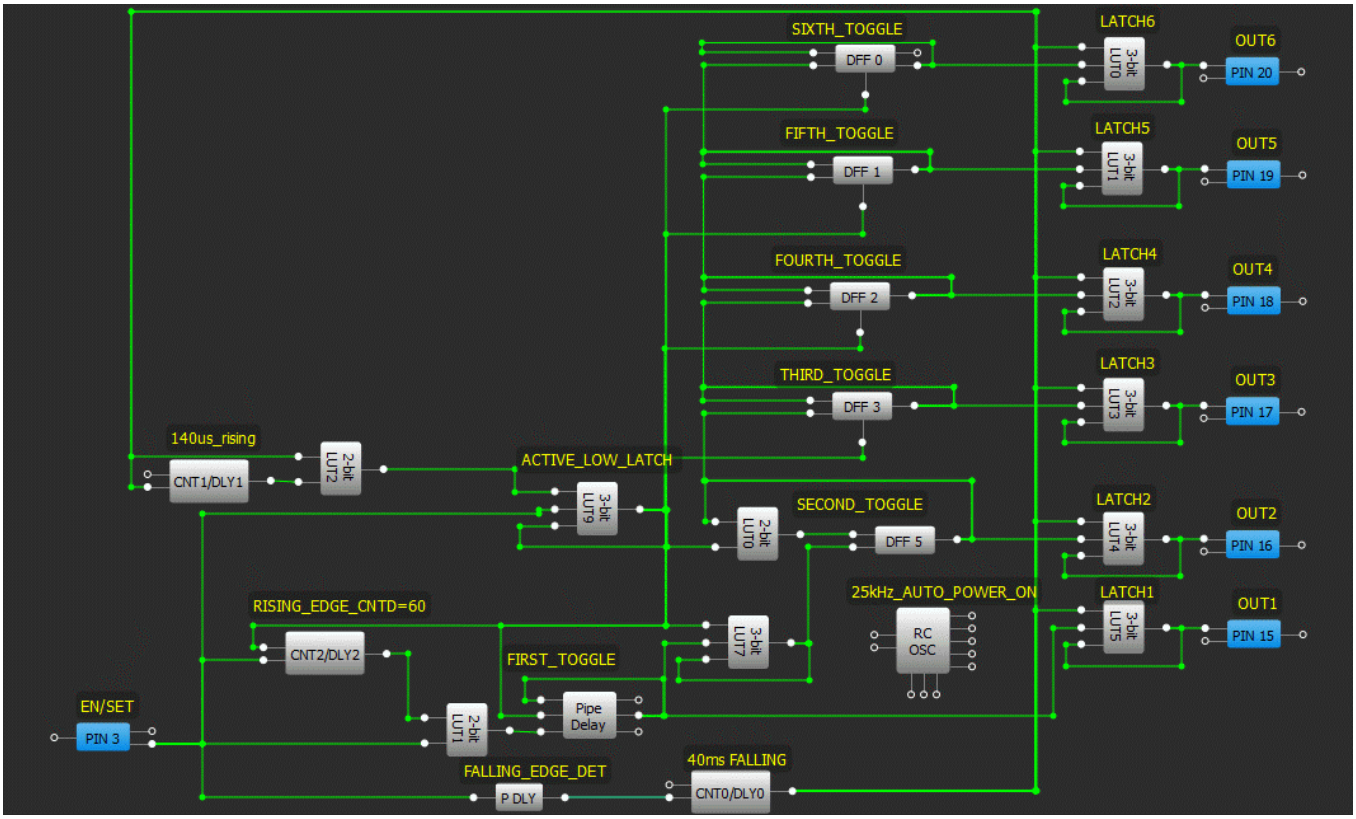

Figure 6. Single Wire circuit design

CLOCK	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1
1	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
2	HIGH	HIGH	HIGH	HIGH	HIGH	LOW
3	HIGH	HIGH	HIGH	HIGH	LOW	HIGH
4	HIGH	HIGH	HIGH	HIGH	LOW	LOW
5	HIGH	HIGH	HIGH	LOW	HIGH	HIGH
6	HIGH	HIGH	HIGH	LOW	HIGH	LOW
7	HIGH	HIGH	HIGH	LOW	LOW	HIGH
8	HIGH	HIGH	HIGH	LOW	LOW	LOW
9	HIGH	HIGH	LOW	HIGH	HIGH	HIGH
10	HIGH	HIGH	LOW	HIGH	HIGH	LOW
11	HIGH	HIGH	LOW	HIGH	LOW	HIGH
12	HIGH	HIGH	LOW	HIGH	LOW	LOW
13	HIGH	HIGH	LOW	LOW	HIGH	HIGH
14	HIGH	HIGH	LOW	LOW	HIGH	LOW
15	HIGH	HIGH	LOW	LOW	LOW	HIGH
16	HIGH	HIGH	LOW	LOW	LOW	LOW
17	HIGH	LOW	HIGH	HIGH	HIGH	HIGH
18	HIGH	LOW	HIGH	HIGH	HIGH	LOW
19	HIGH	LOW	HIGH	HIGH	LOW	HIGH
20	HIGH	LOW	HIGH	HIGH	LOW	LOW
21	HIGH	LOW	HIGH	LOW	HIGH	HIGH
22	HIGH	LOW	HIGH	LOW	HIGH	LOW
23	HIGH	LOW	HIGH	LOW	LOW	HIGH
24	HIGH	LOW	HIGH	LOW	LOW	LOW
25	HIGH	LOW	LOW	HIGH	HIGH	HIGH
26	HIGH	LOW	LOW	HIGH	HIGH	LOW
27	HIGH	LOW	LOW	HIGH	LOW	HIGH
28	HIGH	LOW	LOW	HIGH	LOW	LOW
29	HIGH	LOW	LOW	LOW	HIGH	HIGH
30	HIGH	LOW	LOW	LOW	HIGH	LOW
31	HIGH	LOW	LOW	LOW	LOW	HIGH
32	HIGH	LOW	LOW	LOW	LOW	LOW

CLOCK	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1
33	LOW	HIGH	HIGH	HIGH	HIGH	HIGH
34	LOW	HIGH	HIGH	HIGH	HIGH	LOW
35	LOW	HIGH	HIGH	HIGH	LOW	HIGH
36	LOW	HIGH	HIGH	HIGH	LOW	LOW
37	LOW	HIGH	HIGH	LOW	HIGH	HIGH
38	LOW	HIGH	HIGH	LOW	HIGH	LOW
39	LOW	HIGH	HIGH	LOW	LOW	HIGH
40	LOW	HIGH	HIGH	LOW	LOW	LOW
41	LOW	HIGH	LOW	HIGH	HIGH	HIGH
42	LOW	HIGH	LOW	HIGH	HIGH	LOW
43	LOW	HIGH	LOW	HIGH	LOW	HIGH
44	LOW	HIGH	LOW	HIGH	LOW	LOW
45	LOW	HIGH	LOW	LOW	HIGH	HIGH
46	LOW	HIGH	LOW	LOW	HIGH	LOW
47	LOW	HIGH	LOW	LOW	LOW	HIGH
48	LOW	HIGH	LOW	LOW	LOW	LOW
49	LOW	LOW	HIGH	HIGH	HIGH	HIGH
50	LOW	LOW	HIGH	HIGH	HIGH	LOW
51	LOW	LOW	HIGH	HIGH	LOW	HIGH
52	LOW	LOW	HIGH	HIGH	LOW	LOW
53	LOW	LOW	HIGH	LOW	HIGH	HIGH
54	LOW	LOW	HIGH	LOW	HIGH	LOW
55	LOW	LOW	HIGH	LOW	LOW	HIGH
56	LOW	LOW	HIGH	LOW	LOW	LOW
57	LOW	LOW	LOW	HIGH	HIGH	HIGH
58	LOW	LOW	LOW	HIGH	HIGH	LOW
59	LOW	LOW	LOW	HIGH	LOW	HIGH
60	LOW	LOW	LOW	HIGH	LOW	LOW
61	LOW	LOW	LOW	LOW	HIGH	HIGH
62	LOW	LOW	LOW	LOW	HIGH	LOW
63	LOW	LOW	LOW	LOW	LOW	HIGH
64	LOW	LOW	LOW	LOW	LOW	LOW

Table 1. Single Wire circuit truth table

As counter data CNT2/DLY2 delay cell equals 60, sixty three actual rising edges will be required (Counter Data +3) at its clock input to pass HIGH state from 3-bit LUT9 output to 2-bit LUT1 (see truth table in Figure 7) input which in its turn will block passing clocks from PIN3 (EN/SET) to the FIRST_ TOGGLE – SIXTH_TOGGLE cells. During every RESET state on 3-bit LUT9 (for example, first PIN3 (EN/SET) LOW state after output data was sent) CNT0/DLY0 will also reset to its initial state.

Note: for proper operation of circuit don't forget to correctly configure input and output pins. In case of the schematic you see in Figure 6 input is configured as digital input without Schmitt trigger, and outputs as push-pull.

Related Files

Programming code for **GreenPAK Designer**.

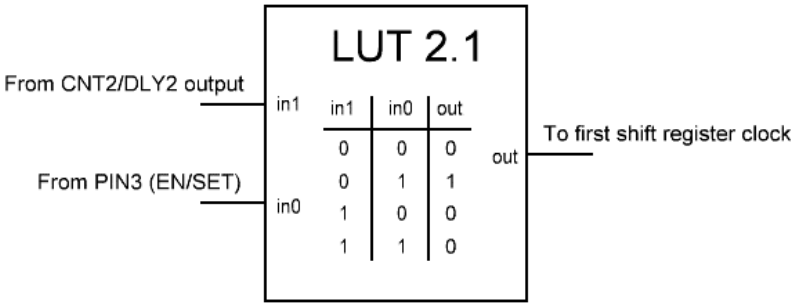

Figure 7. 2-bit LUT1 truth table

Conclusion

A single wire interface is a simple but very useful solution when it comes to minimizing the wiring and contact points in mobile devices, GPIO expansion, etc. The number of bits can be increased to 8 bits or higher by using Dialog's programmable mixed-signal ASICs devices with extended resources.

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