Konverter Analyzer

Evaluation Platform

AN1433
Rev 4.00
Oct 1, 2010

High-Speed ADC Evaluation Platform

- Complete High-Speed ADC Measurement Solution
- 40MSPS to 500MSPS Operation
- Calculation of Critical ADC Parameters (SNR, SINAD, SFDR, Harmonics, INL, DNL, Power)
- Multiple Display Modes: FFT, Time Domain, Logic
- Integrated SPI Control for ADC Configuration
- 18Mb (1MWord) Capture Depth
- Compatible with all Intersil High-Speed ADC Daughter Cards

Evaluation Platform Overview

Intersil's high-speed ADC evaluation platform consists of custom designed hardware and software. The function of the hardware is to provide power to the ADC and to excite and/or measure the appropriate analog and digital inputs and outputs. The software is required to configure the device for initial operation, to modify the device functionality or parameters, and to process and display the output data.

Two versions of the software are provided to support two different ADC families: version 1.15.6c supports all KAD27XX and KAD5XXX devices, while version 1.20c supports the ISLA11XP50 family. Refer to the Konverter Installation Guide (AN1434) for details on installing and running the different versions.

Hardware

There are two components in the hardware portion of the evaluation platform: the daughter card and the motherboard (Figure 1). The ADC is contained on the daughter card, which routes power from the motherboard and contains the analog input circuitry, clock drive and decoupling. The daughter card interfaces to the motherboard through a mezzanine connector. The motherboard contains a USB interface, an FPGA and SRAM. The motherboard serves as the interface between the host PC and the ADC daughter card. Most of the ADC functionality is controlled by the motherboard, although some daughter cards have jumpers to set certain operating modes. The FPGA accepts output data from the ADC and buffers it in the SRAMs before passing it to the PC at a lower speed for post-processing. The maximum buffer depth is approximately one million words.

The user must supply low-jitter RF generators for the clock and analog inputs. Recommendations of suitable generators can be found in Appendix A.

Many low-jitter RF generators exhibit high harmonic spectral content relative to the ADC performance. A band-pass filter is recommended to attenuate the harmonics. A wideband attenuator in series with the band-pass filter is also recommended for daughter cards without on-board attenuators. Current spikes from the ADC's switched capacitor sample-and-hold amplifier can create signal reflections in the coaxial cable. The attenuator reduces these reflections and improves performance.

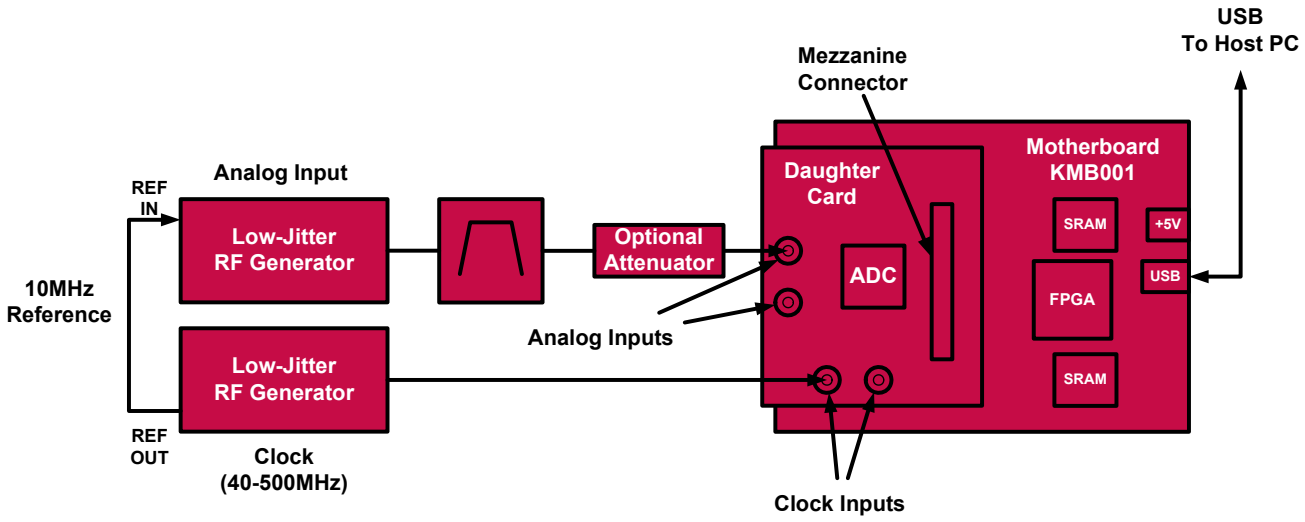


FIGURE 1. EVALUATION PLATFORM BLOCK DIAGRAM

Software

The software component is Konverter Analyzer, a graphical user interface (GUI) created with MATLAB™. A MATLAB Component Runtime engine is supplied, which executes a compiled version of the m-files. Therefore a stand-alone version of MATLAB is not required to run Konverter Analyzer.

The GUI controls the ADC configuration through the SPI port, reads data from the motherboard and performs post-processing and display of the output data. Data can be viewed in the time or frequency domain, and can be saved for later processing. Critical performance parameters such as SNR, SFDR, harmonic distortion, etc. are calculated and displayed on-screen when viewing in the frequency domain.

Initial Start-Up

Referring to Figure 1, connect the daughter card to the motherboard by aligning the two mating mezzanine connectors. Four screws on the motherboard (not shown) align with mounting holes in the daughter card. Next, connect the RF generators to the Clock and Analog input SMA connectors. Set the clock frequency as desired with the power level at +10dBm. Similarly, set the analog input frequency with a power level of approximately +7dBm (the full-scale value will vary depending on the loss of the input path and gain of the ADC). With the RF generators on, apply +5V power (minimum 5W supply) to the motherboard. The daughter card is powered by linear regulators on the motherboard.

Daughter Cards

Each daughter card is designed to produce optimal ADC performance and simplify the evaluation process. Some boards have multiple connections for the analog input and clock. For example, low-frequency and high-frequency input paths are provided on certain boards. A high-frequency input path may have a balun interface, while a low frequency path may use a transformer or buffer amplifier (for DC coupling). Refer to “Appendix B: Daughter Cards” on page 7 for details on specific models.

Motherboard

The only connections required for the motherboard are +5V power and a USB connection to the PC running Konverter Analyzer. No additional configuration of the motherboard is required.

Software Start-Up

The FPGA clock is derived from the ADC output clock, and the FPGA clock must be active for the software to run properly. Therefore, it’s important that the evaluation platform is powered and receiving a conversion clock prior to starting Konverter Analyzer.

The compressed MATLAB files are unpacked the first time the GUI is invoked after installation. Subsequently the graphical window will open more quickly. Complete information can be found in the KMB-001 Installer manual.

The main Konverter Analyzer window is shown in Figure 2. The application opens in FFT mode by default, but other modes can be selected using the radio buttons in the lower left corner. In each mode, relevant parameters are displayed in the data box on the left side of the window.

The following parameters are displayed in the data box in all operating modes:

- Fsamp: Sample clock frequency, automatically detected
- Ffund: Input frequency, automatically detected (assumes sine wave input)
- Fund: Input amplitude
- Samples: Record length
- Power: Total power dissipation, as well as the voltage and current of each supply

Data Acquisition

Press the Run button in the lower left corner of the screen (see Figure 2) to produce a single FFT plot. The Continuous check box can be selected to capture and display successive FFT plots. Multiple acquisitions can be averaged by selecting the Average check box. The number of averaged acquisitions defaults to 10, but can be changed in the Setup Conditions dialog.

Menu items and the toolbar buttons may not function properly if data is being captured in Continuous mode. Stop the acquisition before selecting a menu item or using a toolbar button.

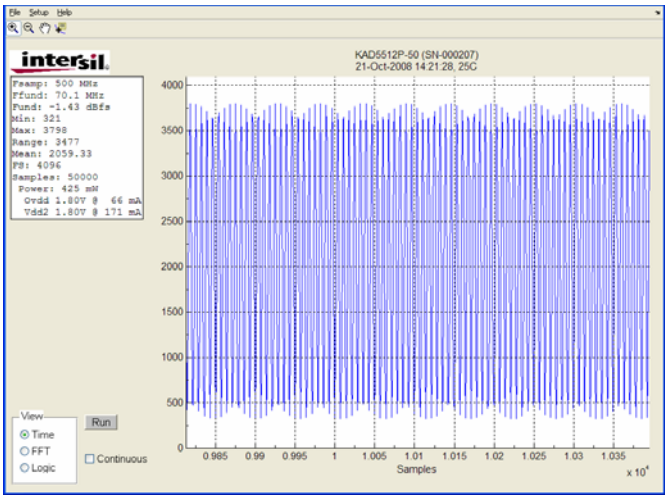


FIGURE 2. TIME-DOMAIN DISPLAY

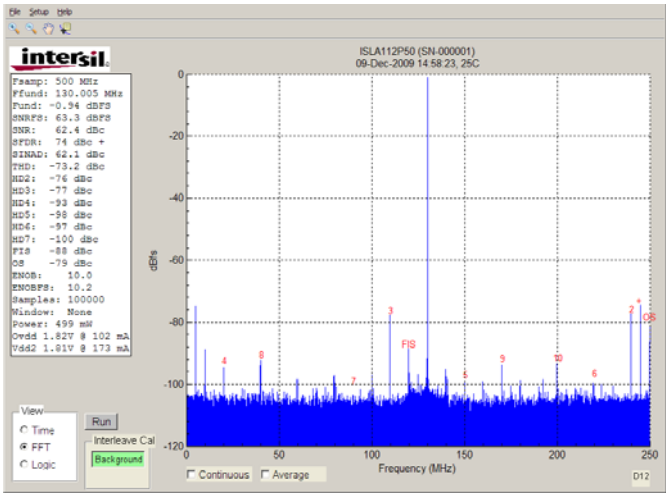


FIGURE 3. FREQUENCY-DOMAIN DISPLAY

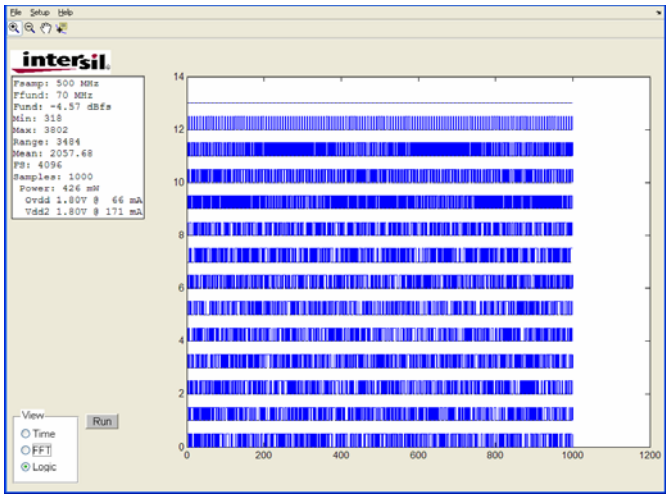


FIGURE 4. LOGIC DISPLAY

Display Options

Time-Domain Display

The time-domain display mode shows ADC code versus sample number for the complete data record (Figure 2). In addition to the standard parameters, the following are displayed:

- Min: Minimum code in data record
- Max: Maximum code in data record
- Range: Code Range (Max – Min)
- Mean: Mean of data record
- FS: Full-scale code

Frequency-Domain Display

The Fast Fourier Transform (FFT) of the data record is displayed from DC to the Nyquist frequency ($f_S/2$), as shown in Figure 3. The following unique parameters are displayed in this mode:

- SNRFS: Signal-to-Noise Ratio related to the ADC Full-Scale input
- SNR: Signal-to-Noise Ratio related to the input signal power
- SFDR: Spurious-Free Dynamic Range
- SINAD: Signal-to-Noise And Distortion ratio
- THD: Total Harmonic Distortion
- HD2—HD7: Second Harmonic Distortion Component (HD2) through seventh Harmonic Distortion Component (HD7)
- FIS: Fundamental Image Spur (interleaved mode only)
- OS: Offset Spur (interleaved mode only)
- ENOB: Effective Number Of Bits
- ENOBFS: ENOB – (Fundamental Amplitude)/6.02
- Window: Window type. Options are Hanning, Blackman-Harris 4-Term or None.

The location of harmonics HD2 through HD10 are indicated with red numbers on the FFT display. The largest frequency spur, which determines the SFDR value, is marked with a red '+' symbol.

For interleaved ADCs there are two additional marked spurs: the Fundamental Image Spur (FIS) and the Offset Spur (OS). These spurs arise in interleaved ADCs due to imperfect matching between the unit ADCs. The FIS occurs at the unit ADC sample rate minus the input frequency, while the OS occurs at the unit ADC sample rate.

When the ISLA112P50 daughter card is connected, the Background Interleave Cal button is enabled. This allows the user to turn the Intersil Interleave Engine (I2E) on or off. Full control of the I2E block is accomplished using the Interleave Control Panel.

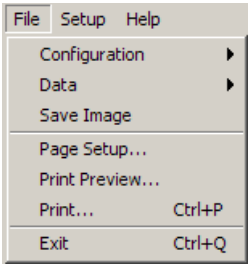
Logic Display

The logic value for each output bit is displayed versus sample number for the complete data record, similar to a logic analyzer (Figure 4). The displayed parameters are the same as those in Time mode.

Logic mode may operate very slowly with large data records. If a warning dialog is displayed when switching to Logic mode, reduce the record length using the Setup FFT dialog.

Menus

File



The file menu allows the user to load or save a data record or configuration file as well as print the current display. Data is stored as an ASCII file in comma-separated value (CSV) format. Configuration files are binary.

A graphical output can be created by selecting Save Image (version 1.20c only). When the dialog box opens (Figure 5), the following formats are available:

- PDF: Portable Document Format
- AI: Adobe Illustrator
- BMP: Bitmap
- EPS: Encapsulated Postscript
- EMF: Enhanced Metafile
- JPG: JPEG

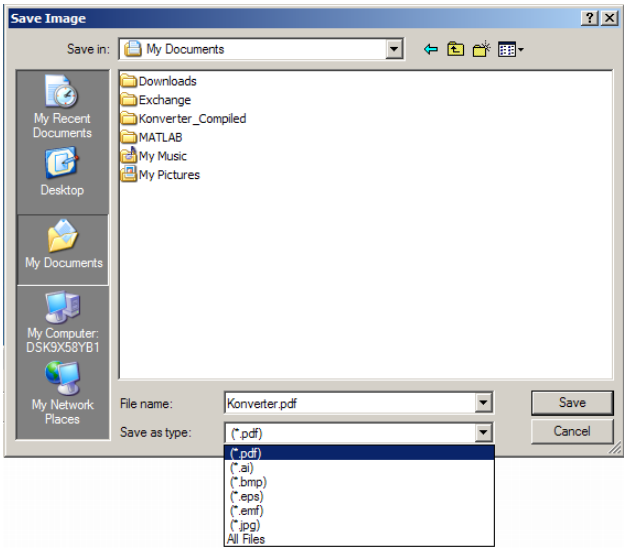
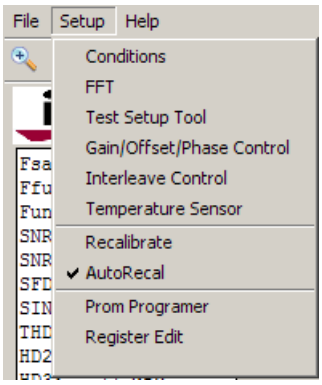


FIGURE 5. SAVE IMAGE DIALOG BOX (VERSION 1.20c ONLY)

The Print Preview command will show how the display will print based on the current printer and page settings. Select Print to create a hard copy.

Setup



The Conditions dialog sets up the basic operating parameters of the system based on the installed daughter card (see Figure 6). Most of these settings are automatically detected by reading an EEPROM on the daughter card and should not be changed. The current state of the daughter card is indicated in red text under 'Current ADC Configuration'. This information can help guide the selection of motherboard modes to match the ADC operating state.

The default data folder can be changed by editing the path or browsing the local directory tree. LVDS or LVCMOS outputs can be selected, however the correct motherboard must be in use (LVDS vs CMOS inputs).

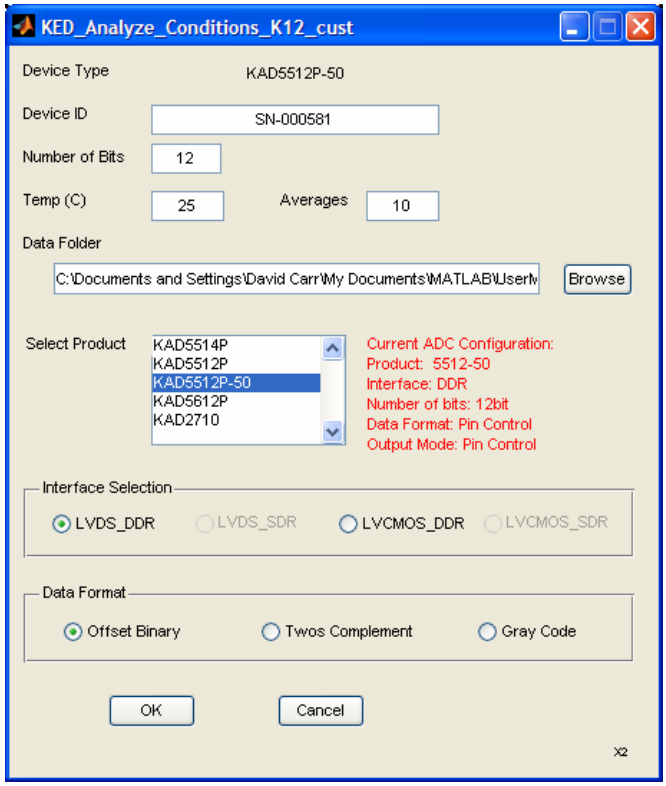


FIGURE 6. CONDITIONS DIALOG

The FFT dialog (Figure 7) allows the selection of several parameters that impact the FFT display and parametric calculations.

- Samples: The length of the data record
- Sample Rate: The ADC sample rate. This option is unavailable unless the Force check box is selected.
- Fundamental Frequency: The input frequency (assumes sine wave). This option is unavailable unless the Force check box is selected.
- Fundamental Leakage: The number of bins around the fundamental that are ignored in the parametric calculations. This can be used to ignore phase noise or side-lobes.
- Harmonic Leakage: The number of bins around the harmonics that are ignored in the parametric calculations.
- DC Leakage: The number of bins above DC that are ignored in the parametric calculations. This can be used to ignore 1/f noise.
- # Harmonics: The number of harmonics displayed in the graph, and used in the THD and SINAD calculations.
- Windowing: Window type. Options are Hanning, Blackman-Harris 4-Term or None.
- Axis Limits: The minimum and maximum extent of the axes and the y-axis units (dBc or dBFS).

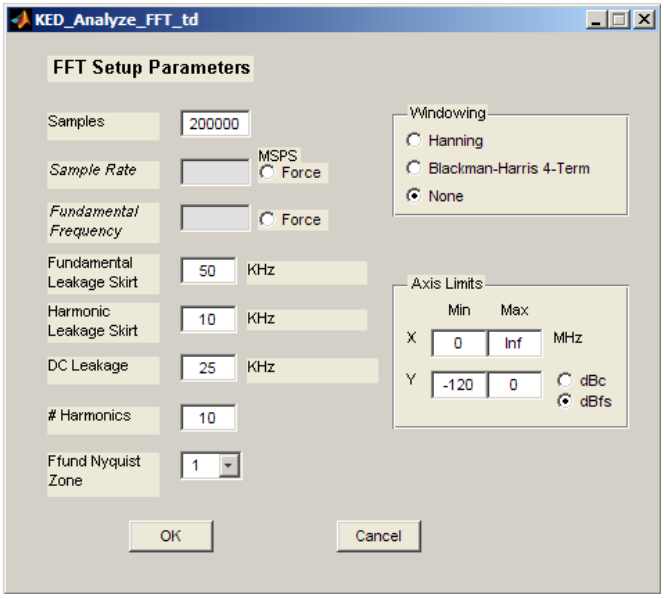


FIGURE 7. FFT DIALOG

The sample rate and fundamental frequency are automatically detected by default, and assume a single tone sine wave input. The estimate of the sample rate is based on the crystal frequency of the USB controller and is rounded to the nearest 100kHz.

The exact sample rate can be specified by selecting the Force radio button in the dialog and entering a new value. This scales the frequency axis of the FFT; it does not change the acquisition rate.

Selecting the Force radio button adjacent to the Fundamental Frequency box allows a different frequency bin to be used as the reference point for the FFT calculations. This is useful when windowing the data to force the fundamental into the center of a frequency bin. It can also be used when an interfering signal is present, in order to force the calculations to be made relative to the desired signal.

If the input frequency and sample rate are selected such that an integer number of cycles is captured in the data record, then windowing should not be used. To reduce spectral leakage, a Hanning or Blackman-Harris 4-Term window can be applied to the data if such a relationship doesn't exist. The window selection depends on the signal being measured and the desired analysis.

By default the software assumes that the input is in the first Nyquist zone and calculates the frequency appropriately. The Ffund Nyquist Zone can be selected to calculate the correct frequency in undersampling applications.

The Test Setup Tool (Figure 8) can be used to properly select the input frequency, sample rate and record length if coherent sampling is desired (version 1.20c only). The current operating conditions (Sample Frequency, Input Frequency and Samples) are loaded when the GUI is opened. If the coherent sampling criteria are met then Strictly Coherent will be displayed next to the Samples field. If not, suggested Input Frequencies or record length can be used under "Try These Values." If the suggested Samples value is selected, the user may update the main GUI by pressing "Update Konverter Samples."

Note that the Estimated DNL Error indicates the minimum DNL that may be achieved given the selected conditions, not the actual DNL performance of the ADC.

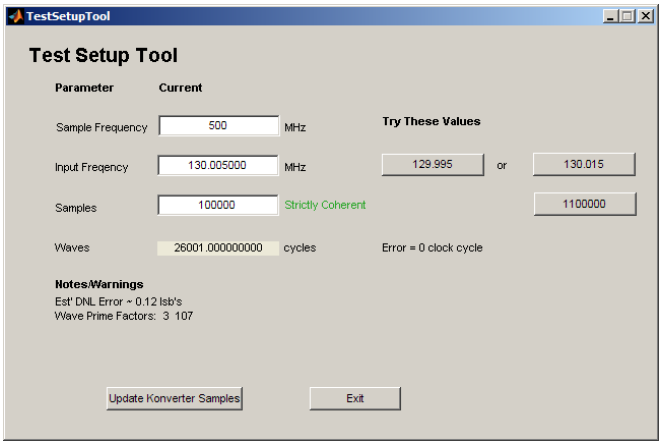


FIGURE 8. TEST SETUP TOOL (VERSION 1.20c ONLY)

The Register Control Panel (Figure 9) is used to adjust the gain, offset and clock skew of the ADC cores and control various functional settings such as data format and output mode. The Phase setting is differential in nature and therefore is only applicable for products with two ADC cores (e.g. KAD5512P-50 and KAD56XX).

Gain and Offset adjustments are made to each ADC core individually. The Channel A/Channel B button selects which core is adjusted. Gain can be adjusted in coarse, medium and fine steps, while offset is adjusted in coarse and fine steps (refer to the product datasheet for the adjustment range and resolution).

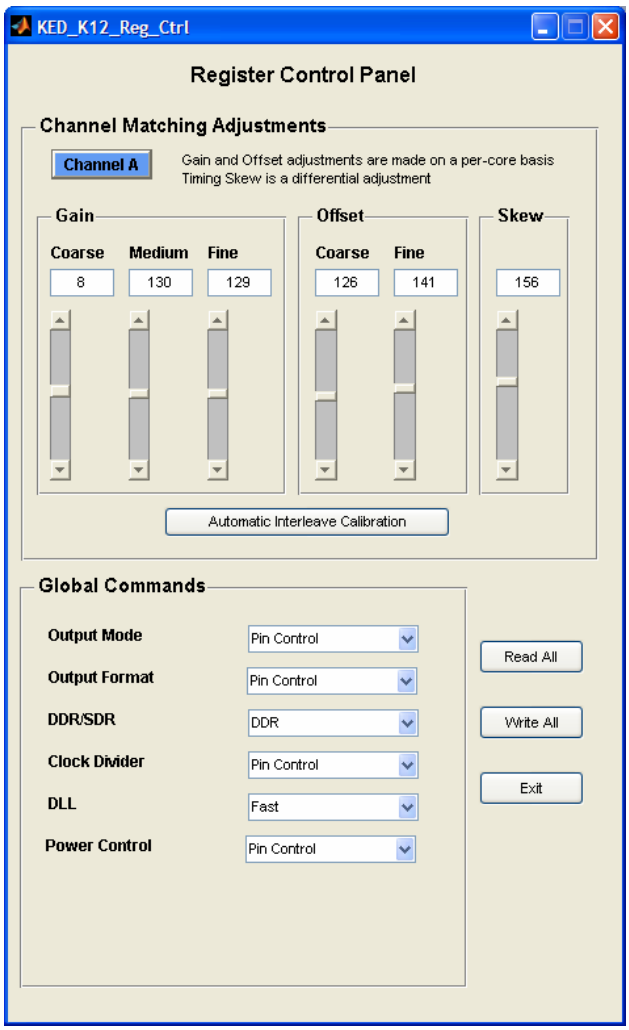


FIGURE 9. REGISTER CONTROL PANEL

Values can be entered manually or adjusted with the slider controls. The Read All button reads the value for each ADC register and adjusts the slider display if necessary. Write All commits the entered values to the ADC. It's not necessary to use Write All when using the sliders—any changes made are committed immediately.

The 'Automatic Interleave Calibration' button executes an algorithm which attempts to match the gain, offset and timing skew between unit ADCs (applies to interleaved ADCs only). After execution, the fundamental image spur (FIS) and offset spur (OS) should both be minimized. This command can be executed after the sample rate or input frequency change substantially.

Operation of the I2E engine is controlled in the Interleave Control Panel (version 1.20c only, Figure 10). The OGP On/Off button determines if updates are made to the unit ADCs, while the bars to the right show the current state of the Offset, Gain and Delay adjustments.

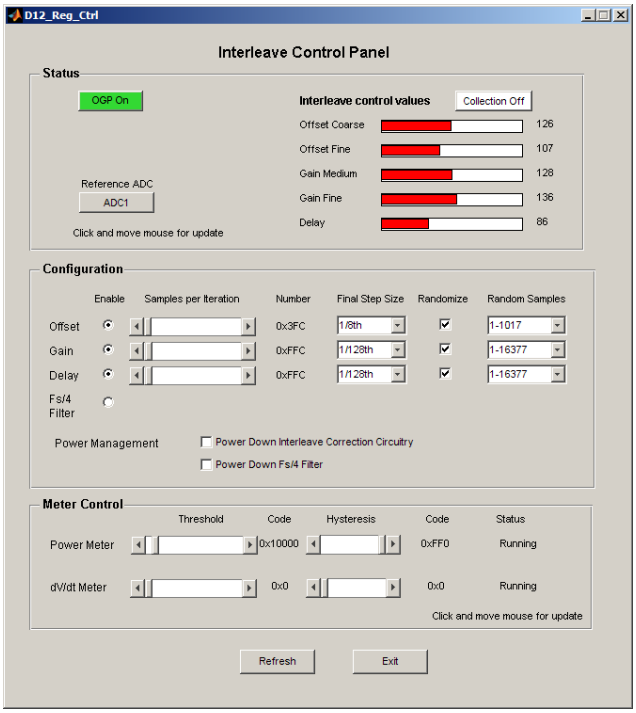


FIGURE 10. INTERLEAVE CONTROL PANEL (VERSION 1.20c ONLY)

In the Configuration section, each adjustment (Offset, Gain and Delay) can be individually enabled and controlled. The number of Samples per Iteration determines how quickly the algorithm will converge, while the Final Step Size sets the granularity. Randomization of the iteration length is recommended for optimum performance, but this can be disabled.

The Power Meter sets the minimum power threshold that the input signal must cross for the algorithm to apply correction factors.

Refer to the applicable product datasheet for more detail on the functions and control of the I2E algorithm.

Some products have an internal temperature sensor, which is accessed using the Temperature Sensor window (version 1.20c only, Figure 11). The absolute accuracy of the internal temperature monitor can range from ±10% to ±15%, but relative accuracy (i.e. accuracy of detecting temperature changes) is much better. The temperature display assumes that the ADC is operating at room temperature (+25°C) when the GUI is invoked.

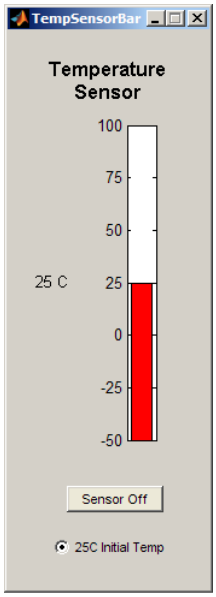


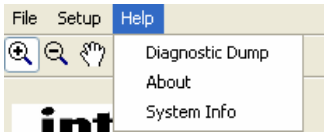
FIGURE 11. TEMPERATURE SENSOR (VERSION 1.20c ONLY)

The Recalibrate menu item resets the ADC, which forces a recalibration. The GUI will automatically recalibrate the ADC when the clock frequency changes if Setup→AutoRecal is selected.

The Prom Programmer menu item is a password protected factory function and is not intended for general usage.

Register Edit allows access to the entire SPI register map. An example is shown in Figure 12. Refer to the product datasheet for specific register definitions.

Help



The Diagnostic Dump menu item saves detailed status information that can be used by the factory to help troubleshoot operational issues.

About shows version information and can display the software license agreement.

System Info displays information about the software and hardware set-up.

Toolbar

Zoom

Selecting one of the magnifying glass icons allows the axis limits to be changed graphically. Right click in the graph window for zoom options (horizontal or vertical) or to reset the axes to default limits.

Pan

The hand icon allows panning the graphic when zoomed.

Markers

Data points can be marked by selecting the marker icon and clicking on the graphic. Multiple markers can be placed by selecting Create New Data tip from the right-click menu. X and Y data is displayed for each marker.

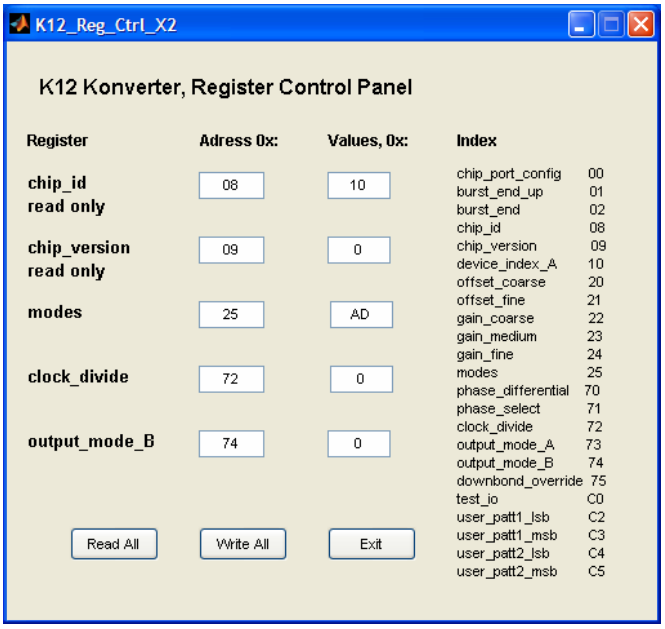


FIGURE 12. REGISTER EDIT DIALOG

Appendix A: RF Generators

Intersil uses the following RF generators as clock and signal sources when characterizing high-speed ADCs:

- Rohde & Schwarz: SMA100A
- Agilent: 8644B (with Low-Noise option)

These generators provide very low jitter to optimize the SNR performance of the ADC under test. Other generators with similar phase noise performance can also be used. Contact Intersil Technical Support for recommendations.

Appendix B: Daughter Cards

KDC5512EVALZ, KDC5512HEVALZ, KDC5512-50EVALZ, KDC5514EVALZ, ISLA112P50IR72EV1Z

These daughter cards use a common design to accommodate the single-input devices from the KAD55XX and ISLA11XP50 families. They allow for two clock input paths and two analog input paths. The clock can be driven through a 4:1 transformer or a CML buffer. The default clock path is through the Mini-Circuits TC4-1W transformer (labeled as CLOCK INPUT XFMR on the PCB). The AC-coupling capacitors in the buffered path (C46, C47) are not populated. To use the clock buffer, install 200pF capacitors in positions C46 and C47 and depopulate the AC-coupling capacitors (C28, C29) in the transformer path.

The two analog input circuits are both transformer-coupled. The path marked Lo Frequency Input uses two back-to-back Mini-Circuits ADT1-1WT transformers. This path provides good performance for input frequencies between 1MHz and 100MHz. The Hi Frequency Input path (default) uses two back-to-back Mini-Circuits ADTL1-12 transformers, which provide good performance from 100MHz to 1GHz. To switch to the Lo Frequency path, remove 0Ω resistors R16 and R17 and install 0Ω resistors R18 and R20.

KDC5512-Q48EVAL, KDC5512H-Q48EVAL, KDC5514-Q48EVAL

These daughter cards contain the 48-QFN version of the product. To switch to the Lo Frequency path, remove 0Ω resistors R14 and R15 and install 0Ω resistors R16 and R18.

KDC5612EVAL

This daughter card was designed to allow for two clock input paths and two analog input paths (for each input). The clock can be driven through a 4:1 transformer or a CML buffer. The default clock path is through the Mini-Circuits TC4-1W transformer (labeled as CLOCK INPUT XFMR on the PCB). The AC-coupling capacitors in the buffered path (C48, C51) are not populated. To use the clock buffer, install 200pF capacitors in positions C48 and C51 and depopulate the AC-coupling capacitors (C45, C49) in the transformer path.

The two analog input circuits are both transformer-coupled, and are replicated for each ADC input. The path marked Lo Frequency Input uses two back-to-back Mini-Circuits ADT1-1WT transformers. This path provides good performance for input frequencies between 1MHz and 100MHz. The Hi Frequency Input path (default) uses two back-to-back Mini-Circuits ADTL1-12 transformers, which provide good performance from 100MHz to 1GHz. To switch to the Lo Frequency path, remove 0Ω resistors R16, R17, R22 and R23 and install 0Ω resistors R18, R20, R24 and R26.

KAD5610P, KAD5510P-50, KAD2708

These products are lower resolution versions of other products and do not have dedicated daughter cards. Performance can be evaluated by ordering the higher resolution card and adjusting the Number of Bits in the Conditions Dialog as follows:

- KAD5610: Order KDC5612EVAL (Number of Bits = 10)
- KAD5510P-50: Order KDC5512-50EVALZ (Number of Bits = 10)
- KAD2708C: Order KDC2710CEVAL (Number of Bits = 8)
- KAD2708L: Order KDC2710LEVAL (Number of Bits = 8)

Revision History and Software Version

DOCUMENT VERSION	RELEASE DATE	KONVERTER GUI VERSION	DOCUMENT CHANGES
1	12/11/07	1.10c	Initial Release
1.1	2/29/08	1.11c	Updated diagrams
1.2	3/21/08	1.11c	Updated Figure 1, added note concerning attenuator
1.3	4/15/08	1.12c	Updated diagrams, added Automatic Interleave Cal description
1.4	9/2/08	1.14c	Updated diagrams, added Rev B Daughter Card description
AN1433.0	10/14/08	1.14c	Converted to Intersil template. Replaced instances of “Kenet” with “Intersil” where applicable and assigned file number AN1433.0 (Rev 0 - as the initial release with this file number).
AN1433.1	10/23/08	1.15.1c	Changed last Feature bullet to “Compatible with all Intersil High-Speed ADC Daughter Cards” and replaced all graphics showing Kenet logo with graphics showing Intersil logo (Fig 2, 3 and 4; graphics below “setup” page 4 and graphic below “Help” page 6).
AN1433.2	1/29/09	1.15.1c	Posted to Internet
AN1433.3	2/4/2010	1.18c	Converted to New Intersil Template Added descriptions of new features: Page 4: Save Image Page 5: Ffund Nyquist Zone and Test Setup Tool Pages 6/7: Interleave Control and Temperature Sensor Pages 7/8: Corrected Daughter Card part numbers, added Q48 daughter cards and instructions for lower resolution products without dedicated cards. Corrected resistor numbers in KDC5612P section
AN1433.4	9/21/10	1.15.6c and 1.20c	Page 1: Added details on two software versions and reference to AN1434 for instructions on installation/operation Page 7: Added references to new daughter cards, updated part numbers with “Z” for boards converted to RoHS status Various Pages: Added reference to “(version 1.20c only)” where appropriate

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