# RENESAS

### ISL6740EVAL3Z

User Guide

The I SL6740EVAL3Z serves as a reference design for a 48V to  $\pm$ 12V, 3.3V and 1.5V isolated power supply. It utilizes an ISL6740 double-ended voltage mode controller in half bridge topology to provide an isolated 48V to  $\pm$ 12V conversion. An ISL6402 dual PWM controller in synchronous buck topology provides the 3.3V and 1.5V outputs from the +12V rail. The reference design also provides pads to implement an optional LDO using the ISL6402 as a controller.

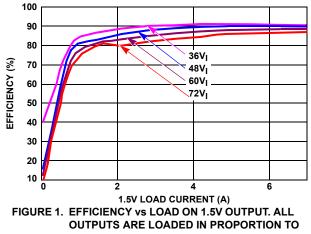
#### Specifications

- Input Voltage: 36V to 72V
- Outputs:

3.3V ±1% @ 4A 1.5V ±1% @ 7A 12V +3.5%/-10% (typical) @ 1.5A -12V +3.5%/-10% (typical) @ 1.5A

• Efficiency at full load: 86.8% (72V input) to 90.3% (36V input)

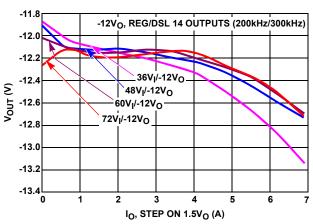
Efficiency is plotted in Figure 1 overload, and for various input voltages V<sub>I</sub>. The current shown on the X axis represents load current on the 1.5V output. In this test, the loads on the 3.3V, +12V and -12V outputs were all varied proportionately to the 1.5V load. At 7A (maximum 1.5A load), for example, the 3.3V output load is 4A and the +12V and -12V outputs are loaded at 1.5A each.

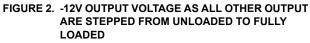


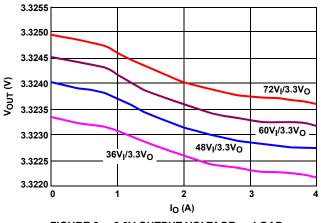
THE 1.5V OUTPUTS' FULL LOAD.

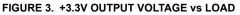
Regulation on the 1.5V and 3.3V outputs is very good over line and load due to individual control loops. The  $\pm$ 12V outputs, however, are regulated together. While this saves cost and board space by eliminating additional feedback circuitry, there is a penalty in terms of regulation performance. Figure 2 shows the worst case scenario of an unloaded -12V output with the remaining outputs being stepped from no load to fully loaded. When full load on the +12V, +3.3V and +1.5V outputs is reached, a worst case error of about -10% is seen. Figures 3 and 4 show typical 3.3V and 1.5V output regulation over load. **USER'S MANUAL** 

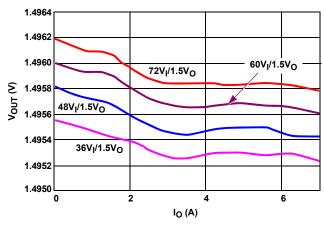
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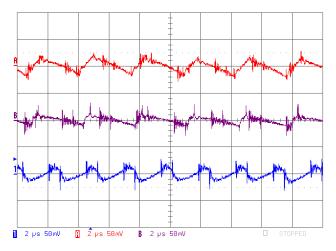




AN1127 Rev 2.00 Aug 1, 2007



Ripple and noise measurements are illustrated in Figure 5 for an input of 48V, with all outputs fully loaded. In general peak noise + ripple on the test board is  $80mV_{P-P}$ .





Start-up response is shown in Figure 6 for  $48V_{IN}$ , with all outputs fully loaded except for -12V, which is unloaded. The 3.3V and 1.5V start-up responses are independent of input voltage. The 12V output exhibits from 0V to 1V of overshoot as input voltage varies from 36V to 72V.

Figures 7 and 8 show transient responses on the 3.3V line as its load is stepped from 0% to 50% (2A), and from 50% to 0%. Likewise, the transient responses of the 1.5V line are shown in Figures 9 and 10. Figures 11 and 12 show the 24V (+12V to -12V) responses to 25% to 75% and 75% to 25% load steps.

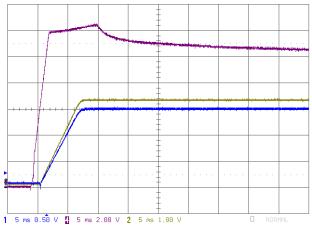
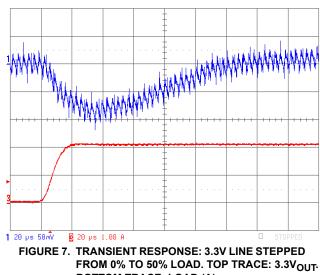


FIGURE 6. START-UP RESPONSE WITH 48VIN AND ALL OUTPUTS FULLY LOADED EXCEPT -12V, WHICH IS OPEN. TOP TO BOTTOM: +12V, +3.3V, +1.5V



BOTTOM TRACE: LOAD (A).

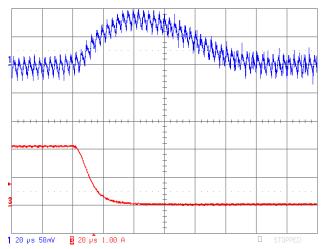
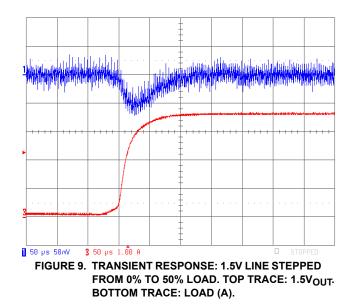


FIGURE 8. TRANSIENT RESPONSE: 3.3V LINE STEPPED FROM 50% TO 0% LOAD. TOP TRACE: 3.3V<sub>OUT</sub>. BOTTOM TRACE: LOAD (A).





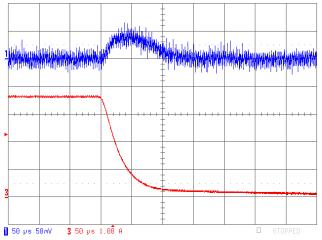


FIGURE 10. TRANSIENT RESPONSE: 1.5V LINE STEPPED FROM 50% TO 0% LOAD. TOP TRACE: 1.5V<sub>OUT</sub>. BOTTOM TRACE: LOAD (A).

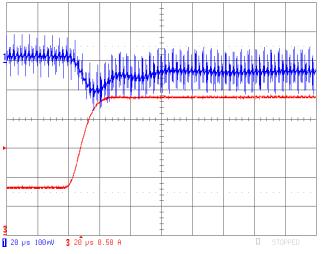


FIGURE 11. TRANSIENT RESPONSE: 24V LINE STEPPED FROM 25% TO 75% LOAD. TOP TRACE: 1.5V<sub>OUT</sub>. BOTTOM TRACE: LOAD (A).

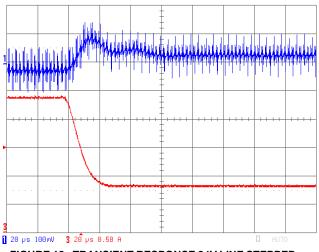


FIGURE 12. TRANSIENT RESPONSE 24V LINE STEPPED FROM 75% LOAD TO 25% LOAD. BOTTOM TRACE: LOAD (A).

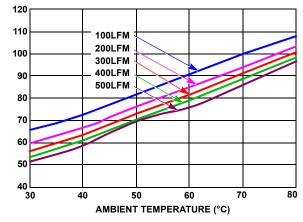


FIGURE 13. HOTTEST PART TEMPERATURE (°C) vs AMBIENT TEMPERATURE (°C) AND AIR FLOW AT 36V INPUT

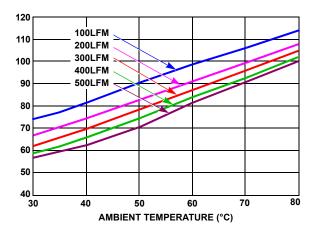


FIGURE 14. HOTTEST PART TEMPERATURE (°C) vs AMBIENT TEMPERATURE (°C) AND AIR FLOW AT 72V INPUT

Thermal data is provided in Figures 13 and 14 for input voltages of 36V and 72V, respectively. These plots show the temperature of the hottest component vs ambient temperature for air flow rates of 100LFM to 500LFM.

Figure 15 shows a thermal image of the board running at an input voltage of 48V. This image was taken with the board running at full power with a 300LFM air flow rate.

Figures 16 through 21 show the layout of the evaluation board. The bill of materials (BOM) and the schematics are shown in the following. This evaluation board has been designed to meet ROHS compliance.



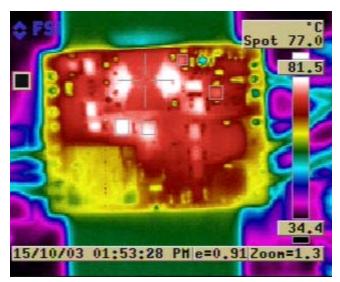


FIGURE 15. THERMAL IMAGE: 48V INPUT, 300LFM AIR FLOW

#### TABLE 1. COMPONENT LIST

REFERENCE DESIGNATOR	VALUE	MANUFACTURER	PARTS
CR1, CR2	Schottky SMD, 30V, 200mA	Fairchild	BAT54S-T
D3, CR3, D4, CR7, CR8, CR9	Schottky SMD, 30V, 200mA	Fairchild	BAT54-T
CR4	DPAK, 60V, 12A, ROHS	IR	12CWQ06FNPBF
CR6, CR5	100V, 3A, ROHS	IR	30BQ100PBF
C1	1µF, 100V, 20%, X7R, ROHS	VENKEL	H1087-00105-100V20-T
C3,C2	3.3µF, 50V, 20%, X7R, ROHS	TDK	H1087-00335-50V20-T
C4, C6, C24, C45, C57	1µF,16V, 10%, X7R, ROHS	VENKEL	H1046-00105-16V10-T
C5, C31, C52	0.1µF, 50V, 10%, X7R, ROHS	TDK	H1045-00104 -50V10-T
C7	1000pF, 16V, 10%, X7R, ROHS	VENKEL	H1045-00102 -16V10-T
C8, C23, C26, C49	22µF, 16V, 20%, X5R, ROHS	TDK	H1087-00226-16V20-T
C9, C22, C32, C34, C39, C59	47µF, 16V, 20%, ROHS	Sanyo	16TQC47M
C10, C14, C50, C51, C54, C55	1000pF, 50V, 10%, X7R, ROHS	MURATA	H1045-00102-50V10-T
C12, C11	1000pF, 100V, 10%, X7R, ROHS	VENKEL	H1045-00102-100V10-T
C13	560pF, 100V, 5%, NPO, ROHS	TDK	H1045-00561-100V5-T
C15, C16, C18, C41, C44, C47	0.1µF, 16V, 10%, X7R, ROHS	MURATA	H1045-00104-16V10-T
C17	220pF, 16V, 10%, X7R, ROHS	TDK	H1045-00221-16V5-T
C19	0.22µF, 16V, 10%, X7R, ROHS	TDK	H1045-00224-16V10-T
C20	220pF, 50V, 5%, C0G, ROHS	VENKEL	H1045-00221-50V5-T
R14, R20, R22, R30, R31, R41, R42, D5, Q6, Q9, C60, C61	DNP		DNP
C25, C58	4.7µF, 25V,10%, X5R, ROHS	PANASONIC	H1082-00475-25V10-T
C27, C30, C38, C40	220µF, 10V, 20%, ROHS	Sanyo	10TPB220M, RADIAL
C21, C28, C33, C35, C36, C43, C48	B DNP		
D1	10V, 200mA, ZENER, SMD	PHILLIPS	BZX84C10-T
D2	6.8V, 350mW, ROHS	Fairchild	BZX84C6V8-T
L1, L3	1µH, 5.28A, ROHS	Cooper Electronic Tech.	DR73-1R0-R
L2	4.5µH, ROHS	Midcom	40748-LF1



#### TABLE 1. COMPONENT LIST (Continued) **REFERENCE DESIGNATOR** VALUE MANUFACTURER PARTS L5, L6 4µH, 10.3A, ROHS Bitech HM65-H4R0LF QR1, QR4, QL, QH N-CHANNEL, 100V, 7.5A, ROHS Fairchild FDS3672-T Q3, Q1 N-CHANNEL, 30V, 30A, LEAD FREE RENESAS TECHNOLOGY HAT2116H-EL-E Q4, Q2 RENESAS TECHNOLOGY HAT2096H-EL-E N-CHANNEL, LFPAK, 30V, 40A Q5 NPN, D-PAK369C, 100V, 3A, ROHS **ON Semiconductor** MJD31CG RT1 10k, ROHS KOA H2511-01002-1/10W1-T R1 VENKEL H2515-03R32-1W1-T 3.3, 1%, 1W, ROHS, 2512 R2 3.01k, 1%, 1W, ROHS, 2512 KOA H2515-03011-1W1-T R3 10, ROHS KOA H2512-00100-1/8W1-T PANASONIC H2512-002R2-1/8W1-T R4, R5, R44, R45, R46 2.2, ROHS R6 200, ROHS PANASONIC H2511-02000-1/10W1-T R7 75k, ROHS KOA H2512-07502-1/8W1-T R8, R9, R10 18.2, ROHS, 2512 KOA H2515-018R2-1W1-T KOA H2511-01000-1/10W1-T R11 100, ROHS R12 8.06k, ROHS KOA H2511-08061-1/10W1-T PANASONIC R13 18.2. ROHS H2511-01822-1/10W1-T R15 1.27k. ROHS KOA H2511-01271-1/10W1-T R16, R33 1k, ROHS KOA H2511-01001-1/10W1-T R17 97.6k, ROHS KOA H2511-09762-1/10W1-T KOA R18 3.01k, ROHS H2511-03011-1/10W1-T KOA R19, R34, R39 499, ROHS H2511-04990-1/10W1-T R21 4.99k, ROHS PANASONIC H2511-04991-1/10W1-T R23 VISHAY 21.5k, MF H2505-02152-1/16WR1-T R24 2.49k, MF VISHAY H2505-02491-1/16WR1-T R25 10.5k, MF VISHAY H2505-01052-1/16WR1-T R26 12.1k, MF VISHAY H2505-02372-1/16WR1-T R27 7.5k, MF VISHAY H2505-07501-1/16WR1-T VISHAY R28 23.7k, MF H2505-02372-1/16WR1-T H2511-01003-1/10W1-T R29, R32, R36, R48 100k, ROHS R37 301, ROHS KOA H2511-03010-1/10W1-T R49, R38 5.11, ROHS YAGEO H2512-05R11-1/8W1-T VENKEL R47 68.1k, ROHS H2511-06812-1/10W1-T PANASONIC R40 H2511-05762-1/10W1-T 86.6k, ROHS 6,83µH, 25%,10kHz, CUSTOM,ROHS 31660-LF1 Τ1 Midcom Pulse P8205NL T2 CT, SMD, 8P, 500µH, 10A, ROHS HALF BRIDGE DRIVER, ROHS U1 Intersil HIP2101IBZ U2 ISO PHOTOCOUPLER, 4P, ROHS Cal. Eastern Lab PS2801-1-A U3 **IC-PWM CONTROLLER, ROHS** Intersil ISL6740IBZ U4 ROHS National Semi LM431BIM3/NOPB

U5

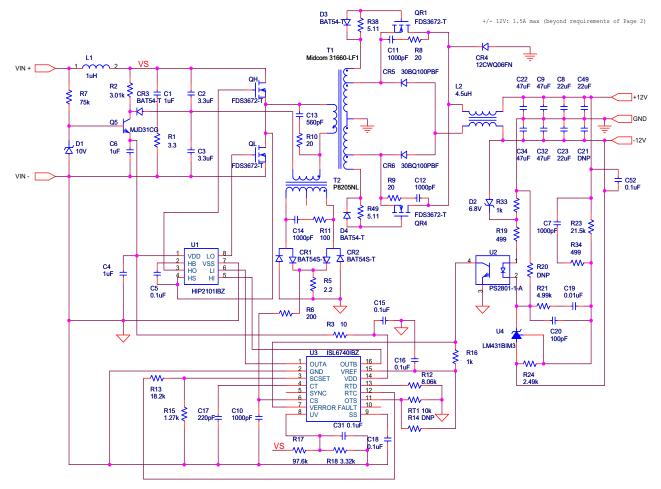


Intersil

DUAL PWM CONTROLLER, ROHS

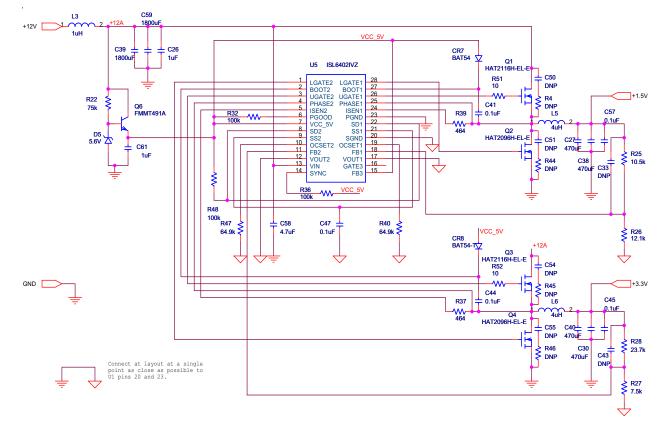
ISL6402IVZ

#### ISL6740EVAL3Z Schematics





### ISL6740EVAL3Z Schematics (Continued)



#### ISL6740EVAL3Z Board Layout

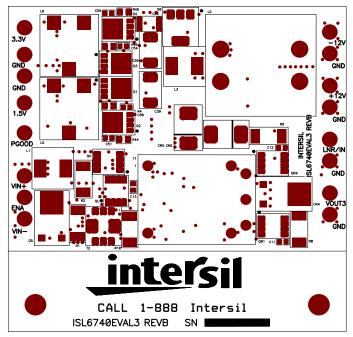


FIGURE 16. TOP LAYER SILKSCREEN



### ISL6740EVAL3Z Board Layout (Continued)

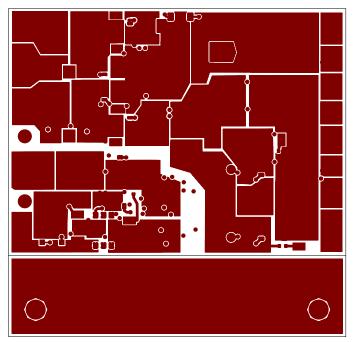
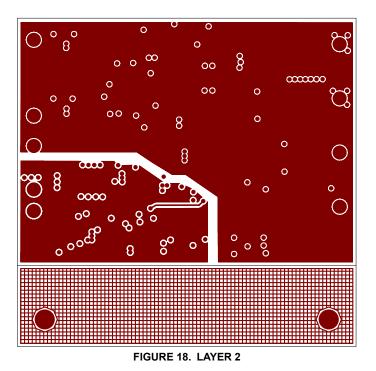


FIGURE 17. TOP LAYER ETCH





### ISL6740EVAL3Z Board Layout (Continued)

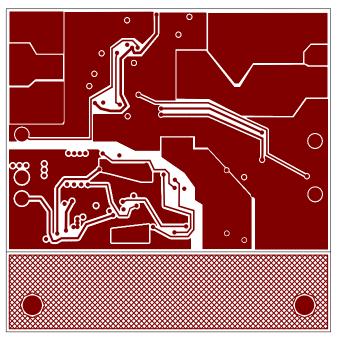


FIGURE 19. LAYER 3

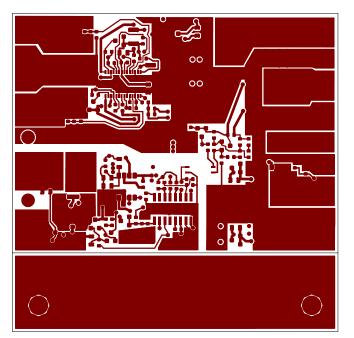


FIGURE 20. BOTTOM LAYER ETCH



### ISL6740EVAL3Z Board Layout (Continued)

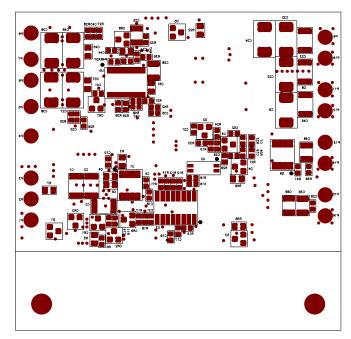


FIGURE 21. BOTTOM LAYER SILKSCREEN



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