

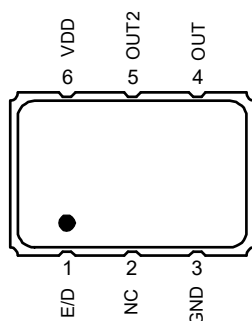
## Description

The Renesas XA devices are ultra-precision crystal oscillators with 750 to 890fs typical phase jitter over 12kHz to 20MHz bandwidth. Available in a wide frequency range from 0.750MHz to 1350MHz, the XA series crystal oscillators utilize a family of proprietary ASICs, with a key focus on noise reduction technologies.

The 3rd order Delta Sigma Modulator reduces noise to the levels that are comparable to traditional Bulk Quartz and SAW oscillators. With short lead-time, low cost, low noise, wide frequency range, excellent ambient performance, the XA devices are an excellent choice over the conventional technologies. The XA devices have stabilities as tight as  $\pm 25$ ppm with extremely quick delivery for both standard and custom frequencies.

## Pin Assignments

**NOTE:** To minimize power supply line noise, a 0.01 $\mu$ F bypass capacitor should be placed between  $V_{DD}$  (Pin 6) and GND (Pin 3).



**Table 1. Pin Description**

| Pin # | Pin Name | Description                         |
|-------|----------|-------------------------------------|
| 1     | E/D      | Enable/Disable <sup>[a][b]</sup>    |
| 2     | NC       | No connect                          |
| 3     | GND      | Connect to ground                   |
| 4     | OUT      | Output                              |
| 5     | OUT2     | Complementary output <sup>[c]</sup> |
| 6     | $V_{DD}$ | Supply voltage                      |

[a] Pulled high internally.

[b] Low = output disabled.

[c] Do not connect for LVCMOS. For XLVCMOS both OUT and OUT2 are ON and in opposite phase.

See [Ordering Information](#) for more details.

## Features

- **Conforms to AEC-Q200**
- Frequency range: 0.750MHz to 1350MHz
- Output types: LVDS, LVPECL, LVCMOS
- Frequency stability:  $\pm 25$ ,  $\pm 50$ , or  $\pm 100$  ppm
- Supply voltage: 2.5V or 3.3V
- Phase jitter (12kHz to 20MHz): 750fs to 890fs typical
- Package options:
  - 3.2 × 2.5 × 1.0 mm
  - 5.0 × 3.2 × 1.2 mm
- Operating temperature: -40°C to +85°C (Grade 3)
  - Frequency stability options:  $\pm 25$ ,  $\pm 50$ , or  $\pm 100$  ppm
- Operating temperature: -40°C to +105°C (Grade 2)
  - Frequency stability options:  $\pm 50$  or  $\pm 100$  ppm

# Contents

|                                         |    |
|-----------------------------------------|----|
| Description . . . . .                   | 1  |
| Pin Assignments . . . . .               | 1  |
| Features . . . . .                      | 1  |
| Absolute Maximum Ratings . . . . .      | 3  |
| ESD Compliance . . . . .                | 3  |
| Mechanical Testing . . . . .            | 3  |
| Solder Reflow Profile . . . . .         | 3  |
| DC Electrical Characteristics . . . . . | 4  |
| AC Electrical Characteristics . . . . . | 6  |
| Output Waveforms – LVDS . . . . .       | 9  |
| Output Waveforms – LVPECL . . . . .     | 9  |
| Output Waveforms – LVCMOS . . . . .     | 10 |
| Package Outline Drawings . . . . .      | 11 |
| Marking Diagrams . . . . .              | 11 |
| Ordering Information . . . . .          | 12 |
| Revision History . . . . .              | 12 |

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the device. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

**Table 2. Absolute Maximum Ratings**

| Item                         | Rating                    |           |                           |           |
|------------------------------|---------------------------|-----------|---------------------------|-----------|
| $V_{DD}$                     | -0.5 to +5.0V             |           |                           |           |
| E/D                          | -0.5V to $V_{DD} + 0.5V$  |           |                           |           |
| OUT                          | -0.5V to $V_{DD} + 0.5V$  |           |                           |           |
| Storage Temperature          | -55°C to 125°C            |           |                           |           |
| Maximum Junction Temperature | 125°C                     |           |                           |           |
| Core Current                 | 65mA maximum              |           |                           |           |
| Theta $J_A$                  | JS6<br>5.0 × 3.2 × 1.2 mm | 89.6 °C/W | JX6<br>3.2 × 2.5 × 1.0 mm | 94.7 °C/W |
| Theta $J_B$                  |                           | 54.3 °C/W |                           | 66.8 °C/W |

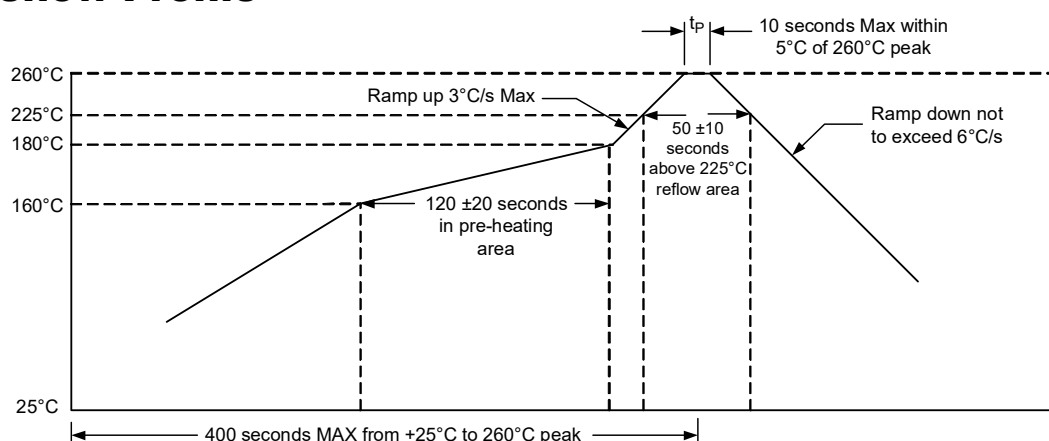
## ESD Compliance

|                        |       |
|------------------------|-------|
| Human Body Model (HBM) | 1000V |
| Machine Model (MM)     | 150V  |

## Mechanical Testing

| Parameter                | Test Method                                                                       |
|--------------------------|-----------------------------------------------------------------------------------|
| Mechanical Shock         | Drop from 75cm to hardwood surface—3 times.                                       |
| Mechanical Vibration     | 10–55Hz, 1.5mm amplitude, 1 minute sweep; 2 hours each in 3 directions (X, Y, Z). |
| High Temperature Burn-in | Under power at 125°C for 2000 hours.                                              |
| Hermetic Seal            | He pressure: 4 ±1kgf/cm <sup>2</sup> 2 hour soak.                                 |

## Solder Reflow Profile



## DC Electrical Characteristics

**Table 3. 3.3V IDD DC Electrical Characteristics**
 $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $-40^{\circ}C$  to  $+105^{\circ}C$ .

| Symbol   | Parameter            | Output Type | Conditions         | Minimum | Typical | Maximum | Units |
|----------|----------------------|-------------|--------------------|---------|---------|---------|-------|
| $I_{DD}$ | Power Supply Current | LVDS        | —                  | —       | —       | 100     | mA    |
|          |                      | LVPECL      | —                  | —       | —       | 120     |       |
|          |                      | LVCMOS      | 0.75MHz to 20MHz.  | —       | —       | 32      |       |
|          |                      |             | 20+MHz to 50MHz.   | —       | —       | 35      |       |
|          |                      |             | 50+MHz to 130MHz.  | —       | —       | 47      |       |
|          |                      |             | 130+MHz to 200MHz. | —       | —       | 55      |       |
|          |                      |             | 200+MHz to 250MHz. | —       | —       | 60      |       |

**Table 4. 2.5V IDD DC Electrical Characteristics**
 $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $-40^{\circ}C$  to  $+105^{\circ}C$ .

| Symbol   | Parameter            | Output Type | Conditions          | Minimum | Typical | Maximum | Units |
|----------|----------------------|-------------|---------------------|---------|---------|---------|-------|
| $I_{DD}$ | Power Supply Current | LVDS        | 0.75MHz to 20MHz.   | —       | —       | 26      | mA    |
|          |                      |             | 20+MHz to 220MHz.   | —       | —       | 34      |       |
|          |                      |             | 220+MHz to 630MHz.  | —       | —       | 44      |       |
|          |                      |             | 630+MHz to 1000MHz. | —       | —       | 65      |       |
|          |                      | LVPECL      | 0.75MHz to 20MHz.   | —       | —       | 33      |       |
|          |                      |             | 20+MHz to 220MHz.   | —       | —       | 41      |       |
|          |                      |             | 220+MHz to 630MHz.  | —       | —       | 63      |       |
|          |                      |             | 630+MHz to 1000MHz. | —       | —       | 72      |       |
|          |                      | LVCMOS      | 0.75MHz to 20MHz.   | —       | —       | 22      |       |
|          |                      |             | 20+MHz to 50MHz.    | —       | —       | 25      |       |
|          |                      |             | 50+MHz to 100MHz.   | —       | —       | 29      |       |
|          |                      |             | 100+MHz to 130MHz.  | —       | —       | 32      |       |
|          |                      |             | 130+MHz to 160MHz.  | —       | —       | 35      |       |
|          |                      |             | 160+MHz to 180MHz.  | —       | —       | 37      |       |

**Table 5. LVDS DC Electrical Characteristics**
 $V_{DD} = 3.3V, 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ . Below are guaranteed for listed standard frequencies.

| Symbol   | Parameter                                          | Conditions              | Minimum       | Typical | Maximum       | Units |
|----------|----------------------------------------------------|-------------------------|---------------|---------|---------------|-------|
| $V_{OD}$ | Differential Output Voltage                        | $V_{DD} = 3.3V \pm 5\%$ | —             | —       | 0.6           | V     |
|          |                                                    | $V_{DD} = 2.5V \pm 5\%$ | —             | —       | 0.4           |       |
| $V_{OS}$ | Output Offset Voltage                              | $V_{DD} = 3.3V \pm 5\%$ | —             | —       | 1.3           |       |
|          |                                                    | $V_{DD} = 2.5V \pm 5\%$ | —             | —       | 1.25          |       |
| $V_{IH}$ | Enable/Disable Input High Voltage (Output enabled) | —                       | $70\% V_{DD}$ | —       | —             |       |
| $V_{IL}$ | Enable/Disable Input Low Voltage (Output disabled) | —                       | —             | —       | $30\% V_{DD}$ |       |

**Table 6. LVPECL DC Electrical Characteristics**
 $V_{DD} = 3.3V, 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ . Below are guaranteed for listed standard frequencies.

| Symbol   | Parameter                                          | Conditions              | Minimum       | Typical | Maximum       | Units |
|----------|----------------------------------------------------|-------------------------|---------------|---------|---------------|-------|
| $V_{OD}$ | Differential Output Voltage                        | $V_{DD} = 3.3V \pm 5\%$ | 2.055         | —       | 2.405         | V     |
|          |                                                    | $V_{DD} = 2.5V \pm 5\%$ | —             | 1.4     | —             |       |
| $V_{OS}$ | Output Offset Voltage                              | $V_{DD} = 3.3V \pm 5\%$ | 1.305         | —       | 1.65          |       |
|          |                                                    | $V_{DD} = 2.5V \pm 5\%$ | —             | 0.68    | —             |       |
| $V_{IH}$ | Enable/Disable Input High Voltage (Output enabled) | —                       | $70\% V_{DD}$ | —       | —             |       |
| $V_{IL}$ | Enable/Disable Input Low Voltage (Output disabled) | —                       | —             | —       | $30\% V_{DD}$ |       |

**Table 7. LVCMOS DC Electrical Characteristics**
 $V_{DD} = 3.3V, 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ . Below are guaranteed for listed standard frequencies.

| Symbol   | Parameter                                          | Conditions              |                    | Minimum       | Typical | Maximum       | Units |
|----------|----------------------------------------------------|-------------------------|--------------------|---------------|---------|---------------|-------|
| $V_{OH}$ | Output High Voltage                                | $V_{DD} = 3.3V \pm 5\%$ | 0.75MHz to 150MHz. | $90\% V_{DD}$ | —       | —             | V     |
|          |                                                    |                         | 150+MHz to 250MHz. | $80\% V_{DD}$ | —       | —             |       |
|          |                                                    | $V_{DD} = 2.5V \pm 5\%$ | 0.75MHz to 160MHz. | $90\% V_{DD}$ | —       | —             |       |
|          |                                                    |                         | 160+MHz to 180MHz. | $80\% V_{DD}$ | —       | —             |       |
| $V_{OL}$ | Output Low Voltage                                 | $V_{DD} = 3.3V \pm 5\%$ | 0.75MHz to 150MHz. | —             | —       | $10\% V_{DD}$ |       |
|          |                                                    |                         | 150+MHz to 250MHz. | —             | —       | $20\% V_{DD}$ |       |
|          |                                                    | $V_{DD} = 2.5V \pm 5\%$ | 0.75MHz to 160MHz. | —             | —       | $10\% V_{DD}$ |       |
|          |                                                    |                         | 160+MHz to 180MHz. | —             | —       | $20\% V_{DD}$ |       |
| $V_{IH}$ | Enable/Disable Input High Voltage (Output enabled) | —                       | —                  | $70\% V_{DD}$ | —       | —             |       |
| $V_{IL}$ | Enable/Disable Input Low Voltage (Output disabled) | —                       | —                  | —             | —       | $30\% V_{DD}$ |       |

# AC Electrical Characteristics

**Table 8. 3.3V AC Electrical Characteristics**

$V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

| Symbol    | Parameter                   | Test Condition                                                  |                          | Minimum  | Typical | Maximum   | Units    |
|-----------|-----------------------------|-----------------------------------------------------------------|--------------------------|----------|---------|-----------|----------|
| F         | Output Frequency Range      | LVDS.                                                           |                          | 0.75     | —       | 1350      | MHz      |
|           |                             | LVPECL.                                                         |                          | 0.75     | —       | 1350      |          |
|           |                             | LVCMOS.                                                         |                          | 0.75     | —       | 250       |          |
|           | Frequency Stability         | Temperature = $-40^\circ C$ to $+85^\circ C$ .                  |                          | $\pm 25$ | —       | $\pm 100$ | ppm      |
|           |                             | Temperature = $-40^\circ C$ to $+105^\circ C$ .                 |                          | $\pm 50$ | —       | $\pm 100$ | ppm      |
|           | Aging (1st year)            | $T_A = 25^\circ C$ .                                            |                          | —        | —       | $\pm 3$   | ppm      |
|           | Aging (10 years)            | $T_A = 25^\circ C$ .                                            |                          | —        | —       | $\pm 10$  | ppm      |
|           | Output Load                 | LVDS.                                                           | Differential.            | —        | 100     | —         | $\Omega$ |
|           |                             | LVPECL.                                                         | $V_{DD} - 2.0V$ .        | —        | 50      | —         |          |
|           |                             | LVCMOS.                                                         | To GND.                  | —        | 15      | —         | pF       |
| $T_{ST}$  | Start-up Time               | Output valid time after $V_{DD}$ meets minimum specified level. |                          | —        | —       | 10        | ms       |
| $t_R$     | Output Rise Time            | LVDS.                                                           | 20% to 80% $V_{pp}$ .    | —        | —       | 400       | ps       |
|           |                             | LVPECL.                                                         |                          | —        | —       | 400       |          |
|           |                             | LVCMOS.                                                         | 10% to 90% $V_{DD}$ .    | —        | —       | 3         | ns       |
| $t_F$     | Output Fall Time            | LVDS.                                                           | 80% to 20% $V_{pp}$ .    | —        | —       | 400       | ps       |
|           |                             | LVPECL.                                                         |                          | —        | —       | 400       |          |
|           |                             | LVCMOS.                                                         | 90% to 10% $V_{DD}$ .    | —        | —       | 3         | ns       |
| $O_{DC}$  | Output Clock Duty Cycle     | LVDS.                                                           |                          | 45       | —       | 55        | %        |
|           |                             | LVPECL.                                                         |                          | 45       | —       | 55        |          |
|           |                             | LVCMOS.                                                         | $F_{OUT} \leq 62.5MHz$ . | 45       | —       | 55        |          |
|           |                             |                                                                 | $F_{OUT} \geq 62.5MHz$ . | 40       | —       | 60        |          |
| $T_{OE}$  | Output Enable/ Disable Time | —                                                               |                          | —        | —       | 100       | ns       |
| $J_{PER}$ | Period Jitter, RMS          | LVDS.                                                           |                          | —        | 3       | —         | ps       |
|           |                             | LVPECL.                                                         |                          | —        | 5.8     | —         |          |
|           |                             | LVCMOS.                                                         | $F_{OUT} = 125MHz$ .     | —        | 5       | —         |          |
| $R_J$     | Random Jitter               | LVDS.                                                           |                          | —        | 1.3     | —         | ps       |
|           |                             | LVPECL.                                                         |                          | —        | 1.29    | —         |          |
|           |                             | LVCMOS.                                                         | $F_{OUT} = 125MHz$ .     | —        | 0.6     | —         |          |
| $D_J$     | Deterministic Jitter        | LVDS.                                                           |                          | —        | 5.8     | —         | ps       |
|           |                             | LVPECL.                                                         |                          | —        | 9.3     | —         |          |
|           |                             | LVCMOS.                                                         | $F_{OUT} = 125MHz$ .     | —        | 10      | —         |          |

**Table 8. 3.3V AC Electrical Characteristics (Cont.)**
 $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

| Symbol       | Parameter                  | Test Condition               | Minimum | Typical | Maximum | Units |
|--------------|----------------------------|------------------------------|---------|---------|---------|-------|
| $T_J$        | Total Jitter               | LVDS.                        | —       | 23.6    | —       | ps    |
|              |                            | LVPECL.                      | —       | 27.7    | —       |       |
|              |                            | LVC MOS. $F_{OUT} = 125MHz.$ | —       | 19      | —       |       |
| $f_{JITTER}$ | Phase Jitter (12kHz–20MHz) | LVDS.                        | —       | 890     | —       | fs    |
|              |                            | LVPECL.                      | —       | 860     | —       |       |
|              |                            | LVC MOS. $F_{OUT} = 125MHz.$ | —       | 750     | —       |       |

**Table 9. 2.5V AC Electrical Characteristics**
 $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

| Symbol   | Parameter                   | Test Condition                                                  | Minimum  | Typical | Maximum   | Units    |
|----------|-----------------------------|-----------------------------------------------------------------|----------|---------|-----------|----------|
| F        | Output Frequency Range      | LVDS.                                                           | 0.75     | —       | 1000      | MHz      |
|          |                             | LVPECL.                                                         | 0.75     | —       | 1000      |          |
|          |                             | LVC MOS.                                                        | 0.75     | —       | 180       |          |
|          | Frequency Stability         | Temperature = $-40^\circ C$ to $+85^\circ C$ .                  | $\pm 25$ | —       | $\pm 100$ | ppm      |
|          |                             | Temperature = $-40^\circ C$ to $+105^\circ C$ .                 | $\pm 50$ | —       | $\pm 100$ | ppm      |
|          | Aging (1st year)            | $T_A = 25^\circ C$ .                                            | —        | —       | $\pm 3$   | ppm      |
|          | Aging (10 years)            | $T_A = 25^\circ C$ .                                            | —        | —       | $\pm 10$  | ppm      |
|          | Output Load                 | LVDS. Differential.                                             | —        | 100     | —         | $\Omega$ |
|          |                             | LVPECL. $V_{DD} - 2.0V$ .                                       | —        | 50      | —         |          |
|          |                             | LVC MOS. To GND.                                                | —        | 15      | —         | pF       |
| $T_{ST}$ | Start-up Time               | Output valid time after $V_{DD}$ meets minimum specified level. | —        | —       | 10        | ms       |
| $t_R$    | Output Rise Time            | LVDS. 20% to 80% $V_{pp}$ .                                     | —        | —       | 400       | ps       |
|          |                             | LVPECL.                                                         | —        | —       | 400       |          |
|          |                             | LVC MOS. 10% to 90% $V_{DD}$ .                                  | —        | —       | 3.5       | ns       |
| $t_F$    | Output Fall Time            | LVDS. 80% to 20% $V_{pp}$ .                                     | —        | —       | 400       | ps       |
|          |                             | LVPECL.                                                         | —        | —       | 400       |          |
|          |                             | LVC MOS. 90% to 10% $V_{DD}$ .                                  | —        | —       | 3         | ns       |
| $O_{DC}$ | Output Clock Duty Cycle     | LVDS.                                                           | 45       | —       | 55        | %        |
|          |                             | LVPECL.                                                         | 45       | —       | 55        |          |
|          |                             | LVC MOS.                                                        | 45       | —       | 55        |          |
| $T_{OE}$ | Output Enable/ Disable Time | —                                                               | —        | —       | 100       | ns       |

**Table 9. 2.5V AC Electrical Characteristics (Cont.)**
 $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

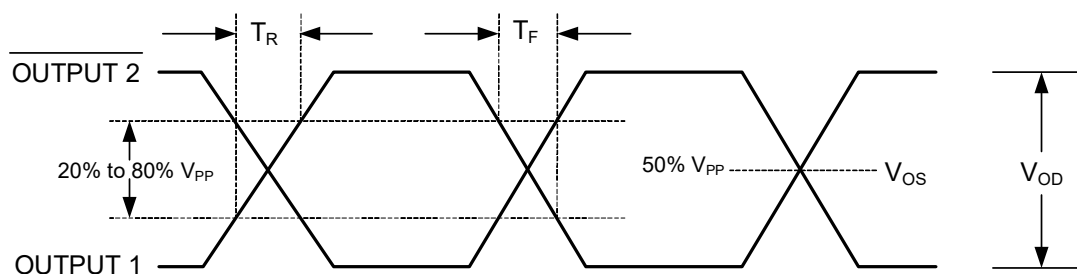
| Symbol       | Parameter                  | Test Condition               | Minimum | Typical | Maximum | Units |
|--------------|----------------------------|------------------------------|---------|---------|---------|-------|
| $J_{PER}$    | Period Jitter, RMS         | LVDS.                        | —       | 4       | —       | ps    |
|              |                            | LVPECL.                      | —       | 5.12    | —       |       |
|              |                            | LVC MOS. $F_{OUT} = 125MHz.$ | —       | 3.3     | —       |       |
| $R_J$        | Random Jitter              | LVDS.                        | —       | 1.4     | —       | ps    |
|              |                            | LVPECL.                      | —       | 1.36    | —       |       |
|              |                            | LVC MOS. $F_{OUT} = 125MHz.$ | —       | 1.3     | —       |       |
| $D_J$        | Deterministic Jitter       | LVDS.                        | —       | 9.2     | —       | ps    |
|              |                            | LVPECL.                      | —       | 10      | —       |       |
|              |                            | LVC MOS. $F_{OUT} = 125MHz.$ | —       | 6.7     | —       |       |
| $T_J$        | Total Jitter               | LVDS.                        | —       | 29.2    | —       | ps    |
|              |                            | LVPECL.                      | —       | 29.3    | —       |       |
|              |                            | LVC MOS. $F_{OUT} = 125MHz.$ | —       | 25.6    | —       |       |
| $f_{JITTER}$ | Phase Jitter (12kHz–20MHz) | LVDS.                        | —       | 1040    | —       | fs    |
|              |                            | LVPECL.                      | —       | 1200    | —       |       |
|              |                            | LVC MOS. $F_{OUT} = 125MHz.$ | —       | 850     | —       |       |

Notes for all AC Electrical Characteristics tables:

<sup>1</sup> All jitter values provided at 156.25MHz, unless noted otherwise.

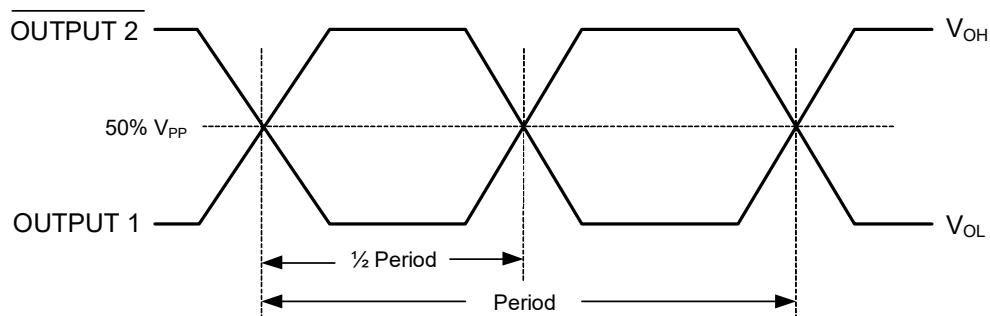
## Output Waveforms – LVDS

Output Levels/Rise Time/Fall Time Measurements



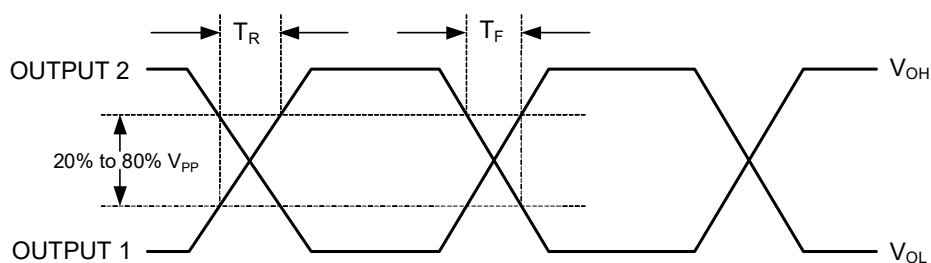
Oscillator Symmetry

Ideally, Symmetry should be 50/50 for  $\frac{1}{2}$  period –Other expressions are 45/55 or 55/45

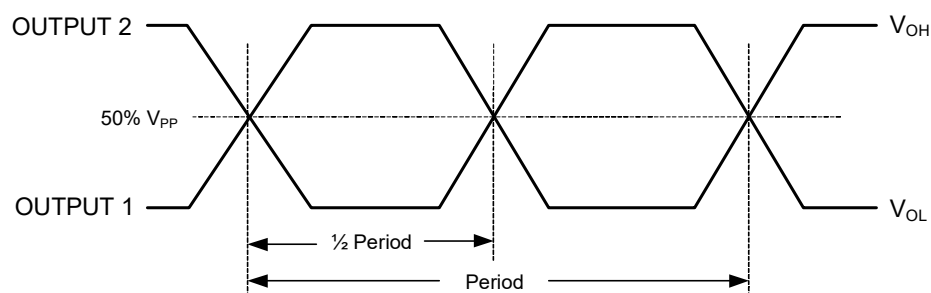


## Output Waveforms – LVPECL

Rise Time/Fall Time Measurements

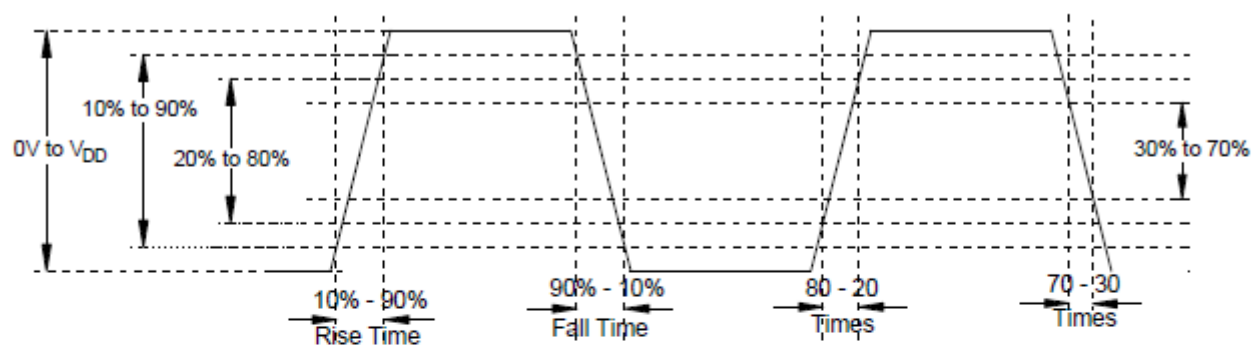


Oscillator Symmetry

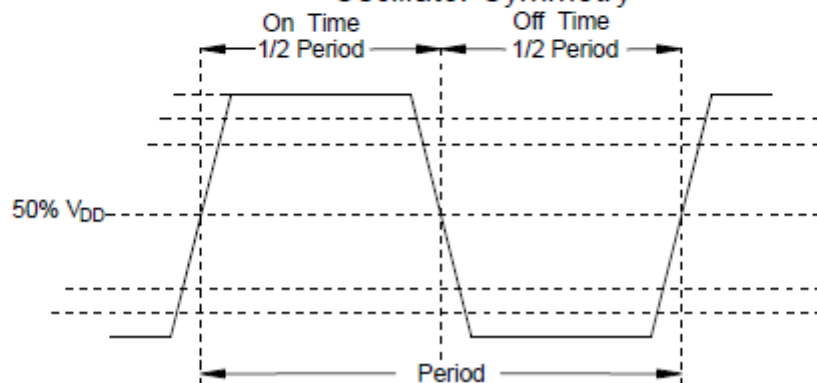


## Output Waveforms – LVCMOS

Rise Time / Fall Time Measurements



Oscillator Symmetry

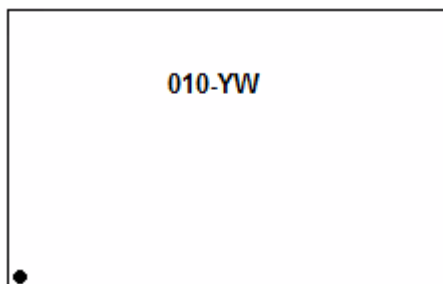


## Package Outline Drawings

The package outline drawings (JS6, JX6) are appended at the end of this document. The package information is the most current data available.

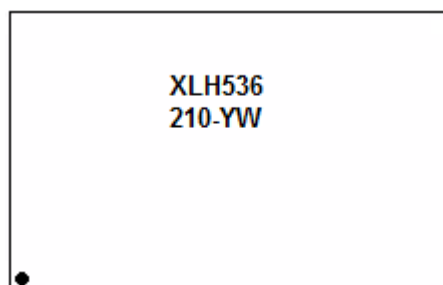
## Marking Diagrams

JX6 3.2 × 2.5 mm Package Option (example based on XLH320010.000000I)



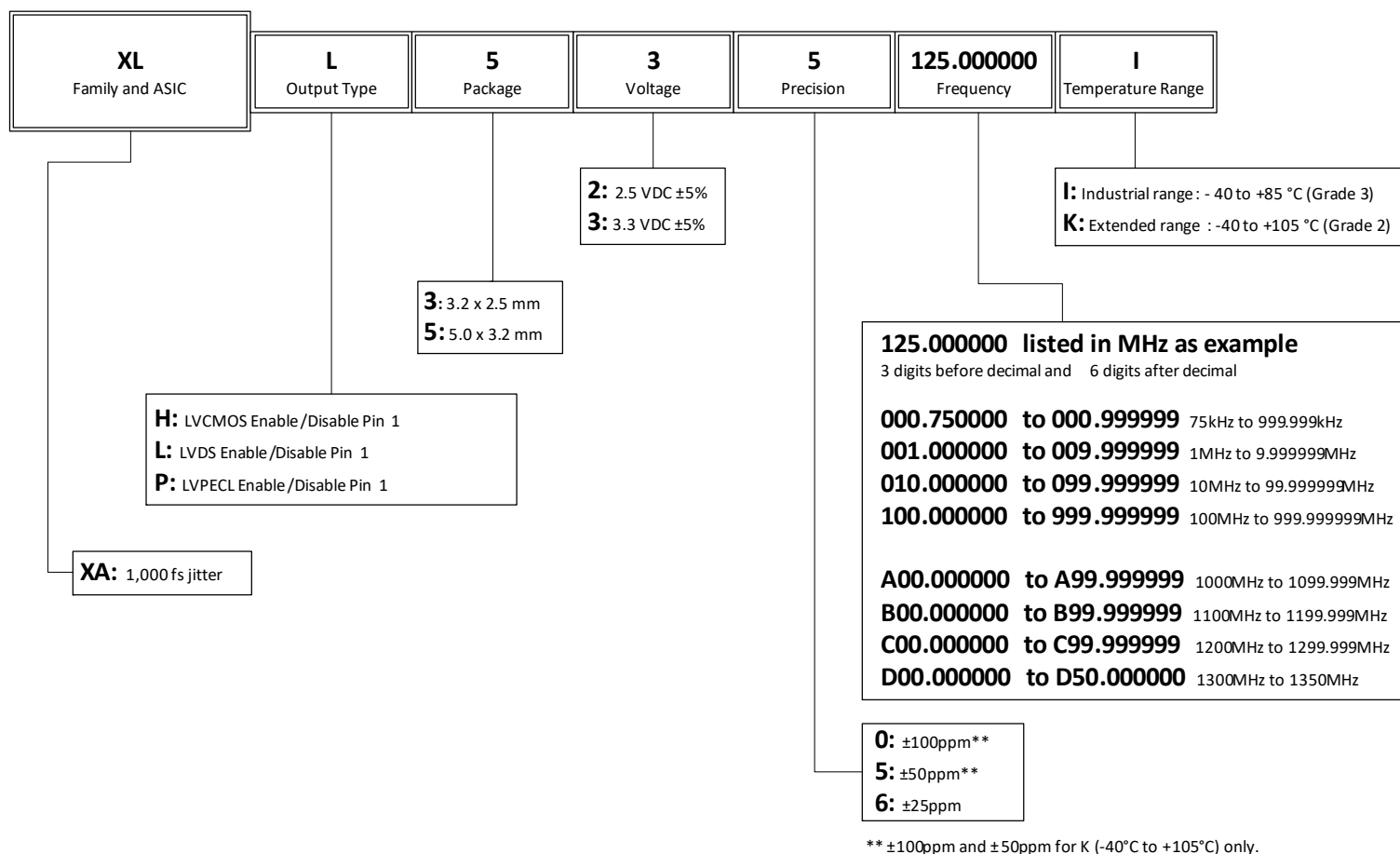
- Line 1:
  - “010” denotes last three digits to the left of the decimal point as shown in the above example. This number will vary depending upon the frequency value selected in the orderable part number.
  - “YW” denotes the last digit of the year and work week the part was assembled.

JS6 5.0 × 3.2 mm Package Option (example based on XLH536210.380000I)



- Line 1:
  - “XL” = family; “H” = output type; “5” = package size; “3” = voltage; “6” = precision level. This number will vary depending upon the output type, voltage, and precision values selected in the orderable part number.
- Line 2:
  - “210” denotes last three digits to the left of the decimal point as shown in the above example. This number will vary depending upon the frequency value selected in the orderable part number.
  - “YW” denotes the last digit of the year and work week the part was assembled.

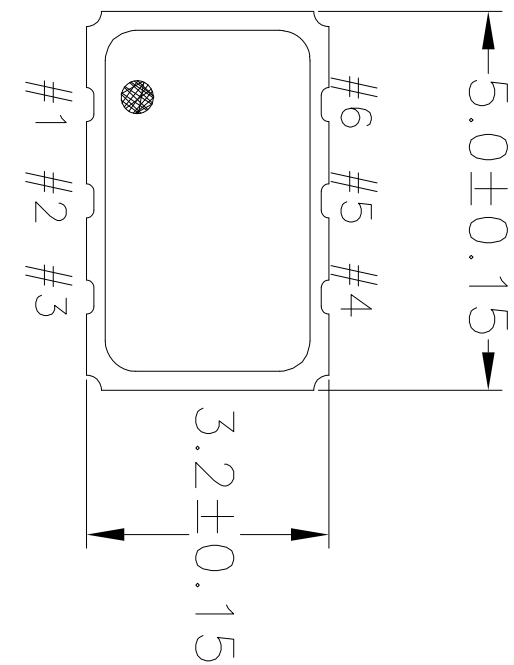
# Ordering Information



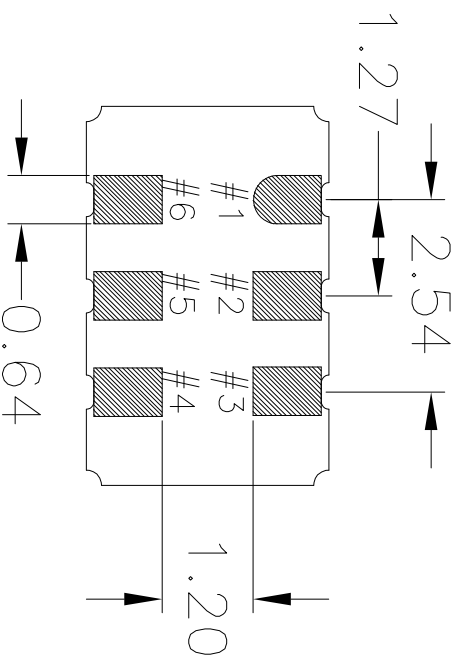
# Revision History

| Revision Date    | Description of Change                                                                                                                                                                                                                                 |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| January 15, 2021 | <ul style="list-style-type: none"> <li>Removed 4-pin package description table, figure, and package drawing references.</li> <li>Added footnote for pin 5 in Table 1.</li> <li>Added footnote under "Output Type" in Ordering Information.</li> </ul> |
| January 13, 2021 | Added Marking Diagrams section and updated Package Outline Drawings links.                                                                                                                                                                            |
| May 24, 2018     | Updated LVCMOS Output Clock Duty Cycle, FOOT test condition.                                                                                                                                                                                          |
| April 27, 2018   | Initial release.                                                                                                                                                                                                                                      |

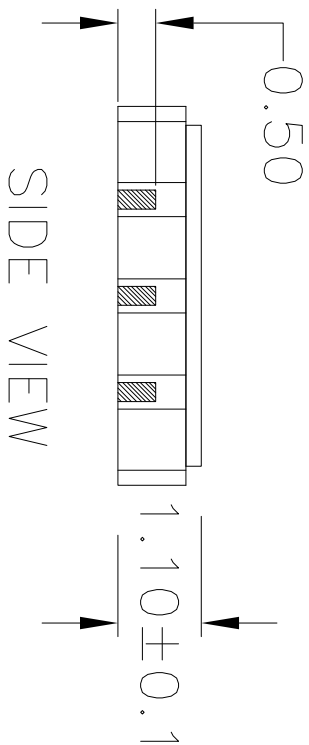
| REVISIONS |                        |          |          |
|-----------|------------------------|----------|----------|
| REV       | DESCRIPTION            | DATE     | APPROVED |
| 00        | INITIAL RELEASE        | 04/2/12  | DP       |
| 01        | ADDED LID IN TOP VIEW  | 07/12/12 | KS       |
| 02        | UPDATED LID TOLERANCES | 12/03/12 | KS       |
| 03        | UPDATE PACKAGE DRAWING | 8/8/14   | JHUA     |



TOP VIEW



BOTTOM VIEW



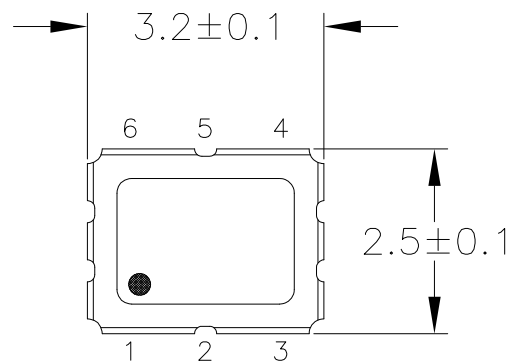
SIDE VIEW

NOTES:  
1. ALL DIMENSIONS IN MM.

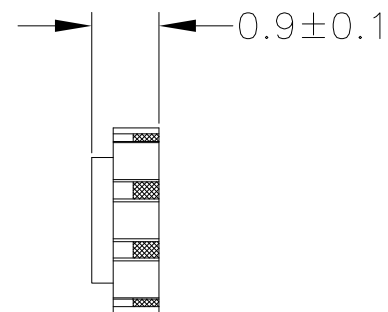
|                                |             |                                                                                                                                                 |  |
|--------------------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------|--|
| TOLERANCES<br>UNLESS SPECIFIED |             | 6024 Silver Creek Valley Rd<br>San Jose, CA 95138<br>PHONE: (408) 727-6116<br>FAX: (408) 492-8674                                               |  |
| DECIMAL                        | ANGULAR     |  <b>IDT™</b><br><a href="http://www.IDT.com">www.IDT.com</a> |  |
| XX±                            | ±           |                                                                                                                                                 |  |
| XXX±                           |             |                                                                                                                                                 |  |
| XXXX±                          |             |                                                                                                                                                 |  |
| APPROVALS                      | DATE        | TITLE JS6 PACKAGE OUTLINE                                                                                                                       |  |
| DRAWN <i>02AC</i>              | 04/2/12     | 5.0 x 3.2 mm BODY                                                                                                                               |  |
| CHECKED                        |             | 1.1 mm Thick                                                                                                                                    |  |
| SIZE                           | DRAWING No. | REV                                                                                                                                             |  |
| C                              | PSC-4411    | 03                                                                                                                                              |  |
| DO NOT SCALE DRAWING           |             | SHEET 1 OF 2                                                                                                                                    |  |



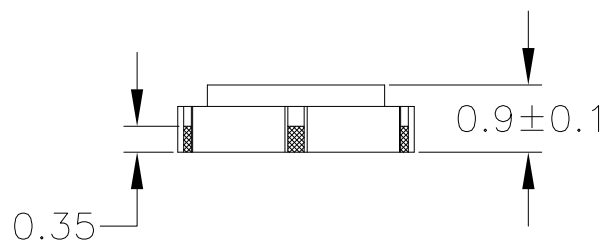
| REVISIONS                              |                 |              |        |
|----------------------------------------|-----------------|--------------|--------|
| REV                                    | DESCRIPTION     | DATE CREATED | AUTHOR |
| 00                                     | INITIAL RELEASE | 8/11/14      | J.HUA  |
| 01                                     | ADD PITCH       | 11/17/16     | J.HUA  |
| REFER TO DCP FOR OFFICIAL RELEASE DATE |                 |              |        |



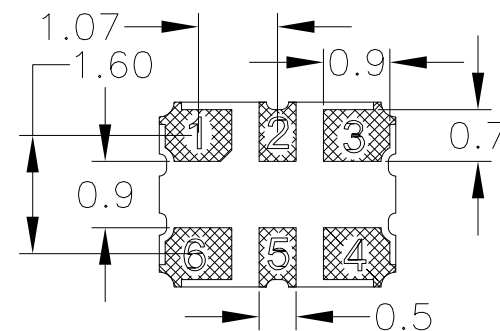
TOP VIEW



END VIEW



SIDE VIEW



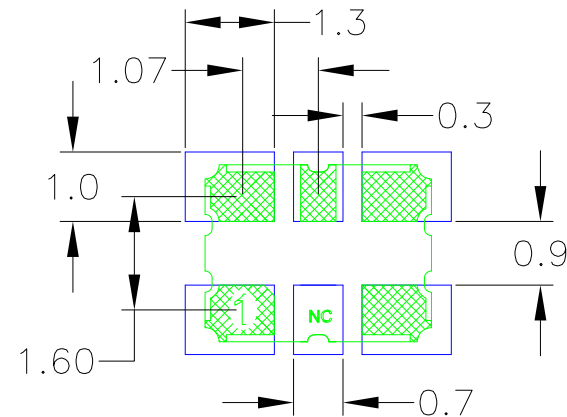
BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS IN MM.

|                                |             |                                                                                                                                                                                                                                                        |  |
|--------------------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| TOLERANCES<br>UNLESS SPECIFIED |             |  <b>IDT™</b><br>6024 Silver Creek Valley Rd<br>San Jose, CA 95138<br>PHONE: (408) 727-6116<br>FAX: (408) 492-8674<br><a href="http://www.IDT.com">www.IDT.com</a> |  |
| DECIMAL                        | ANGULAR     |                                                                                                                                                                                                                                                        |  |
| XX±                            | ±           |                                                                                                                                                                                                                                                        |  |
| XXX±                           |             |                                                                                                                                                                                                                                                        |  |
| XXXX±                          |             |                                                                                                                                                                                                                                                        |  |
|                                |             | TITLE JX6 PACKAGE OUTLINE<br>3.2 x 2.5 mm BODY<br>0.9 mm Thick                                                                                                                                                                                         |  |
| SIZE                           | DRAWING No. | REV                                                                                                                                                                                                                                                    |  |
| C                              | PSC-4412    | 01                                                                                                                                                                                                                                                     |  |
| DO NOT SCALE DRAWING           |             | SHEET 1 OF 2                                                                                                                                                                                                                                           |  |

| REVISIONS                              |                 |              |        |
|----------------------------------------|-----------------|--------------|--------|
| REV                                    | DESCRIPTION     | DATE CREATED | AUTHOR |
| 00                                     | INITIAL RELEASE | 8/11/14      | J.HUA  |
| 01                                     | ADD PITCH       | 11/17/16     | J.HUA  |
| REFER TO DCP FOR OFFICIAL RELEASE DATE |                 |              |        |



## RECOMMENDED LAND PATTERN DIMENSION

### NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

|                                |             |                                                                                                                                                                                                               |  |
|--------------------------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| TOLERANCES<br>UNLESS SPECIFIED |             |  6024 Silver Creek Valley Rd<br>San Jose, CA 95138<br>PHONE: (408) 727-6116<br>FAX: (408) 492-8674<br><b>www.IDT.com</b> |  |
| DECIMAL                        | ANGULAR     |                                                                                                                                                                                                               |  |
| XX±                            | ±           |                                                                                                                                                                                                               |  |
| XXX±                           |             |                                                                                                                                                                                                               |  |
| XXXX±                          |             |                                                                                                                                                                                                               |  |
|                                |             | TITLE JX6 PACKAGE OUTLINE<br>3.2 x 2.5 mm BODY<br>0.9 mm Thick                                                                                                                                                |  |
| SIZE                           | DRAWING No. | REV                                                                                                                                                                                                           |  |
| C                              | PSC-4412    | 01                                                                                                                                                                                                            |  |
| DO NOT SCALE DRAWING           |             | SHEET 2 OF 2                                                                                                                                                                                                  |  |

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

## Renesas Electronics:

|                                          |                                          |                                          |                                          |                                          |
|------------------------------------------|------------------------------------------|------------------------------------------|------------------------------------------|------------------------------------------|
| <a href="#"><u>XAL525780.000000I</u></a> | <a href="#"><u>XAL535033.000000K</u></a> | <a href="#"><u>XAL335250.000000K</u></a> | <a href="#"><u>XAL335080.000000K</u></a> | <a href="#"><u>XAL335500.000000K</u></a> |
| <a href="#"><u>XAH335006.005285K</u></a> | <a href="#"><u>XAH335032.000000K</u></a> | <a href="#"><u>XAL325500.000000K</u></a> | <a href="#"><u>XAL335133.000000K</u></a> | <a href="#"><u>XAL335135.000000K</u></a> |
| <a href="#"><u>XAL335266.000000K</u></a> | <a href="#"><u>XAL335300.000000K</u></a> | <a href="#"><u>XA50-4DEVALZ</u></a>      |                                          |                                          |