

# SLG59H1341C

A Reverse Blocking 70 mΩ, 1.3 A nFET  
Load Switch in 1.46 mm<sup>2</sup> WLCSP

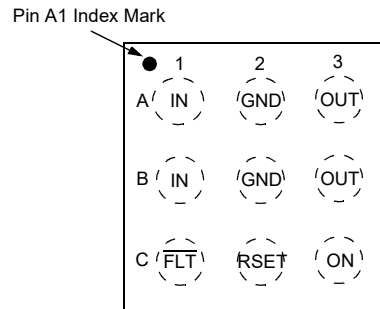
## General Description

Operating from a 2.5 V to 5.5 V power supply, the SLG59H1341C is a self-powered, high-performance, 70 mΩ nFET load switch designed for high-side power-rail applications up to 1.3 A. When ON, internal reverse-current protection will quickly open the switch in the event of a reverse-voltage condition is detected (a  $V_{OUT} > V_{IN} + 50$  mV condition opens the switch). When OFF, an internal back-to-back reverse-current blocking circuit prevents reverse path leakage current.

## Features

- Integrated 1.3 A Continuous  $I_{DS}$  nFET Load Switch
- Integrated Low  $R_{DS(ON)}$  nFET switch: 70 mΩ
- Input Voltage: 2.5 V to 5.5 V
- Operating Temperature: -40 °C to 85 °C
- Resistor-adjustable Active Current Limit
  - ±10% accuracy for 0.2 A to 1.5 A Current Limit Thresholds
  - ±15% accuracy for 0.15 A to 0.2 A Current Limit Thresholds
- Open Drain FLT Signaling
- Output OVP Protection
- Absolute  $V_{OUT}$  maximum voltage rating: 28 V<sub>DC</sub>
- Over-temperature Protection
- Under-Voltage Lockout
- True Reverse-Current Blocking
- Low  $\theta_{JA}$ , 9-pin 1.21 mm x 1.21 mm, 0.4 mm pitch 9L WLCSP Packaging
  - Pb-Free / Halogen-Free / RoHS compliant

## Pin Configuration

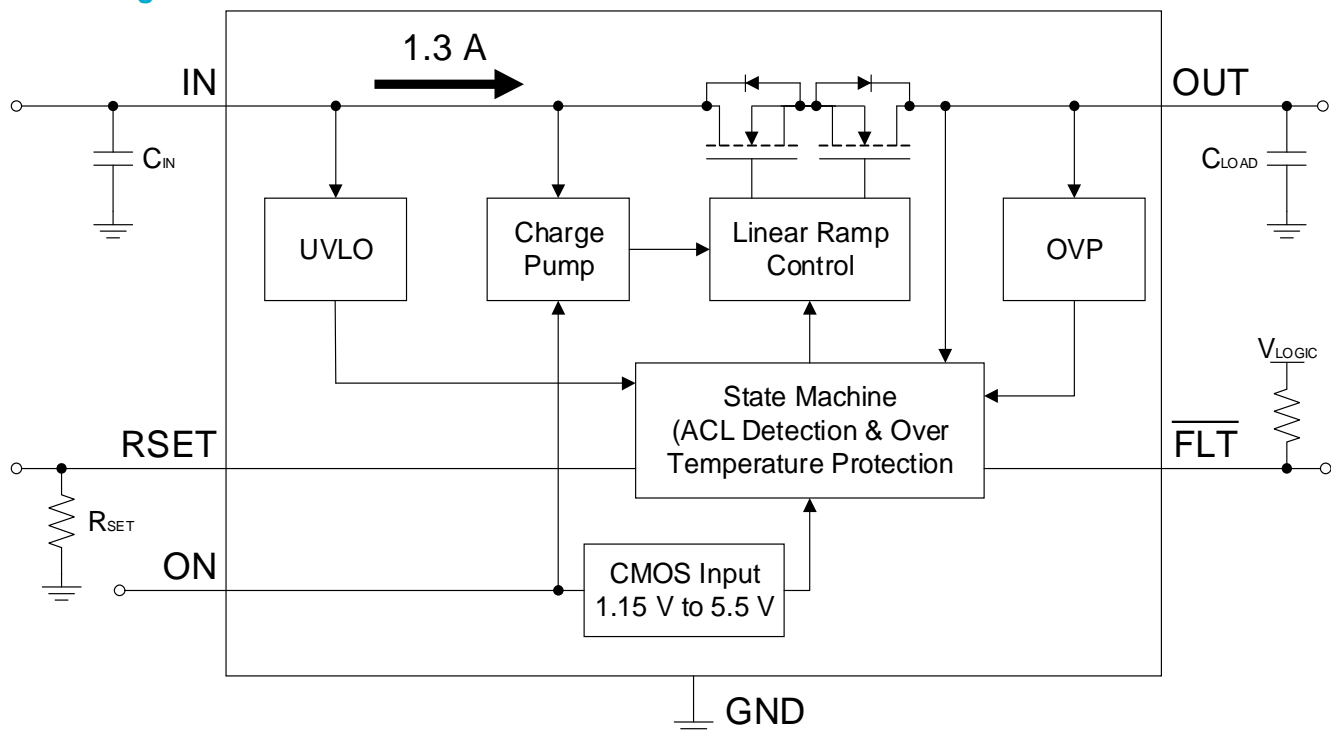


**9L WLCSP**  
(Laser Marking View)

## Applications

- Fast Turn On/Off power rail switching
- Frequent wake & sleep power cycle
- Mobile devices and portable devices

## Block Diagram



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### Pin Description

Pin #	Pin Name	Type	Pin Description
A1, B1	IN	MOSFET	Input terminal connection of the n-channel MOSFET. Capacitors used at IN should be rated at a voltage higher than maximum input voltage ever present.
A2, B2	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.
A3, B3	OUT	MOSFET	Output terminal connection of the n-channel MOSFET. Capacitors used at OUT should be rated at a voltage higher than maximum output voltage ever present.
C1	$\overline{\text{FLT}}$	Output	An open drain output, $\overline{\text{FLT}}$ is asserted within $T_{\overline{\text{FLT}}_{\text{LOW}}}$ when a current-limit condition is detected.
C2	RSET	Input	A 1%-tolerance, metal-film resistor between 6.49 kΩ and 680 Ω sets the SLG59H1341C's active current limit. A 6.49 kΩ resistor sets the SLG59H1341C's active current limit to 0.16 A and a 680 Ω resistor sets the active current limit to 1.62 A.
C3	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59H1341C. ON is an asserted HIGH, level-sensitive CMOS input with $\text{ON\_V}_{\text{IL}} < 0.65 \text{ V}$ and $\text{ON\_V}_{\text{IH}} > 1.15 \text{ V}$ . While there is an internal pull-down circuit to GND (~14 MΩ), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.

### Ordering Information

Part Number	Type	Production Flow
SLG59H1341C	WLCSP 9L	Industrial, -40 °C to 85 °C
SLG59H1341CTR	WLCSP 9L (Tape and Reel)	Industrial, -40 °C to 85 °C

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### Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V <sub>IN</sub>	Load Switch Input Voltage		--	--	6	V
V <sub>OUT</sub> to V <sub>IN</sub>	Load Switch Output Voltage to V <sub>IN</sub>	Continuous	-0.3	--	28	V
V <sub>OUT</sub> to GND	Load Switch Output Voltage to GND	Continuous	-0.3	--	28	V
ON, $\overline{\text{FLT}}$ , RSET to GND	ON, $\overline{\text{FLT}}$ , and RSET Pin Voltages to GND		-0.3	--	V <sub>IN</sub>	V
T <sub>S</sub>	Storage Temperature		-65	--	140	°C
ESD <sub>HBM</sub>	ESD Protection	Human Body Model	2000	--	--	V
ESD <sub>CDM</sub>	ESD Protection	Charged Device Model	2500	--	--	V
ESD <sub>SYS</sub>	IEC 61000-4-2 System ESD	Air Gap (V <sub>IN</sub> , V <sub>OUT</sub> , V <sub>ON</sub> to GND)	15	--	--	kV
		Contact (V <sub>IN</sub> , V <sub>OUT</sub> , V <sub>ON</sub> to GND)	8	--	--	kV
MSL	Moisture Sensitivity Level		1			
θ <sub>JA</sub>	Package Thermal Resistance, Junction-to-Ambient	1.21 x 1.21 mm 9L WLCSP; Determined using a 0.5 in <sup>2</sup> , 1 oz. copper pad under each IN and OUT terminal and FR4 pcb material.	--	76	--	°C/W
MOSFET IDS <sub>PK</sub>	Peak Current from IN to OUT	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	2	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Electrical Characteristics

T<sub>A</sub> = -40 °C to 85 °C. Typical values are at V<sub>IN</sub> = 5 V and T<sub>A</sub> = 25 °C unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V <sub>IN</sub>	Load Switch Input Voltage	-40 °C to 85 °C	2.5	--	5.5	V
V <sub>IN(UVLO)</sub>	V <sub>IN</sub> Undervoltage Lockout Threshold	V <sub>IN</sub> ↑	--	2.4	--	V
		V <sub>IN</sub> ↓	--	2.2	--	V
V <sub>OUT(OVP)</sub>	V <sub>OUT</sub> Overvoltage Lockout Threshold	V <sub>OUT</sub> ↑	5.5	5.8	6	V
		V <sub>OUT</sub> ↓	--	5.5	--	V
V <sub>OUT(OVP)_HYS</sub>	V <sub>OUT</sub> Overvoltage Lockout Hysteresis	V <sub>OUT</sub> ↓	--	300	--	mV
t <sub>OVP</sub>	OVP Response Time	V <sub>OUT</sub> step from 5.5 V to 6 V; I <sub>DS</sub> = 0.5 A, C <sub>LOAD</sub> = 1 μF; T <sub>A</sub> = 25 °C	1	--	4	μs
I <sub>IN</sub>	Load Switch Current (Pin A1, B1)	When OFF, No load; V <sub>OUT</sub> = Open	--	1	2	μA
		When ON, No load	--	65	100	μA
I <sub>ON_LKG</sub>	ON Pin Input Leakage	V <sub>ON</sub> = 0 V to 5 V	--	--	1	μA
RDS <sub>ON</sub>	ON Resistance	V <sub>IN</sub> = 3.7 V, I <sub>DS</sub> = 1 A	--	75	105	mΩ
		V <sub>IN</sub> = 5 V, I <sub>DS</sub> = 1 A	--	70	100	mΩ
		V <sub>IN</sub> = 5 V, I <sub>DS</sub> = 1.5 A	--	70	--	mΩ
MOSFET IDS	Current from IN to OUT	Continuous	--	--	1.3	A

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## Electrical Characteristics (continued)

T<sub>A</sub> = -40 °C to 85 °C. Typical values are at V<sub>IN</sub> = 5 V and T<sub>A</sub> = 25 °C unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I <sub>LIMIT</sub>	Active Current Limit, I <sub>ACL</sub>	V <sub>IN</sub> = 5 V; R <sub>SET</sub> = 6.49 kΩ; C <sub>IN</sub> = 30 μF; C <sub>RSET</sub> = 10 pF; C <sub>LOAD</sub> = 0.1 μF; V <sub>OUT</sub> = 1.68 V to 5 V	0.136	0.160	0.184	A
		V <sub>IN</sub> = 5 V; R <sub>SET</sub> = 2.1 kΩ; C <sub>IN</sub> = 30 μF; C <sub>RSET</sub> = 10 pF; C <sub>LOAD</sub> = 1 μF; V <sub>OUT</sub> = 1.68 V to 5 V	0.46	0.51	0.56	A
		V <sub>IN</sub> = 5 V; R <sub>SET</sub> = 1.07 kΩ; C <sub>IN</sub> = 30 μF; C <sub>RSET</sub> = 10 pF; C <sub>LOAD</sub> = 4.4 μF; V <sub>OUT</sub> = 1.68 V to 5 V	0.92	1.02	1.12	A
T <sub>ACL</sub>	Active Current Limit Response Time	I <sub>DS</sub> > I <sub>ACL</sub> ; V <sub>OUT</sub> ≤ V <sub>IN</sub>	--	7	--	μs
T <sub>HACL</sub>	Hard Active Current Limit Response Time	I <sub>DS</sub> > I <sub>ACL</sub> ; V <sub>OUT</sub> = 0 V	--	6	--	μs
I <sub>FET_OFF</sub>	MOSFET OFF Leakage Current	ON = LOW; V <sub>OUT</sub> = 0 V, V <sub>IN</sub> = 5.5 V	--	0.1	4	μA
V <sub>RVD_T</sub>	Reverse-voltage Detect Threshold Voltage	V <sub>OUT</sub> - V <sub>IN</sub> ; ON = HIGH	--	50	--	mV
T <sub>RVD_T</sub>	Reverse-voltage Detect Threshold Response Time	V <sub>IN</sub> = 5 V; ON = HIGH	--	2	--	μs
V <sub>RVD_R</sub>	Reverse-voltage Detect Release Threshold Voltage	V <sub>IN</sub> - V <sub>OUT</sub> ; ON = HIGH	--	0	--	mV
V <sub>RVD_HYS</sub>	Reverse-voltage Detect Hysteresis		--	50	--	mV
I <sub>REVERSE</sub>	MOSFET Reverse Leakage Current	V <sub>ON</sub> = 0 V; V <sub>OUT</sub> = 5.5 V	--	7	--	μA
T <sub>ON_Delay</sub>	ON Delay Time	10% ON to 10% V <sub>OUT</sub> ↑; T <sub>A</sub> = -40 °C to 85 °C; V <sub>IN</sub> = 5 V; R <sub>LOAD</sub> = 3.8 Ω, C <sub>LOAD</sub> = 10 μF	--	650	780	μs
		10% ON to 10% V <sub>OUT</sub> ↑; V <sub>IN</sub> = 5 V; R <sub>LOAD</sub> = 100 Ω, C <sub>LOAD</sub> = 1 μF	--	670	--	μs
T <sub>Total_ON</sub>	Total Turn ON Time	10% ON to 90% V <sub>OUT</sub> ↑; T <sub>A</sub> = -40 °C to 85 °C; V <sub>IN</sub> = 5 V; R <sub>LOAD</sub> = 3.8 Ω, C <sub>LOAD</sub> = 10 μF	--	1.3	1.6	ms
		10% ON to 90% V <sub>OUT</sub> ↑; V <sub>IN</sub> = 5 V; R <sub>LOAD</sub> = 100 Ω, C <sub>LOAD</sub> = 1 μF	--	1.36	--	ms
T <sub>RISE</sub>	V <sub>OUT</sub> Rise Time	10% V <sub>OUT</sub> to 90% V <sub>OUT</sub> ↑; T <sub>A</sub> = -40 °C to 85 °C; V <sub>IN</sub> = 5 V; R <sub>LOAD</sub> = 3.8 Ω, C <sub>LOAD</sub> = 10 μF	--	0.65	0.82	ms
		10% V <sub>OUT</sub> to 90% V <sub>OUT</sub> ↑; V <sub>IN</sub> = 5 V; R <sub>LOAD</sub> = 100 Ω, C <sub>LOAD</sub> = 1 μF	--	0.69	--	ms

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## Electrical Characteristics (continued)

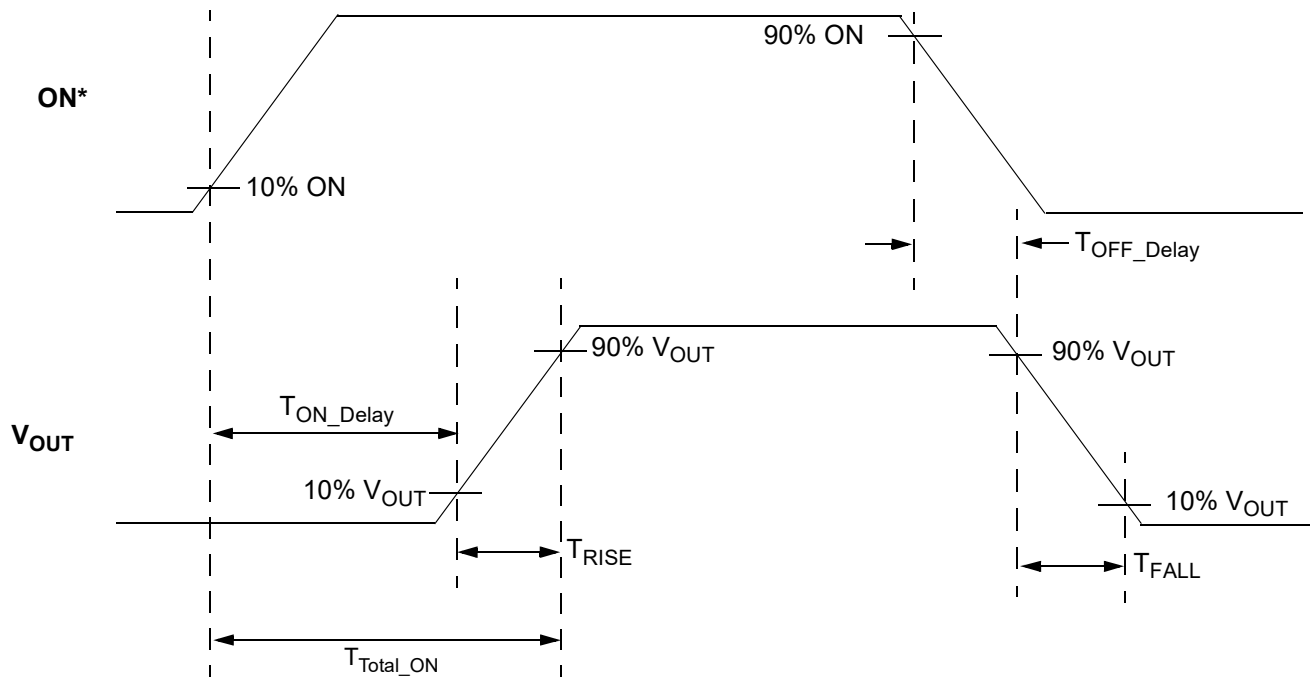
T<sub>A</sub> = -40 °C to 85 °C. Typical values are at V<sub>IN</sub> = 5 V and T<sub>A</sub> = 25 °C unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T <sub>OFF_Delay</sub>	OFF Delay Time	90% ON to 90% V <sub>OUT</sub> ↓; T <sub>A</sub> = -40 °C to 85 °C; V <sub>IN</sub> = 5 V; R <sub>LOAD</sub> = 3.8 Ω, C <sub>LOAD</sub> = 10 μF	--	4	10	μs
		90% ON to 90% V <sub>OUT</sub> ↓; V <sub>IN</sub> = 5 V; R <sub>LOAD</sub> = 100 Ω, C <sub>LOAD</sub> = 1 μF	--	10	--	μs
T <sub>FALL</sub>	V <sub>OUT</sub> Fall Time	90% V <sub>OUT</sub> to 10% V <sub>OUT</sub> ; T <sub>A</sub> = -40 °C to 85 °C; ON = HIGH-to-LOW; V <sub>IN</sub> = 5 V; R <sub>LOAD</sub> = 3.8 Ω, C <sub>LOAD</sub> = 10 μF	--	76	120	μs
		90% V <sub>OUT</sub> to 10% V <sub>OUT</sub> ; ON = HIGH-to-LOW; V <sub>IN</sub> = 5 V; R <sub>LOAD</sub> = 100 Ω, C <sub>LOAD</sub> = 1 μF	--	220	--	μs
C <sub>LOAD</sub>	Output Load Capacitance	C <sub>LOAD</sub> connected from OUT to GND	--	--	220	μF
T <sub>FLT_LOW</sub>	FLT Assertion Time	Abnormal Step Load Current event to FLT ↓;	--	8	--	ms
FLT <sub>VOL</sub>	FLT Output Low Voltage	I <sub>SINK</sub> = 10 mA; V <sub>IN</sub> = 5 V;	--	0.1	0.2	V
		I <sub>SINK</sub> = 10 mA; V <sub>IN</sub> = 2.5 V;	--	0.15	0.3	V
I <sub>FLT_Leakage</sub>	FLT Output High Leakage Current	V <sub>IN</sub> = 5 V; Switch is in On state	--	--	1	μA
ON_V <sub>IH</sub>	High Input Voltage on ON pin		1.15	--	--	V
ON_V <sub>IL</sub>	Low Input Voltage on ON pin		-0.3	0	0.65	V
THERM <sub>ON</sub>	Thermal Protection Shutdown Threshold		--	150	--	°C
THERM <sub>OFF</sub>	Thermal Protection Restart Threshold		--	130	--	°C

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## Timing Parameter Details



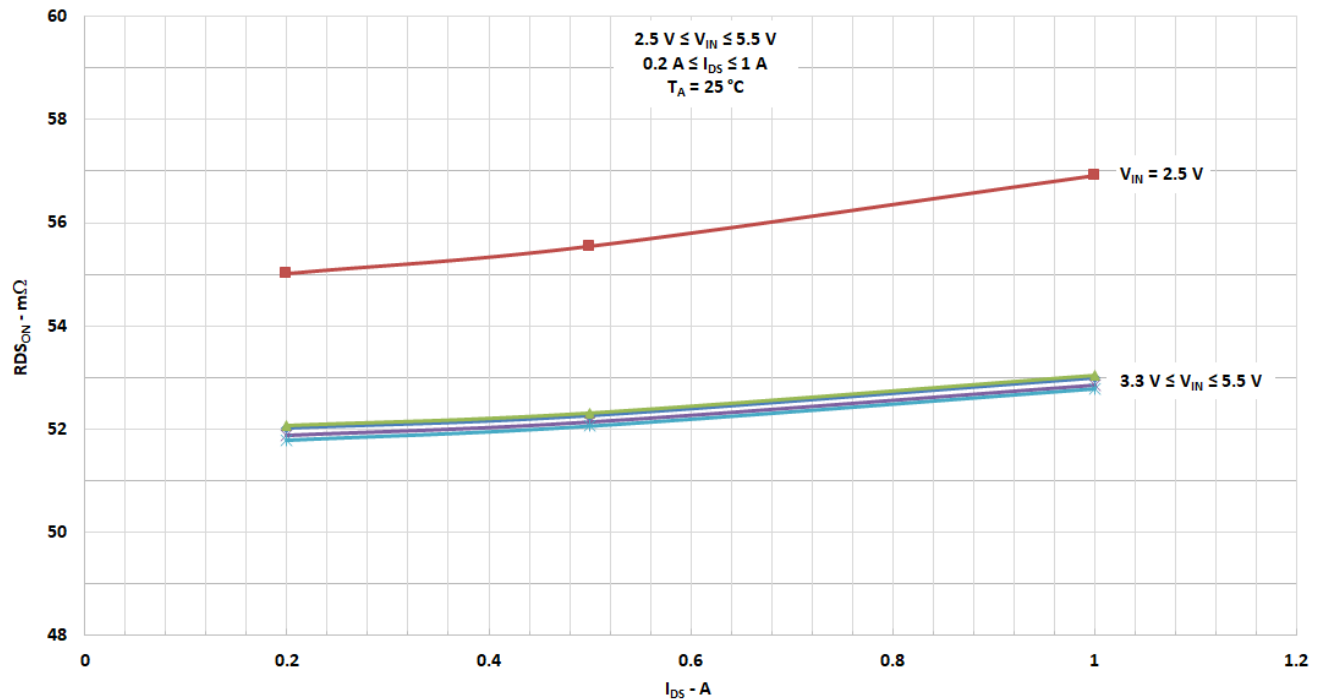
\*Rise and Fall Times of the ON Signal are 100 ns

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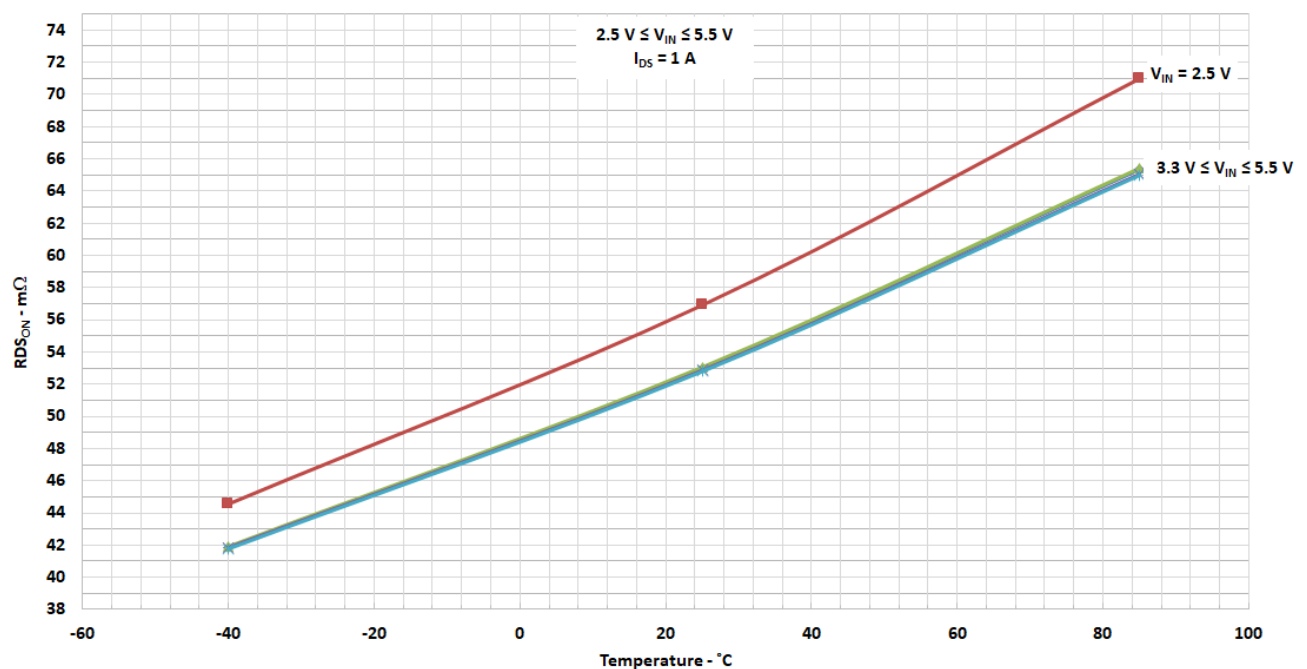
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## Typical Performance Characteristics

### RDS<sub>ON</sub> vs. I<sub>DS</sub> and V<sub>IN</sub>



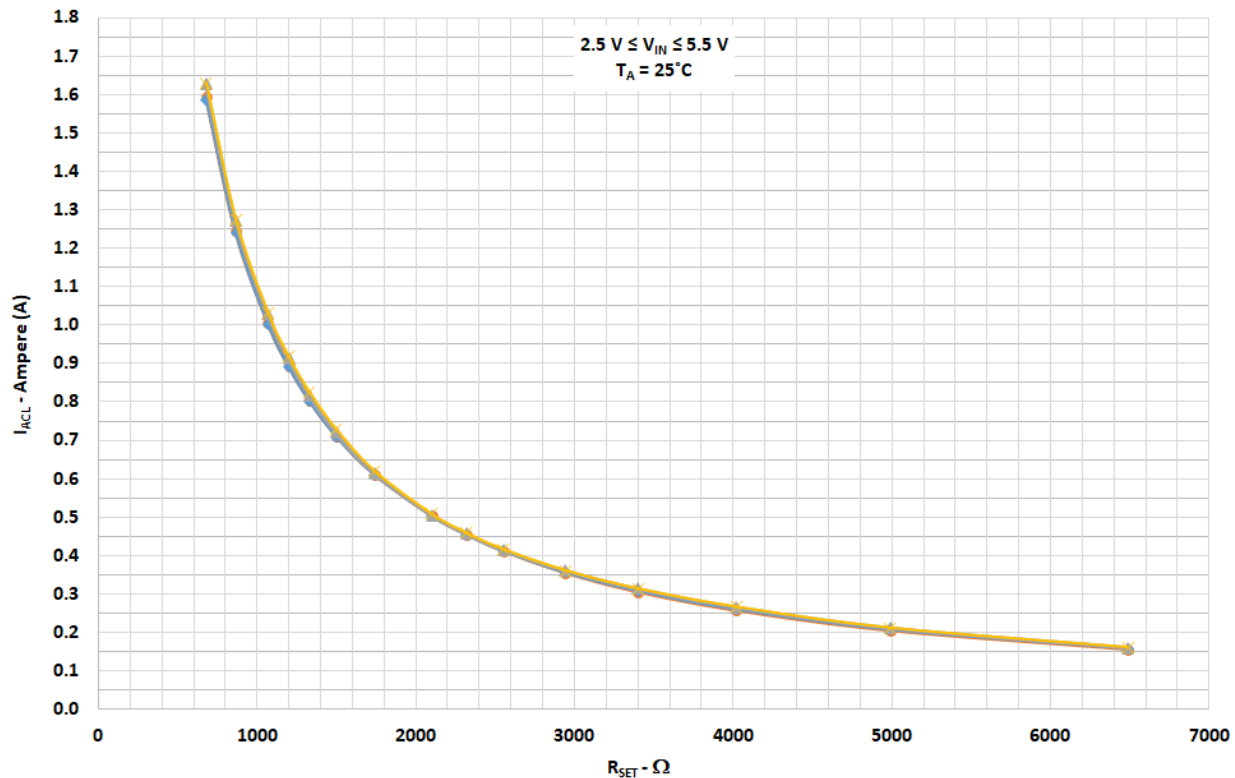
### RDS<sub>ON</sub> vs. Temperature and V<sub>IN</sub>



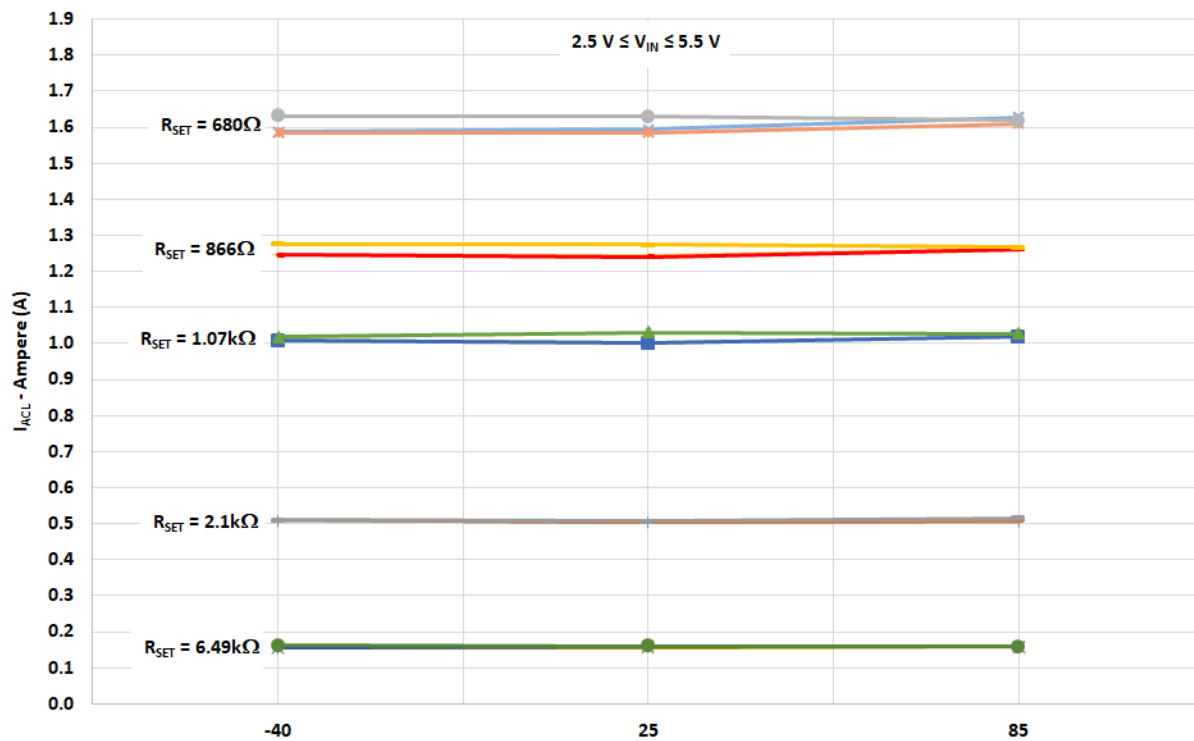
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## $I_{ACL}$ vs. $R_{SET}$ and $V_{IN}$



## $I_{ACL}$ vs. Temperature, $V_{IN}$ , and $R_{SET}$





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## Typical Turn ON Operation Waveforms

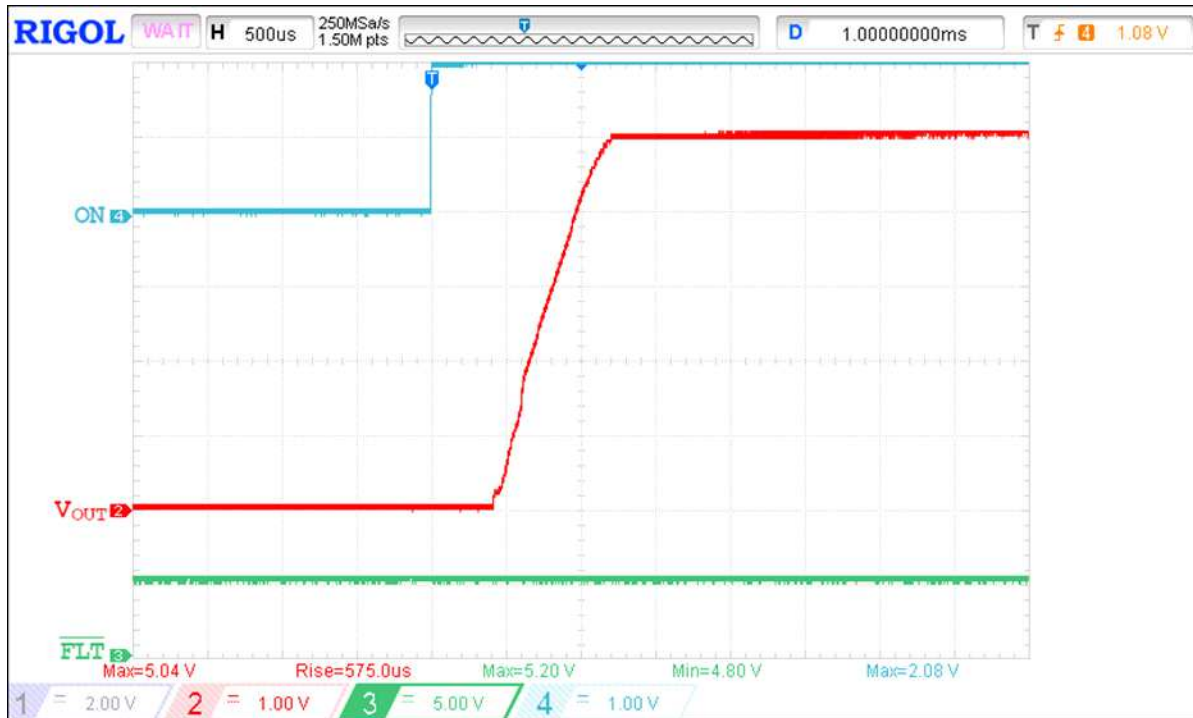


Figure 1. Typical Turn ON operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 100\ \Omega$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$

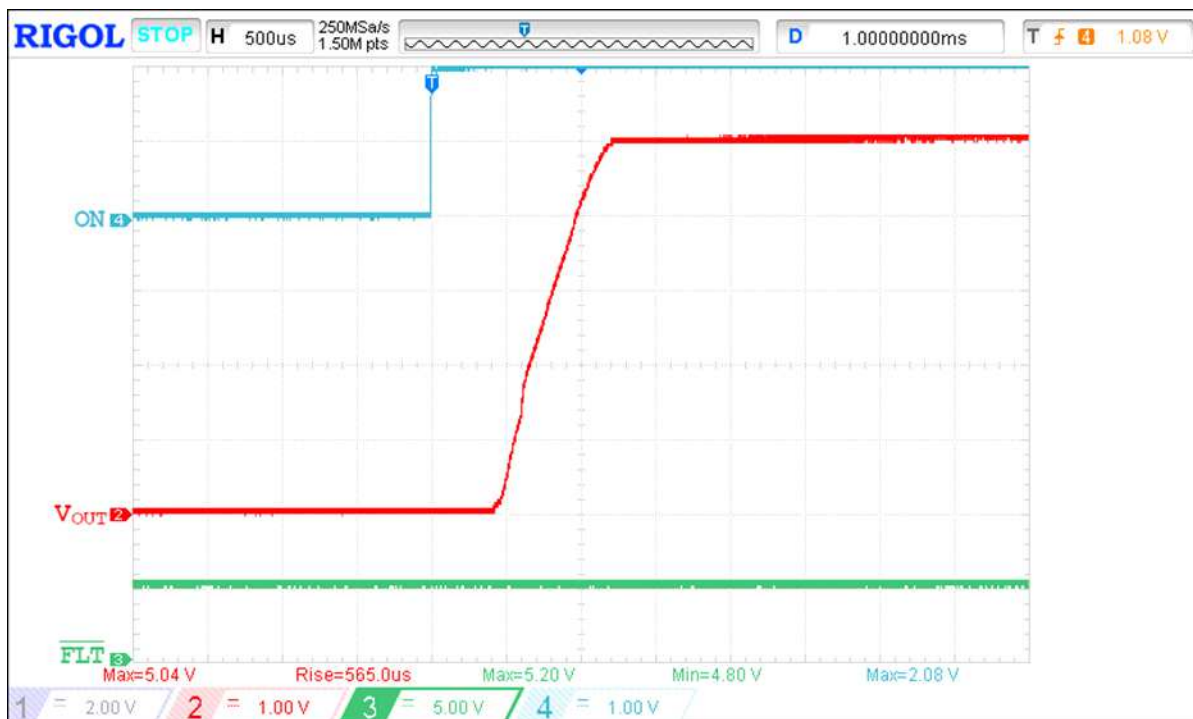


Figure 2. Typical Turn ON operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 100\ \Omega$ ,  $C_{LOAD} = 1\ \mu\text{F}$

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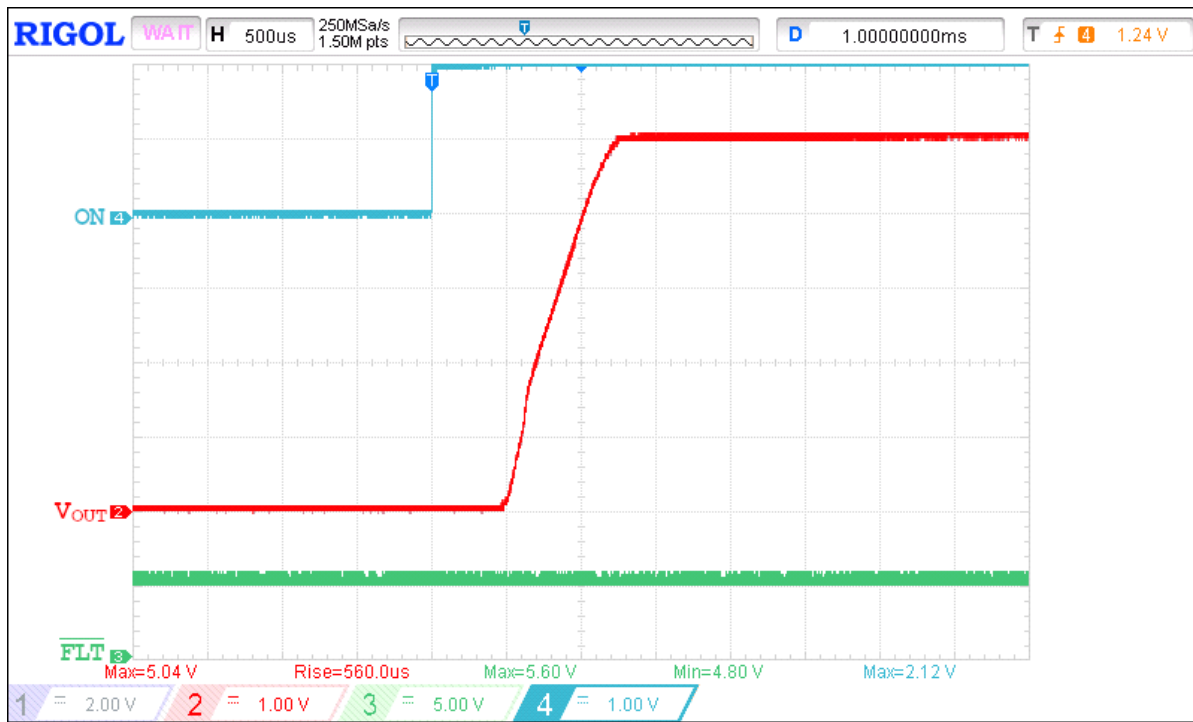


Figure 3. Typical Turn ON operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 100\ \Omega$ ,  $C_{LOAD} = 10\ \mu\text{F}$

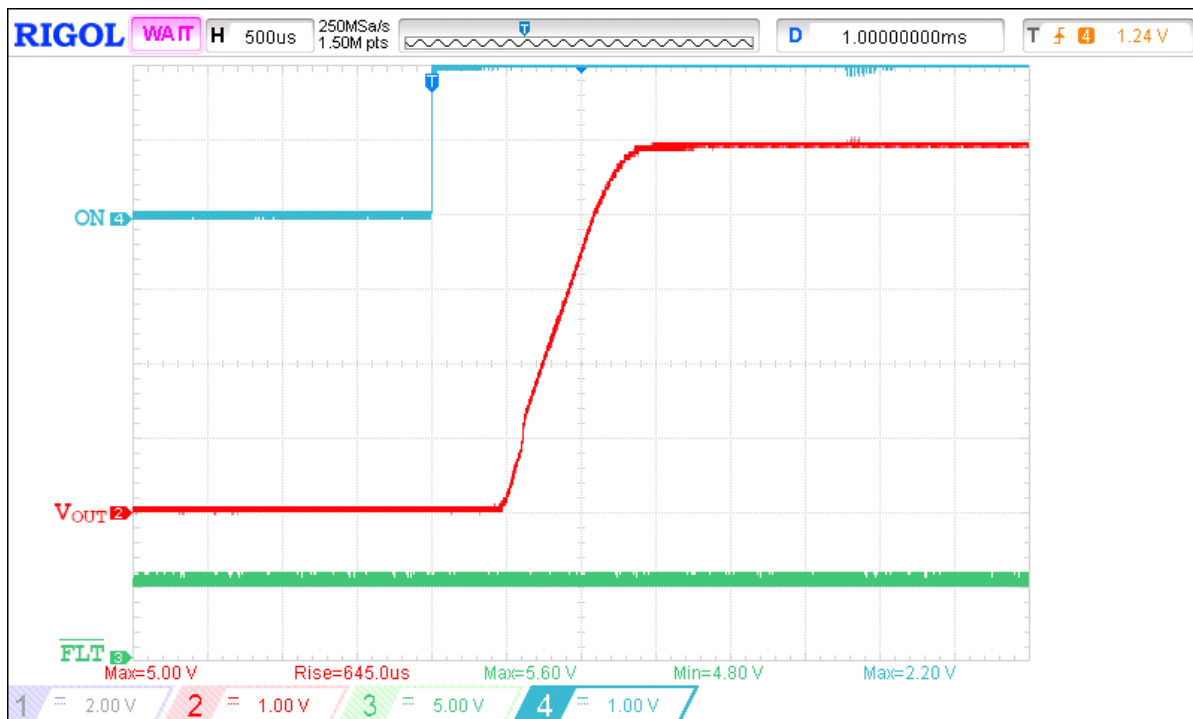


Figure 4. Typical Turn ON operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 3.8\ \Omega$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$

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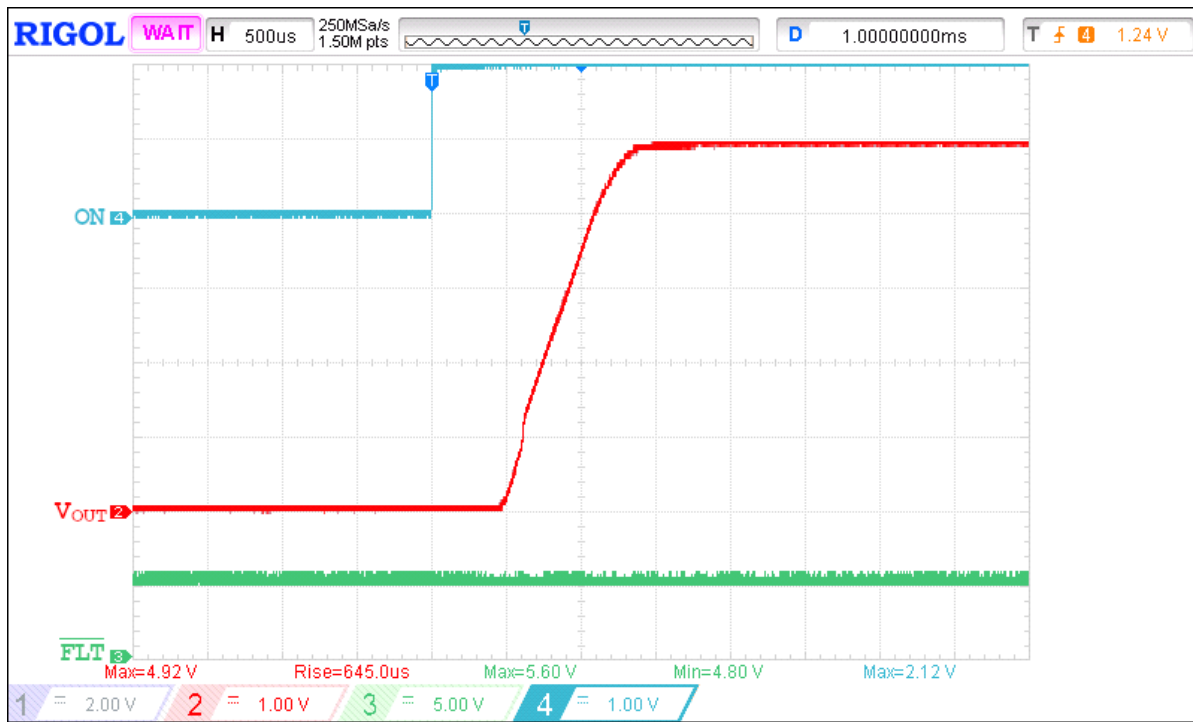


Figure 5. Typical Turn ON operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 3.8\ \Omega$ ,  $C_{LOAD} = 1\ \mu\text{F}$

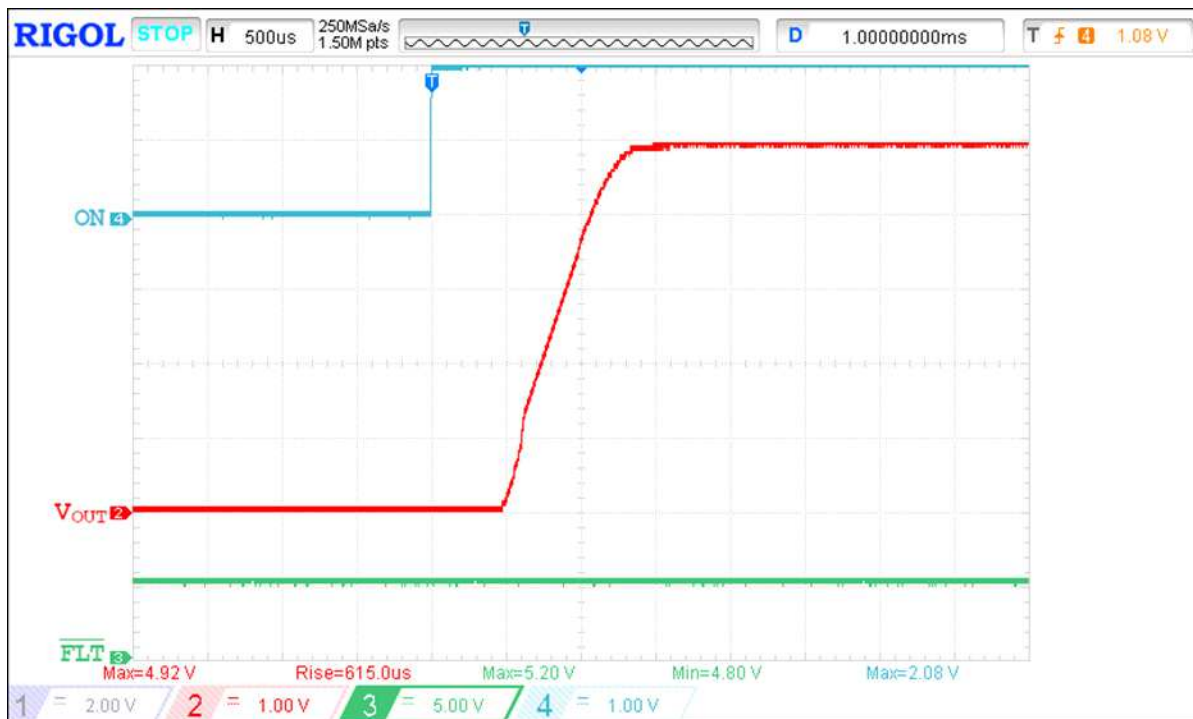


Figure 6. Typical Turn ON operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 3.8\ \Omega$ ,  $C_{LOAD} = 10\ \mu\text{F}$

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## Typical Turn OFF Operation Waveforms

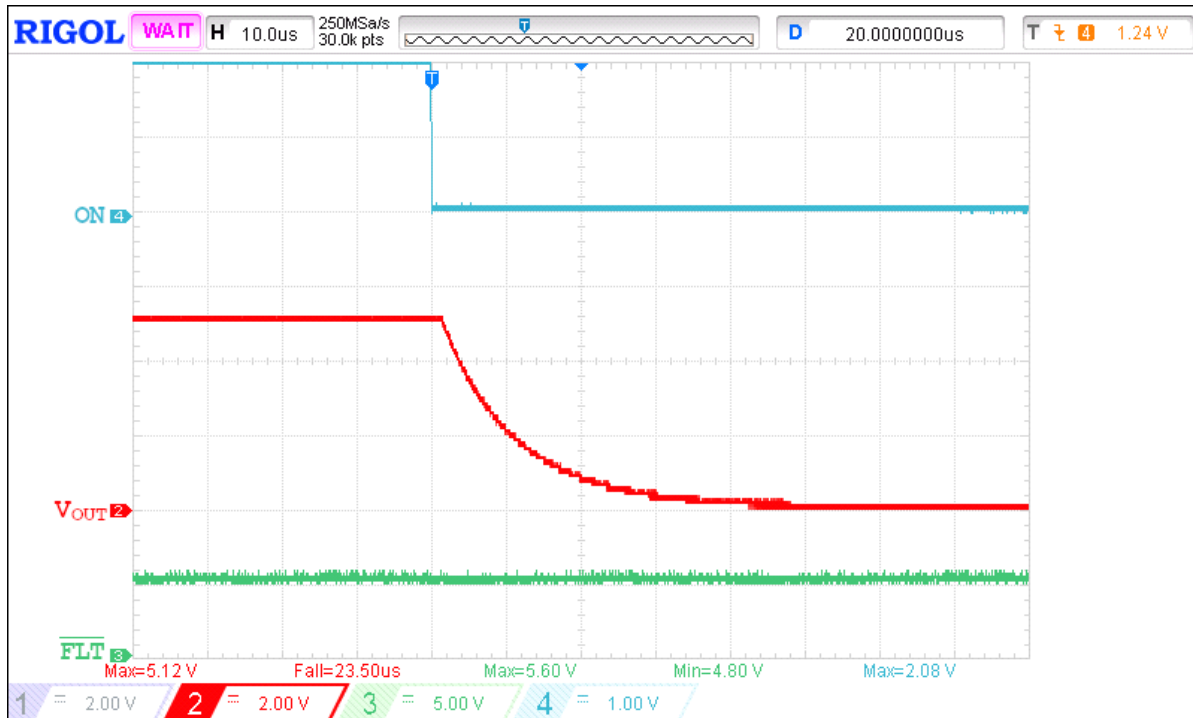


Figure 7. Typical Turn OFF operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 100\ \Omega$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$

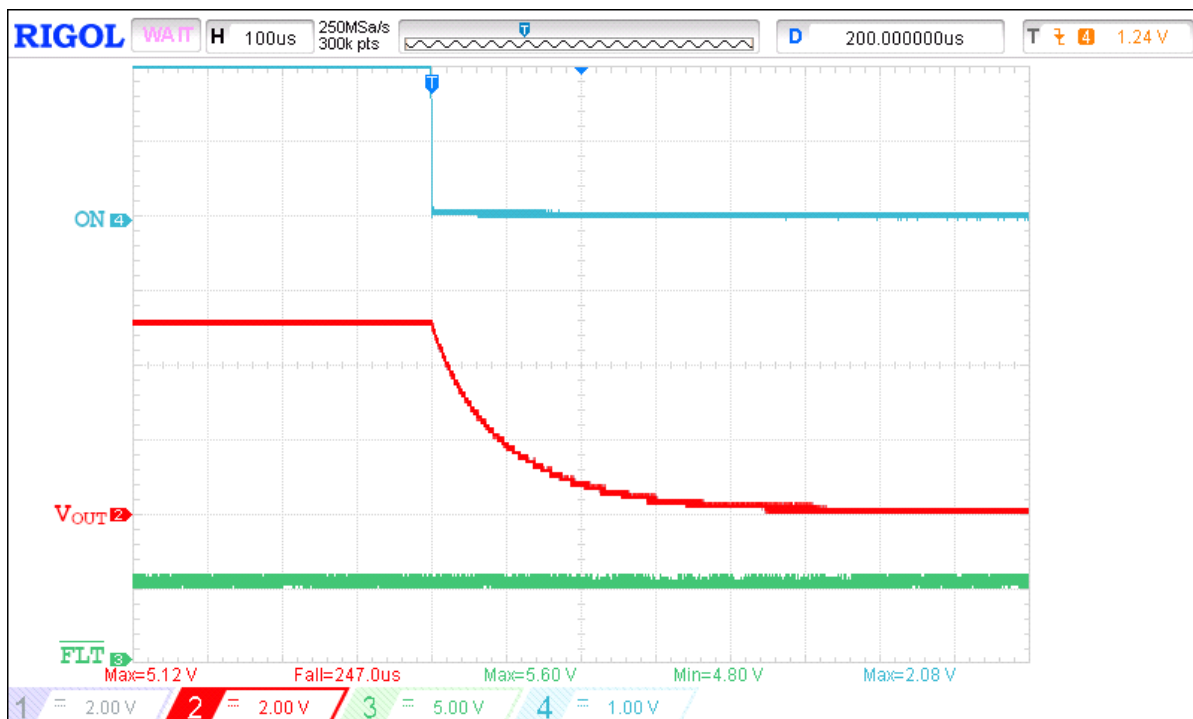


Figure 8. Typical Turn OFF operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 100\ \Omega$ ,  $C_{LOAD} = 1\ \mu\text{F}$

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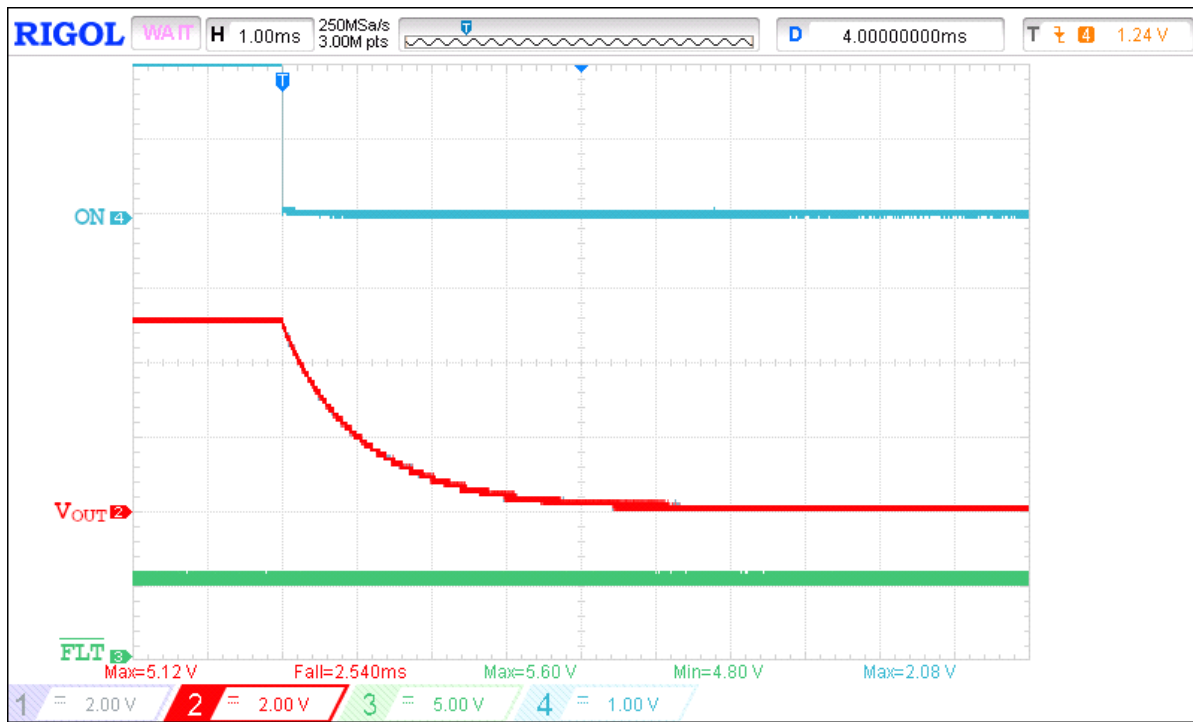


Figure 9. Typical Turn OFF operation waveform for  $V_{IN} = 5$  V,  $R_{LOAD} = 100$   $\Omega$ ,  $C_{LOAD} = 10$   $\mu$ F

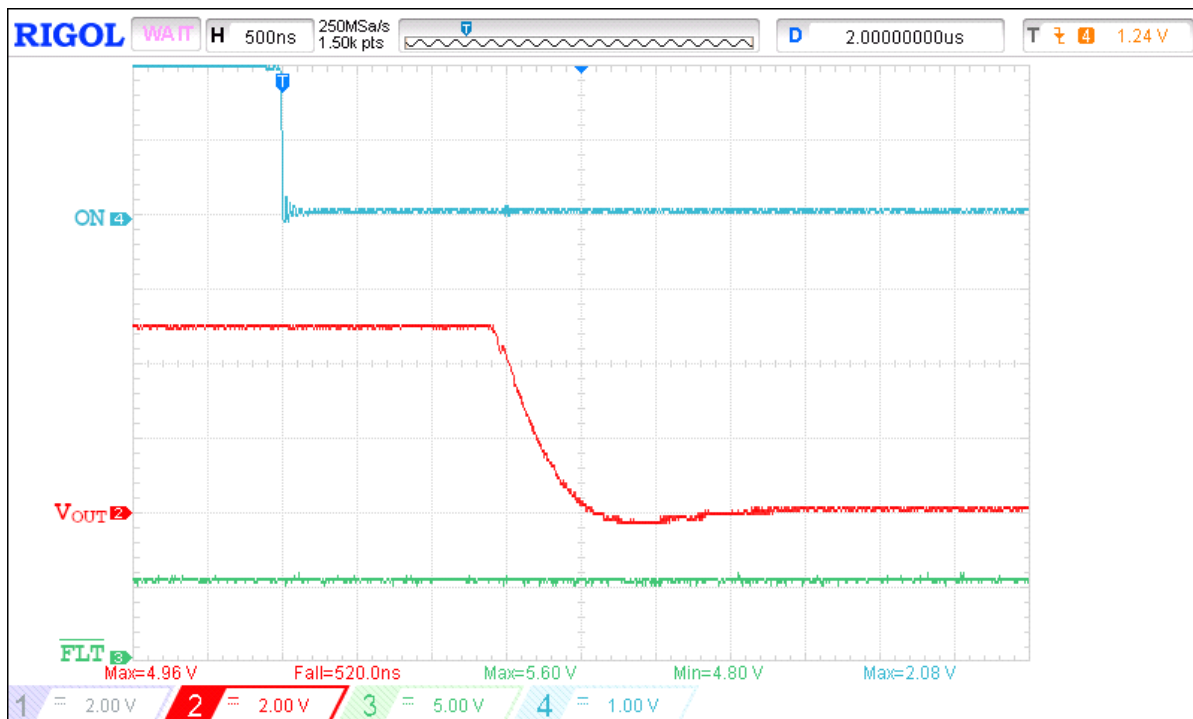


Figure 10. Typical Turn OFF operation waveform for  $V_{IN} = 5$  V,  $R_{LOAD} = 3.8$   $\Omega$ ,  $C_{LOAD} = 0.1$   $\mu$ F

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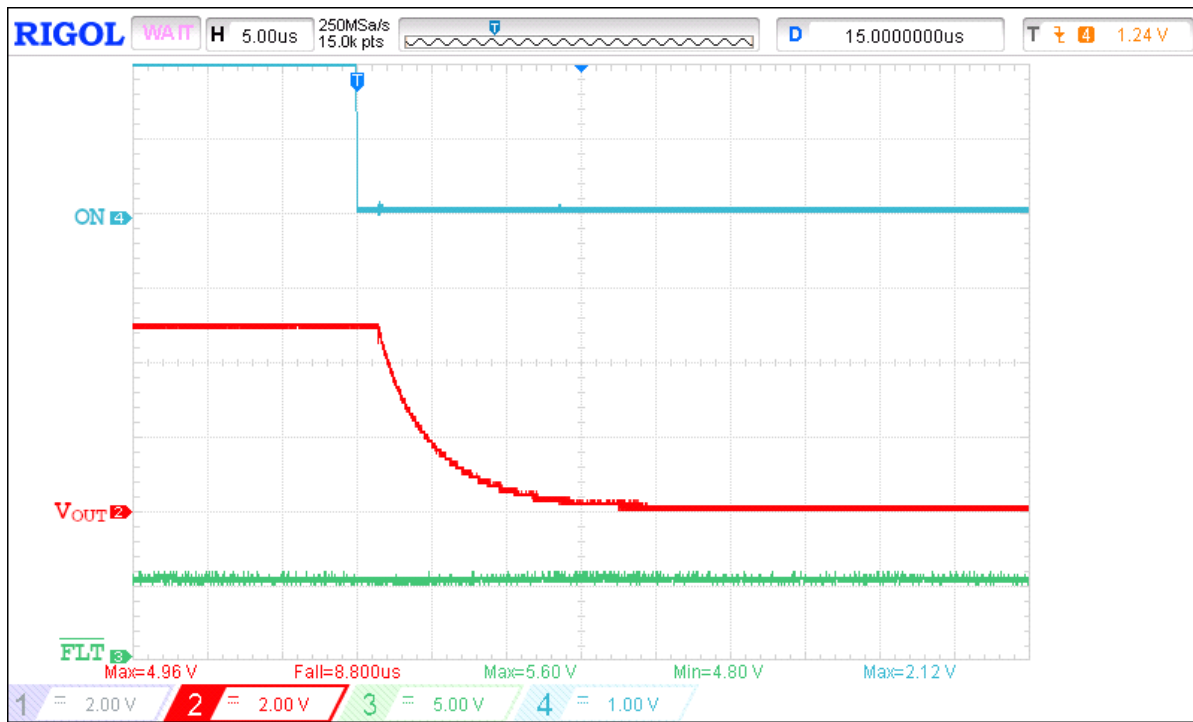


Figure 11. Typical Turn OFF operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 3.8\ \Omega$ ,  $C_{LOAD} = 1\ \mu\text{F}$

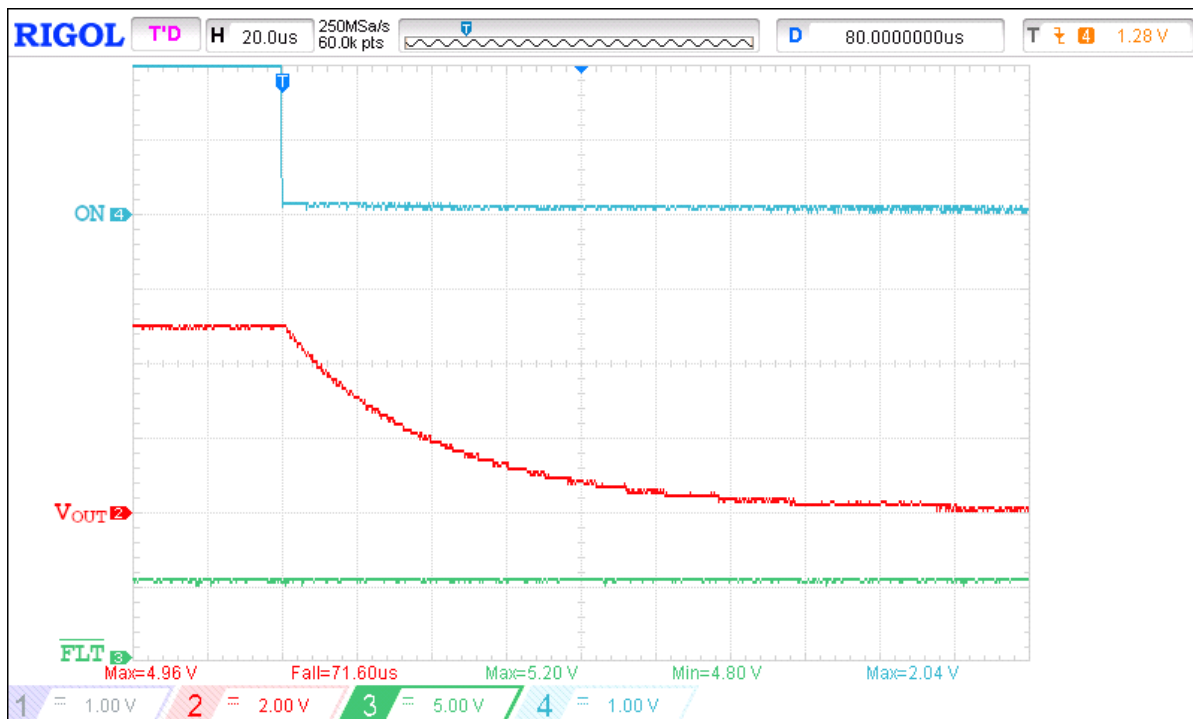


Figure 12. Typical Turn OFF operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 3.8\ \Omega$ ,  $C_{LOAD} = 10\ \mu\text{F}$

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## Typical FLT Operation Waveforms

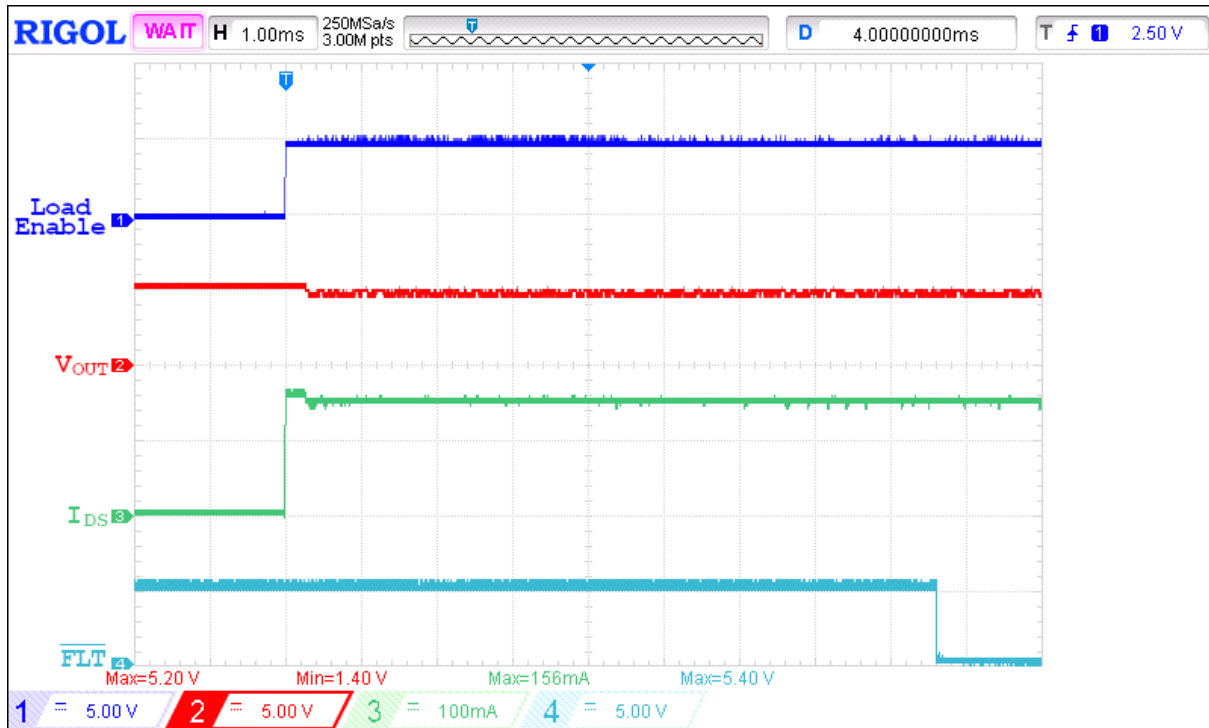


Figure 13. FLT assertion operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 30\ \Omega$ ,  $R_{SET} = 6.49\text{ k}\Omega$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$

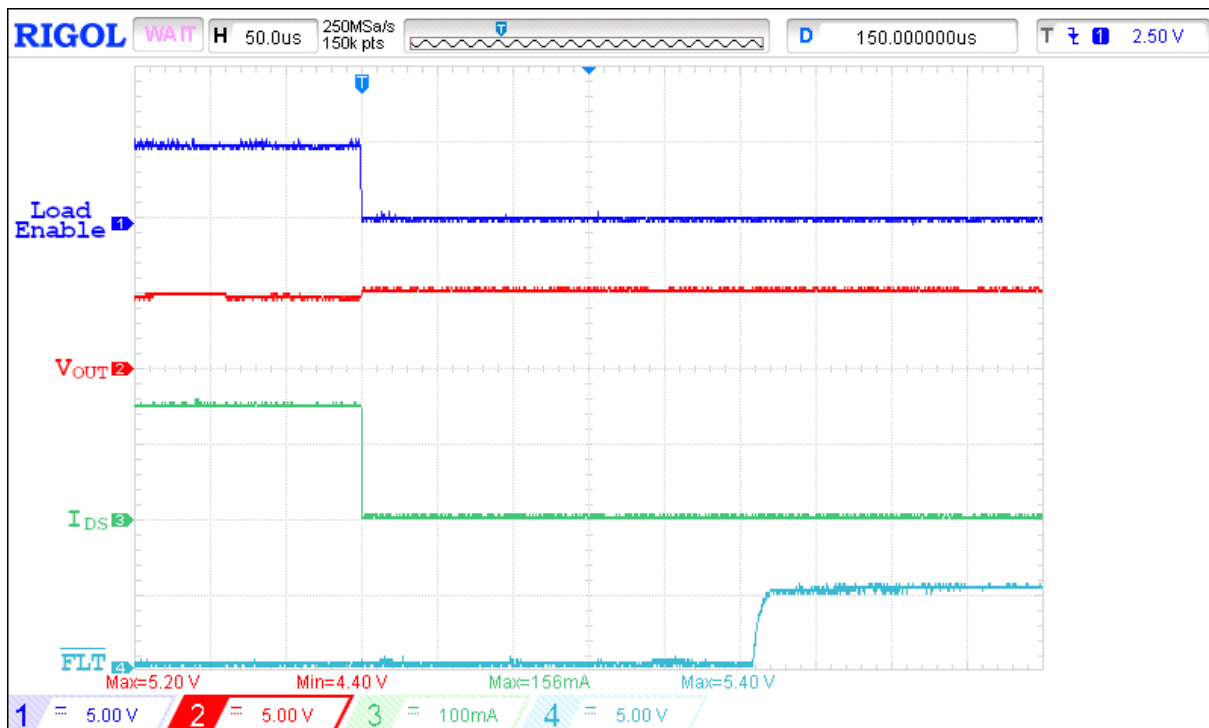


Figure 14. FLT de-assertion operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 30\ \Omega$ ,  $R_{SET} = 6.49\text{ k}\Omega$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$

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## Typical ACL Operation Waveforms

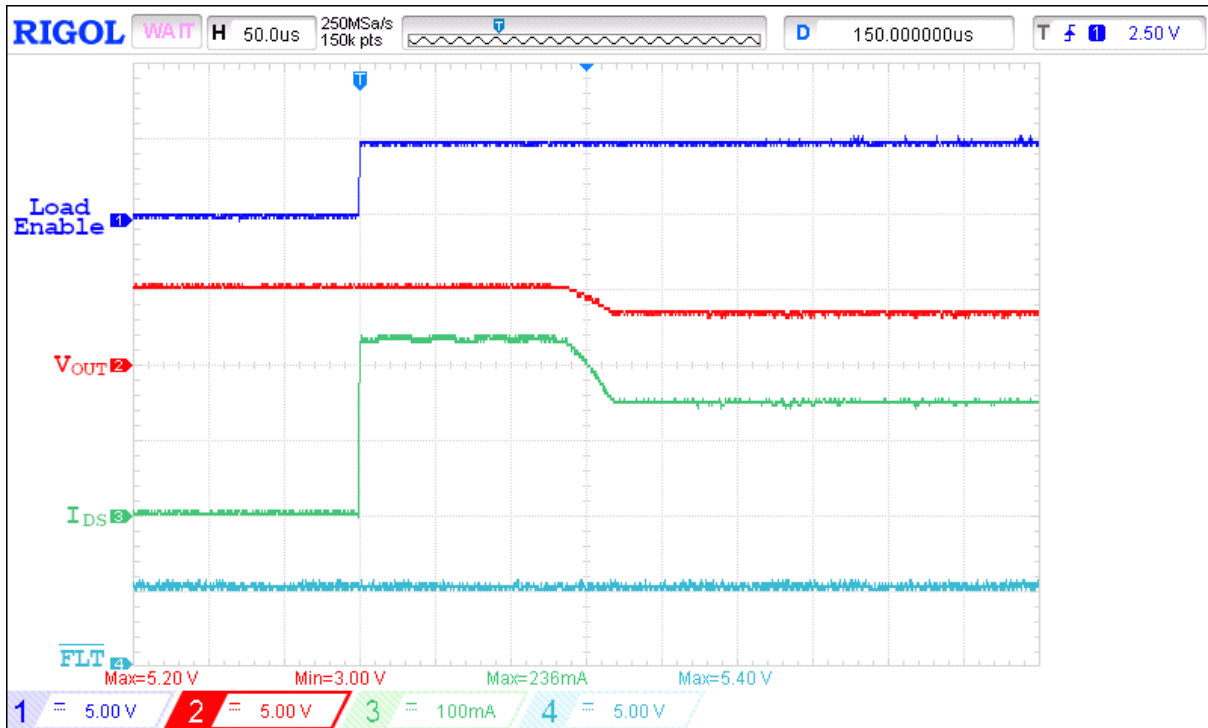


Figure 15. Typical ACL operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 22\ \Omega$ ,  $R_{SET} = 6.49\text{ k}\Omega$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$

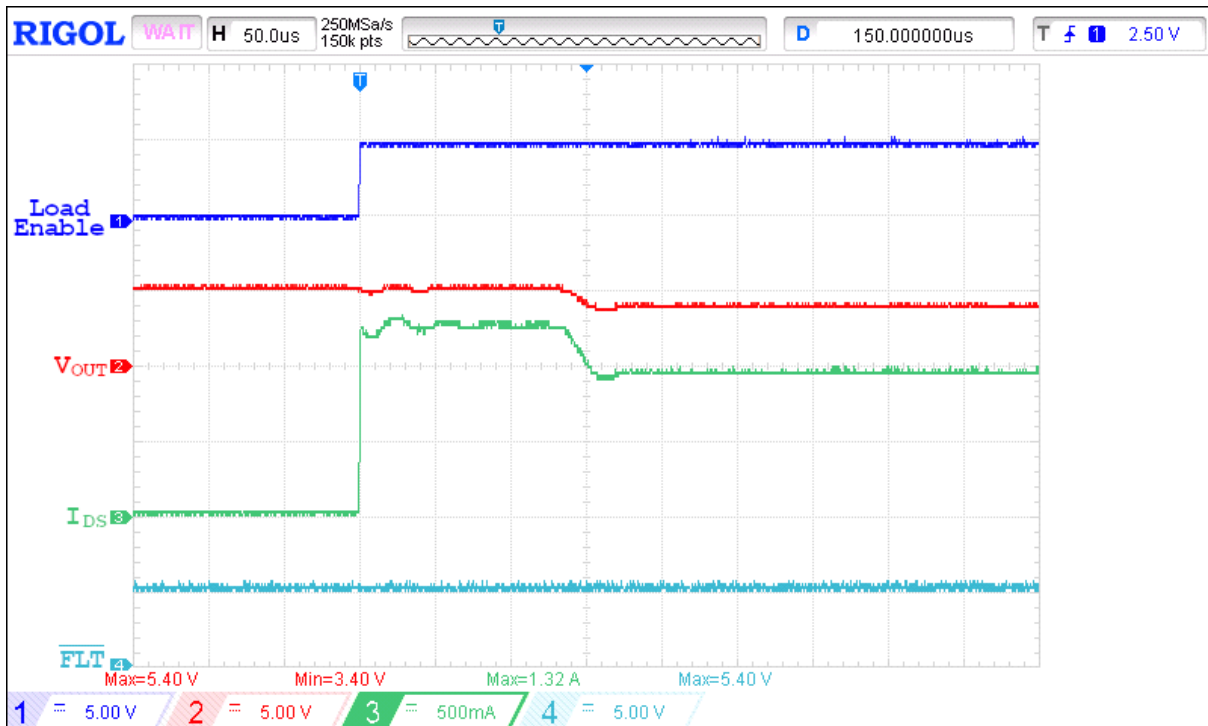


Figure 16. Typical ACL operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 3.9\ \Omega$ ,  $R_{SET} = 1.07\text{ k}\Omega$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$



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A Reverse Blocking 70 mΩ, 1.3 A nFET  
Load Switch in 1.46 mm<sup>2</sup> WLCSP

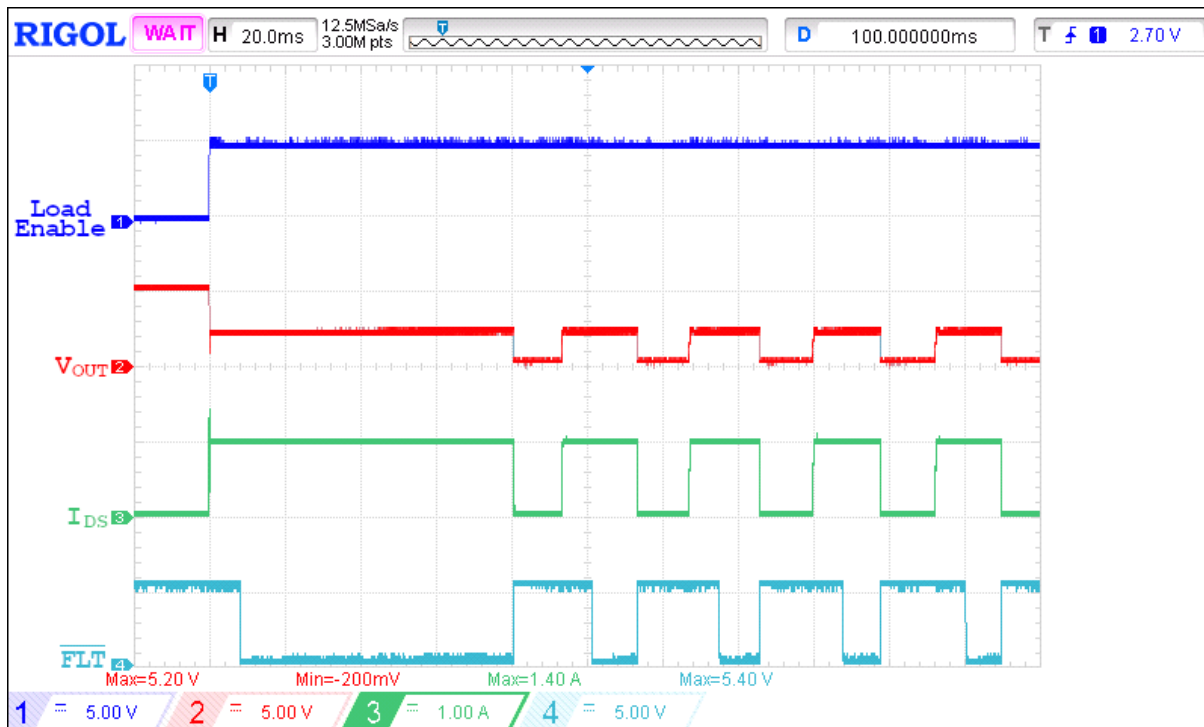


Figure 17. Typical ACL wit Thermal Shutdown Protection operation waveform for  
 $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 2.2\ \Omega$ ,  $R_{SET} = 1.07\text{ k}\Omega$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$

# SLG59H1341C

A Reverse Blocking 70 mΩ, 1.3 A nFET  
Load Switch in 1.46 mm<sup>2</sup> WLCSP

## Typical OVP Operation Waveforms

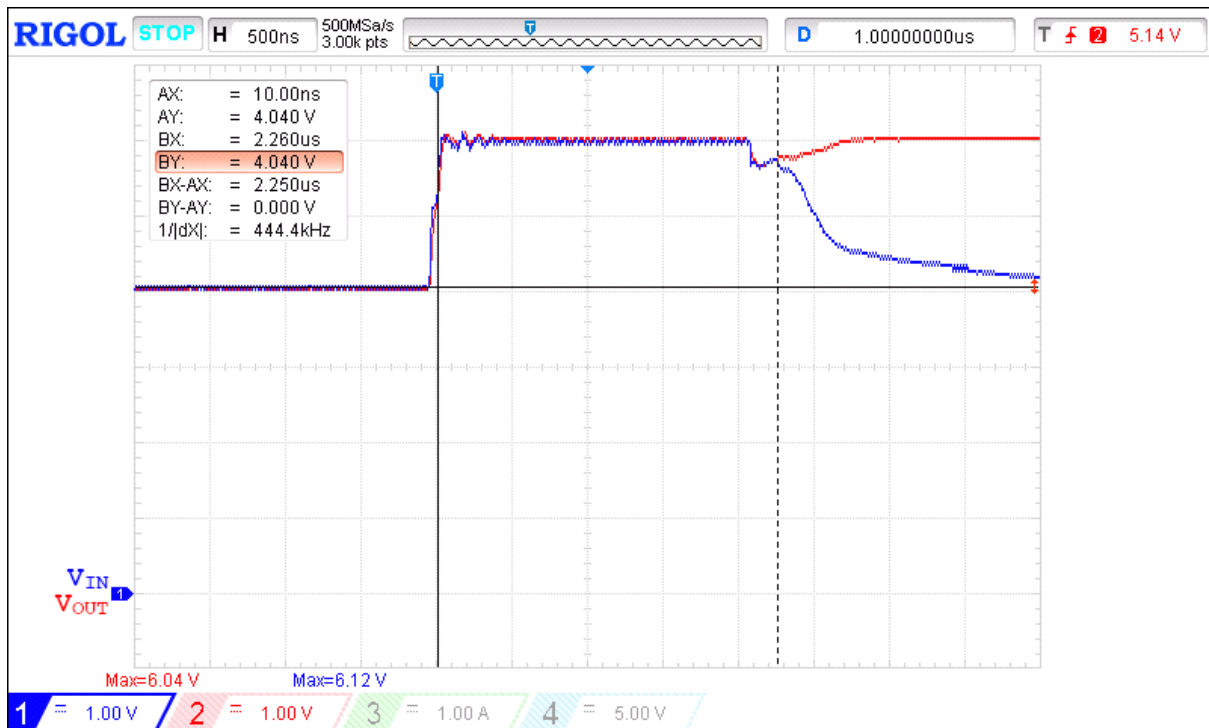


Figure 18. OVP Response operation waveform for  $V_{OUT}$  step from 4 V to 6 V, no  $R_{LOAD}$ , no  $C_{LOAD}$

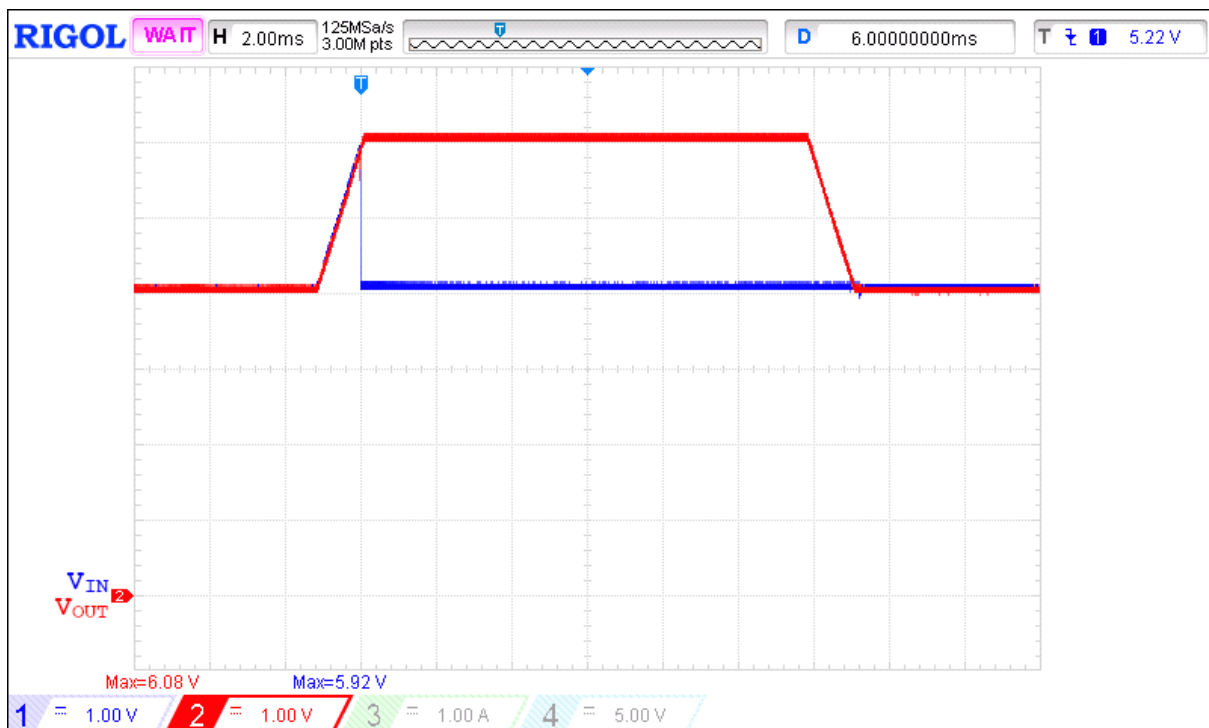


Figure 19. Typical Overvoltage Protection operation waveform.  
 $V_{IN} = 4$  V.  $V_{OUT}$  step from 4 V to 6 V to 4 V, no  $R_{LOAD}$ , no  $C_{LOAD}$

## SLG59H1341C

A Reverse Blocking 70 mΩ, 1.3 A nFET  
Load Switch in 1.46 mm<sup>2</sup> WLCSP

### SLG59H1341C Current Limiting Operation

After power up the output current is initially limited to the Active Current Limit ( $I_{ACL}$ ) specification listed in the Electrical Characteristics table. The ACL monitor's response time is very fast and is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the load switch's  $I_{ACL}$  threshold. During active current-limit operation,  $V_{OUT}$  is also reduced by  $I_{ACL} \times R_{DS(on)(ACL)}$ .

When a current-limit event is detected, the  $\overline{FLT}$  signal becomes asserted in approximately  $T_{FLT\_LOW}$  and the SLG59H1341C operates in constant current mode with the output current set by  $R_{SET}$  (see  $R_{SET}$ -Current Limit Table). The SLG59H1341C continues to operate in constant current mode indefinitely until the current-limit event has elapsed.

### SLG59H1341C $\overline{FLT}$ Operation

As previously stated in the Pin Description section, the open-drain  $\overline{FLT}$  output is asserted when an active-current limit (ACL) condition is detected. This output becomes asserted in  $T_{FLT\_LOW}$  upon the detection of a fault condition. If the ON pin is toggled HIGH-to-LOW while the  $\overline{FLT}$  output is low, the  $\overline{FLT}$  output is deasserted without delay.

### Setting the SLG59H1341C Output Current Limit with $R_{SET}$

The current-limit operation of the SLG59H1341C begins by choosing the appropriate  $\pm 1\%$ -tolerance  $R_{SET}$  value for the application. The recommended range for  $R_{SET}$  is:

$$6.49 \text{ k}\Omega \geq R_{SET} \geq 680 \text{ }\Omega$$

which corresponds to an output constant current limit in the following range:

$$0.16 \text{ A} \leq I_{ACL} \leq 1.62 \text{ A}$$

**Table 1: Setting Current Limit Threshold vs.  $R_{SET}$ ,  $C_{IN} = 30 \text{ }\mu\text{F}$ ,  $C_{RSET} = 10 \text{ pF}$**

$R_{SET} (\Omega)$	Min. Current Limit (A)	Typ. Current Limit (A)	Max. Current Limit (A)
680	1.460	1.620	1.780
866	1.140	1.260	1.380
1070	0.920	1.020	1.120
1200	0.820	0.910	1.000
1330	0.730	0.810	0.890
1500	0.650	0.720	0.790
1740	0.560	0.620	0.680
2100	0.460	0.510	0.560
2320	0.414	0.460	0.506
2550	0.374	0.415	0.456
2940	0.329	0.365	0.401
3400	0.284	0.315	0.346
4020	0.239	0.265	0.291
4990	0.194	0.215	0.236
6490	0.136	0.160	0.184

## SLG59H1341C

A Reverse Blocking 70 mΩ, 1.3 A nFET  
Load Switch in 1.46 mm<sup>2</sup> WLCSP

### Power Dissipation Considerations

The junction temperature of the SLG59H1341C depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the  $R_{DS(ON)}$  generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59H1341C is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = R_{DS(ON)} \times I_{DS}^2$$

where:

$PD_{TOTAL}$  = Total package power dissipation, in Watts (W)

$R_{DS(ON)}$  = Power MOSFET ON resistance, in Ohms (Ω)

$I_{DS}$  = Output current, in Amps (A)

and

$$T_J = PD_{TOTAL} \times \theta_{JA} + T_A$$

where:

$T_J$  = Die junction temperature, in Celsius degrees (°C)

$\theta_{JA}$  = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

$T_A$  = Ambient temperature, in Celsius degrees (°C)

In nominal operating mode, the SLG59H1341C's power dissipation can also be calculated by taking into account the voltage drop across the switch ( $V_{IN} - V_{OUT}$ ) and the magnitude of the switch's output current ( $I_{DS}$ ):

$$PD_{TOTAL} = (V_{IN} - V_{OUT}) \times I_{DS} \text{ or}$$

$$PD_{TOTAL} = (V_{IN} - (R_{LOAD} \times I_{DS})) \times I_{DS}$$

where:

$PD_{TOTAL}$  = Total package power dissipation, in Watts (W)

$V_{IN}$  = Switch input Voltage, in Volts (V)

$R_{LOAD}$  = Output Load Resistance, in Ohms (Ω)

$I_{DS}$  = Switch output current, in Amps (A)

$V_{OUT}$  = Switch output voltage, or  $R_{LOAD} \times I_{DS}$

In current-limit mode, the SLG59H1341C's power dissipation can be calculated by taking into account the voltage drop across the load switch ( $V_{IN} - V_{OUT}$ ) and the magnitude of the output current in current-limit mode ( $I_{ACL}$ ):

$$PD = (V_{IN} - V_{OUT}) \times I_{ACL} \text{ or}$$

$$PD = (V_{IN} - (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

$PD$  = Power dissipation, in Watts (W)

$V_{IN}$  = Input Voltage, in Volts (V)

$R_{LOAD}$  = Load Resistance, in Ohms (Ω)

$I_{ACL}$  = Output limited current, in Amps (A)

$V_{OUT} = R_{LOAD} \times I_{ACL}$

## SLG59H1341C

A Reverse Blocking 70 mΩ, 1.3 A nFET  
Load Switch in 1.46 mm<sup>2</sup> WLCSP

### Layout Guidelines

1. Since the VIN and VOUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 20, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;
2. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C<sub>IN</sub> and output C<sub>LOAD</sub> low-ESR capacitors as close as possible to the SLG59H1341Cs VIN and VOUT pins;
3. The GND pin should be connected to system analog or power ground plane.

### SLG59H1341C Evaluation Board:

4. A High Voltage GreenFET Evaluation Board for SLG59H1341C is designed according to the statements above and is illustrated on Figure 20. Please note that evaluation board Sense pads. They cannot carry high currents and dedicated only for RDS<sub>ON</sub> evaluation.

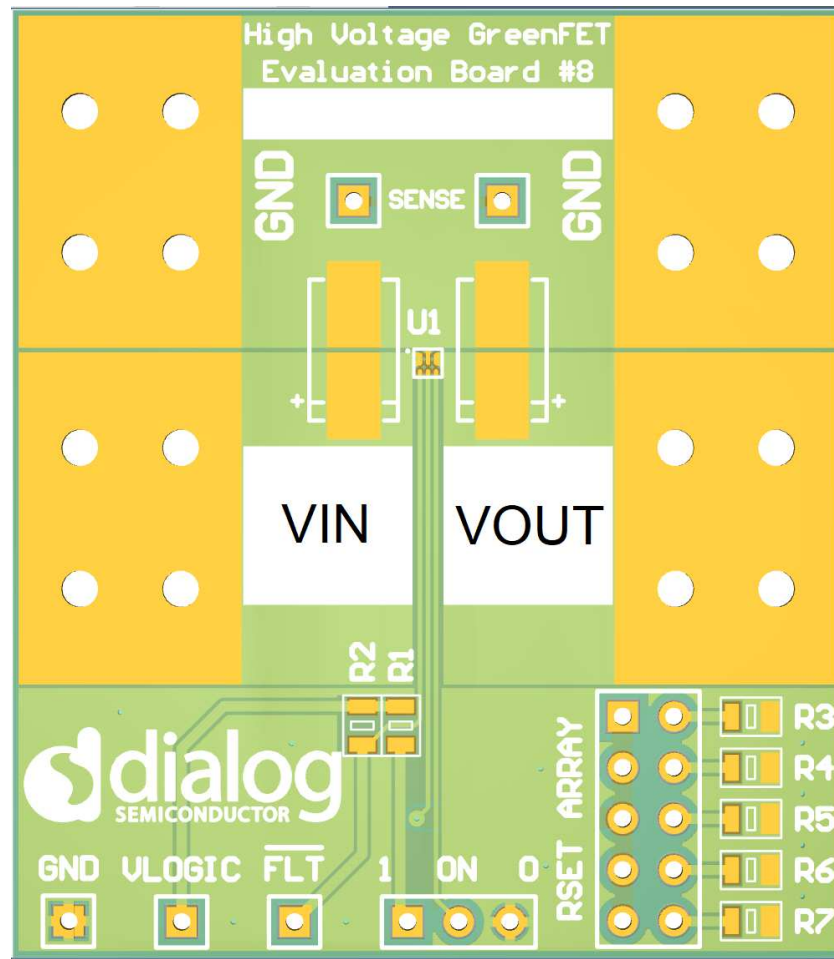
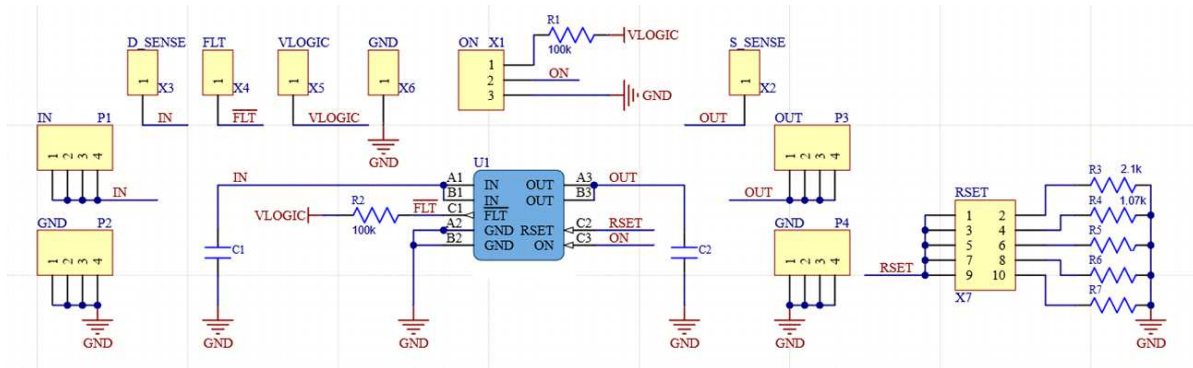


Figure 20. SLG59H1341C Evaluation Board

## A Reverse Blocking 70 m $\Omega$ , 1.3 A nFET Load Switch in 1.46 mm<sup>2</sup> WLCSP



**Figure 21. SLG59H1341C Evaluation Board Connection Circuit**

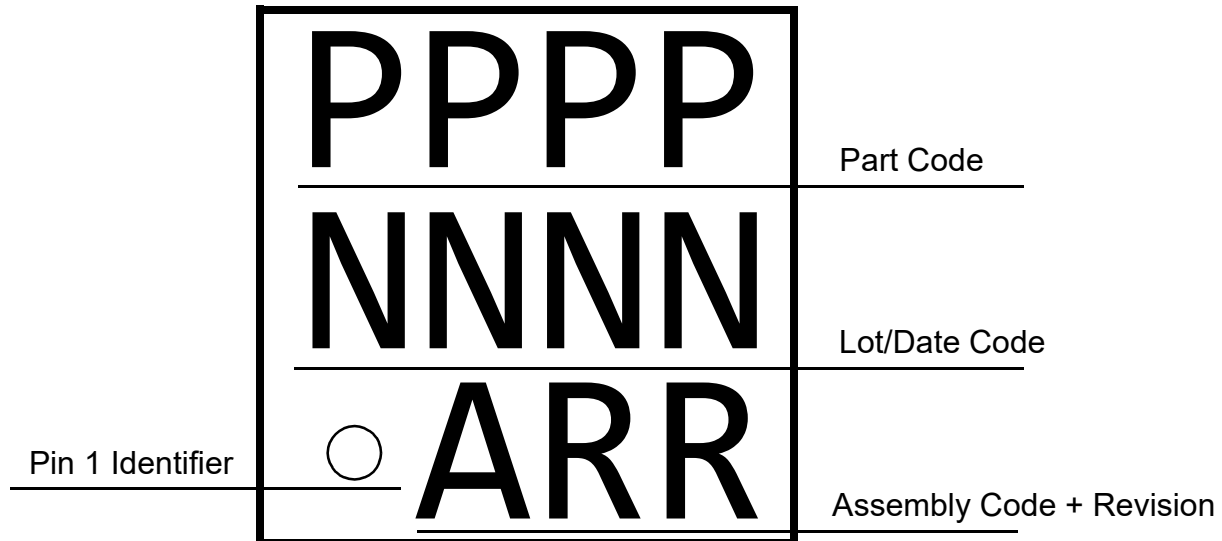
## Basic EVB Configuration

1. Connect oscilloscope probes to VIN, VOUT, ON, etc.;
2. Turn on Power Supply and set desired  $V_{IN}$  from 2.5 V...5.5 V range;
3. Toggle ON signal High or Low to observe SLG59H1341C operation;

# SLG59H1341C

A Reverse Blocking 70 mΩ, 1.3 A nFET  
Load Switch in 1.46 mm<sup>2</sup> WLCSP

## Package Top Marking System Definition



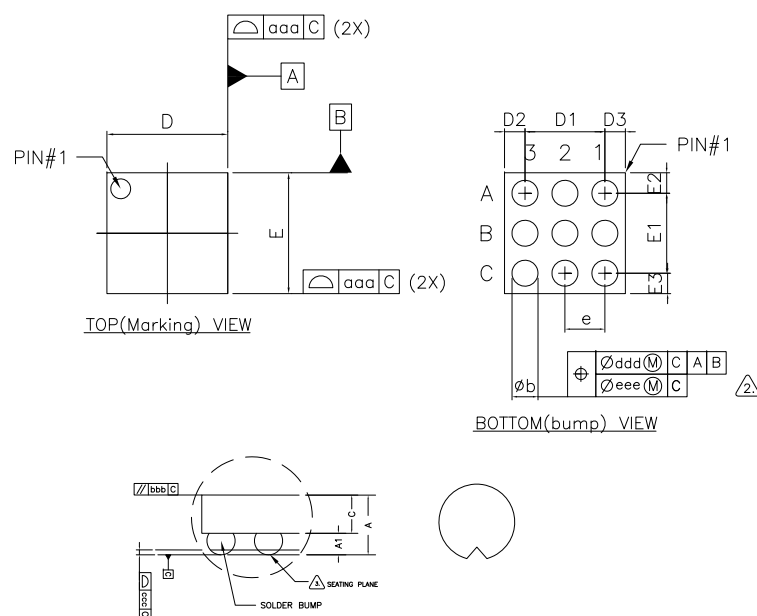
# SLG59H1341C

A Reverse Blocking 70 mΩ, 1.3 A nFET

Load Switch in 1.46 mm<sup>2</sup> WLCSP

## Package Drawing and Dimensions

9 Pin WLCSP Green Package 1.21x 1.21 mm



Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.5470	0.5860	0.6250	0.0215	0.0231	0.0246
A1	0.1870	0.2080	0.2290	0.0074	0.0082	0.0090
c	0.3530	0.3780	0.4030	0.0139	0.0149	0.0159
D	1.1850	1.2100	1.2350	0.0467	0.0476	0.0486
E	1.1850	1.2100	1.2350	0.0467	0.0476	0.0486
b	0.2340	0.2600	0.2860	0.0092	0.0102	0.0113
D1	---	0.8000	---	---	0.0315	---
D2	---	0.2050	---	---	0.0081	---
D3	---	0.2050	---	---	0.0081	---
E1	---	0.8000	---	---	0.0315	---
E2	---	0.2050	---	---	0.0081	---
E3	---	0.2050	---	---	0.0081	---
e	---	0.4000	---	---	0.0157	---
aaa	---	0.025	---	---	0.001	---
bbb	---	0.060	---	---	0.002	---
ccc	---	0.030	---	---	0.001	---
ddd	---	0.050	---	---	0.002	---
eee	---	0.050	---	---	0.002	---

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.

2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

4. THE SOLDER BALL SIZE PRIOR REFLOW IS 250 UM.

RENESAS

STATUS:

RELEASED

TERMINAL FINISH:

SAC405

TITLE:

CABRERA WLCSP 9L  
1.21x1.21x0.586mm 0.4P  
PACKAGE OUTLINE

REV:

A

REVISION NOTE:

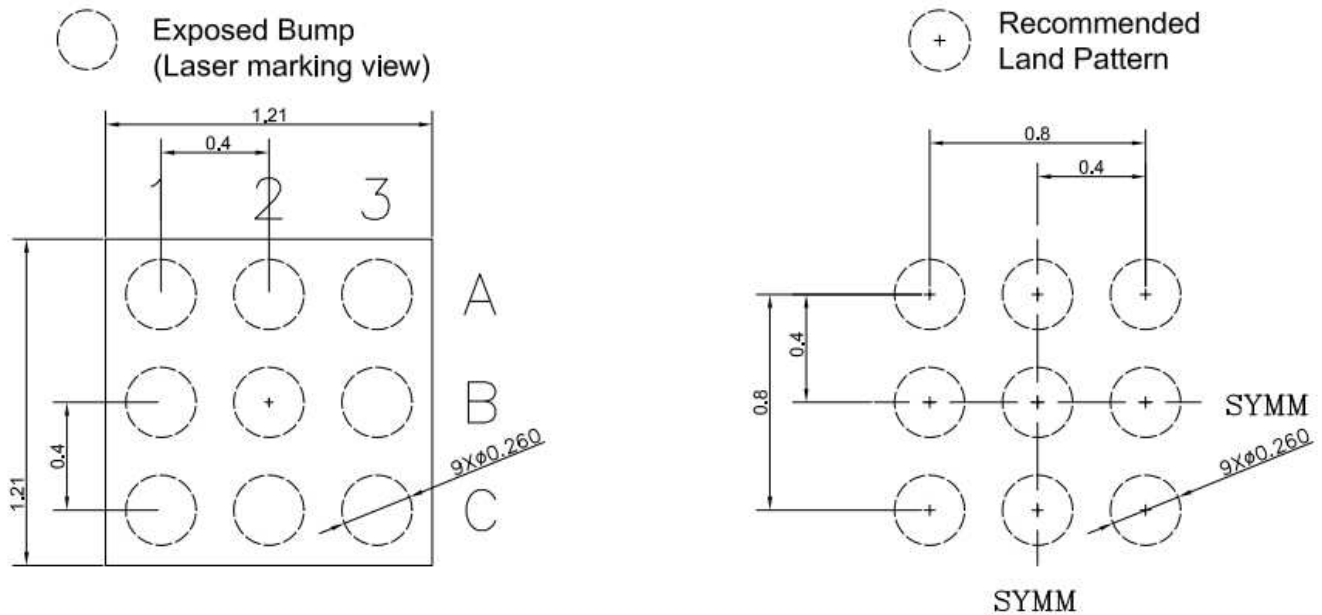
NEW DRAWING



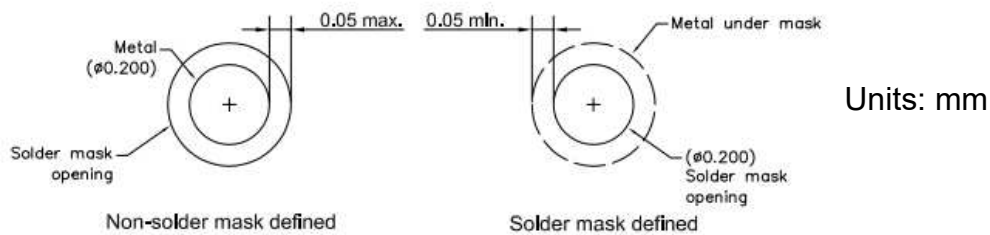
# SLG59H1341C

A Reverse Blocking 70 mΩ, 1.3 A nFET  
Load Switch in 1.46 mm<sup>2</sup> WLCSP

## Recommended Landing Pattern



TOP(marking view)



Units: mm

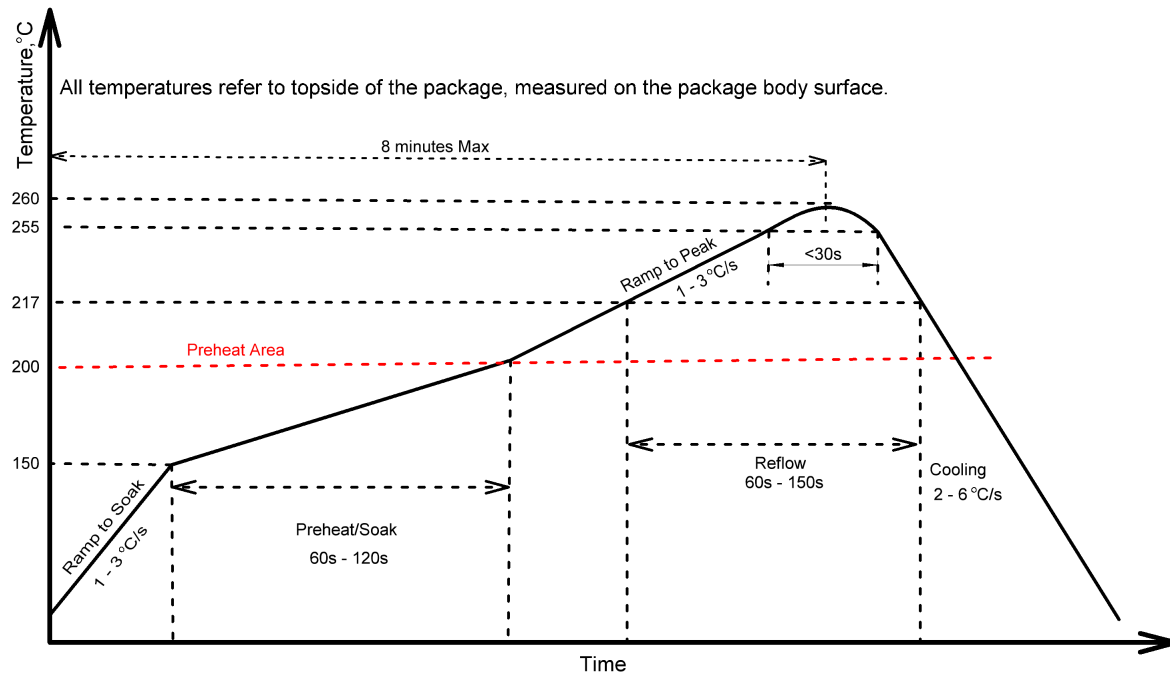
Solder mask detail (not to scale)

# SLG59H1341C

A Reverse Blocking 70 mΩ, 1.3 A nFET  
Load Switch in 1.46 mm<sup>2</sup> WLCSP

## Recommended Reflow Soldering Profile

For successful reflow of the SLG59H1341C a recommended thermal profile is illustrated below:



Note: This reflow profile is for classification/preconditioning and are not meant to specify board assembly profile. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed parameters depicted on figure above.

Please see more information on IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.553 mm<sup>3</sup> (nominal).

# SLG59H1341C

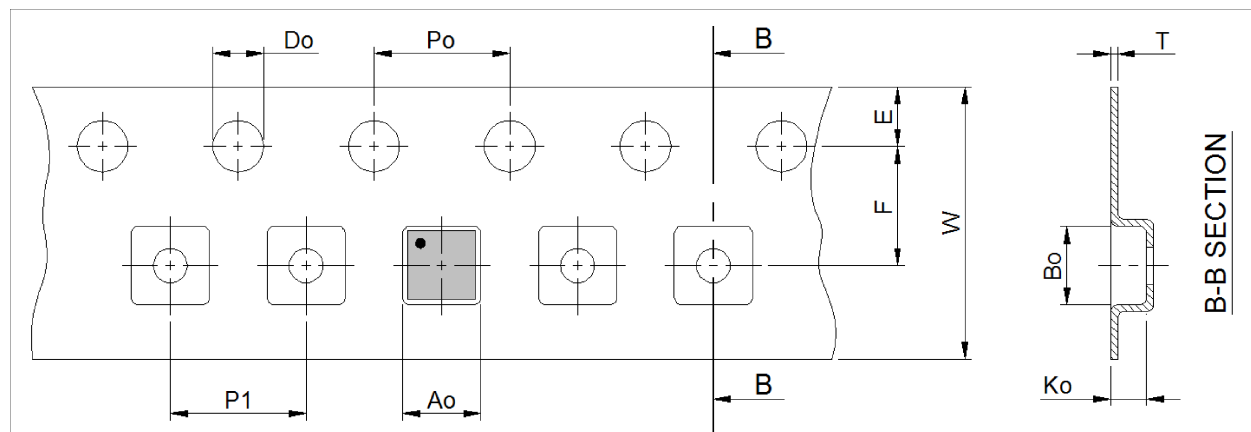
A Reverse Blocking 70 mΩ, 1.3 A nFET  
Load Switch in 1.46 mm<sup>2</sup> WLCSP

## Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
WLCSP9L 1.21 x 1.21 mm 0.4P Green	9	1.21 x 1.21 x 0.586	3,000	3,000	178 / 60	100	400	100	400	8	4

## Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width	Tape Thickness
	A0	B0	K0	P0	P1	D0	E	F	W	T
WLCSP 9L 1.21x 1.21 mm 0.4P Green	1.38	1.38	0.7	4	4	1.5	1.75	3.5	8	0.2



Note: 1.Orientation in carrier: Pin1 is at upper left corner (Quadrant 1).

Refer to EIA-481 specification

## SLG59H1341C

A Reverse Blocking 70 mΩ, 1.3 A nFET  
Load Switch in 1.46 mm<sup>2</sup> WLCSP

### Revision History

Date	Version	Change
18-Jul-2022	1.0	Production Release

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
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