RAA212832

4.5V to 72V Input, 0.5A Buck Regulator with 2 Linear Regulator Outputs

The RAA212832 is a triple output regulator combining a 4.5V to 72V input, 0.5A buck regulator with two LDO outputs. The buck regulator has a fixed switching frequency of 350kHz in Continuous Conduction mode (CCM) and operates in Pulse Skipping mode at lighter loads when it enters Discontinuous Conduction mode (DCM). The two LDOs operate from a 12V (or lower) input voltage. The LDOs are rated at 100mA and 50mA of output current. The buck regulator output is fixed at either 6V or 12V, which is controlled by the STBY pin. The LDOs can support an input voltage range of 6V to 12V and the output voltages are fixed at 3.3V and 5V. The IC provides a compact, highly integrated power management solution. Its integrated buck regulator and LDO outputs minimize system component count.

The buck converter uses peak current mode control, providing 500mA current for load and downstream LDO regulators, while the LDOs provide 5V and 3.3V regulated outputs for the system. The current-mode buck converter provides a fast transient response and cycle-by-cycle switching current limit. All output voltages are fixed internally with few external components required.

At light load or no-load operation on the buck regulator output, the RAA212832 operates in a Pulse Skipping mode in DCM. When the output load is increased, and the buck regulator enters CCM, the controller operates at 350kHz.

The RAA212832 offers comprehensive protection including UVLO, high-side overcurrent, output undervoltage, and over-temperature protection.

The device is available in SOIC8-E package.

Features

- Buck Converter:
  - 4.5V to 72V input voltage
  - Fixed output voltage 12V or 6V
  - 500mA output load capability
  - 0.6Ω high-side MOSEFT $r_{DS(ON)}$
  - Fixed switching frequency 350kHz in CCM operation
  - Pulse skipping mode in DCM operation
  - Standby function by STBY pin setting output voltage
  - High-side OCP, UVP, UVLO, OTP fault protection
- 5V LDO Regulator:
  - 6V to 12V input voltage
  - Fixed output voltage 5V
  - 100mA output load capability
  - Current limit foldback function
- 3.3V LDO Regulator:
  - 4.5V to 12V input voltage
  - Fixed output voltage 3.3V
  - 50mA output load capability
  - Current limit foldback function
- SOIC8-E package

Applications

- Electric-bike power management
- Motor driver control board power supply

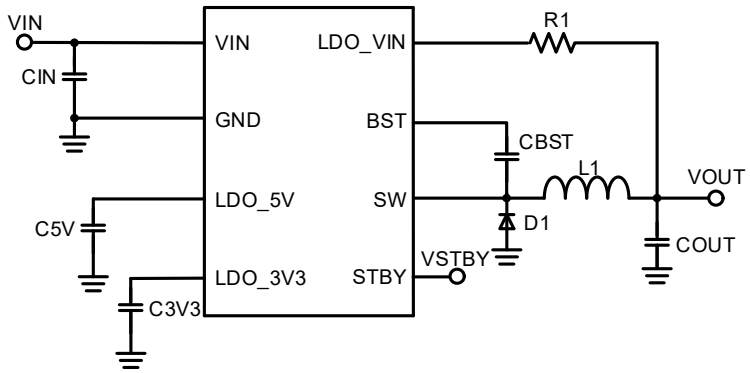


Figure 1. Typical Application Diagram

Contents

1. Overview

1.1 Block Diagram

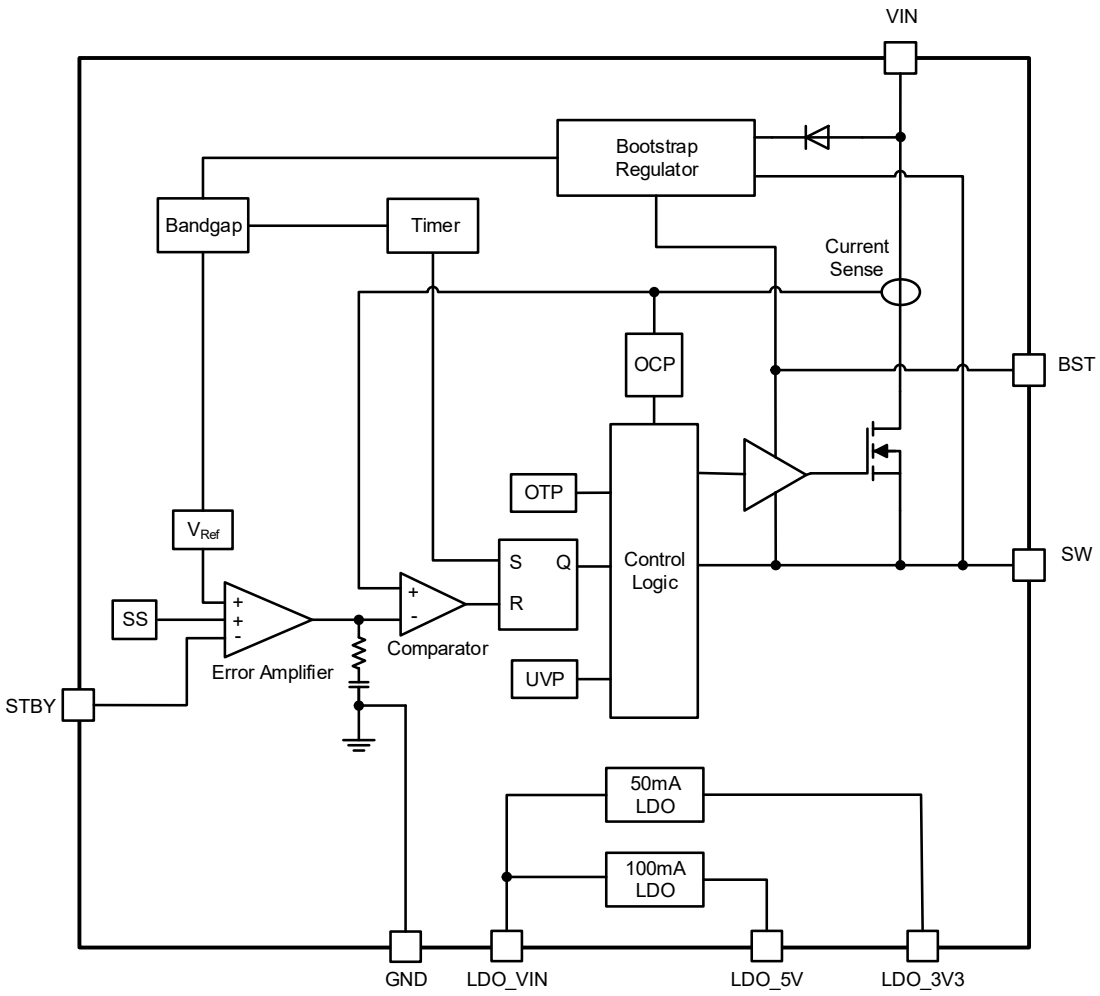
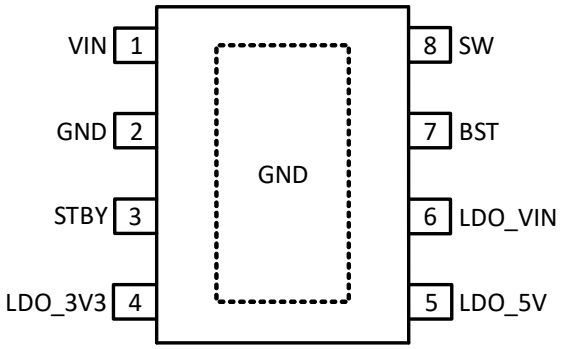


Figure 2. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	VIN	Input voltage for the IC and buck converter
2	GND	Ground
3	STBY	STBY mode pin. This signal is detected high and then the V_{OUT} of the buck converter is reduced from 12V down to 6V.
4	LDO_3V3	LDO output voltage, fixed 3.3V
5	LDO_5V	LDO output voltage, fixed 5V
6	LDO_VIN	Input voltage for the LDOs
7	BST	Bootstrap supply pin
8	SW	Switch node output

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VIN	-0.3	76	V
SW	-0.7	VIN + 0.3	V
BST		SW + 4	V
BST to SW	-0.3	4	V
LDO_VIN	-0.3	15	V
LDO_5V	-0.3	LDO_VIN + 0.3 or 6	V
LDO_3V3	-0.3	LDO_VIN + 0.3 or 4.3	V
All other pins	-0.3	4	V

3.2 ESD Ratings

ESD Model/Test	Rating	Unit
Human Body Model (Tested per JS-001-2017)	2	kV
Charged Device Model (Tested per JS-002-2018)	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100	mA

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Units
Supply Voltage, V_{IN}	4.5	72	V
Supply Voltage, LDO_VIN for both LDOs active	6	12	V
Supply Voltage, LDO_VIN for LDO_3V3 only	4.5	12	V
Output Current, I_{OUT}	0	0.5	A
Output Current, I_{LDO_5V}	0	0.1	A
Output Current, I_{LDO_3V3}	0	0.05	A

3.4 Thermal Specifications

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
SOIC8-E Package	48	7

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-40	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Ambient Temperature Range	-40	+125	°C
Pb-Free Reflow Profile	See TB493		

3.5 Electrical Specifications

V_{IN} = 24V, V_{OUT} = 12V, unless otherwise noted. Typical values are at TA= +25°C. **Boldface limits apply across the junction temperature range, -40°C to +125°C**.

Parameter	Symbol	Test Conditions	Minimum[1]	Typical	Maximum[1]	Unit
VIN Voltage Range	V_{IN}		**4.5**		**72**	V
Quiescent Current	I_Q	V_{FB} = 1.35V, no switching, included LDOs operation	240	325	400	µA
VIN Undervoltage Lockout	V_{UVLO_VIN}	V_{IN} Rising	**4**	4.25	**4.45**	V
VIN UVLO Hysteresis	$V_{HYS\_VIN-UVLO}$	V_{IN} Falling		250		mV
Switching Frequency Range	FS	V_{FB} = 1.25V	**318**	350	**389**	kHz
Foldback Frequency	FS	V_{FB} = 0V		90		kHz
Buck Output Voltage	V_{OUT}	V_{IN} = 24V, STBY = 0V,	**11.70**	12	**12.30**	V
		V_{IN} = 24V, STBY = 3V,	**5.85**	6	**6.15**	V
Peak Current Limit		Duty Cycle = 90%, 25°C	0.7	0.82	0.97	A
Minimum Off-Time		25°C, Boot voltage need to work for smaller minimum off-time		260		ns
Minimum On-Time		Need to regulate 350kHz, 72V_{IN} to 3.3V_{OUT}		92	105	ns
High-Side FET $r_{DS(ON)}$				600		mΩ
UVP		Fault threshold, V_{FB} falling, Soft-start completed		30		%
Internal Soft-Start Time				1.9		ms
Hiccup Timer				23		ms
Thermal Shutdown	OT			155		°C
Thermal hysteresis				20		°C

V_{IN} = 24V, V_{OUT} = 12V, unless otherwise noted. Typical values are at TA= +25°C. **Boldface limits apply across the junction temperature range, -40°C to +125°C**. (Cont.)

Parameter	Symbol	Test Conditions	Minimum[1]	Typical	Maximum[1]	Unit
LDO_3V3						
LDO_VIN Voltage Range	LDO_VIN		**4.5**		**12**	V
LDO_3.3V Voltage Range	LDO_3V3	I_{OUT} = 1mA to 50mA	**3.17**	3.3	**3.43**	V
LDO Supply Current		LDO_3V3 = 3.3V, I_{OUT} = 0A		40	**70**	µA
Current Limit		LDO_3V3 = 3.3V		75		mA
Current Limit Foldback		LDO_3V3 < 50% normal voltage		25		mA
PSRR		LDO_3V3 = 3.3V, I_{OUT} = 50mA, C_{OUT} = 4.7µF, FREQ = 100Hz		72		dB
		LDO_3V3 = 3.3V, I_{OUT} = 50mA, C_{OUT} = 4.7µF, FREQ = 10kHz		82		dB
		LDO_3V3 = 3.3V, I_{OUT} = 50mA, C_{OUT} = 4.7µF, FREQ = 100kHz		66		dB
Noise		I_{OUT} = 50mA, C_{OUT} = 4.7µF, BW = 10Hz - 100kHz		466		µVrms
LDO_5V						
LDO_VIN Voltage Range	LDO_VIN		**6**		**12**	V
LDO_5V Voltage Range	LDO_5V	I_{OUT} = 1mA to 100mA	**4.75**	5	**5.25**	V
LDO Supply Current		LDO_5V = 5V, I_{OUT} = 0A		40	**70**	µA
Current Limit		LDO_5V = 5V		150		mA
Current Limit Foldback		LDO_5V < 50% normal voltage		50		mA
PSRR		LDO_5V = 5V, I_{OUT} = 100mA, C_{OUT} = 4.7µF, FREQ = 100Hz		56		dB
		LDO_5V = 5V, I_{OUT} = 100mA, COUT = 4.7µF, FREQ = 10kHz		69		dB
		LDO_5V = 5V, I_{OUT} = 100mA, C_{OUT} = 4.7µF, FREQ = 100kHz		76		dB
Noise		I_{OUT} = 100mA, C_{OUT} = 4.7µF, BW = 10Hz - 100kHz		711		µVrms

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

4. Typical Performance Graphs

V_{IN} = 56V, V_{OUT} = 6V, T_A = +25°C, unless otherwise noted.

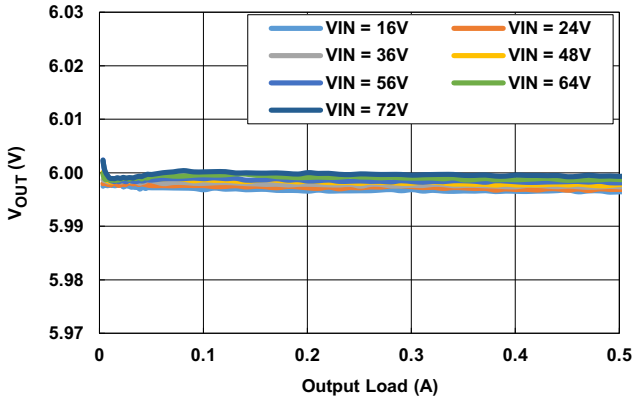


Figure 3. Load Regulation

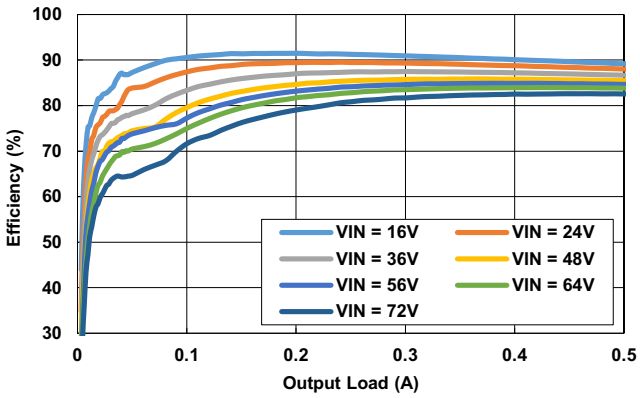


Figure 4. Efficiency

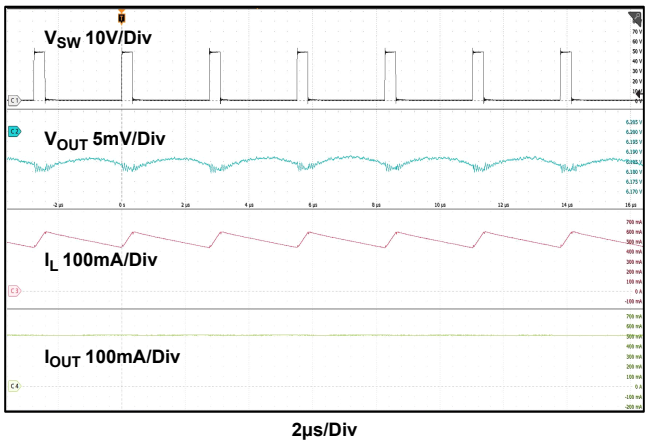


Figure 5. Buck Output Ripple at Full Load

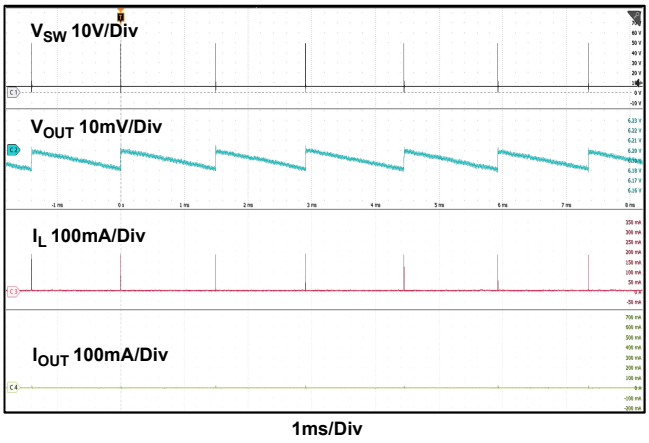


Figure 6. Buck Output Ripple at No Load

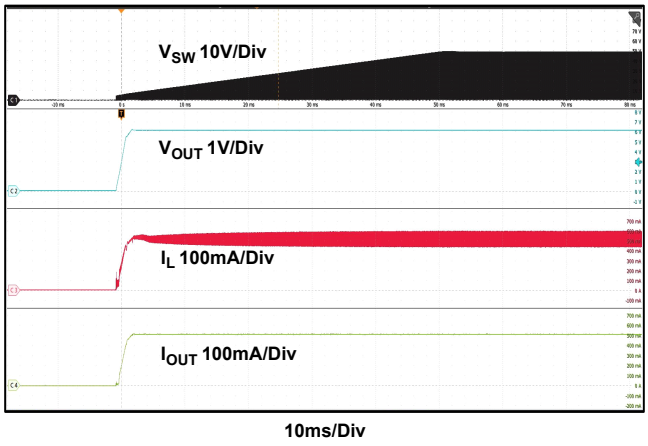


Figure 7. Power-On at Full Load

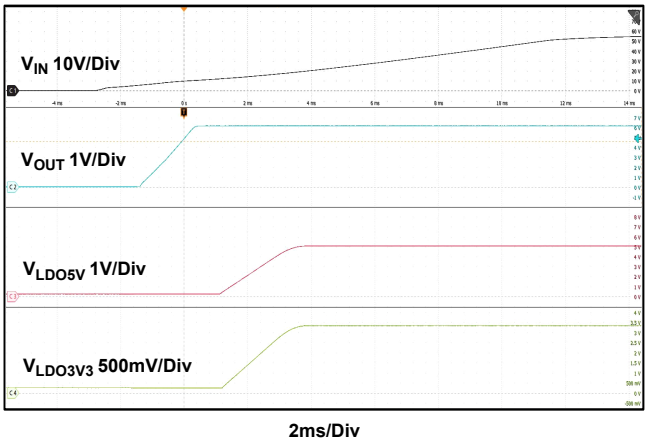


Figure 8. Power-On at Full Load with LDO Channels

V_{IN} = 56V, V_{OUT} = 6V, T_A = +25°C, unless otherwise noted.

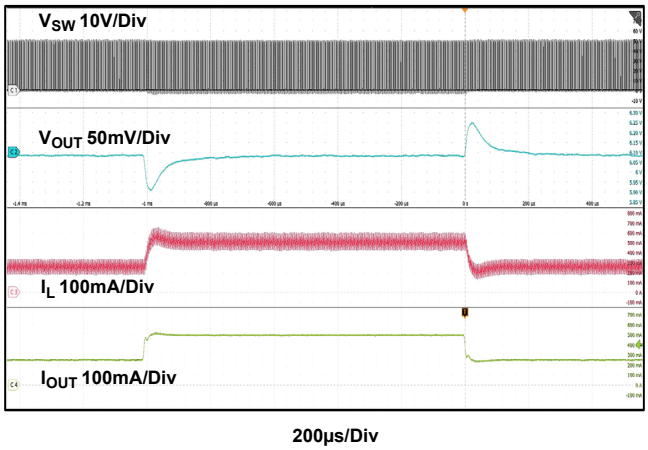


Figure 9. Load Transient between 0.25A to 0.5A

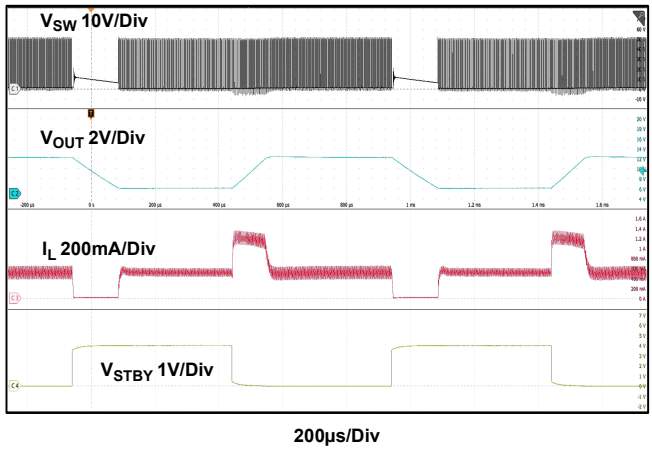


Figure 10. Standby Function at Full Load

V_{IN} = 56V, V_{OUT} = 12V, T_A = +25°C, unless otherwise noted.

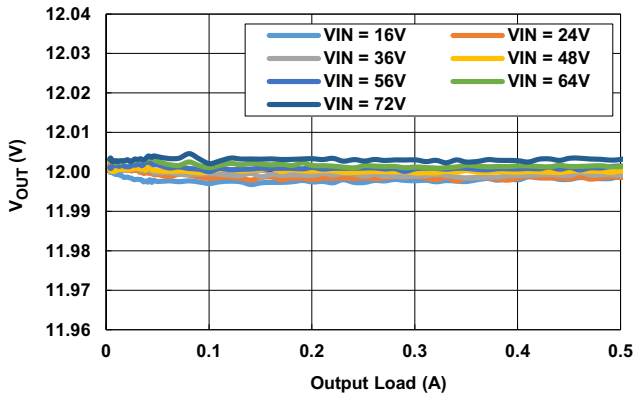


Figure 11. Load Regulation

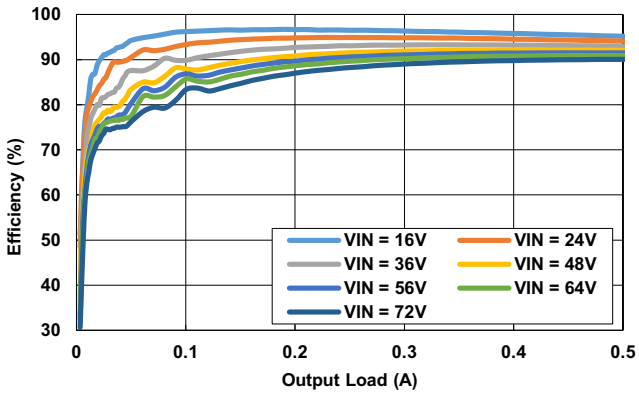


Figure 12. Efficiency

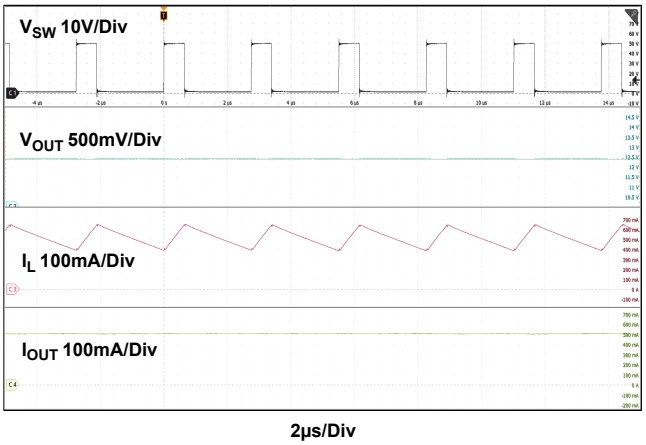


Figure 13. Buck Output Ripple at Full Load

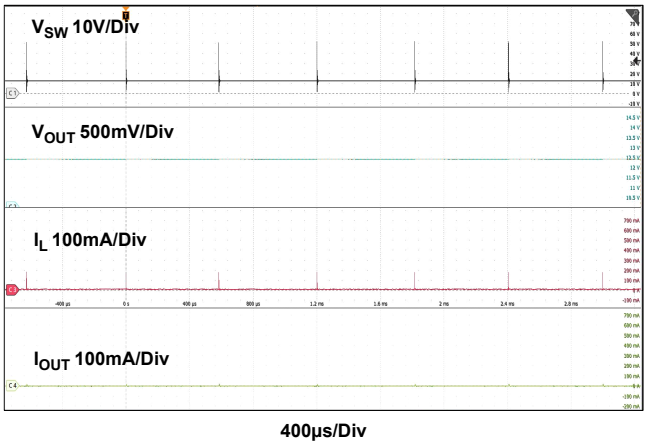


Figure 14. Buck Output Ripple at No Load

V_{IN} = 56V, V_{OUT} = 12V, T_A = +25°C, unless otherwise noted.

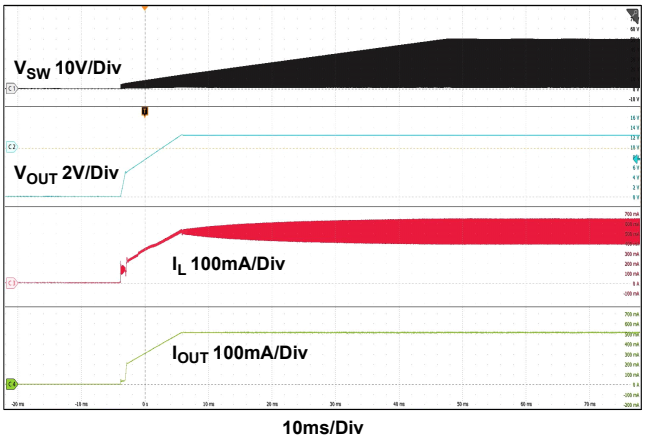


Figure 15. Power-On at Full Load

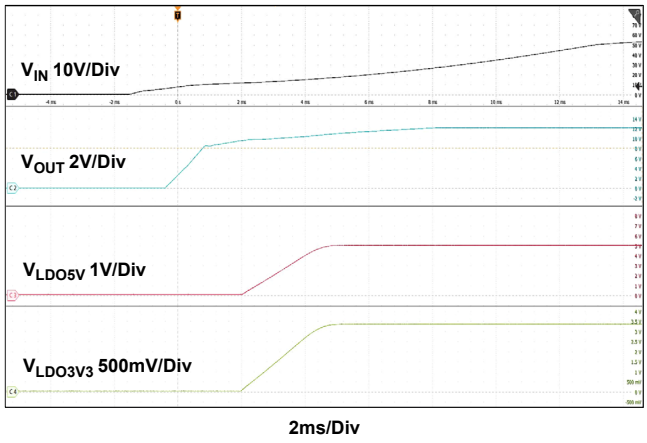


Figure 16. Power-On at Full Load with LDO Channels

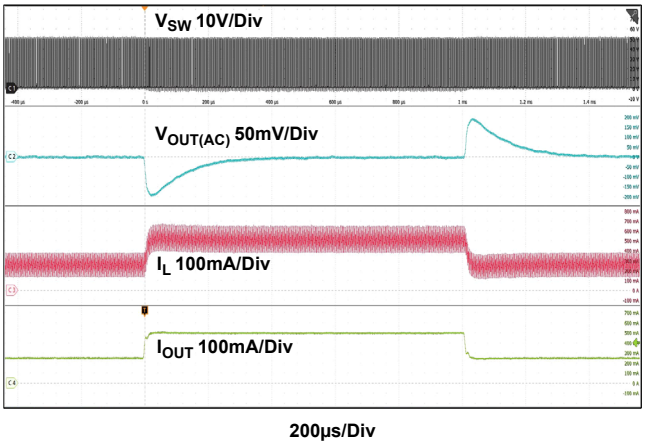


Figure 17. Load Transient between 0.25A to 0.5A

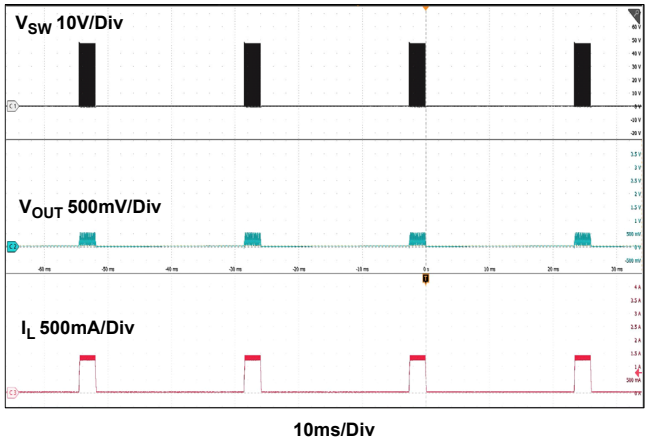


Figure 18. UVP Fault with Hiccup

V_{OUT} = VINLDO = 6V, VLDO5V = 5V, VLDO3V3 = 3.3V, T_A = +25°C, unless otherwise noted.

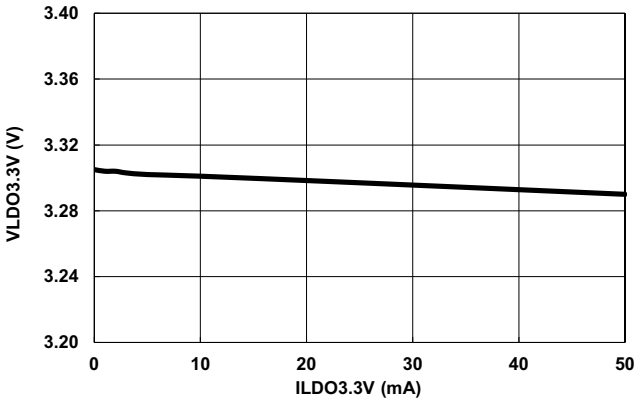


Figure 19. VLDO3V3 Load Regulation

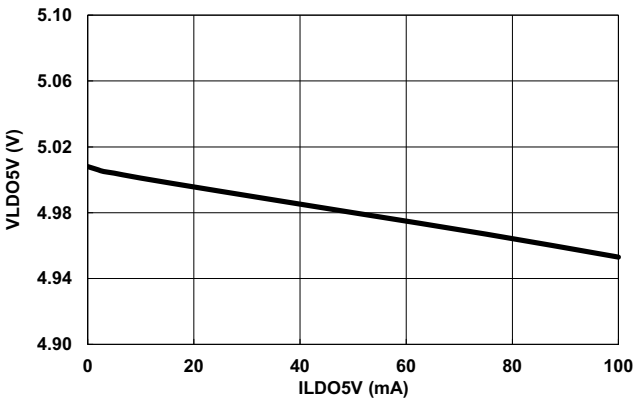


Figure 20. VLDO5V Load Regulation

V_{OUT} = VINLDO = 6V, VLDO5V = 5V, VLDO3V3 = 3.3V, T_A = +25°C, unless otherwise noted. (Cont.)

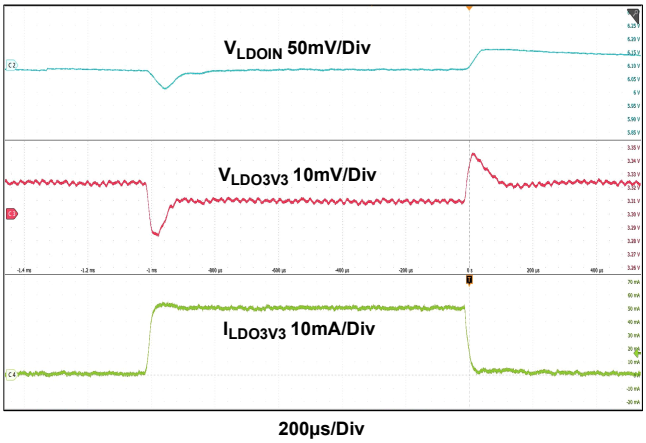


Figure 21. VLDO3V3 Load Transient between 0A to 0.05A

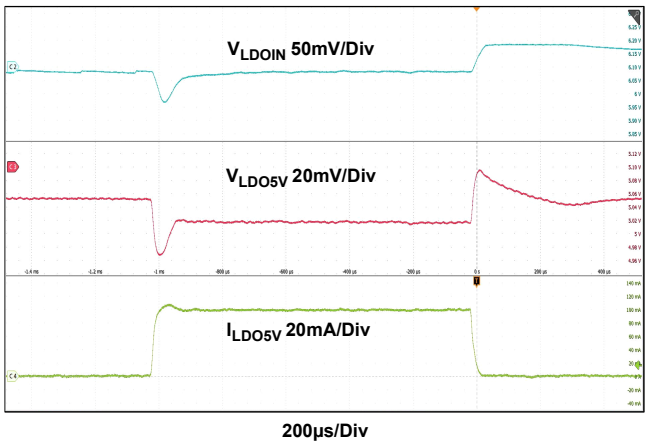


Figure 22. VLDO5V Load Transient between 0A to 0.1A

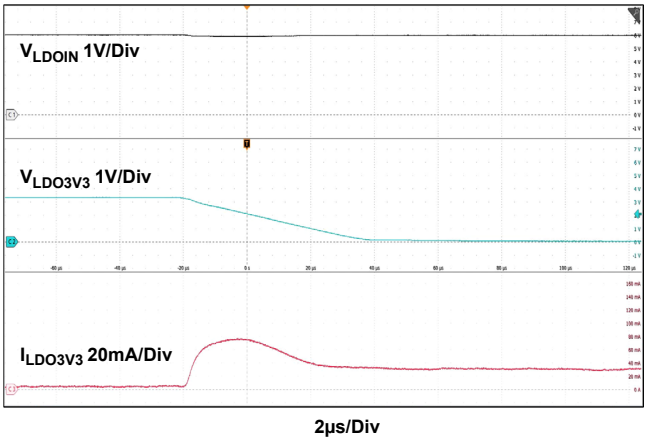


Figure 23. VLDO3V3 OCP Fault with Current Foldback

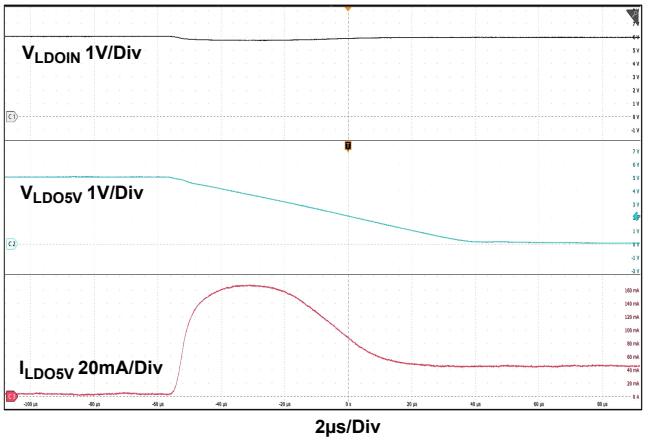


Figure 24. VLDO5V OCP Fault with Current Foldback

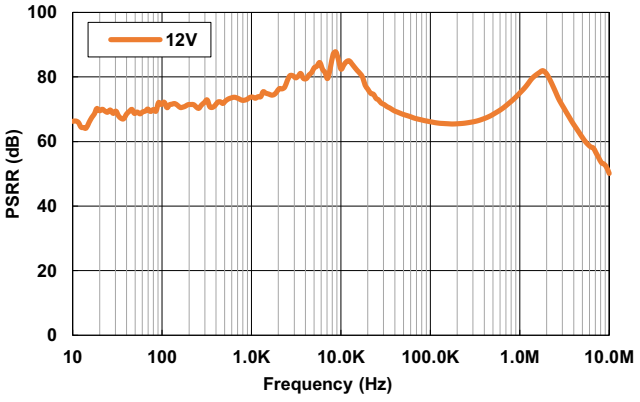


Figure 25. VLDO3V3 PSRR at Full Load

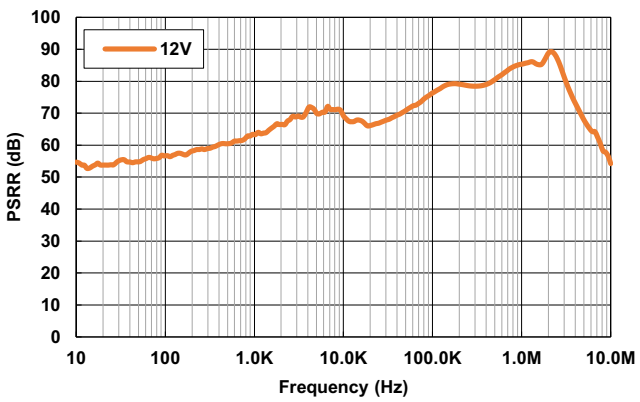


Figure 26. VLDO5V PSRR at Full Load

V_{OUT} = VINLDO = 6V, VLDO5V = 5V, VLDO3V3 = 3.3V, T_A = +25°C, unless otherwise noted. (Cont.)

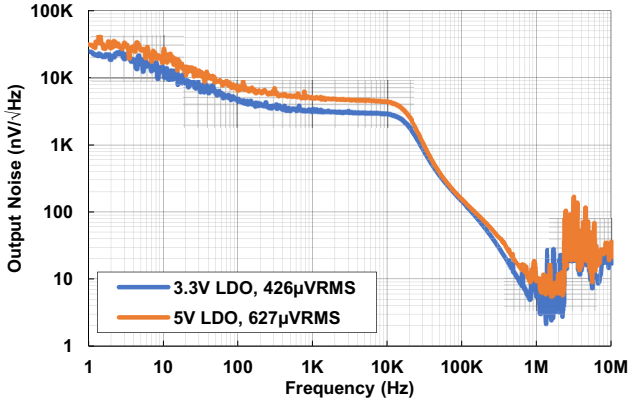


Figure 27. Output Noise vs Frequency
V_{OUT} = VINLDO = 6V, C_{OUT} = 4.7µF,0.1µF

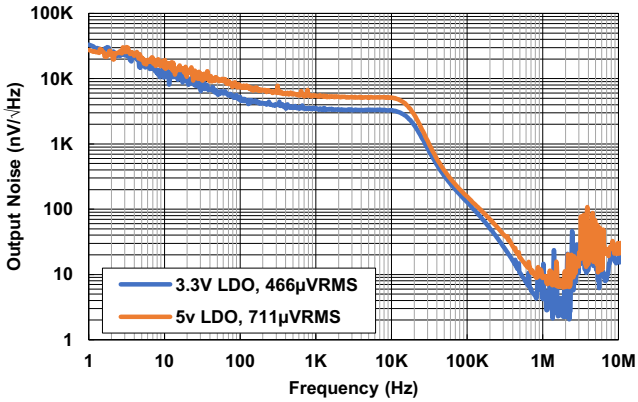


Figure 28. Output Noise vs Frequency
V_{OUT} = VINLDO = 12V, C_{OUT} = 4.7µF,0.1µF

5. Functional Description

The following operating description of the RAA212832 refers to the functional block diagram shown in Figure 2 and the application diagram shown in Figure 1. The RAA212832 generates a regulated output voltage by switching the internal NMOS control switch at constant frequency and variable duty cycle. The external inductor, freewheel diode, and output capacitor filter the switching waveform and create the DC output voltage.

A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal NMOS control switch. During this on-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current sense amplifier that generates an output proportional to the switch current. The sense signal is summed with the corrective ramp of the regulator and is compared to the output of the error amplifier, which is proportional to the difference between the feedback voltage and VREF.

When the PWM comparator output goes high, the output switch turns off until the next switching cycle begins. During the switch off-time, the inductor current discharges through the Schottky freewheel diode, forcing the SW pin to swing below ground by the forward voltage (VD) of the Schottky freewheel diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

To increase the light load efficiency of the buck converter, the chip enters Pulse Skipping mode and reduces the switching frequency. This occurs when the reduction in load current causes the buck regulator to transition from CCM to DCM. If the output load on buck converter is increased, CCM operation resumes and the PWM switching frequency is fixed at 350kHz.

The buck output voltage should be connected to the LDO_VIN pin to provide bias for LDO_3V3 and LDO_5V. The LDO_VIN pin is also used as an undervoltage monitor for the buck output voltage.

5.1 Soft-Start for Buck

Soft-start forces the regulator output to ramp up in a controlled fashion, which helps reduce input inrush current into the buck output capacitors. During the soft-start period for the buck converter, the reference voltage of the error amplifier ramps from 0V to its nominal value of 1.25V in approximately 1.8ms.

5.2 Soft-Start for LDOs

This function forces the LDOs output voltages to increase at a controlled rate during start-up. During soft-start for the two LDOs, the reference voltage of the error amplifier ramps from 0V to its nominal value of 1.25V in approximately 2.550ms.

5.3 Undervoltage Lockout

Undervoltage lockout (UVLO) prevents the RAA212832 from operating until the input voltage exceeds 4.25V (typical). The UVLO threshold has approximately 250mV of hysteresis; therefore, the device operates until V_{IN} drops below 4V (typical). Hysteresis prevents the part from turning off during power up if V_{IN} is non-monotonic.

5.4 Current Limit for Buck

The RAA212832 uses cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 0.82A (typical) and turns off the switch until the next switching cycle begins.

To reduce the current limit at low duty cycle, the RAA212832 has a frequency foldback function that depends on the feedback voltage to control the switching frequency. For example, if the feedback voltage is 0V, the switching frequency is 90kHz (typical).

5.5 Current Limit for LDOs

The RAA212832 has internal current limiting functionality to protect the regulator during fault conditions. The RAA212832 has two levels of current limit protection. During an overcurrent event, when the output voltage has fallen to less than 50% of the nominal setpoint voltage, the chip enters current limit foldback operation with a lower current limit value. If the short or overload is removed from the LDO output, the output returns to normal voltage regulation mode.

5.6 Output Undervoltage Protection for Buck

The undervoltage comparator compares the LDO_VIN pin voltage to a reference level that is 30% of the buck output voltage. Assuming the buck output voltage is set to 12V, and this voltage drops below 30% of nominal setpoint (3.6V), and the chip is also operating in current limit protection mode, the controller turns off the internal high-side FET and engage hiccup mode operation. When this fault is removed and V_{OUT} is above 30% of nominal setpoint (3.6V), the buck output rail returns to normal voltage regulation mode.

5.7 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 155°C (typical). After thermal shutdown occurs, the output switch does not turn on until the junction temperature drops to approximately 135°C (typical).

6. Applications Information

6.1 Input Capacitor Selection

The input capacitor is used in Buck converter to maintain the input voltage by suppressing the voltage ripple induced by discontinuous switching current. The required RMS current rating $I_{IN(RMS)}$ of the input capacitor is calculated using Equation 1 where $I_{OUT(MAX)}$ is the maximum average load current and D is the duty ratio..

(EQ. 1) $$I_{IN(RMS)} = I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

When D equals 0.5, $I_{IN(RMS)}$ has the maximum value which is $I_{OUT(MAX)}/2$.

The voltage rating of the input capacitor should be higher than the maximum input voltage. The required capacitance C_{IN} of the input capacitor to ensure the expected peak-to-peak input voltage ripple ΔV_{IN} is calculated using Equation 2 where f_{sw} is the switching frequency. :

(EQ. 2) $$C_{IN} = I_{OUT(MAX)} \times \frac{D \times (1 - D)}{f_{SW} \times \Delta V_{IN}}$$

The required capacitance also has the maximum value when D equals 0.5. It is suggested to use ceramic capacitors as input capacitor, which has low ESR and low ESL. When selecting the ceramic capacitor, it should be considered that the effective capacitance reduces with DC bias voltage across it. Also, Renesas recommends using X7R ceramic capacitors because of their small temperature coefficient.

If the part is connected to the power source through a high impedance path, Renesas recommends adding an electrolytic capacitor in addition to the ceramic capacitor to damp the input voltage oscillation.

6.2 Output Voltage for Buck and LDOs

The output voltage for the buck regulator output is fixed at 6V or 12V and is controlled by the STBY pin.

The output voltage for the LDO_3V3 rail is fixed at 3.3V. The output voltage for the LDO_5V rail is fixed at 5V. Renesas recommends using the buck output voltage to supply LDO_VIN between 6V and 12V for both LDOs to be operational. If only the LDO_3V3 rail is required, LDO_VIN can be between 4.5V and 12V, with LDO_5V failing to regulate.

6.3 Inductor Selection

The inductor value determines the ripple current of the buck converter. A reasonable starting point for choosing the ripple current, ΔI_L, is 30% to 60% of total load current. The inductor value is then calculated using Equation 3:

(EQ. 3) $$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times \Delta I} \times \frac{V_{OUT}}{V_{IN}}$$

As an example, using V_{IN} = 56V, V_{OUT} = 12V, f_{SW} is fixed at 350kHz, I_{OUT} = 500mA, and $\Delta I/I_{OUT}$ = 45%, the inductance is calculated as follows:

(EQ. 4) $$L = \frac{56V - 12V}{350kHz \times 0.45 \times 500mA} \times \frac{12V}{56V} = 120\mu H$$

Increasing the inductance value reduces the ripple current and the ripple voltage. However, the larger inductance value may reduce the response time of the converter to a load transient. **Note:** The inductor current rating should not be exceeded in overcurrent conditions to avoid saturation.

For lowest loss and smallest output voltage ripple, chose an inductor with the smallest possible DC resistance, provided its mechanical dimensions meet application requirements. For typical RAA212832 applications, inductor values generally lie in the 70µH to 120µH range. See Table 1 when selecting the inductor value for typical values of V_{OUT}.

6.4 Output Capacitor Selection (Buck)

The output capacitor determines both steady state performance and transient performance of the Buck converter. Factors such as output voltage ripple, output voltage variation during transients, and control loop stability should be considered when selecting the output capacitor. X7R dielectric ceramic capacitors are recommended.
Note: When selecting the ceramic capacitor, the actual capacitance may be considerably lower than the advertised value. Consult the datasheet of the manufacturer to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published; however, an assumption of ~20% further reduction generally suffices. The result of these considerations may mean an effective capacitance 50% lower than nominal, and this value

should be used in all design calculations. However, ceramic capacitors are a good choice in many applications because of their reliability and extremely low ESR.

For the ceramic capacitor, its capacitance is dominating the voltage ripple. Therefore, the required capacitance $C_{OUT(RIPPLE)}$ for the expected peak-to-peak output voltage ripple $\Delta V_{OUT(RIPPLE)}$ is calculated using Equation 5 where ΔI_L is the peak-to-peak inductor ripple current, f_{sw} is fixed at 350kHz, and $\Delta V_{OUT(RIPPLE)}$ is required ripple voltage.

(EQ. 5)
$$C_{OUT(RIPPLE)} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT(RIPPLE)}}$$

To meet the output voltage variation requirements during load transient with step up and step down, the required capacitance $C_{OUT(STEPUP)}$ is calculated using Equation 6 and $C_{OUT(STEPDOWN)}$ is calculated using Equation 7 where L is the inductor value, I_{STEP} is the transient load step, ΔI_L is the peak-to-peak inductor ripple current, and ΔV_{OUT} is the expected voltage variation during the transient.:

(EQ. 6)
$$C_{OUT(STEPUP)} = \frac{L \times \left(I_{STEP} + \frac{\Delta I_L}{2}\right)^2}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT}}$$

(EQ. 7)
$$C_{OUT(RIPPLE)} = \frac{L \times \left(I_{STEP} + \frac{\Delta I_L}{2}\right)^2}{2 \times V_{OUT} \times \Delta V_{OUT}}$$

For convenience, Table 1 can be referenced when selecting output capacitors for typical V_{OUT} applications.

6.5 Output Capacitor Selection (LDOs)

For a compact and high performance solution, the RAA212832 has two integrated LDOs that are designed specifically to work with low ESR X7R ceramic output capacitors. Using an X7R ceramic capacitor with capacitance of at least 4.7µF and ESR larger than 1mΩ on the RAA212832 output ensures stability. Nevertheless, the RAA212832 still works well with other types of output capacitors that have higher ESR values. Place the output capacitor no more than 0.5 inch from the output pin of the RAA212832.

6.6 Diode Selection

The RAA212832 requires a freewheeling diode for inductor current to flow when the internal high-side MOSFET is turned off. Select a diode with reverse voltage rating at least 20% higher than the maximum input voltage. The continuous current rating of the diode should be greater than the highest output current. For better efficiency, select a diode with low forward voltage drop and fast reverse recovery time. Schottky diodes are recommended for this application

6.7 Boot Capacitor Selection

A capacitor is needed between BST pin and SW pin to provide gate voltage for the high-side internal MOSFET. Renesas recommends using a 16V X7R 0.1µF ceramic capacitor as the bootstrap capacitor for most applications.

Table 1. Recommended Components Selection for Typical Applications

STBY (V)	V_{OUT} (V)	L (µH)	C_{OUT} for Buck	C_{OUT} for LDOs
3	6	60	2×10µF/1206/35V/X7R	4.7µF/0805/10V/X7R
0	12	120	2×10µF/1206/35V/X7R	4.7µF/0805/10V/X7R

7. Layout Guidelines

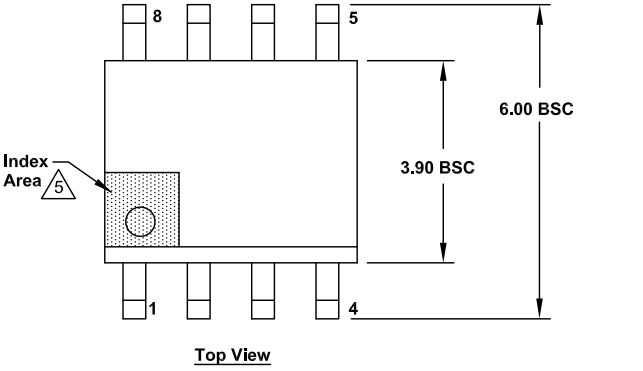
- Place the input ceramic capacitor(s) as close as possible to the IC VIN pin and the diode. Keep the power loop (input ceramic capacitor, IC VIN pin, and diode) as small as possible to minimize VSW node voltage ringing induced by trace parasitic inductance. This also results in better EMI performance.
- If an aluminum electrolytic capacitor is used, place it as close as possible to the IC VIN pin.
- Keep the VSW node copper area small for less parasitic capacitance but large enough to handle the load current.
- Place the output capacitor(s) close to the inductor and freewheel diode.
- Connect the power ground (CIN, diode, and COUT ground) to the analog ground plane, which connects to the GND pin. Use a single point connection.
- Route the buck output etches close to the LDO_VIN pin and away from the VSW node.

8. Package Outline Drawing

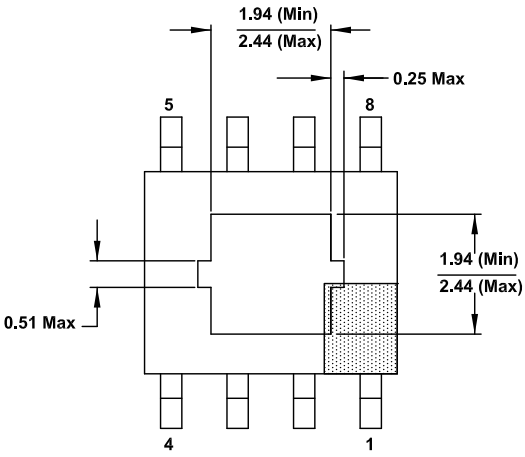
For the most recent package outline drawing, see M8.15H.

M8.15H

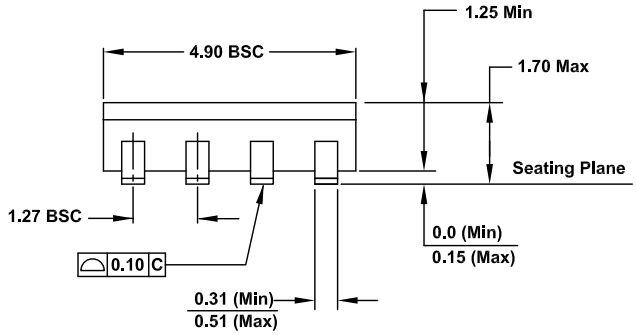
8 Lead Narrow Body Small Outline Exposed Pad Plastic Package (EPSOIC)
Rev 1, 1/20



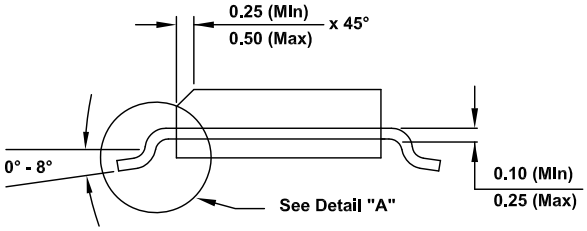
Top View



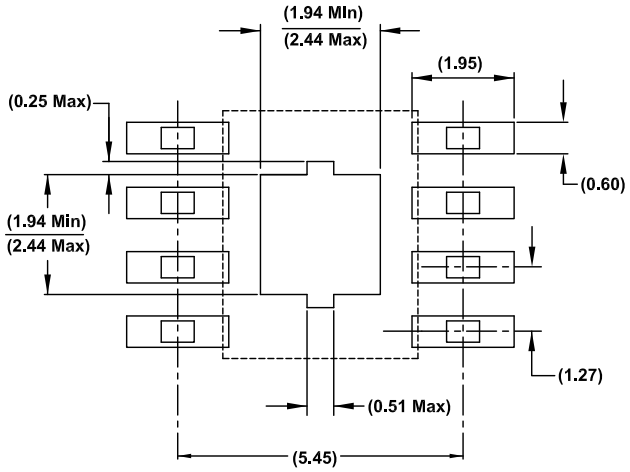
Bottom View



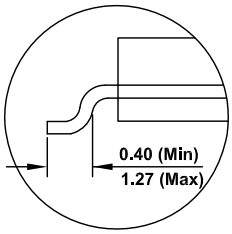
Side View



End View



Typical Recommended Land Pattern



Detail 'A'

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.255mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

9. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp Range
RAA2128324GSP#HA0	RAA 212832	8 Ld EPSOIC	M8.15H	Reel, 2.5k	-40 to +125°C
RTKA212832DR0000BU	Demonstration Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Moisture Sensitivity Level (MSL), see the RAA212832 product page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

Table 2. Key Differences Between Family of Parts

Part Number	Buck V_{OUT}	Pin Difference
RAA212831	1.25V to V_{IN}×Dmax by FB resistor settings	FB Pin
RAA212832	6V or 12V by STBY pin settings	STBY Pin

10. Revision History

Revision	Date	Description
1.02	Mar 13, 2023	Updated Table 2.
1.01	Apr 19, 2022	Updated 3.3V LDO input voltage bullet on page 1. Added Supply Voltage, LDO_VIN for LDO_3V3 only operating condition. Updated the following specifications in the Electrical Specifications section: ▪ Changed Switching Frequency Range minimum value from 317.8kHz to 318kHz and the maximum spec from 388.5kHz to 389kHz. ▪ Changed Buck Output Voltage test conditions, minimum values from 11.82V to 11.70V and 11.64V to 5.85V, and maximum values from 12.18V to 12.30V and from 12.36V to 6.15V. Also, updated typical for the second one from 12V to 6V. ▪ Added Min On-Time maximum specification value and changed typical from 96ns to 92ns. ▪ Changed LDO_VIN Voltage Range minimum spec from 6V to 4.5V. ▪ Changed LDO_3.3V Voltage Range minimum spec from 3.168V to 3.17V and the maximum spec from 3.432V to 3.43V. ▪ Updated LDO_3V3 PSRR Test conditions and typical values from 58dB to 72dB, from 40dB to 82dB, and from 28dB to 66dB. ▪ Updated LDO_5V Voltage Range changed minimum value from 4.8V to 4.75V and the maximum from 5.2V to 5.25V. ▪ Updated LDO_5V PSRR Test conditions and typical values from 58dB to 56dB, from 40dB to 69dB, and from 28dB to 76dB. ▪ Added Output Current and Noise specifications for both LDO_3V3 and LDO_5V. Updated Figures 25 and 26. Added Figures 27 and 28. Updated Output Voltage for Buck and LDOs section. Updated Ordering information table.
1.00	Sep 27, 2021	Initial release.

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