

F2934

High Reliability SP2T RF Switch 50MHz to 6000MHz

The F2934 is a high reliability, low insertion loss, 50Ω SP2T absorptive RF switch designed for a multitude of wireless and other RF applications. This device covers a broad frequency range from 50MHz to 6000MHz. In addition to providing low insertion loss, the F2934 delivers high linearity and high isolation performance while providing a 50Ω termination to the unused RF input ports.

The F2934 uses a single positive supply voltage of 2.7V to 5.25V supporting three states using either 3.3V or 1.8V control logic.

Competitive Advantage

The F2934 provides the following advantages:

- Constant impedance $K_{|Z|}$ during switching transition
- Insertion Loss = 0.8dB (at 2GHz)
- RFX to RFC Isolation = 73dB (at 2GHz)
- IIP3 = +61dBm (at 2GHz)
- Active Port Operating Power Handling = 34dBm
- Term Port Operating Power Handling = 27dBm

Block Diagram

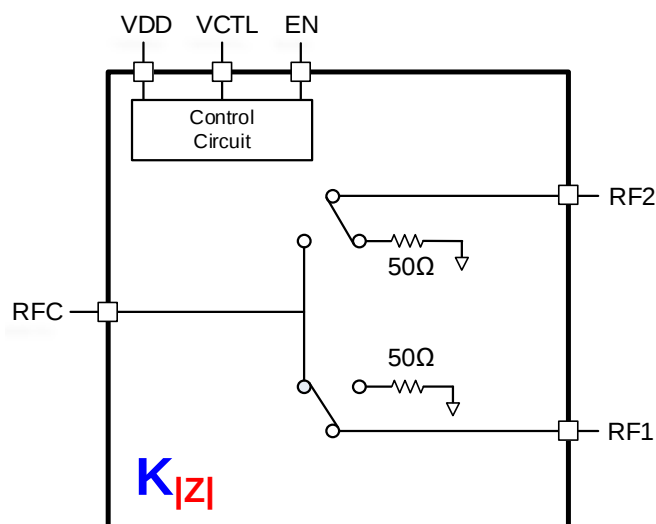


Figure 1. Block Diagram

Features

- High Isolation:
 - 74dB at 1GHz
 - 73dB at 2GHz
 - 70dB at 3GHz
 - 66dB at 4GHz
- High Linearity:
 - IIP3 of 61dBm at 2GHz
- Wide single 2.75V to 5.25V supply voltage range
- 3.3V and 1.8V compatible control logic
- Operating temperature -40°C to +105°C
- 3 × 3 mm 16-VFQFPN package

Applications

- Base Station 2G, 3G, 4G, 5G
- Portable Wireless
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- WIMAX Receivers and Transmitters
- Military Systems and JTRS radios
- RFID handheld and portable readers
- Test / ATE Equipment

Contents

1. Pin Information	4
1.1 Pin Assignments	4
1.2 Pin Descriptions	4
2. Specifications	5
2.1 Absolute Maximum Ratings	5
2.2 Recommended Operating Conditions	6
2.3 Thermal Information	7
2.4 Electrical Specifications	8
3. Control Mode	10
4. Typical Performance Graphs	10
5. Application Information	14
5.1 Default Start-up	14
5.2 Logic Control	14
5.3 Power Supplies	14
5.4 Control Pin Interface	14
6. Evaluation Board	15
6.1 Board Images	15
6.2 Setup and Configuration	16
6.2.1. External Supply Setup	16
6.2.2. Logic Control Setup	16
6.2.3. Turn On Procedure	16
6.2.4. Turn Off Procedure	16
6.3 Application Circuit	17
6.4 Bill of Materials	17
7. Package Outline Drawings	18
8. Ordering Information	18
9. Revision History	18

Figures

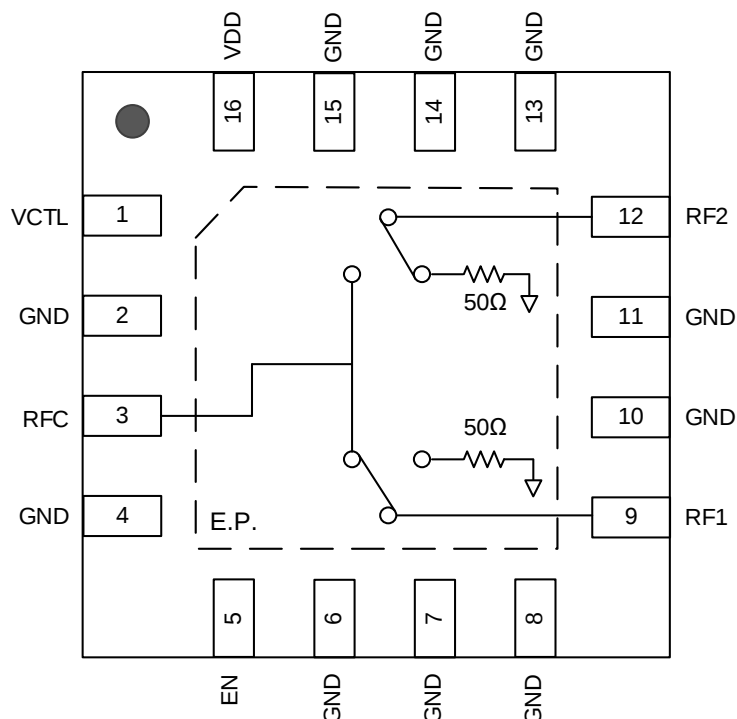
Figure 1. Block Diagram	1
Figure 2. Maximum RF Input Operating Power vs. Frequency	7
Figure 3. RF1 - RFC Insertion Loss.....	11
Figure 4. RF2 - RFC Insertion Loss.....	11
Figure 5. RF1 Return Loss	11
Figure 6. RF2 Return Loss	11
Figure 7. RFC Return Loss.....	11
Figure 8. RF1 to RF2 Isolation.....	11
Figure 9. RF1 to RFC Isolation	12
Figure 10. RF2 to RFC Isolation	12
Figure 11. Input IP3	12
Figure 12. P0.1dB Compression (50MHz).....	12
Figure 13. P0.1dB Compression (2GHz).....	12
Figure 14. P0.1dB Compression (3GHz).....	12
Figure 15. P0.1dB Compression (4GHz).....	13
Figure 16. T _{ON} Switching Time	13
Figure 17. T _{OFF} Switching Time	13
Figure 18. Typical Application Circuit	14
Figure 19. Evaluation Board – Top View	15
Figure 20. Evaluation Board – Bottom View.....	15

Tables

Table 1. Pin Descriptions	4
Table 2. Switch Control Truth Table	10
Table 3. Bill of Materials (BOM).....	17

1. Pin Information

1.1 Pin Assignments



1.2 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	VCTL	Controls the selected path when EN is low. It is disabled when EN is logic high (see Table 2).
2, 4, 6, 7, 8, 10, 11, 13, 14, 15	GND	Ground. Also, internally connected to the ground paddle. Ground this pin as close to the device as possible.
3	RFC	RF Common Port. Matched to 50Ω when one of the two RF ports is selected. If this pin is not 0V DC then an external coupling capacitor must be used.
5	EN	EN as a logic low allows VCTL to control the selected switch path. With EN set to logic high puts the part in all paths off state and disables the control of VCTL (Table 2).
9	RF1	RF1 Port. Matched to 50Ω. If this pin is not 0V DC, then an external coupling capacitor must be used.
12	RF2	RF2 Port. Matched to 50Ω. If this pin is not 0V DC, then an external coupling capacitor must be used.
16	VDD	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
	EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device and into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

2. Specifications

2.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F2934 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Parameter		Symbol	Minimum	Maximum	Unit
VDD to GND		V _{DD}	-0.3	+5.5	V
VCTL, EN to GND		V _{logic}	-0.3	3.6	V
RF1, RF2, RFC to GND		V _{RF}	-0.3	+0.3	V
RF Input Power ^[1]	RF1 or RF2 as an input (Connected to RFC)	P _{RF12}		36 ^[2]	dBm
	RFC as an input (Connected to RF1 or RF2)	P _{RF12}		36	
	RFC as an input (All off state)	P _{RF12_OFF}		30	
	RF1 or RF2 as input (Terminated states)	P _{RF12_TERM}		30 ^[2]	
	RF1 and RF2 as inputs (All off state)	P _{RF12_OFF}		30 ^[2]	
Maximum Junction Temperature		T _{Jmax}		+125	°C
Storage Temperature Range		T _{ST}	-65	+150	°C
Lead Temperature (soldering, 10s)		T _{LEAD}		+260	°C
ESD Voltage – HBM (Per JESD22-A114)		V _{ESDHBM}		1000	V
ESD Voltage – CDM (Per JESD22-C101)		V _{ESDCDM}		500	V

1. VDD = 2.7V to 5.25V, 250MHz ≤ FRF ≤ 6000MHz, T_c = 105°C, Z_S = Z_L = 50Ω.
2. Each port.

2.2 Recommended Operating Conditions

Parameter	Symbol	Conditions		Minimum	Typical	Maximum	Unit
Supply Voltage	V_{DD}			2.7		5.25	V
Operating Temperature Range	T_{CASE}	Exposed Paddle Temperature		-40		+105	°C
RF Frequency Range	F_{RF}			50		6000	MHz
RF Continuous Input CW Power (Non-Switched)	P_{RF}	RFC connected to RF1 or RF2 ^[2]	$T_C = 85^\circ\text{C}$			34	dBm
			$T_C = 105^\circ\text{C}$			34	
		RF1/ RF2 Input, Terminated State ^{[3][4]}	$T_C = 85^\circ\text{C}$			27	
			$T_C = 105^\circ\text{C}$			27	
		RFC Input, All off State	$T_C = 85^\circ\text{C}$			27	
			$T_C = 105^\circ\text{C}$			27	
RF Continuous Input Power (RF Hot Switching CW) ^[1]	$P_{RF\text{SW}}$	RFC Input, switching between RF1 and RF2.	$T_C = 85^\circ\text{C}$			30	dBm
			$T_C = 105^\circ\text{C}$			30	
		RFC Input, switching into or out of, All off State.	$T_C = 85^\circ\text{C}$			27	
			$T_C = 105^\circ\text{C}$			27	
		RF1 or RF2 as input, switched between RFC and Term.	$T_C = 85^\circ\text{C}$			27	
			$T_C = 105^\circ\text{C}$			27	
		RF1 and RF2 as inputs, switching into or out of All off State. ^[4]	$T_C = 85^\circ\text{C}$			27	
			$T_C = 105^\circ\text{C}$			27	
RF1/2 Port Impedance	Z_{RFx}				50		Ω
RFC Port Impedance	Z_{RFC}				50		Ω

1. Levels based on: $V_{DD} = 3.1\text{V to } 5.25\text{V}$, $250\text{MHz} \leq F_{RF} \leq 6000\text{MHz}$, $Z_S = Z_L = 50\Omega$. See Figure 2 for power handling derating vs. RF frequency.
2. Input could be: RFC, RF1, or RF2 (applied to only one input).
3. Any RF1 / RF2 termination state. Power level specified is for each port.
4. Power level specified is for each port.

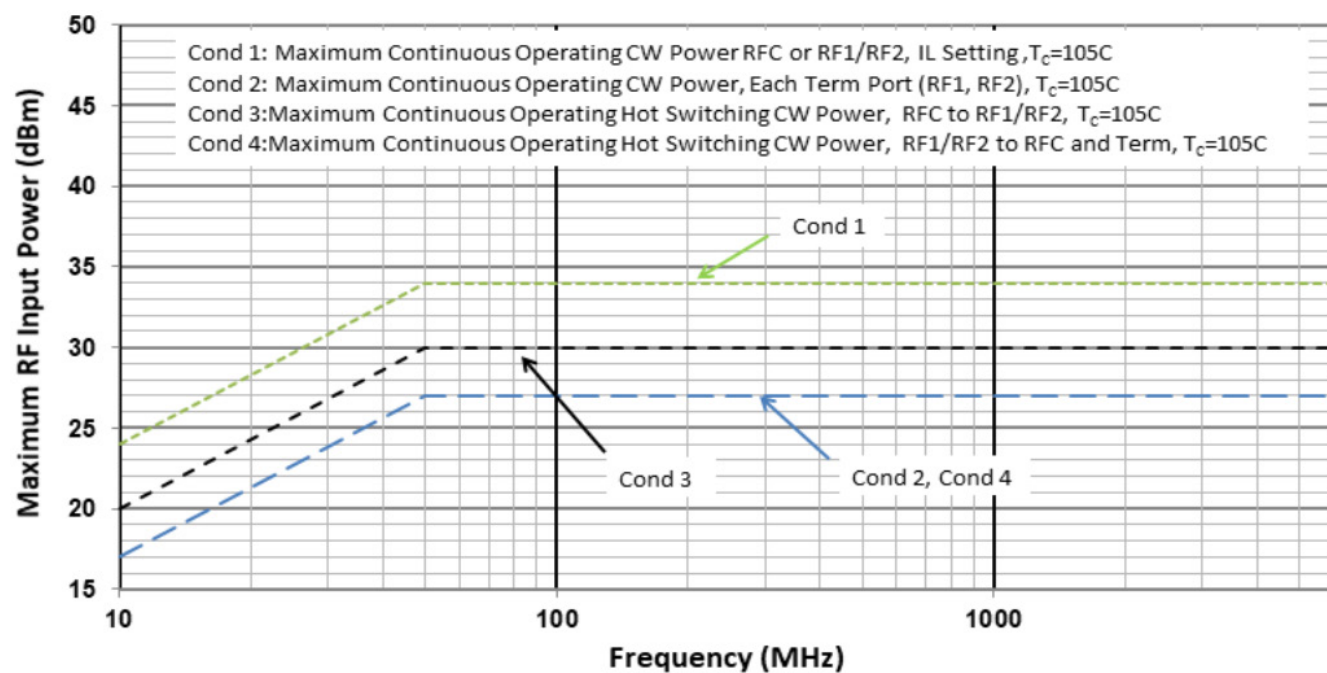


Figure 2. Maximum RF Input Operating Power vs. Frequency

2.3 Thermal Information

Symbol	Parameter	Value	Units
Θ_{JA}	Theta JA. Junction to ambient.	46.3	$^{\circ}\text{C/W}$
Θ_{JC}	Theta JC. Junction to case. The case is defined as the exposed paddle.	1.5	$^{\circ}\text{C/W}$
MSL	Moisture Sensitivity Rating (Per J-STD-020)	MSL1	

2.4 Electrical Specifications

Typical Application Circuit, $V_{DD} = 5.0V$, $T_C = +25^\circ C$, $F_{RF} = 2000MHz$, Driven Port = RF1, RF2, input power = 10dBm, $Z_S = Z_L = 50\Omega$, PCB board trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Logic Input High Threshold	V_{IH}		1.1		3.6	V
Logic Input Low Threshold	V_{IL}		-0.3		0.6	V
Logic Current	I_{IH}, I_{IL}	For each control pin	-1		+1	μA
DC Current	I_{DD}	$V_{DD} = 3.3 V$		205	400 ^[1]	μA
		$V_{DD} = 5.0 V$		250	450	
Insertion Loss RFC to RF1 / RF2	I_L	50MHz		0.7		dB
		1GHz		0.8		
		2GHz		0.8	1	
		3GHz		0.9		
		4GHz		0.9		
		6GHz		1.1		
Isolation RFC to RF1 / RF2	ISOCS	50MHz	74 ^[2]	79		dB
		1GHz	71	74		
		2GHz	69	73		
		3GHz	65	70		
		4GHz	60	66		
		6GHz	50	53		
Isolation RF1 to RF2	ISOX	50MHz		86		dB
		1GHz		62		
		2GHz		57		
		3GHz		53		
		4GHz		50		
		6GHz		46		
Return Loss RFC, RF1, RF2	RF_{RL}	50MHz		25		dB
		1GHz		28		
		2GHz		26		
		3GHz		22		
		4GHz		18		

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
		6GHz			21		
Return Loss RF1, RF2 terminated	RFT _{RL}	50MHz			25		dB
		1GHz			26		
		2GHz			28		
		3GHz			22		
		4GHz			18		
		6GHz			19		
Input 1dB Compression	ICP _{1dB}	50MHz			33		dBm
		1GHz			35		
		2GHz			36		
		3GHz			36		
		4GHz			35		
Input 0.1dB Compression ^[3]	ICP _{0.1dB}	V _{DD} = 5.0 V	50MHz		34		dBm
			2GHz		33.5		
			3GHz		33.5		
			4GHz		33.5		
		V _{DD} = 3.1 V	50MHz		33.5		
			2GHz		34		
			3GHz		34		
			4GHz		33		
Input IP3	IIP3	RF Input = RF1 or RF2 P _{IN} = +15 dBm/tone Δ F = 1MHz	50MHz		62		dBm
			1GHz		61		
			2GHz		62		
			2.5GHz		62.5		
			4GHz		61.5		
Non-RF Driven Spurious ^[4]	Spur _{MAX}	At any RF port when externally terminated to 50Ω (RBW = 100Hz)			-114		dBm
Switching Time ^[5]	T _{SW}	50% control to 90% RF			325		ns
		50% control to 10% RF			255		
Maximum Switching Rate ^[6]					25		kHz

- Items in minimum/maximum columns in **bold italics** are confirmed by Test.
- Items in minimum/maximum columns that are not bold/italics are confirmed by Design Characterization.

3. The input 0.1dB compression point is a linearity figure of merit. For the maximum operating power levels, see Recommended Operating Conditions.
4. Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 5.2MHz.
5. $F_{RF} = 2\text{GHz}$.
6. Minimum time required between switching of states = $1 / \text{Maximum Switching Rate}$.

3. Control Mode

Table 2. Switch Control Truth Table

VCTL	EN	RFC to RF1	RFC to RF2
0	0	OFF	ON
1	0	ON	OFF
0	1	OFF	OFF
1	1	OFF	OFF

4. Typical Performance Graphs

Unless otherwise noted for the typical performance graphs on the following pages, the following conditions apply:

- $V_{DD} = 5\text{V}$
- $T_C = +25^\circ\text{C}$ (T_C = Temperature of Exposed Paddle)
- $F_{RF} = 2000\text{MHz}$
- $Z_S = Z_L = 50\Omega$
- $P_{IN} = 0\text{ dBm}$ for all small signal tests.
- $P_{IN} = +15\text{ dBm/tone}$ applied to RF1 or RF2 port for two tone linearity tests.
- Two-tone frequency spacing = 1MHz .
- RF1 or RF2 is the driven RF port and RFC is the output port.
- All unused RF ports terminated into 50Ω .
- For Insertion Loss and Isolation plots, RF trace and connector losses are de-embedded.
- Plots for Isolation and Insertion Loss over temperature and voltage are for a typical path. For performance of a specific path, refer to the online S-Parameter file.

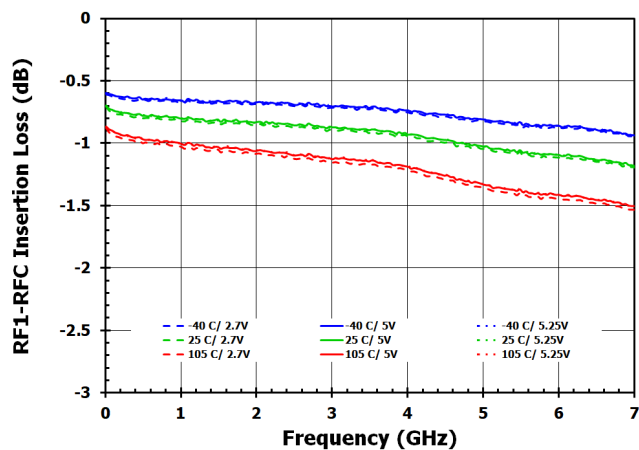


Figure 3. RF1 - RFC Insertion Loss

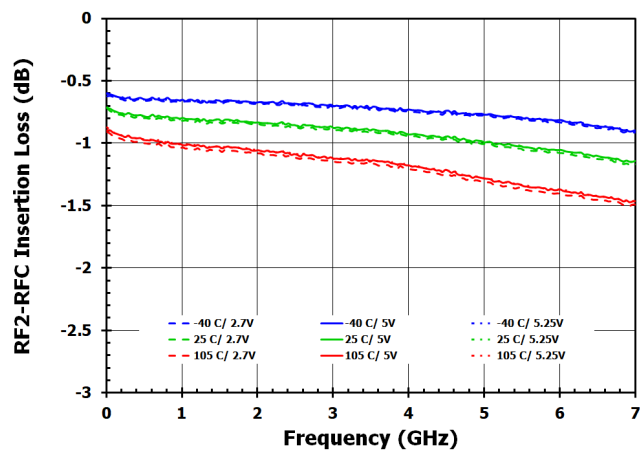


Figure 4. RF2 - RFC Insertion Loss

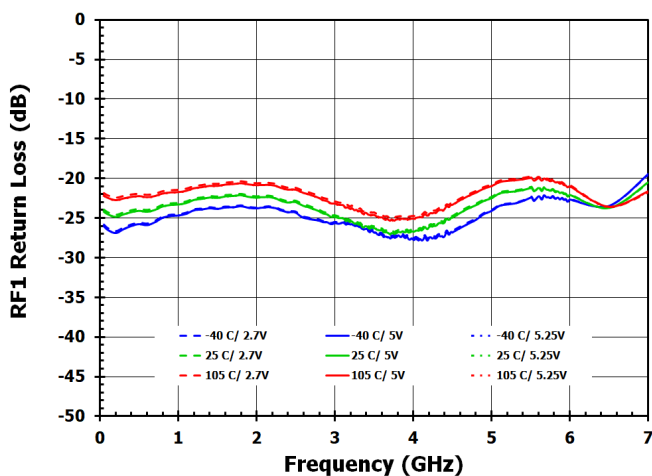


Figure 5. RF1 Return Loss

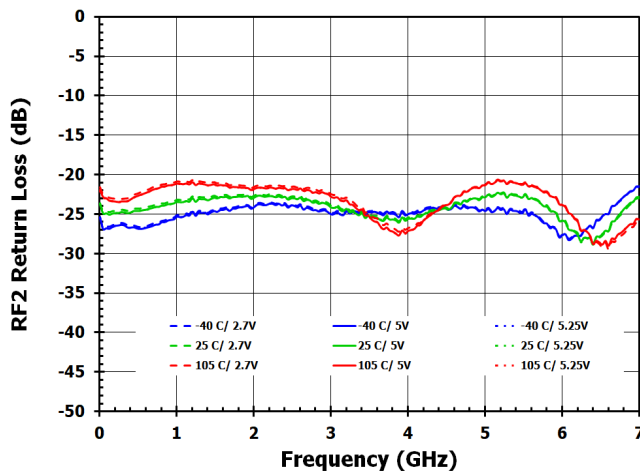


Figure 6. RF2 Return Loss

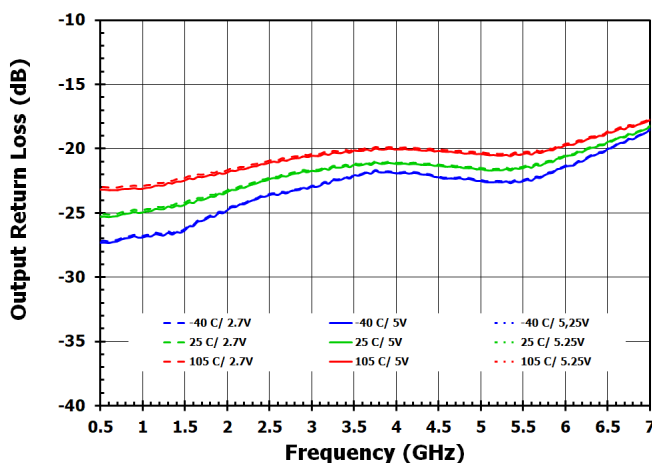


Figure 7. RFC Return Loss

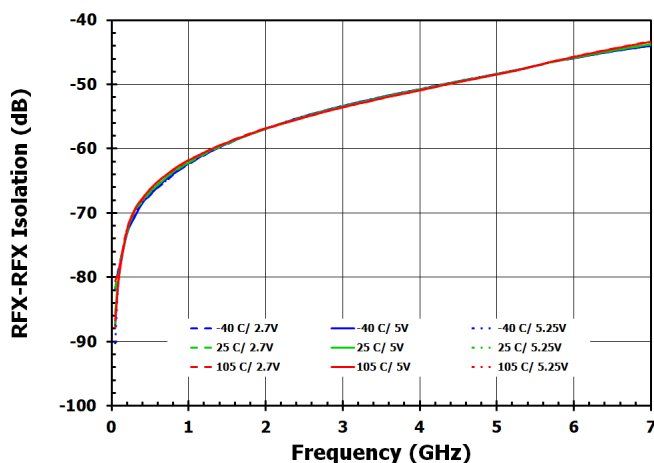


Figure 8. RF1 to RF2 Isolation

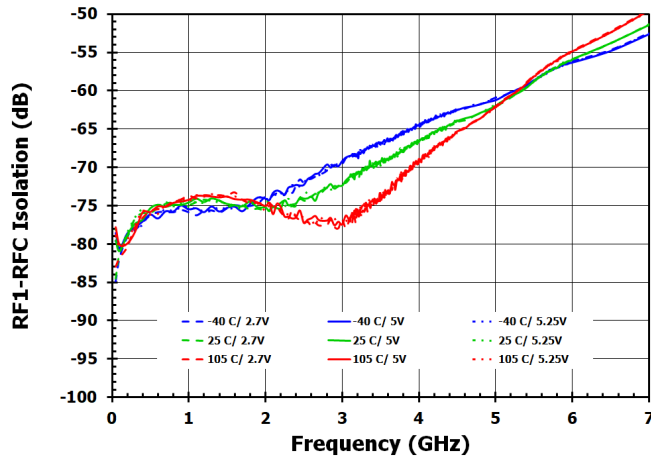


Figure 9. RF1 to RFC Isolation

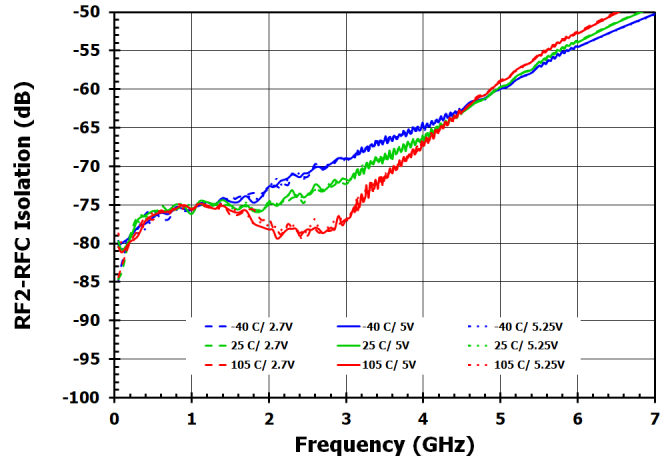


Figure 10. RF2 to RFC Isolation

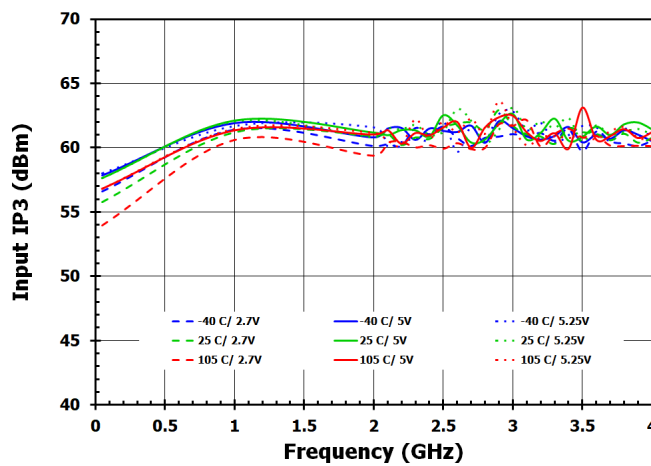


Figure 11. Input IP3

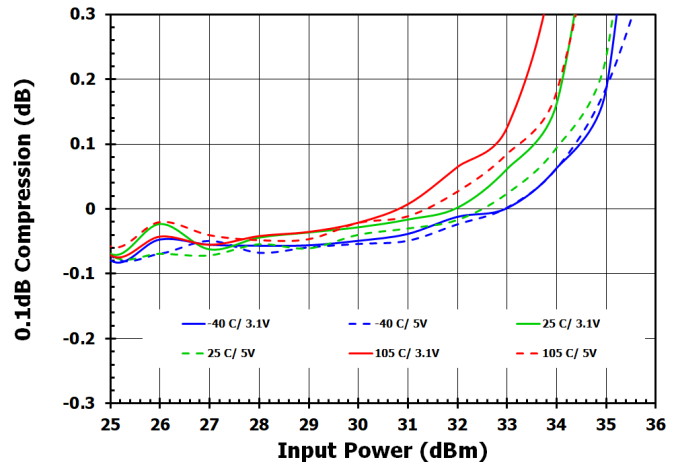


Figure 12. P0.1dB Compression (50MHz)

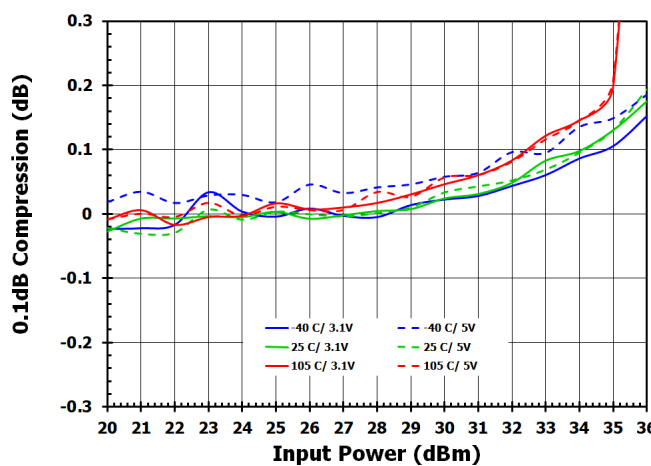


Figure 13. P0.1dB Compression (2GHz)

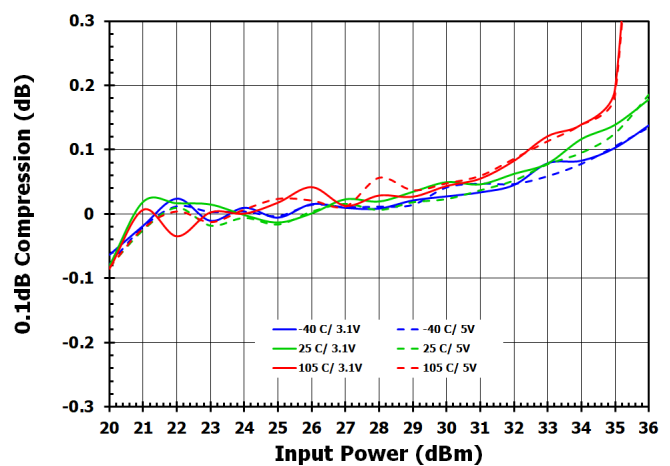


Figure 14. P0.1dB Compression (3GHz)

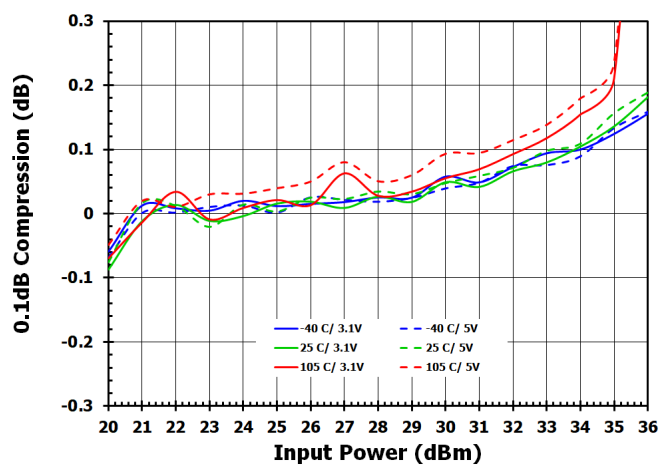


Figure 15. P0.1dB Compression (4GHz)

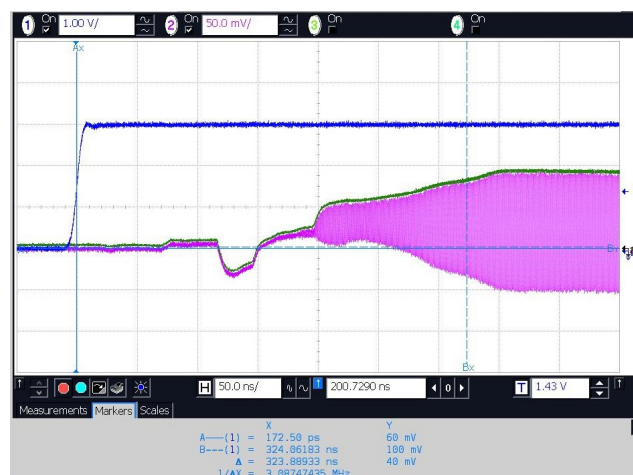


Figure 16. TON Switching Time

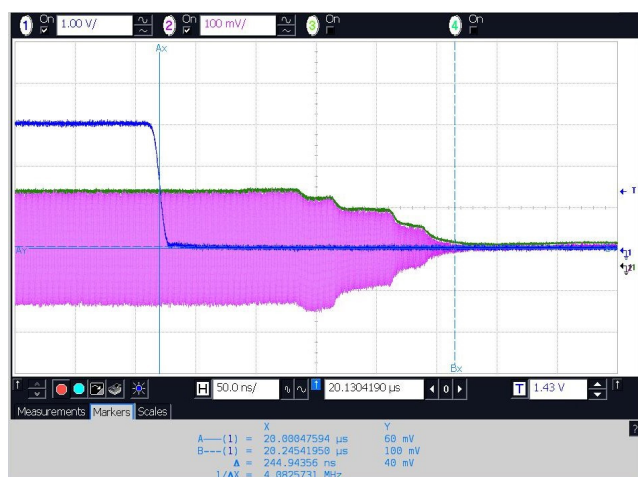


Figure 17. TOFF Switching Time

5. Application Information

5.1 Default Start-up

There are no internal pull-up or pull-down resistors on the VCTL or EN pins.

5.2 Logic Control

Control pins VCTL and EN are used to set the state of the SP2T switch (see Table 2).

5.3 Power Supplies

A common V_{DD} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than $1V / 20\mu s$. In addition, all control pins should remain at 0V ($\pm 0.3V$) while the supply voltage ramps or while it returns to zero.

5.4 Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pin 1 (VCTL) and pin 5 (EN) as shown below.

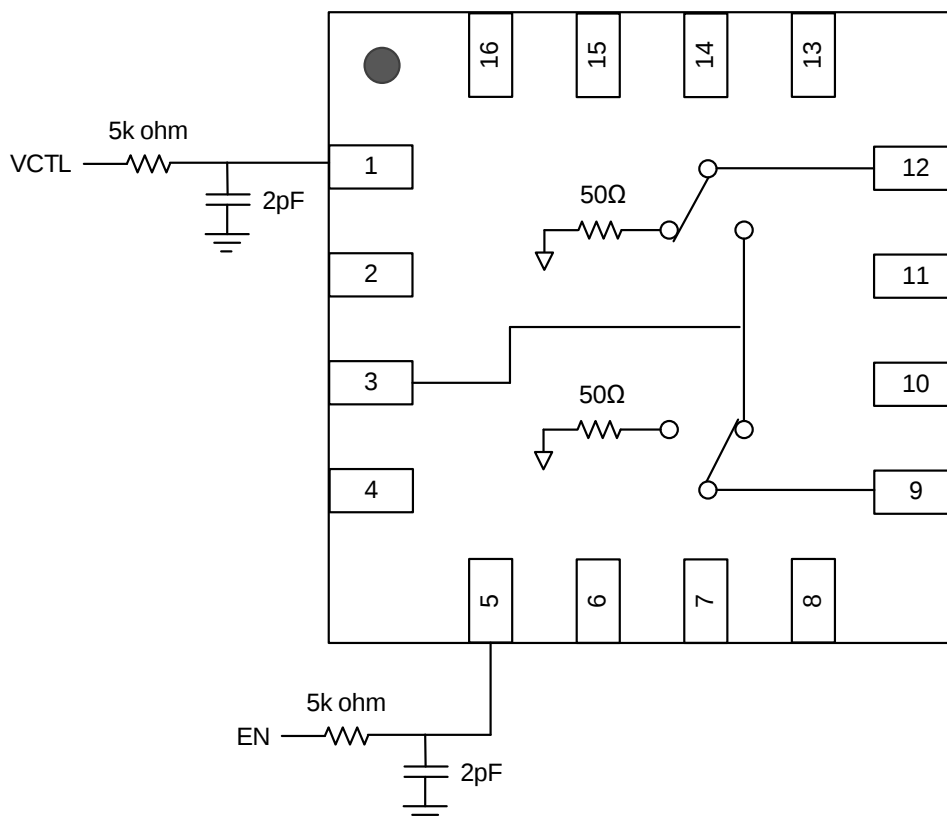


Figure 18. Typical Application Circuit

6. Evaluation Board

6.1 Board Images

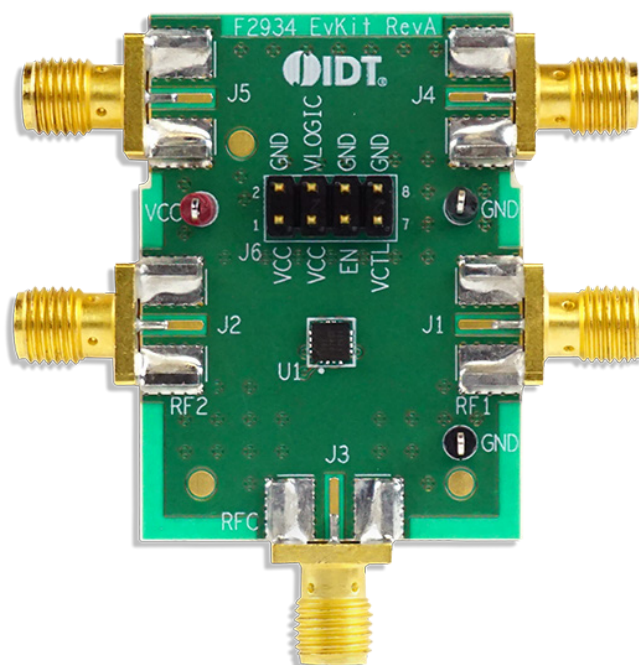


Figure 19. Evaluation Board – Top View

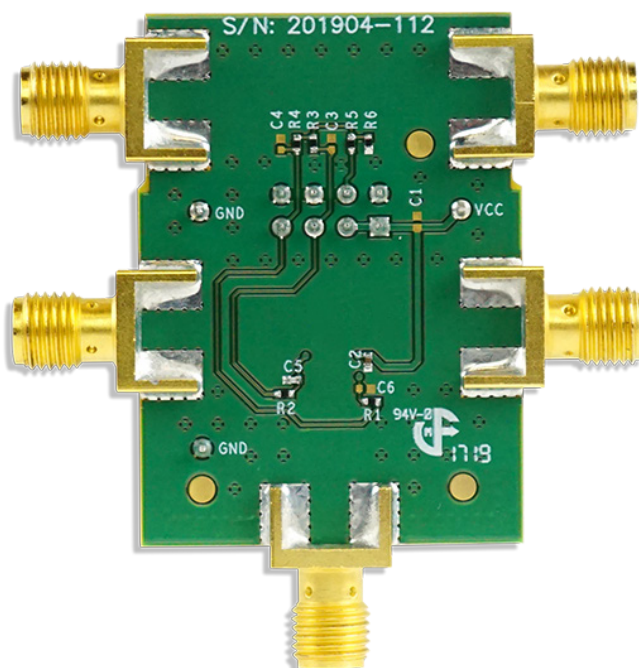


Figure 20. Evaluation Board – Bottom View

6.2 Setup and Configuration

6.2.1. External Supply Setup

Set up a VCC power supply in the voltage range of 2.7V to 5.25V and disable the power supply output.

6.2.2. Logic Control Setup

Using the evaluation board to manually set the control logic:

On connector J6 connect a 2-pin shunt from pin 3 (V_{CC}) to pin 4 (V_{LOGIC}). This connection provides the VCC voltage supply to the Eval Board logic control pull up network. Resistors R5 and R6 form a voltage divider to set the V_{high} level over the 2.7V to 5.25V V_{CC} range for manual logic control.

Connector J6 has 2 logic input pins: EN (pin 5) and V_{CTL} (pin 7). See Table 2 for Logic Truth Table. With the pull-up network enabled (as noted above) these pins can be left open to provide a logic high through pull-up resistors R3 and R4. To set a logic low for EN and V_{CTL} connect 2-pin shunts on J6 from pin 5 (EN) to pin 6 (GND) and from pin 7 (V_{CTL}) to pin 8 (GND).

Note that when using the on board R5 / R6 voltage divider the current draw from the V_{CC} supply will be higher by approximately $V_{CC} / 37k\Omega$.

Using external control logic:

External logic controls are applied to J6 pin 5 (EN) and pin 7 (V_{CTL}). See Table 2 for Logic Truth Table.

6.2.3. Turn On Procedure

Setup the supplies and Evaluation Board as noted in the **External Supply Setup** and **Logic Control Setup** sections above.

Connect the preset disabled V_{CC} power supply to the red V_{CC} loop and ground to GND1 or GND2.

Enable the V_{CC} supply.

Set the desired logic setting using J6 pin 5 (EN) and pin 7 (V_{CTL}) to achieve the desired Table 2 setting. Note that external control logic should not be applied without V_{CC} being present.

6.2.4. Turn Off Procedure

If using external control logic for EN and V_{CTL} then set them to a logic low.

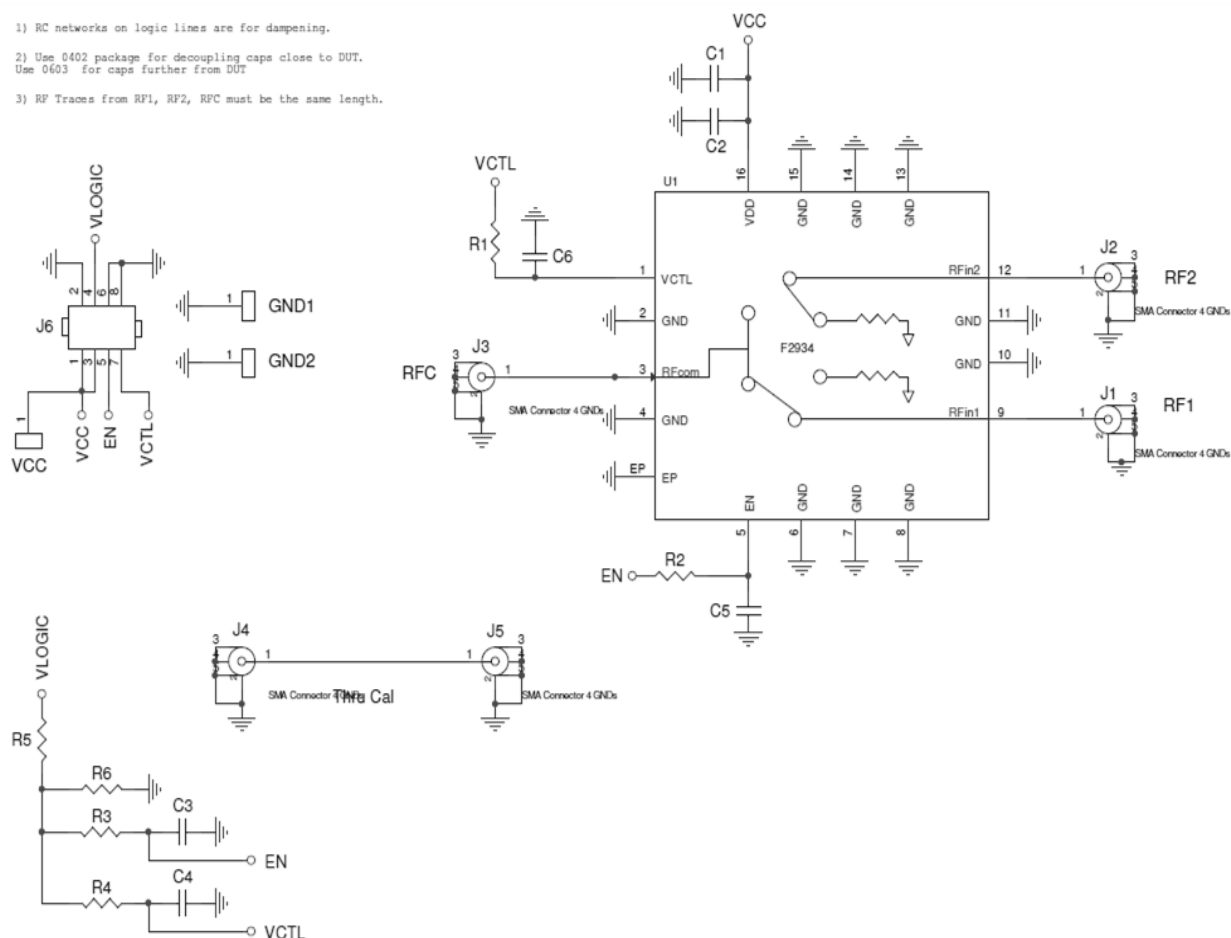
Disable the V_{CC} supply.

6.3 Application Circuit

1) RC networks on logic lines are for dampening.

2) Use 0402 package for decoupling caps close to DUT.
Use 0603 for caps further from DUT

3) RF Traces from RF1, RF2, RFC must be the same length.



6.4 Bill of Materials

Table 3. Bill of Materials (BOM)

Qty	Ref. Designator	Description	Mfr. Part #	Mfr.
0	C1	Not Installed (0402)		
1	C2	0.1μF ±10%, 16V, X7R, Ceramic Capacitor (0402)	GRM155R71C104K	Murata
0	C3, C4, C6	Not Installed (0402)		
1	C5	100pF ±5%, 50V, C0G, Ceramic Capacitor (0402)	GRM1555C1H101J	Murata
2	R1, R2	100Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	Panasonic
2	R3, R4	100kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1003X	Panasonic
1	R5	15kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1502X	Panasonic
1	R6	22kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2202X	Panasonic
5	J1 – J5	SMA Edge Launch (0.375 inch pitch ground tabs)	142-0701-851	Emerson Johnson
1	F2934	SP2T Switch 3 mm x 3 mm QFN16-EP	F2934NTGI8	Renesas
1		Printed Circuit Board	F2934 EVKIT REVA	Renesas

7. Package Outline Drawings

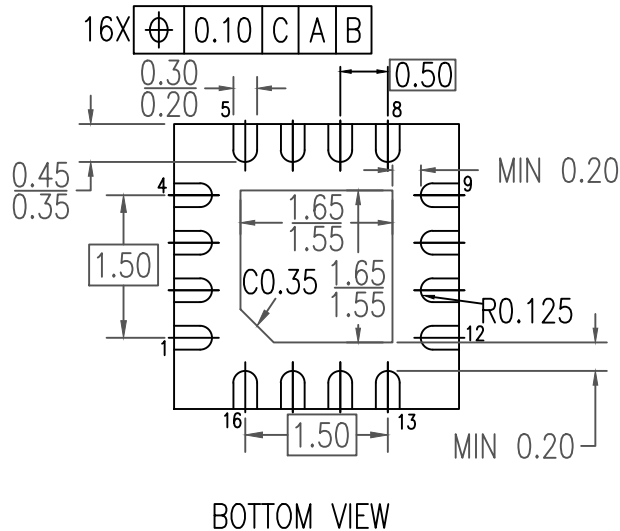
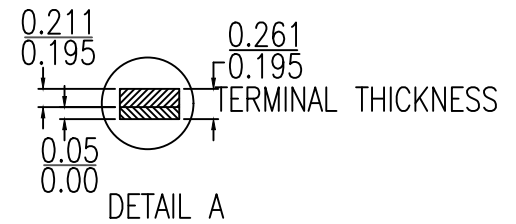
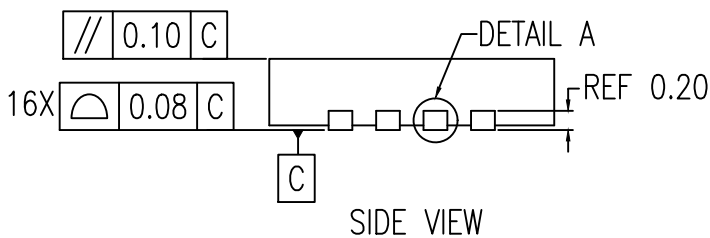
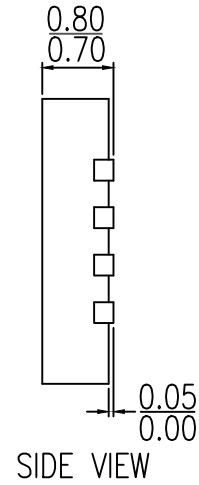
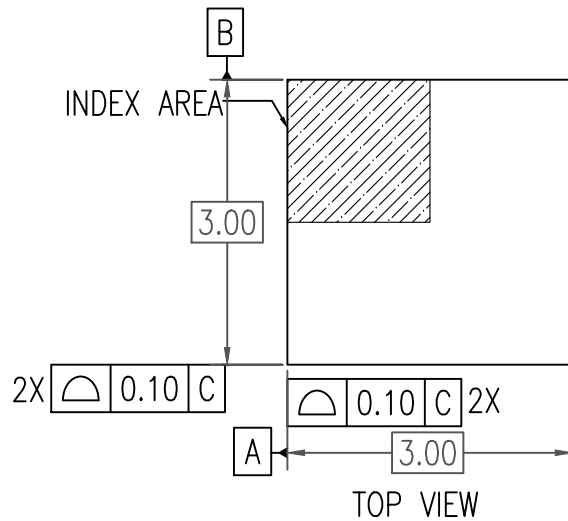
The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

8. Ordering Information

Part Number	Package Description	Carrier Type	Temperature Range
F2934NTGI8	3 × 3 mm, 16-VFQFPN	Tape and Reel	-40 to +85°C

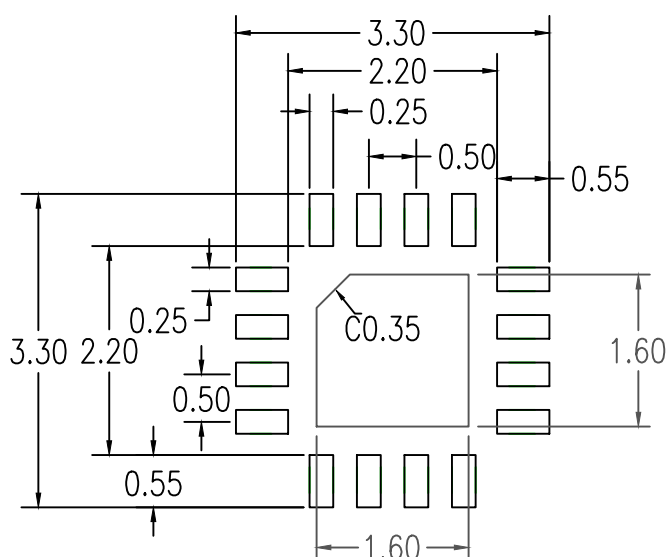
9. Revision History

Revision	Date	Description
1.1	Apr 28, 2021	Updated Figure 9 and Figure 10
1.0	Mar 9, 2021	Initial release.



NOTE :

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
COPLANARITY SHALL NOT EXCEED 0.05 MM.
3. WARPAGE SHALL NOT EXCEED 0.05 MM.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. REFER JEDEC MO-220.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
July 8, 2019	Rev 03	Correct Typo Error Minimum
Sept 5, 2018	Rev 02	Add "K" Value 0.20 Minimum

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Renesas Electronics:](#)

[F2934NTGI](#)