Description

This document describes the specifications for the F1180 Dual Path RF Receiver consisting of an RF Amplifier w/bypass function, Digital Step Attenuator (DSA), and RF Mixer in each signal path. Applications include Multi-mode, Multi-carrier BaseStation Receivers & Repeaters. The F1180 supports the following frequencies: RF from 1400MHz to 2700MHz, LO from 1350MHz to 2900MHz, and IF from 25MHz to 400MHz. Refer to the Part # Matrix below describing the complete series.

The F1180 RF front-end offers 16.5dB gain with 3.5dB NF and +38dBm OIP3 performance at 2100MHz. The digital step attenuator provides 30dB adjustment range in 2dB steps via the SPI interface controller. For strong signal conditions, each RF amplifier can be configured to be internally bypassed via the SPI interface. The RF front-end output and mixer input signals are bonded to separate pins to allow interstage image-reject filtering.

Each of the dual mixer paths provide 8.2dB power gain, 10.5dB NF and +35dBm OIP3 performance. An external LO signal is applied to the mixer LO port.

This device is packaged in a 7 x 7 mm, 48-pin Thin QFN with 50 ohm single-ended RF & LO inputs and 200 ohm differential IF output impedance for ease of integration into the receiver lineup.

Competitive Advantage

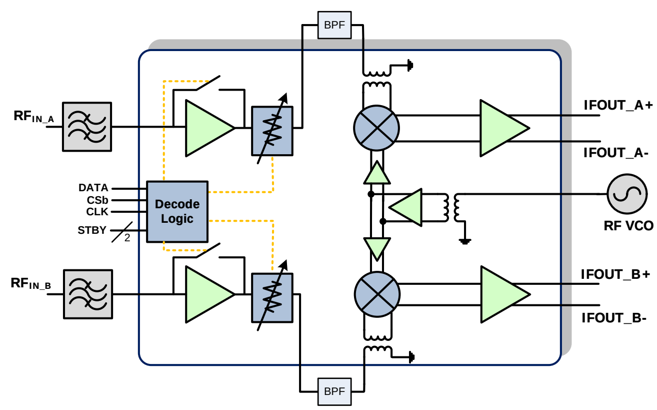
This device integrates the critical elements and features necessary for high performance 3G and 4G receivers in TDD and FDD wireless infrastructure

- ✓ The Amplifier bypass option improves SNR in signal blocking conditions and reduces power consumption.
- ✓ The on-chip 4-bit RF digital step attenuator (DSA) has very low insertion loss and low distortion.
- ✓ The device is optimized for < 1.9 Watts of power consumption with both paths on.
- ✓ The device has fast-settling independent power down modes for each channel for TDD applications.
- ✓ The mixer provides outstanding linearity and 2x2 performance (OIP3 > 35 dBm).

Features

- Dual Path RF amp, DSA, RF Mixer and IF amp for Diversity / MIMO Receivers
- for Diversity / MIMO Receivers
- RF: 1400MHz to 2700MHz
- LO: 1350MHz to 2900MHz
- IF: 25MHz to 400MHz
- Bypassable RF amplifiers for blockers
- 16.5dB RF front-end power gain
- +38dBm RF front-end OIP3 (Bypass OFF)
- +40dBm RF front-end OIP3 (Bypass ON)
- 3.5dB front-end NF at 2100MHz
- 8.2dB mixer power gain
- +35dBm mixer OIP3
- 50 Ω RF & LO impedance
- 200 Ω differential IF output impedance
- Independent CHA, CHB path standby mode
- 30dB gain control range, 2dB steps
- 3 bit SPI control
- I_{CC} = 365mA
- 7 x 7 mm, 48-pin VFQFPN package

Functional Block Diagram



Part# Matrix

Part#	RF freq range (MHz)	UTRA bands	IF freq range (MHz)	LO freq range (MHz)
F1130	400 - 1100	5,6,8,12,13,14,1718,19,20, 26	25 – 400	500 - 1300
F1180	1400 - 2700	1,2,3,4,7,9,10, 11,15,16,21,23, 24,25,33,34,35, 36,37,39,40,41	25 – 400	1350 - 2900

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
VCC to GND	V_{CC}	-0.3	+5.5	V
SPI DATA, SPI LE, SPI CLK, STBY_A, STBY_B	V_{Logic}	-0.3	V_{cc} + 0.25	V
IFOUT_A+, IFOUT_A-, IFOUT_B+, IFOUT_B-,	I_{IF}	1.00	V_{cc} + 0.30	V
LO_IN, RFIN_A, RFIN_B, MIXRFIN_A, MIXRFIN_B	V_{Cntl}	-0.3	+0.30	V
LO_BIAS	V_{LO}	+2.1	+4.0	V
RFA_BIAS, RFB_BIAS	V_{RFIN}	-0.3	+1.50	V
RFAMP_BIAS, IFA_BIAS, IFB_BIAS	V_{Bias}	-0.3	+2.20	V
RF Input Power applied for 24 hours maximum – Bypass OFF	P_{RFIN_A} P_{RFIN_B}		+24	dBm
RF Input Power applied for 24 hours maximum – Bypass ON	P_{RFIN_A} P_{RFIN_B}		+22	dBm
RF Input Power to Mixer applied for 24 hours maximum	P_{RFMIX_A} P_{RFMIX_B}		+21	dBm
Continuous Power Dissipation	P_{diss}		2.15	W
Junction Temperature	T_j		150	°C
Storage Temperature Range	T_{st}	-65	150	°C
Lead Temperature (soldering, 10s)			260	°C
ElectroStatic Discharge – HBM (JEDEC/ESDA JS-001-2012)			1500 (Class 1C)	Volts
ElectroStatic Discharge – CDM (JEDEC 22-C101F)			750 (Class C4)	Volts

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

θ_{JA} (Junction – Ambient)	32 °C/W
θ_{JC} (Junction – Case) [The Case is defined as the exposed paddle]	3 °C/W
Moisture Sensitivity Rating (Per J-STD-020)	MSL1

F1180 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage(s)	V_{CC}	All VCC pins	4.75		5.25	V
Operating Temperature Range	T_{CASE}	Case Temperature	-40		+105	°C
RF Freq Range	F_{RF}		1400		2700	MHz
LO Freq Range	F_{LO}		1350		2900	MHz
LO Power	P_{LO}		-3		+3	dBm
IF Freq Range	F_{IF}		25		400	MHz
RF Amplifier Source Impedance	Z_{RFIN_A} Z_{RFIN_B}	Single Ended		50		Ω
RF Amplifier Load Impedance	Z_{RFOUT_A} Z_{RFOUT_B}	Single Ended		50		Ω
Mixer RF Source Impedance	$Z_{MXRRFIN\_A}$ $Z_{MXRRFIN\_B}$	Single Ended		50		Ω
Mixer LO Source Impedance	$Z_{MXRLOIN\_A}$ $Z_{MXRLOIN\_B}$	Single Ended		50		Ω
Mixer IF Load Impedance	$Z_{MXRIFOUT\_A}$ $Z_{MXRIFOUT\_B}$	Differential		200		Ω

F1180 SPECIFICATION

Specifications apply at V_{CC} = +5.00V, T_{CASE} = +25°C, F_{RF} = 2100MHz, F_{IF} = 200MHz, F_{LO} = 1900MHz, PLO = 0dBm, For bypass ON, RF VGA input = +5dBm, for Bypass OFF, RF VGA input = -20dBm/tone, Attenuator = 0dB, STBY_A, STBY_B = GND unless otherwise noted. Trace, Connector, and external transformer losses are de-embedded.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
General						
Logic Input High	V_{IH}	All Control Pins	***1.17***			V
Logic Input Low	V_{IL}	All Control Pins			***0.67***	V
Logic Current	I_{IH}, I_{IL}	All Control Pins	***-140***		***+20***	µA
Standby Mode Logic	STBY	STBY = V_{IH}	Power OFF			
		STBY = V_{IL}	Power ON			
Supply Current	I_{CC_ON}	Bypass OFF, 2 Channels		***365***	***410***[1]	mA
	I_{CC_OFF1}	Bypass ON, 1 Channels (CHA or CHB)		***295***	***330***	
	I_{CC_OFF2}	Bypass ON, 2 Channels (CHA and CHB)		***230***	***260***	
	I_{CC_STBY}	Standby Mode		***20***	***26***	
RF Switching time[3]	τ_{RF}	10% to 90% risetime		250		ns
DSA Settling time[3]	τ_{SET}	10% to 90% risetime		100		ns
Turn ON time[3]	τ_{ON}	10% to 90% risetime		225		ns
Turn OFF time[3]	τ_{OFF}	10% to 90% risetime		25		ns
Control Interface	SPI_{BIT}			14		bit
Serial Clock Speed	SPI_{CLK}			24		MHz

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: Speeds are measured after SPI programming is completed (data latched with LE = HIGH).
Note 4: Gain across the entire frequency band is affected by the inclusion of the RF switch.

F1180 Specification (continued)

Specifications apply at V_{CC} = +5.00V, T_{CASE} = +25°C, F_{RF} = 2100MHz, F_{IF} = 200MHz, F_{LO} = 1900MHz, PLO = 0dBm, For bypass ON, RF VGA input = +5dBm, for Bypass OFF, RF VGA input = -20dBm/tone, Attenuator = 0dB, STBY_A, STBY_B = GND unless otherwise noted. Trace, Connector, and external transformer losses are de-embedded.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RF VGA – Bypass OFF						
Gain[4]	G_{VGA}	F_{RF} = 1400 MHz		18.6		dB
		F_{RF} = 2100 MHz	***15***	***16.5***	***18***	
		F_{RF} = 2700 MHz		14.9		
Gain Flatness	G_{VGA_FLAT}	F_{RF} = 1400 MHz to 2700 MHz over any 100 MHz bandwidth		± 0.3		dB
Gain Variation	G_{VGA_T}	T_{case} =-40 to +105 °C		-0.4 to +0.1		dB
Noise Figure	NF_{VGA}	F_{RF} = 1400 MHz		3.3		dB
		F_{RF} = 2100 MHz		3.5		
		F_{RF} = 2700 MHz		3.7		
Input 1 dB Pwr Compression	$IP1dB_{LBVGA}$			1.0		dBm
Output Third Order Intercept Point	$OIP3_{VGA}$	Pout = 0 dBm/Tone, 1 MHz tone separation	34[2]	38		dBm
RF VGA – Bypass ON						
Gain	G_{BYPASS}		***-4***	***-3***		dB
Gain Flatness	G_{BYPASS_FLAT}	F_{RF} = 1400 MHz to 2700 MHz over any 100 MHz bandwidth		± 0.1		dB
Gain Variation	G_{BYPASS_T}	T_{case} =-40 to +105 °C		± 0.25		dB
Input 1 dB Pwr Compression	$IP1dB_{LBBYPASS}$			23		dBm
Output Third Order Intercept Point	$OIP3_{BYPASS\_0}$	Attenuation = 0dB 1 MHz tone separation	38	40		dBm
Output Third Order Intercept Point	$OIP3_{BYPASS\_6}$	Attenuation = 6dB 1 MHz tone separation	32	34		dBm
RF VGA – Bypass ON or OFF						
DSA Gain Control Range	DSA_{RANGE}			30		dB
DSA Gain Step	DSA_{STEP}			2		dB
DSA Glitching	$ATTN_A$		-2.3		+1	dB
Gain Accuracy	DSA_{ACC}	ATTN ≤ 6dB	***-0.4***		***+0.4***	dB
		ATTN > 6dB	***±(0.05 + 0.05*ATTN) Max***			
Channel Isolation	$ISO_{A/B}$	RFA Input to RFB Output RFB Input to RFA Output	40	48		dB
VGA Input Match	$S11_{VGA}$			-15		dB
VGA Output Match	$S22_{VGA}$			-17		dB
Isolation between VGA RFout and Mixer RFin	$ISO_{VGA/MIX}$	No Connection between ports	45	48		dB

F1180 Specification (continued)

Specifications apply at V_{CC} = +5.00V, T_{CASE} = +25°C, F_{RF} = 2100MHz, F_{IF} = 200MHz, F_{LO} = 1900MHz, PLO = 0dBm, For bypass ON, RF VGA input = +5dBm, for Bypass OFF, RF VGA input = -20dBm/tone, Attenuator = 0dB, STBY_A, STBY_B = GND unless otherwise noted. Trace, Connector, and external transformer losses are de-embedded.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RF VGA – Bypass OFF to ON						
Gain Range Accuracy [5]	$GRANGE_{12dB\_1}$	Attenuator = 12dB	***6.2***	7.3	***8.2***	dB
		Attenuator = 12dB Voltage Extremes Temperature Extremes	6.5	7.3	8.2	
	$GRANGE_{12dB\_2}$	Attenuator = 12dB F_{RF} = 1.5 GHz	8.5	9.3	10.0	
	$GRANGE_{12dB\_3}$	Attenuator = 12dB F_{RF} = 1.8 GHz	7.5	8.1	8.8	
	$GRANGE_{12dB\_4}$	Attenuator = 12dB F_{RF} = 2.6 GHz	5.4	6.3	7.1	

Note 5: Gain difference between (bypass OFF + X dB attenuation) to (bypass ON + 0dB attenuation)

F1180 SPECIFICATION (CONTINUED)

Specifications apply at V_{CC} = +5.00V, T_{CASE} = +25°C, F_{RF} = 2100MHz, F_{IF} = 200MHz, F_{LO} = 1900MHz, PLO = 0dBm, For bypass ON, RF VGA input = +5dBm, for Bypass OFF, RF VGA input = -20dBm/tone, Attenuator = 0dB, STBY_A, STBY_B = GND unless otherwise noted. Trace, Connector, and external transformer losses are de-embedded.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Mixer						
Gain	G_{MXR}		***7.2***	***8.2***	***9.2***	dB
Gain Flatness	G_{MXR_FLAT}	F_{RF} = 1400 MHz to 2700 MHz over any 100 MHz bandwidth		± 0.25		dB
IF Gain Flatness Bandwidth	G_{IF_FLAT1}	Fixed LO Flatness = 0.5 dB		100		MHz
	G_{IF_FLAT2}	Fixed LO Flatness = 0.8 dB		150		MHz
Gain Variation	G_{MXR_T}	T_{case} =-40 to +105 °C		-0.9 to 0.7		dB
Noise Figure	NF_{MXR}			10.5		dB
Blocking Noise Figure	NF_{MXR_BLK}	+100 MHz offset Pin (Blocker) = + 4dBm		15		dB
Input 1 dB Compression	$IP1dB_{MXR}$		7	9		dBm
Output Third Order Intercept Point	$OIP3_{MXR}$	1 MHz tone separation	32	35		dBm
Output Second Order Intercept Point	$OIP2_{MXR}$	1 MHz tone separation		58		dBm
2RF – 2LO rejection	$2x2_{MXR}$	F_{RF} – F_{IF}/2		65		dBc
3RF – 3LO rejection	$3x3_{MXR}$	Frequency = F_{RF} – 2*F_{IF}/3		72		dBc
Second Harmonic	$HD2_{MXR}$			67		dBc
Third Harmonic	$HD3_{MXR}$			82		dBc
Settling Time	τ_{MXR_SET}	Pin = -13 dBm STBY VIH to VIL Time for IF to settle to 0.1 dB of final value		170		ns
Mixer RF Input Match	$S11_{MXR\_RF}$			-16		dB
Mixer LO Input Match	$S11_{MXR\_LO}$			-14		dB
Mixer IF Output Match	$S22_{MXR\_IF}$			-19		dB
Channel Isolation	ISO_{IF}	IFOUT_A to IFOUT_B		63		dBc
RF to IF Isolation	ISO_{RI}	Pin = -10 dBm Ratio of IF level to RF leakage at IF port		48		dBc
LO to RF Leakage	ISO_{LR}			-33		dBm
LO to IF Leakage	ISO_{LI}			-30		dBm

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: Speeds are measured after SPI programming is completed (data latched with LE = HIGH).
Note 4: Gain across the entire frequency band is affected by the inclusion of the RF switch.

Serial Control Mode

Data is clocked in LSB first via serial mode. Serial data is formatted as a 14-bit word. The 14-bit word contains logic for bypass mode, 4-bit attenuator setting, and guard bit. Each word contains the following sequence:

Table 1 - 14 Bit SPI Word Sequence

D13	RX Path 2 bypass mode
D12	Guard bit
D11	RX Path 1 bypass mode
D10	Guard bit
D9	Attenuator 2
D8	Attenuator 2
D7	Attenuator 2
D6	Attenuator 2
D5	Guard bit
D4	Attenuator 1
D3	Attenuator 1
D2	Attenuator 1
D1	Attenuator 1
D0	Guard bit

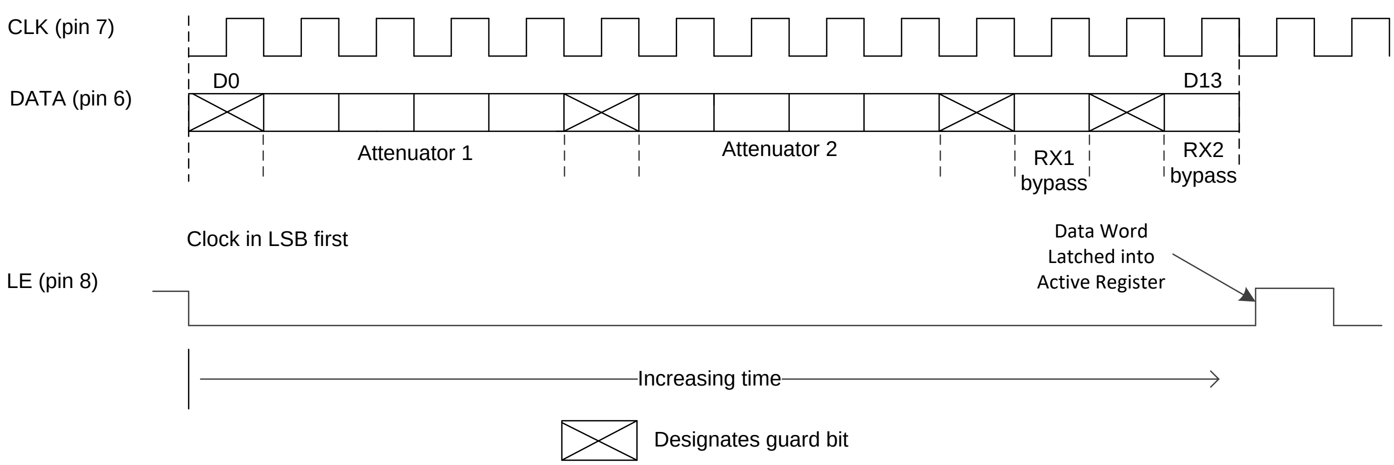


Figure 1 - Serial Register Timing Diagram

Pin 8 Latch Enable (LE):

When LE is high (> VIH), the CLK input is disabled. IDT recommends keeping LE high to reduce F1180 sensitivity to CLK bus noise when SPI is not being programmed. When LE is low (< VIL), the DATA word can be programmed into the shift registers. The programmed word is then latched into F1180 on the LE rising edge (refer to Figure 1). End of data occurs after 14th bit.

Table 2 – Attenuator Data Word Bit Sequence

Attenuation Setting	Attenuator 1 D4, D3, D2, D1	Attenuator 2 D9, D8, D7, D6
Insertion Loss	0000	0000
2 dB	0001	0001
4 dB	0010	0010
6 dB	0011	0011
8 dB	0100	0100
10 dB	0101	0101
12 dB	0110	0110
14 dB	0111	0111
16 dB	1000	1000
18 dB	1001	1001
20 dB	1010	1010
22 dB	1011	1011
24 dB	1100	1100
26 dB	1101	1101
28 dB	1110	1110
30 dB	1111	1111

Table 3 - RF Bypass Data Word Bit Sequence

RF Switch ByPass Mode	RX1 D11	RX2 D13
OFF	0	0
ON	1	1

DEFAULT REGISTER SETTING:

After power on, the default setting for the VGA is Bypass OFF mode with attenuation set to 30dB. This means the amplifier is in the signal path.

SPI TIMING:

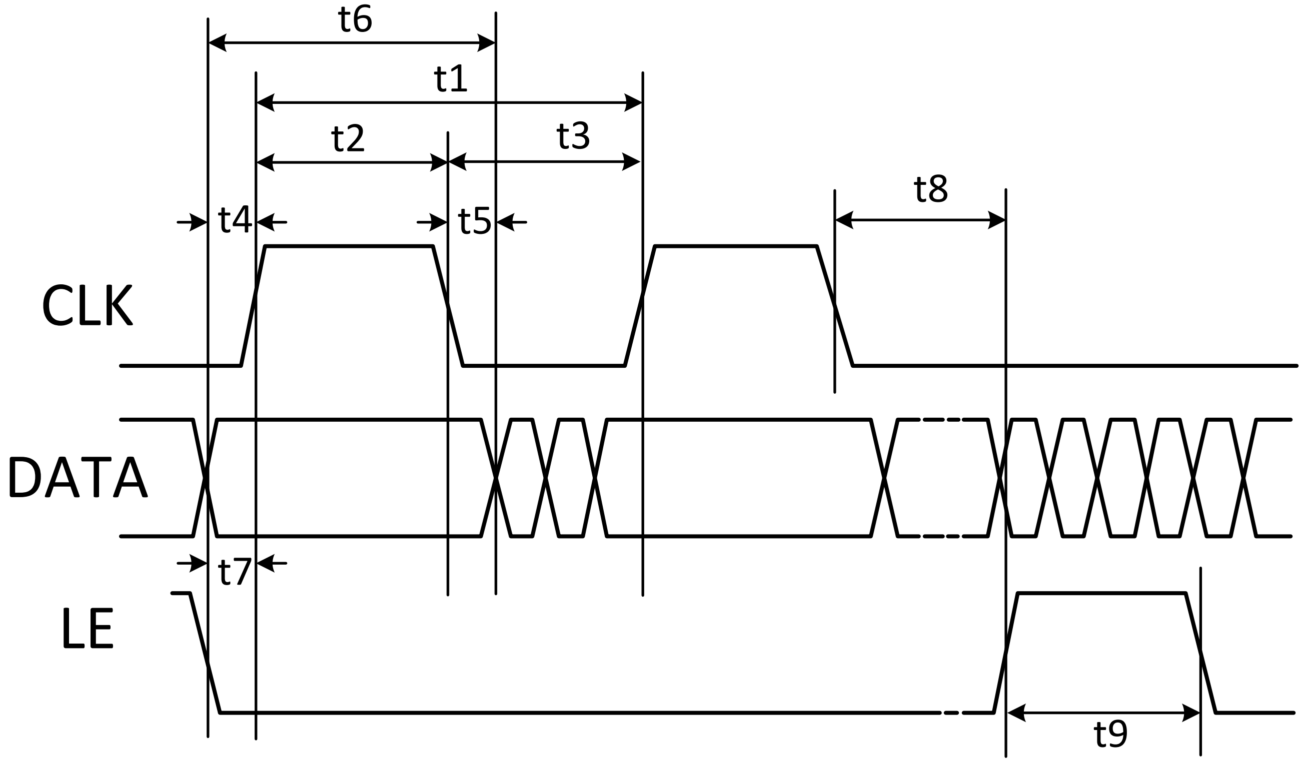


Figure 2 - SPI Timing Diagram

Table 4 - SPI Preset Timing Parameters Calcuated for 24 MHz

Parameter	Symbol	Min	Typ	Max	Units
Clock Frequency			24		MHz
Data Setup			20.83		ns
Data Hold			20.83		ns
Data to CLK Setup Time		5			ns
Data to CLK Hold Time		5			ns
Data Valid			30.83		ns
LE to CLK Setup Time		5			ns
CLK to LE Setup Time		5			ns
LE Pulse Time			20		ns

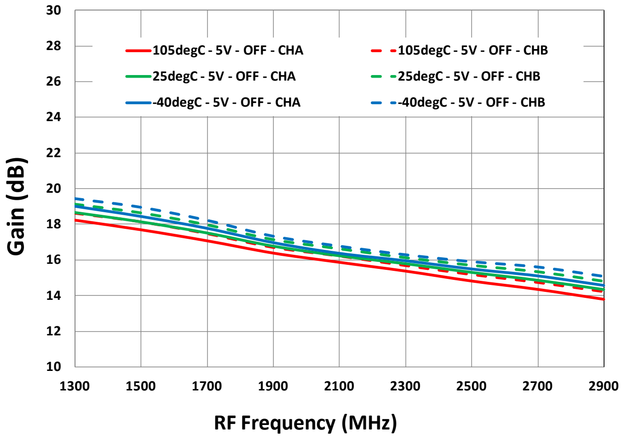
TYPICAL OPERATING CONDITIONS (TOC)

Unless otherwise noted for the TOC graphs on pages XX to YY, the following conditions apply.

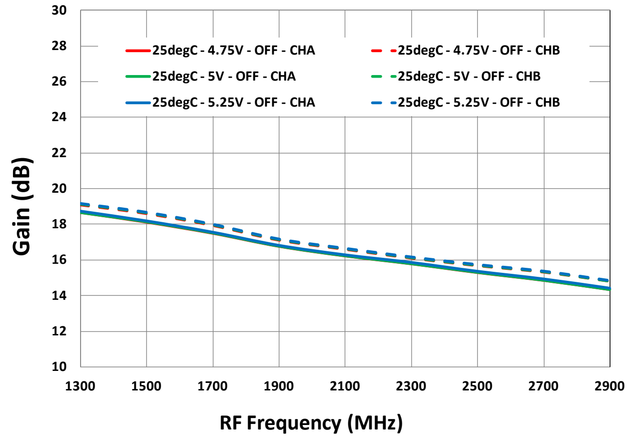
- **V_{CC} = +5.00 V**
- **T_{CASE} = +25 °C**
- **F_{RF} = 2100 MHz**
- **F_{IF} = 200 MHz**
- **F_{LO} = 1900 MHz**
- **P_{LO} = 0 dBm**
- **RF VGA output = -5 dBm/tone**
- **RF Mixer output = 0 dBm/tone**
- **Attenuator = 0 dB**
- **STBY_A, STBY_B = GND**

VGA Bypass OFF: Typical Operating Conditions (- 1 -)

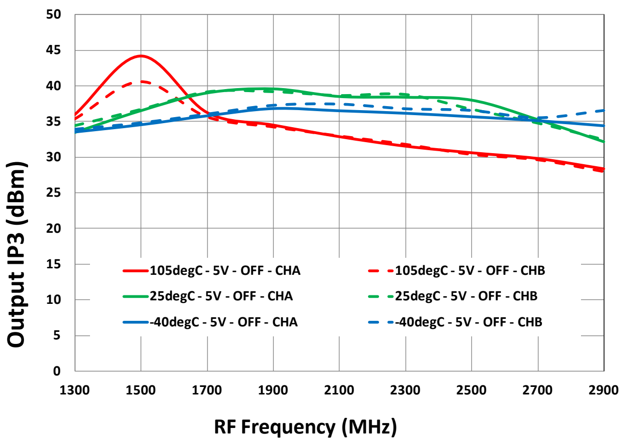
Gain vs. T_{case} [G_{VGA}]



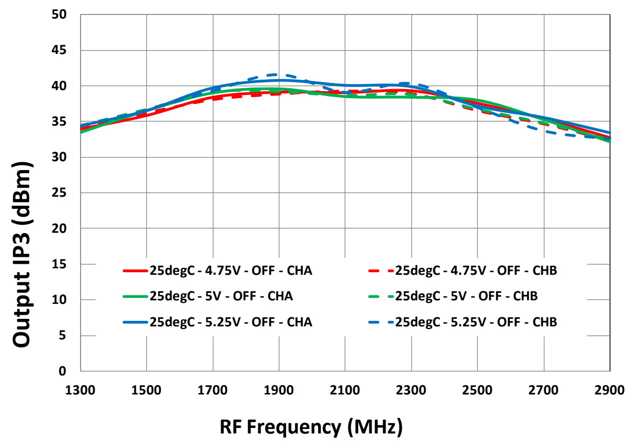
Gain vs. V_{cc} [G_{VGA}]



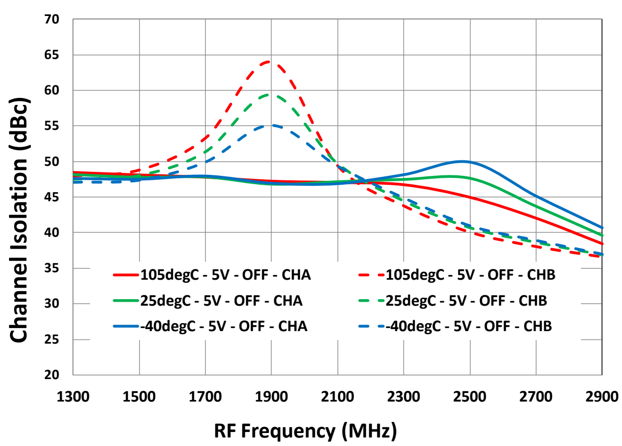
Output IP3 vs. T_{case} [$OIP3_{VGA}$]



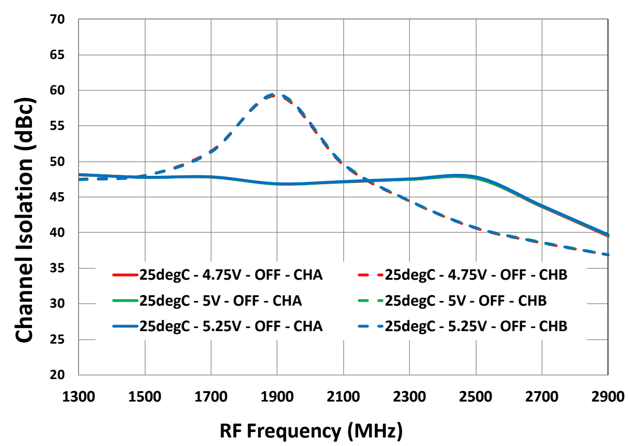
Output IP3 vs. V_{cc} [$OIP3_{VGA}$]



Channel Isolation vs. T_{case} [$ISO_{A/B}$]

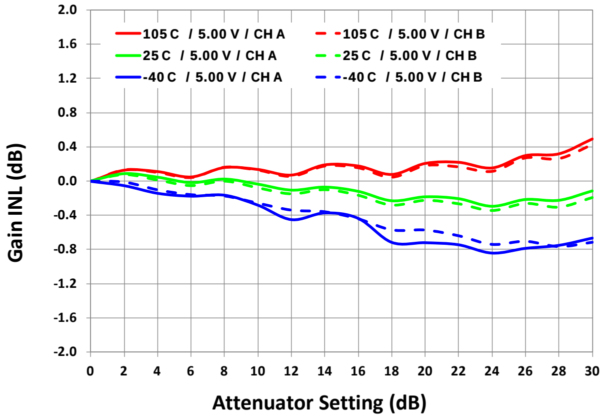


Channel Isolation vs. V_{cc} [$ISO_{A/B}$]

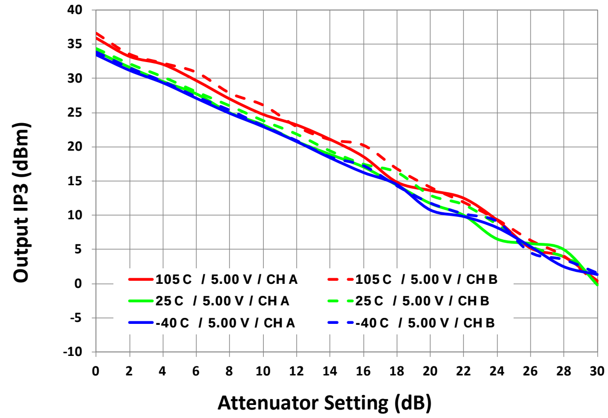


VGA BYPASS OFF: TYPICAL OPERATING CONDITIONS (- 2 -)

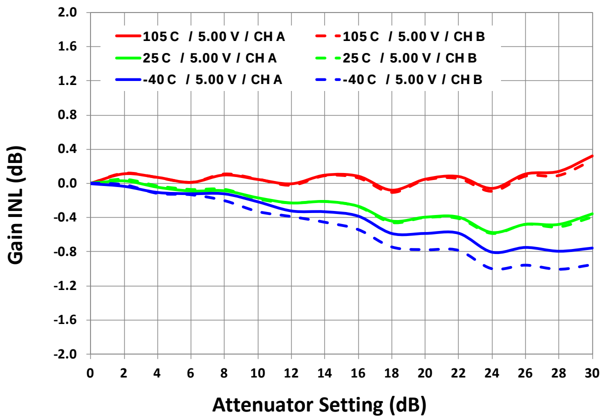
Gain Accuracy [DSA_{ACC} 1400MHz]



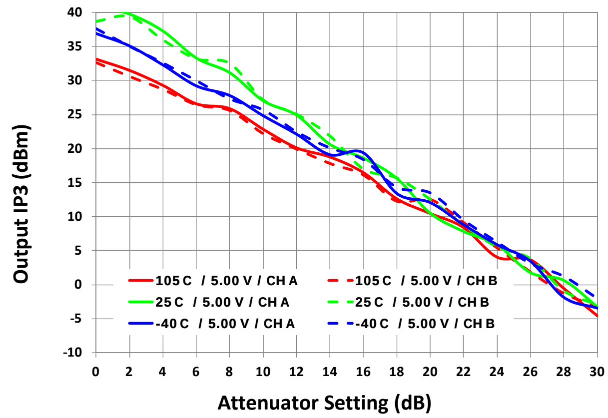
OIP3 vs. Attenuation [1400MHz]



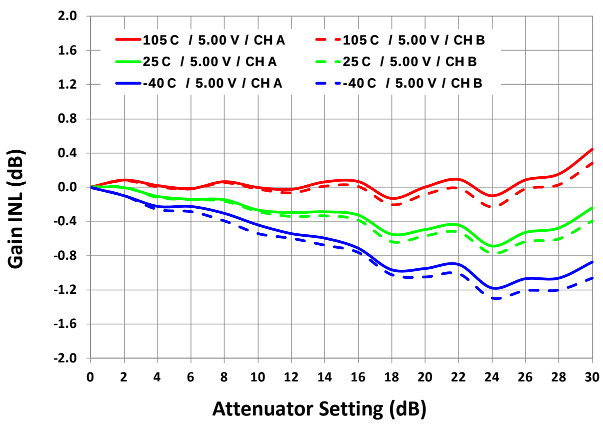
Gain Accuracy [DSA_{ACC} 2100MHz]



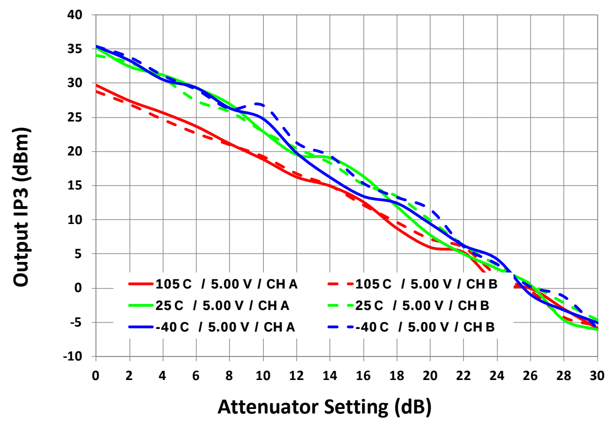
OIP3 vs. Attenuation [2100MHz]



Gain Accuracy [DSA_{ACC} 2700MHz]

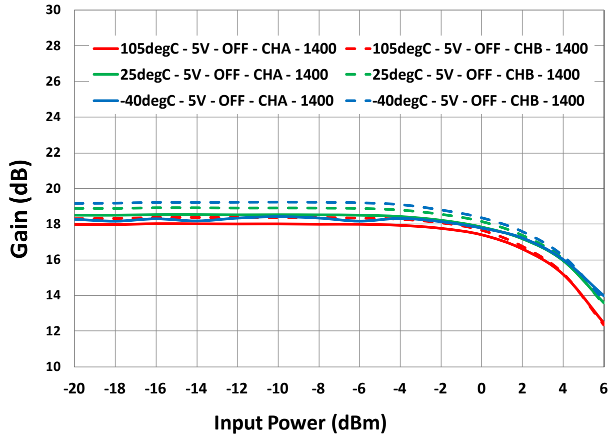


OIP3 vs. Attenuation [2700MHz]

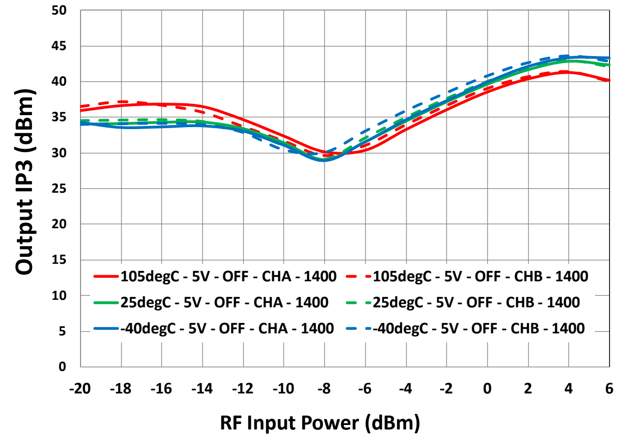


VGA Bypass OFF: Typical Operating Conditions (- 3 -)

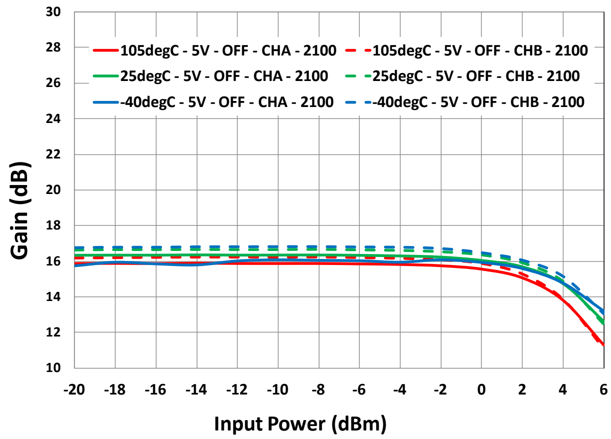
Gain vs. Input Power [1400MHz]



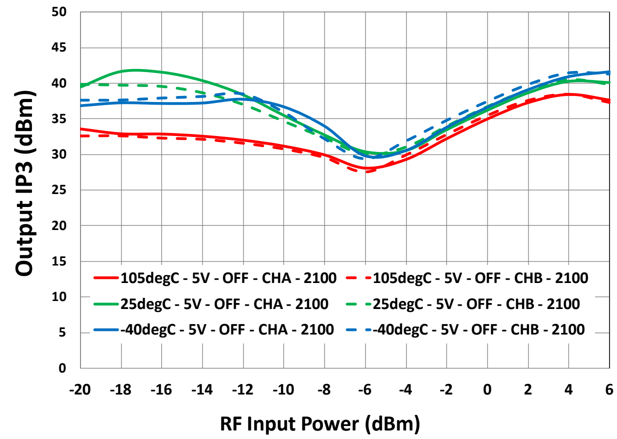
OIP3 vs. Input Power [1400MHz]



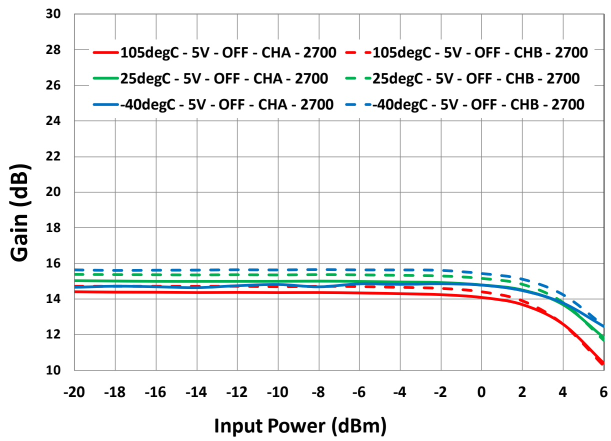
Gain vs. Input Power [2100MHz]



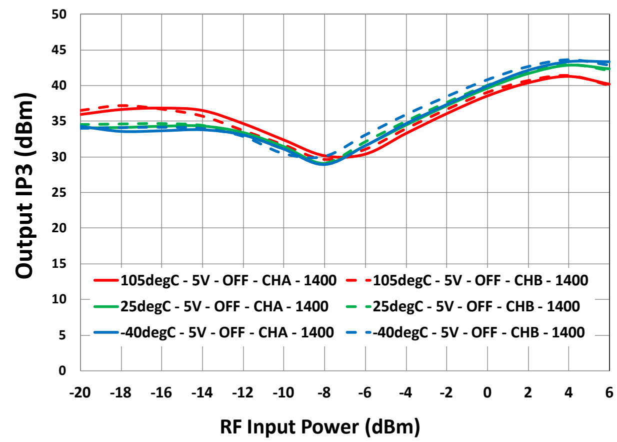
OIP3 vs. Input Power [2100MHz]



Gain vs. Input Power [2700MHz]

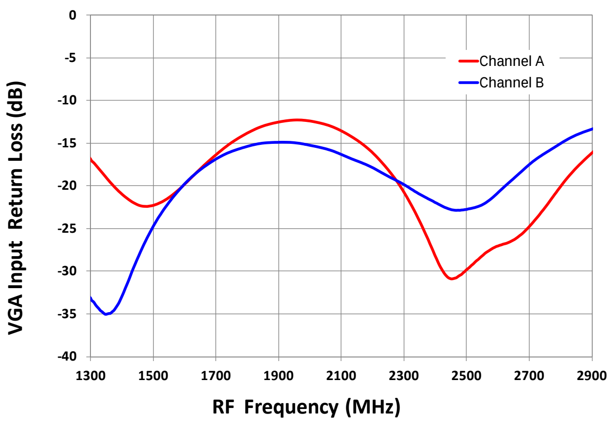


OIP3 vs. Input Power [2700MHz]

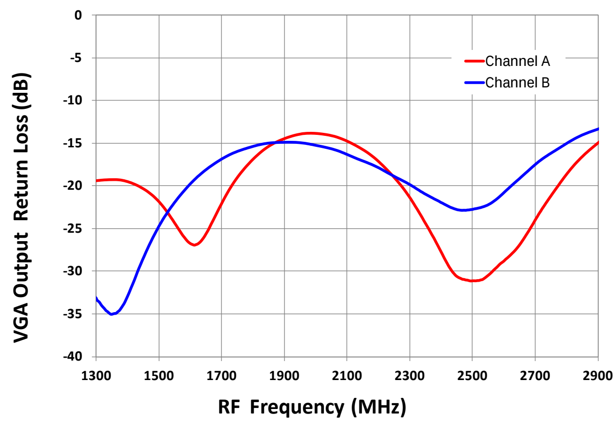


VGA BYPASS OFF: TYPICAL OPERATING CONDITIONS (- 4 -)

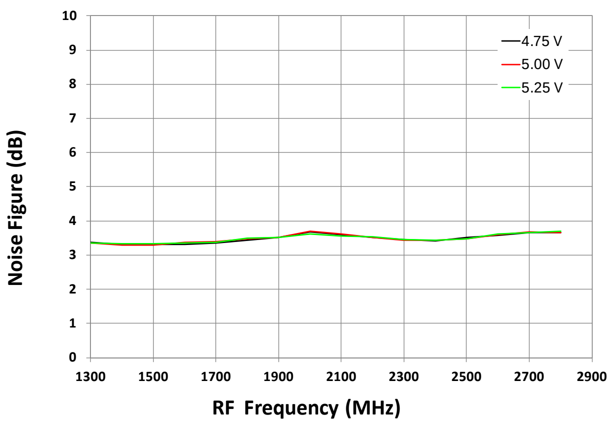
Input Match – [S11$_{VGA}$]



Output Match – [S22$_{VGA}$]

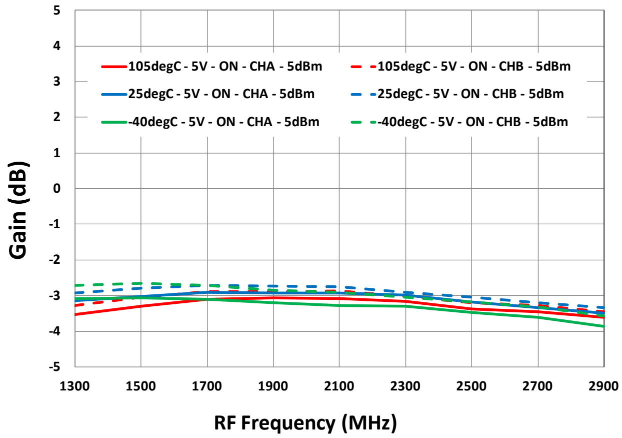


Noise Figure [NF$_{VGA}$], +25 °C

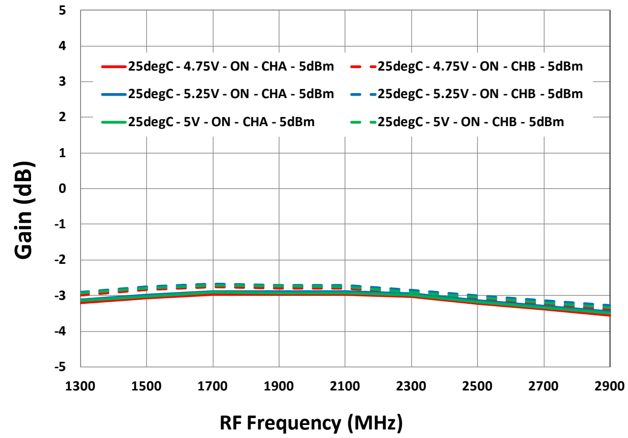


VGA Bypass ON: Typical Operating Conditions (- 5 -)

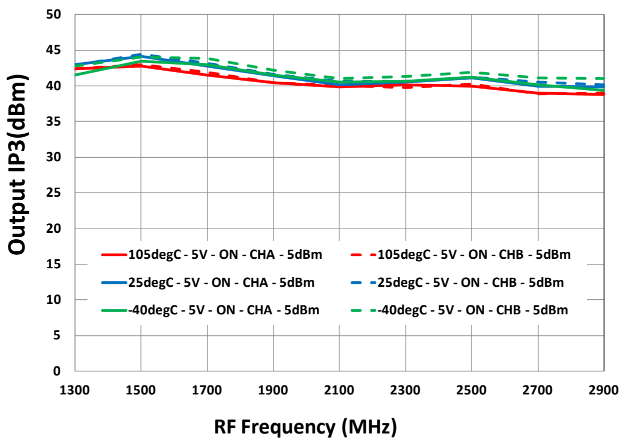
Gain vs. T_{case} [G_{BYPASS}]



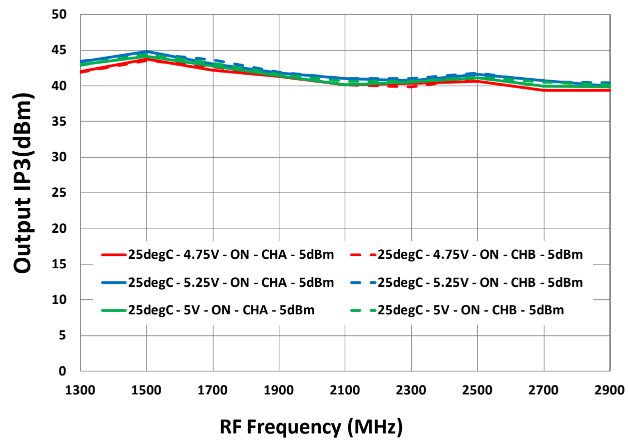
Gain vs. V_{cc} [G_{BYPASS}]



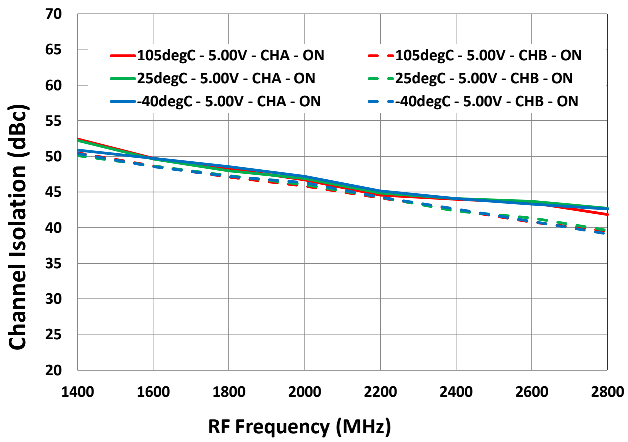
Output IP3 vs. T_{case} [$OIP3_{BYPASS\_0}$]



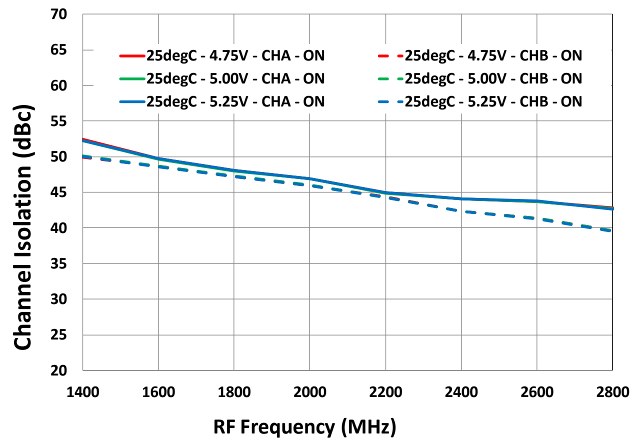
Output IP3 vs. V_{cc} [$OIP3_{BYPASS\_0}$]



Channel Isolation vs. T_{case} [$ISO_{A/B}$]

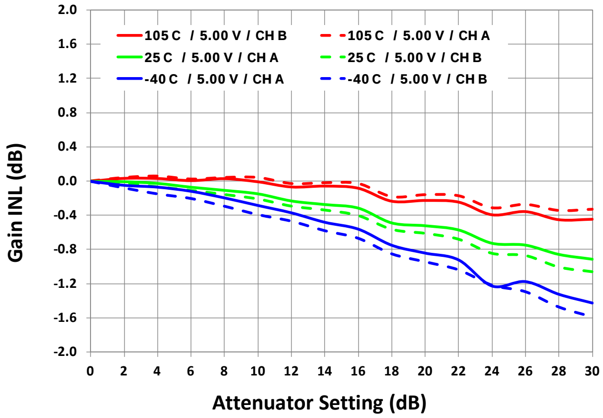


Channel Isolation vs. V_{cc} [$ISO_{A/B}$]

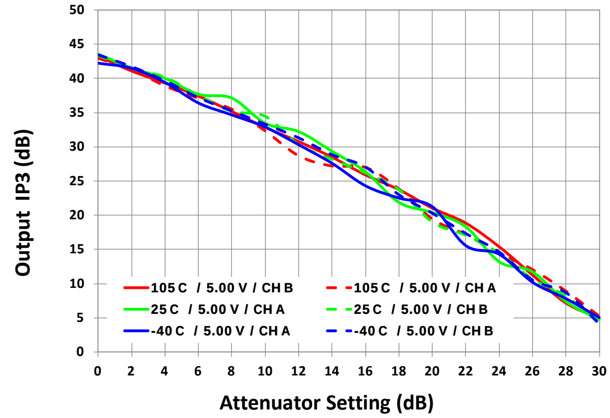


VGA BYPASS ON: TYPICAL OPERATING CONDITIONS (- 6 -)

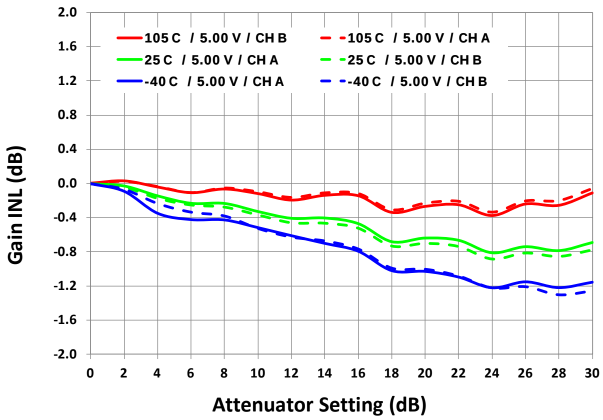
Gain Accuracy [DSA_{ACC} 1400MHz]



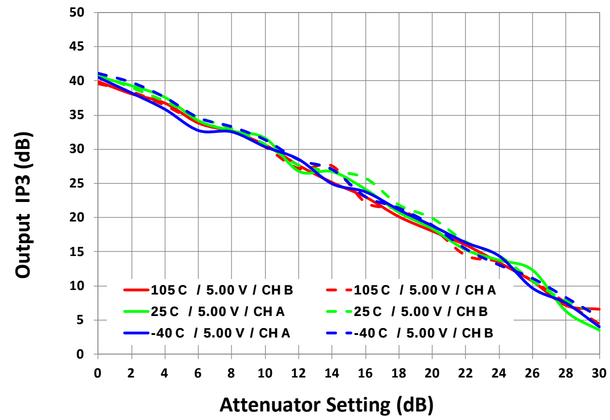
OIP3 vs. Attenuation [1400MHz]



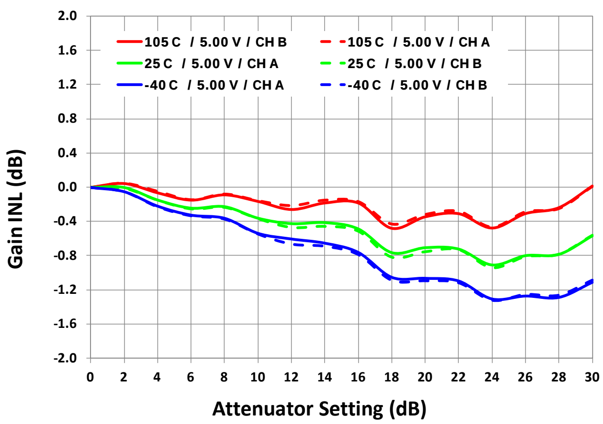
Gain Accuracy [DSA_{ACC} 2100MHz]



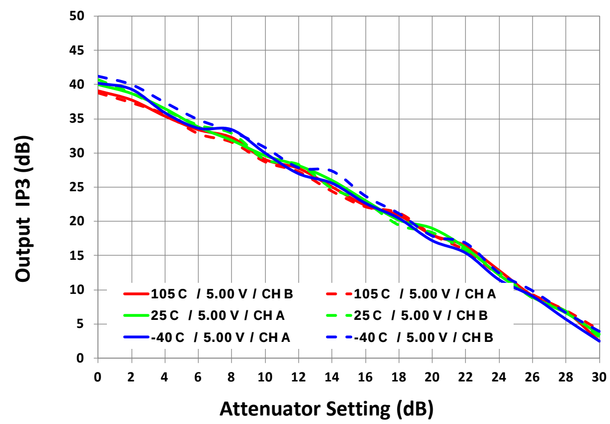
OIP3 vs. Attenuation [2100MHz]



Gain Accuracy [DSA_{ACC} 2700MHz]

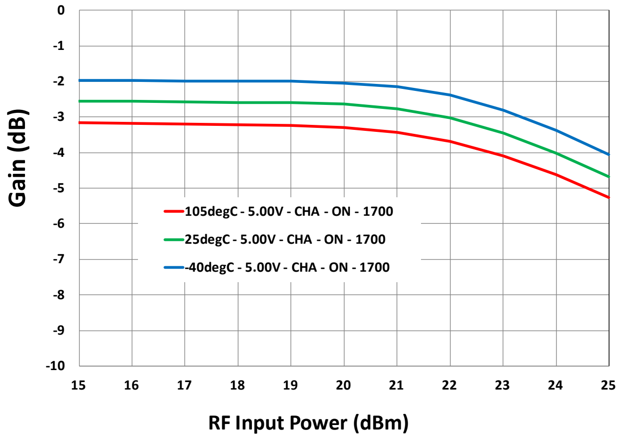


OIP3 vs. Attenuation [2700MHz]

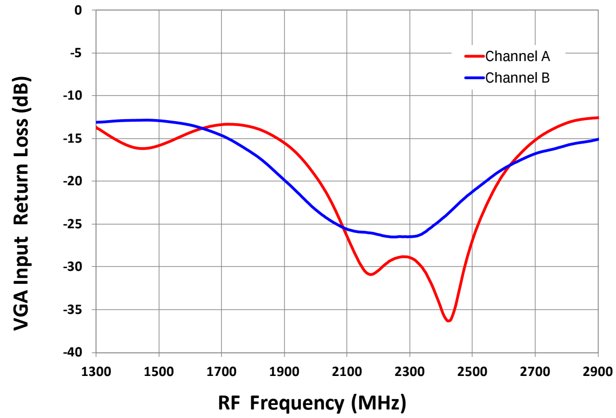


VGA Bypass ON: Typical Operating Conditions (- 7 -)

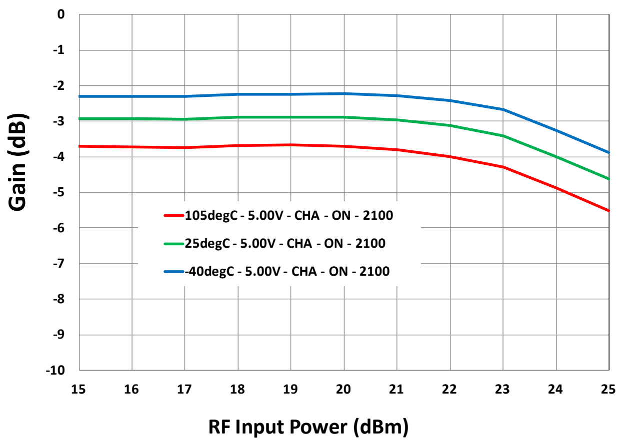
Gain vs. Input Power [1700MHz]



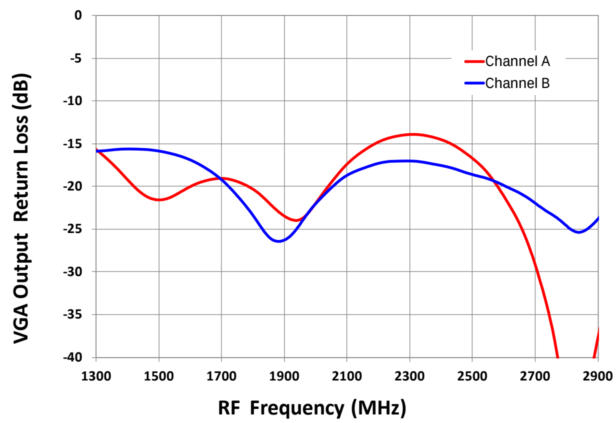
Input Match - S11 $_{VGA}$



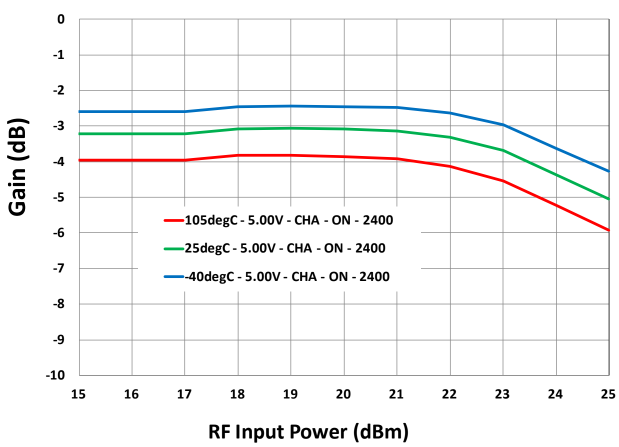
Gain vs. Input Power [2100MHz]



Output Match - S22 $_{VGA}$

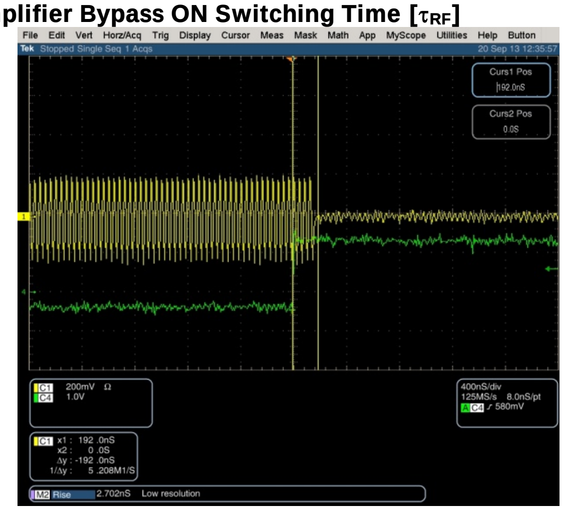


Gain vs. Input Power [2400MHz]

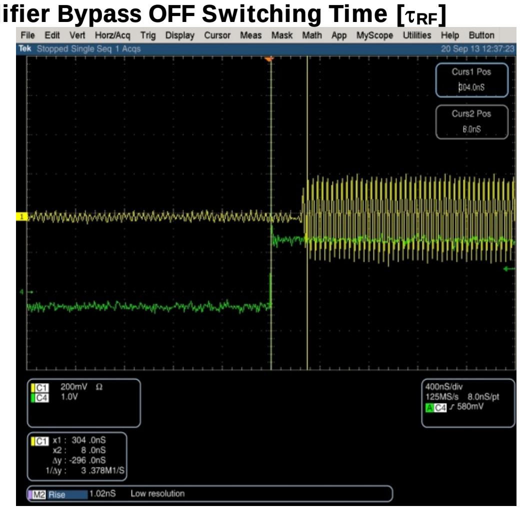


VGA: Typical Operating Conditions (- 8 -)

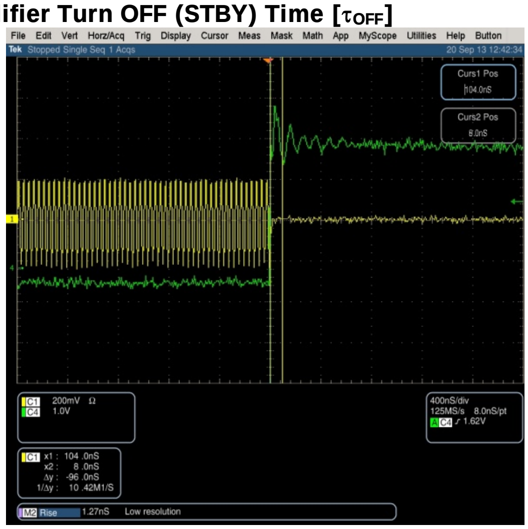
Amplifier Bypass ON Switching Time [τ_{RF}]



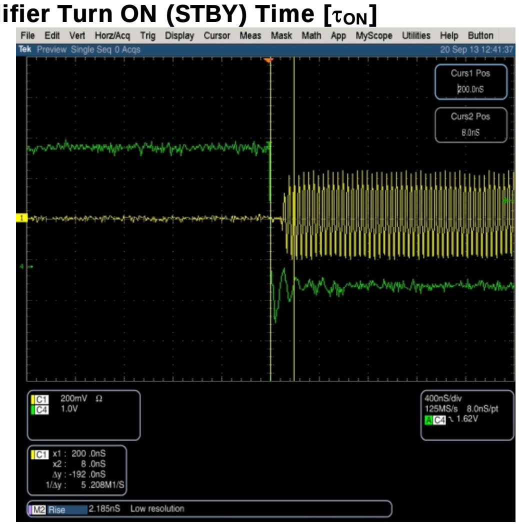
Amplifier Bypass OFF Switching Time [τ_{RF}]



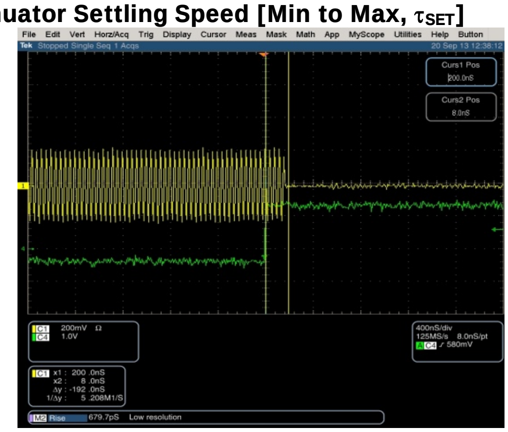
Amplifier Turn OFF (STBY) Time [τ_{OFF}]



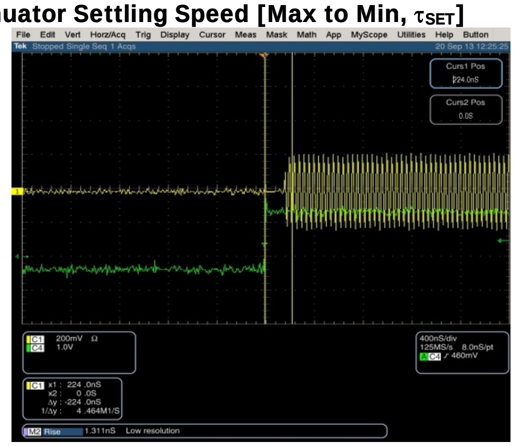
Amplifier Turn ON (STBY) Time [τ_{ON}]



Attenuator Settling Speed [Min to Max, τ_{SET}]

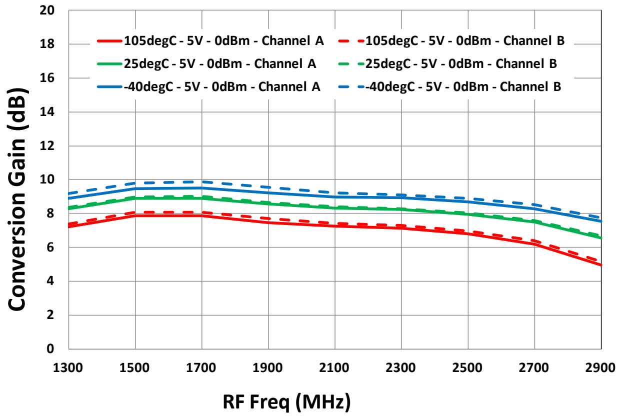


Attenuator Settling Speed [Max to Min, τ_{SET}]

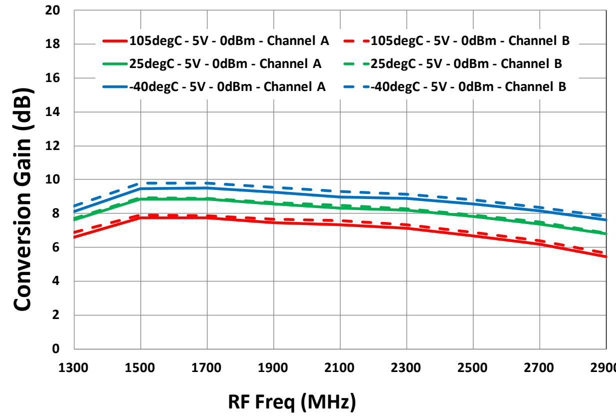


MIXER: TYPICAL OPERATING CONDITIONS (- 9 -)

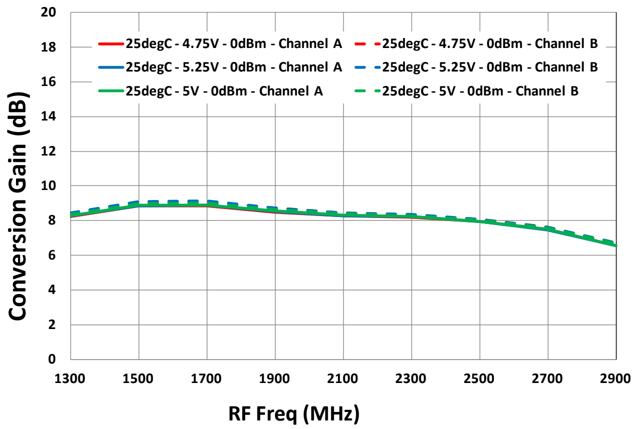
Gain vs. T_{case} [G_{MXR}, HS Injection]



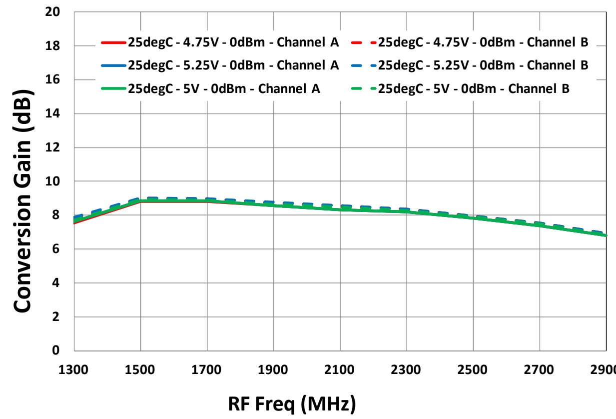
Gain vs. T_{case} [G_{MXR}, LS Injection]



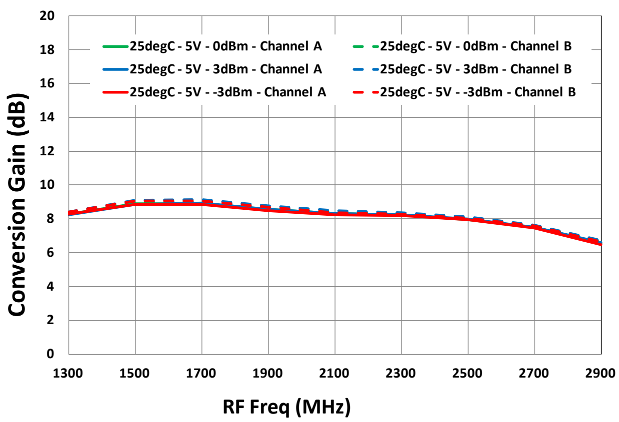
Gain vs. V_{cc} [G_{MXR}, HS Injection]



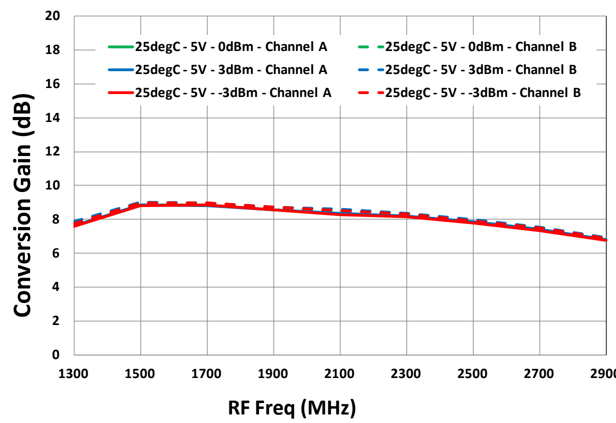
Gain vs. V_{cc} [G_{MXR}, LS Injection]



Gain vs. LO Power [G_{MXR}, HS Injection]

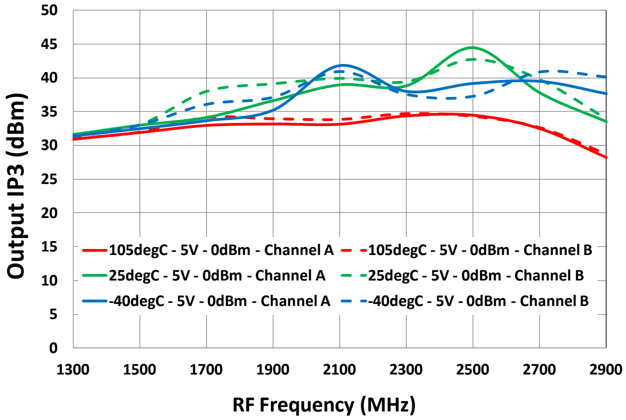


Gain vs. LO Power [G_{MXR}, LS Injection]

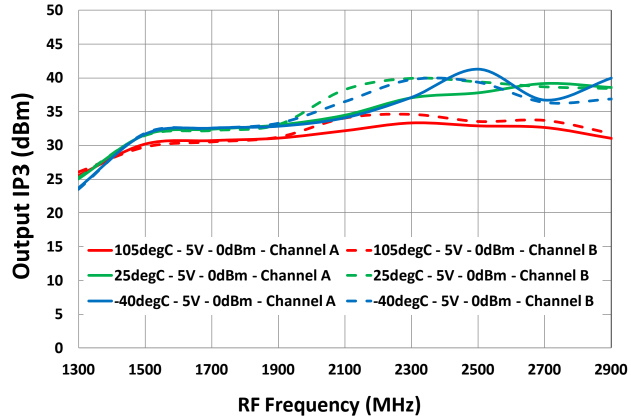


MIXER: TYPICAL OPERATING CONDITIONS (- 10 -)

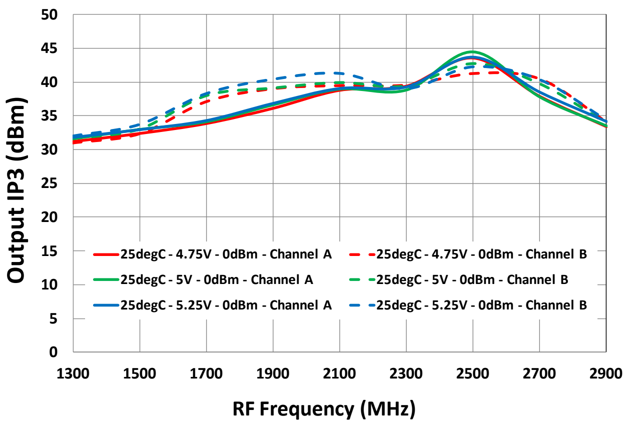
OIP3 vs. T_{case} [$OIP3_{MXR}$, HS injection]



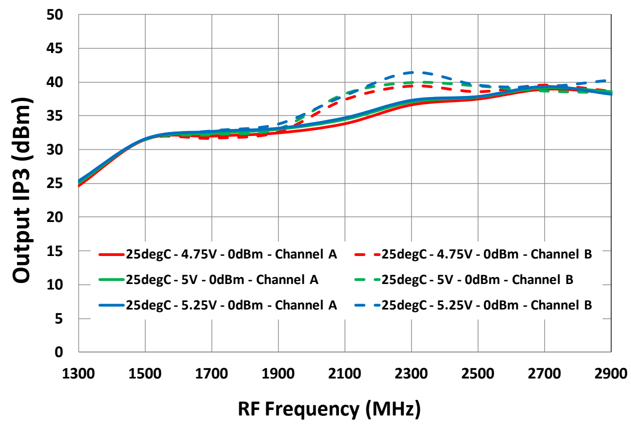
OIP3 vs. T_{case} [$OIP3_{MXR}$, LS injection]



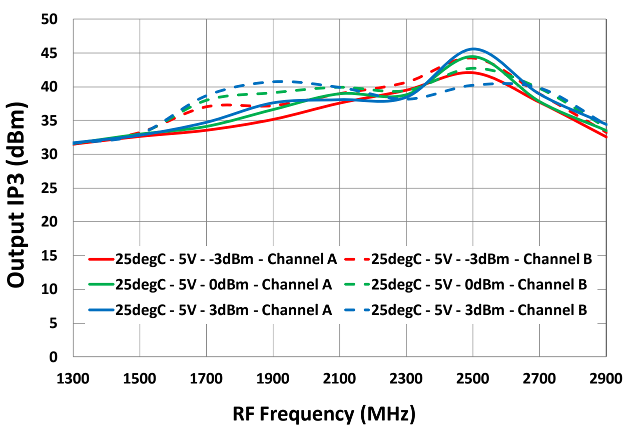
OIP3 vs. V_{CC} [$OIP3_{MXR}$, HS injection]



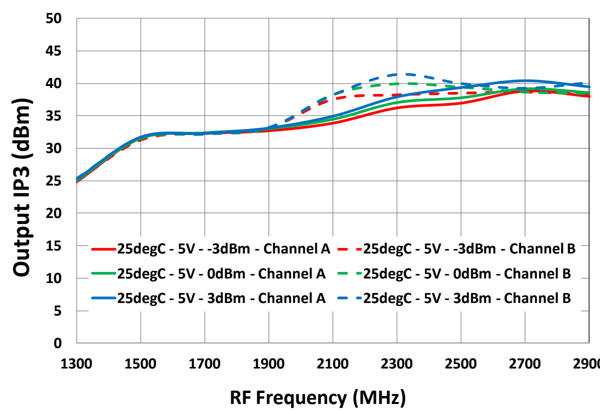
OIP3 vs. V_{CC} [$OIP3_{MXR}$, LS injection]



OIP3 vs. LO Power [$OIP3_{MXR}$, HS injection]

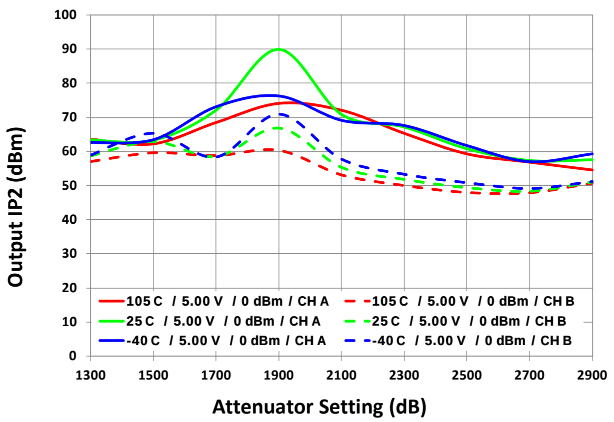


OIP3 vs. LO Power [$OIP3_{MXR}$, LS injection]

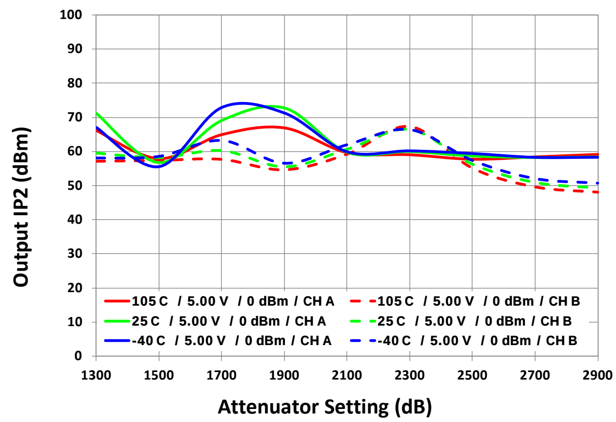


MIXER: TYPICAL OPERATING CONDITIONS (- 11 -)

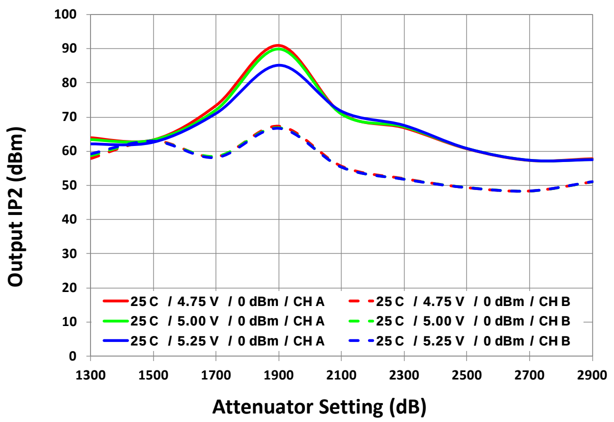
OIP2 vs. T_{case} [$OIP2_{MXR}$, HS injection]



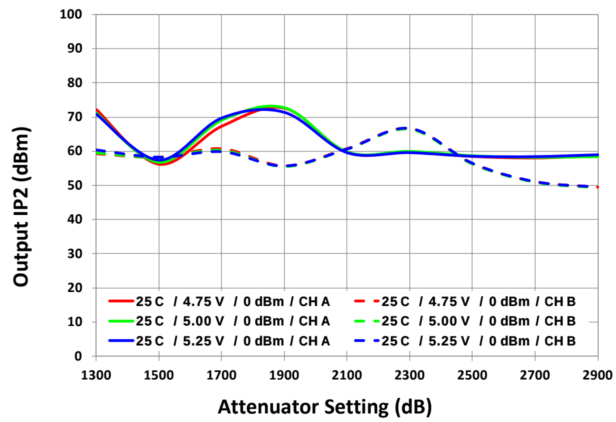
OIP2 vs. T_{case} [$OIP2_{MXR}$, LS injection]



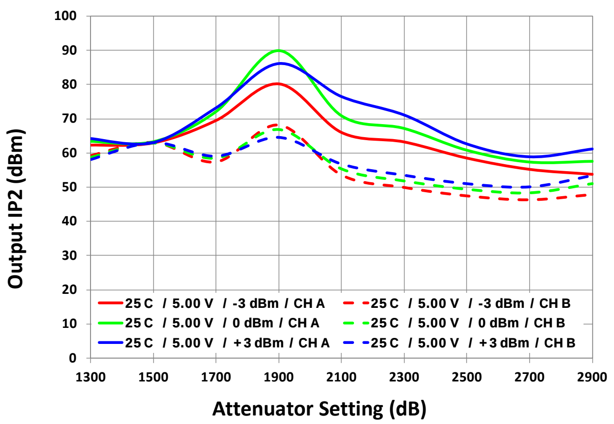
OIP2 vs. V_{cc} [$OIP2_{MXR}$, HS injection]



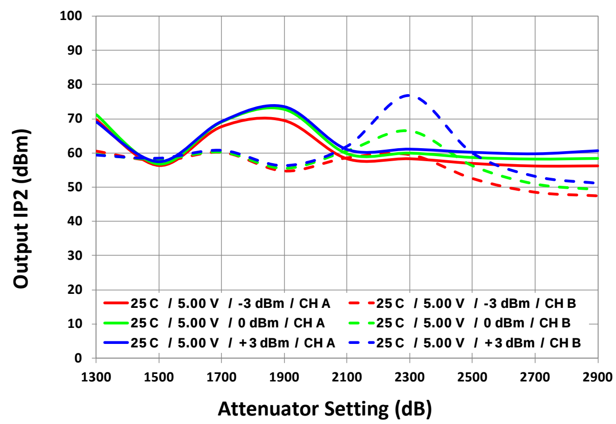
OIP2 vs. V_{cc} [$OIP2_{MXR}$, LS injection]



OIP2 vs. LO Power [$OIP2_{MXR}$, HS injection]

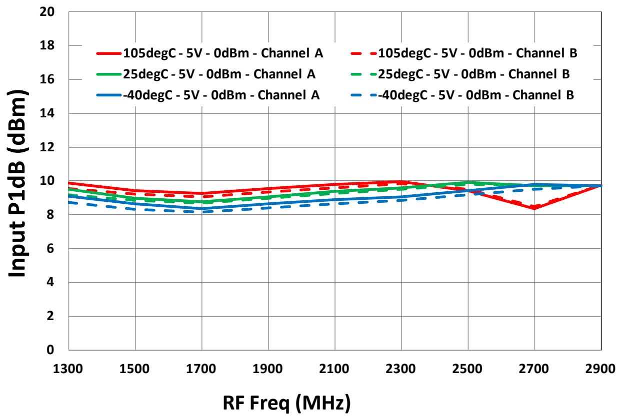


OIP2 vs. LO Power [$OIP2_{MXR}$, LS injection]

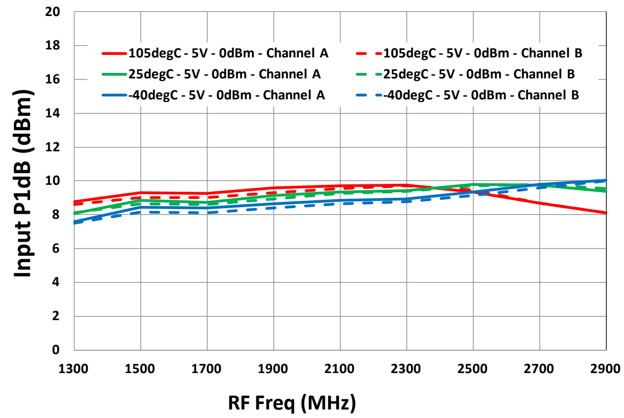


MIXER: TYPICAL OPERATING CONDITIONS (- 12 -)

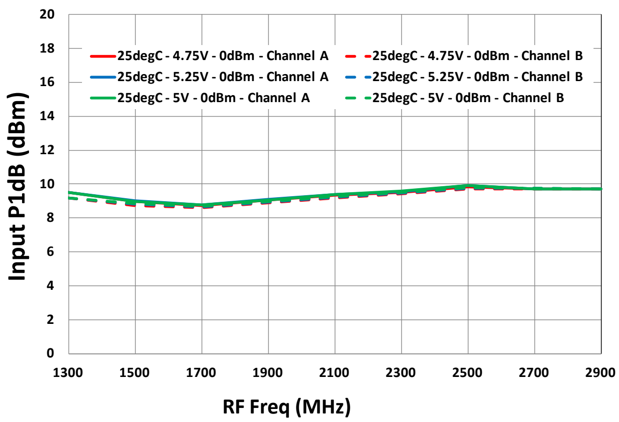
IP1dB vs. T_{case} [$IP1dB_{MXR}$, HS injection]



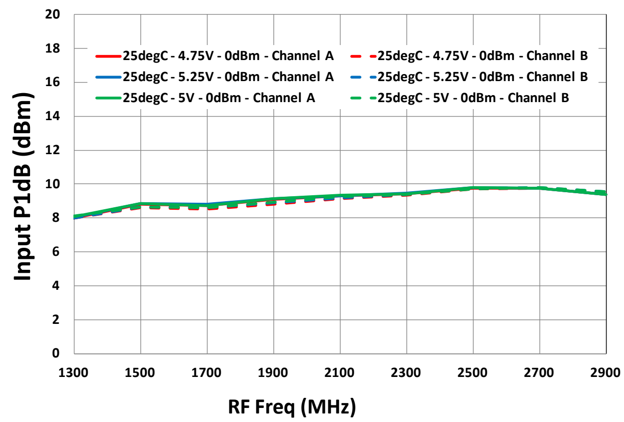
IP1dB vs. T_{case} [$IP1dB_{MXR}$, LS injection]



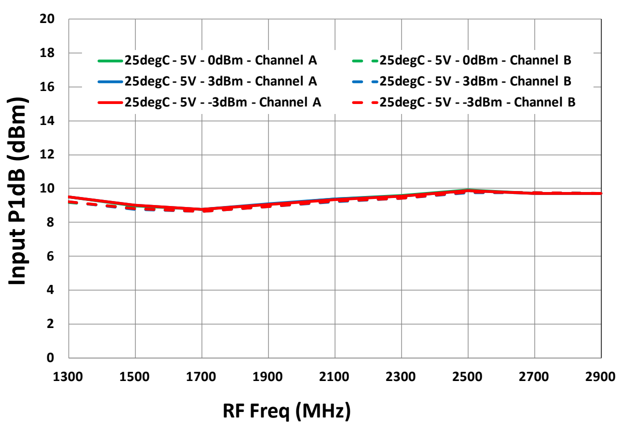
IP1dB vs. V_{cc} [$IP1dB_{MXR}$, HS injection]



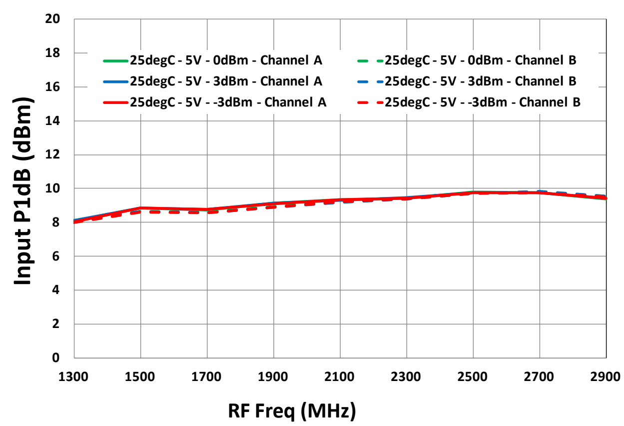
IP1dB vs. V_{cc} [$IP1dB_{MXR}$, LS injection]



IP1dB vs. LO Power [$IP1dB_{MXR}$, HS injection]

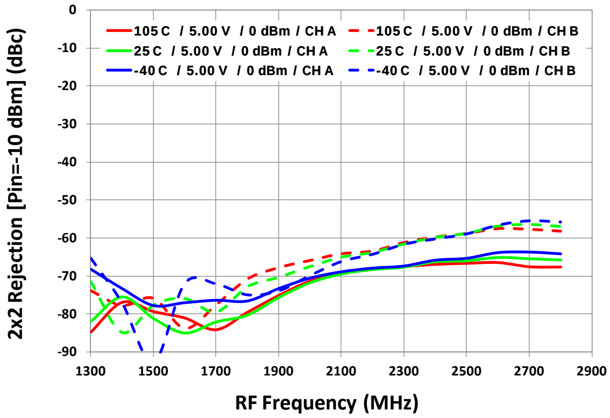


IP1dB vs. LO Power [$IP1dB_{MXR}$, LS injection]

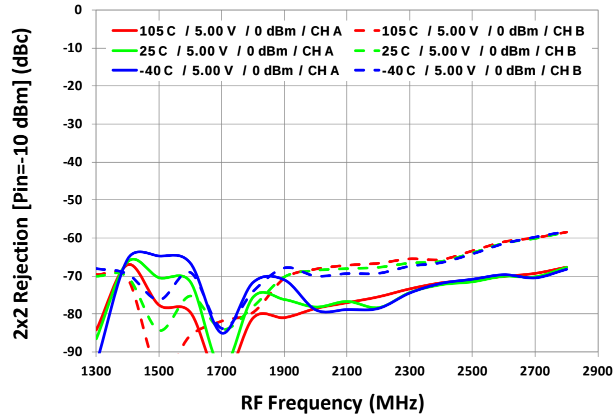


MIXER: TYPICAL OPERATING CONDITIONS (- 13 -)

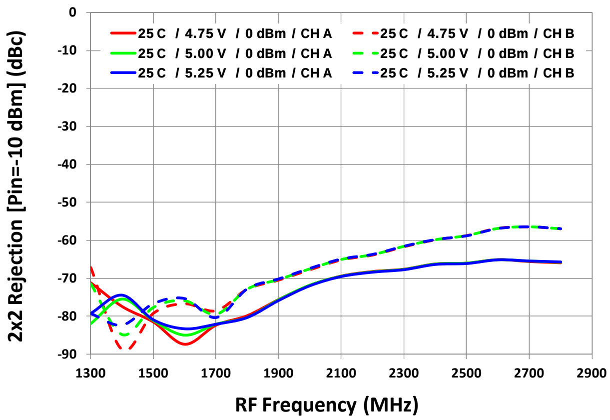
2x2 Rejection vs. T_{case} [$2x2_{MXR}$, HS rejection]



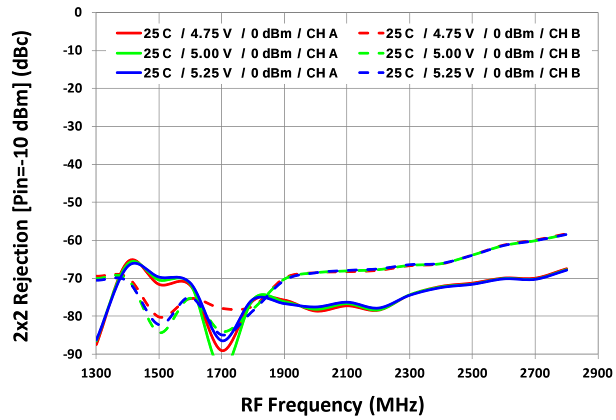
2x2 Rejection vs. T_{case} [$2x2_{MXR}$, LS rejection]



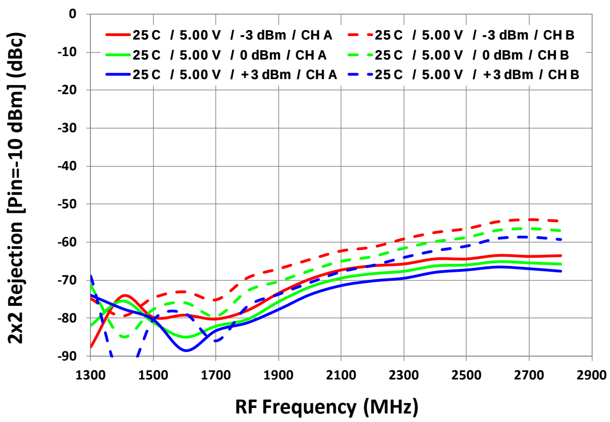
2x2 Rejection vs. V_{cc} [$2x2_{MXR}$,HS rejection]



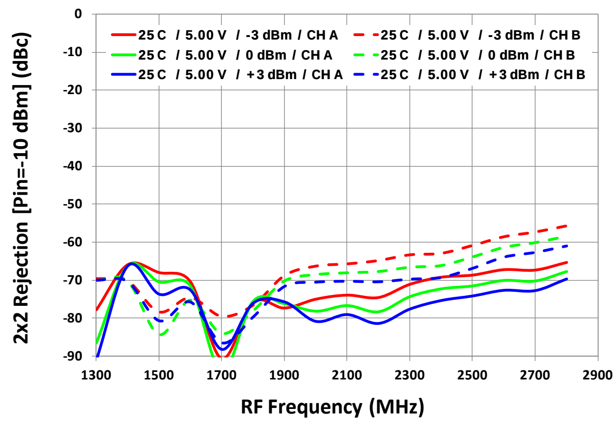
2x2 Rejection vs. V_{cc} [$2x2_{MXR}$, LS rejection]



2x2 Rejection vs. LO Power [$2x2_{MXR}$, HS rejection]

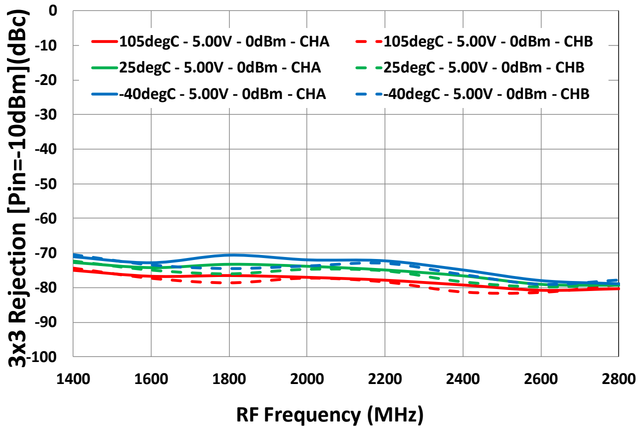


2x2 Rejection vs. LO Power [$2x2_{MXR}$, LS rejection]

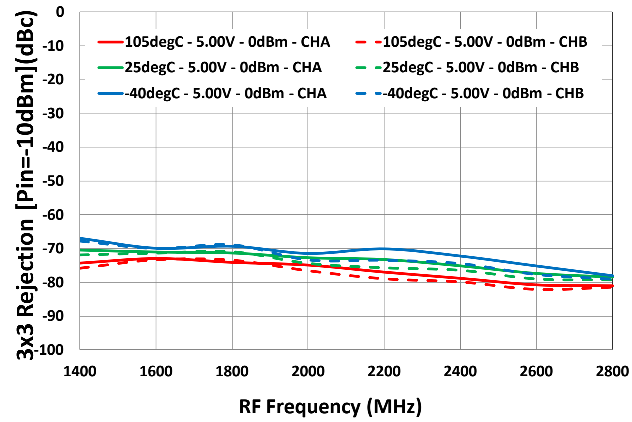


MIXER: TYPICAL OPERATING CONDITIONS (- 14 -)

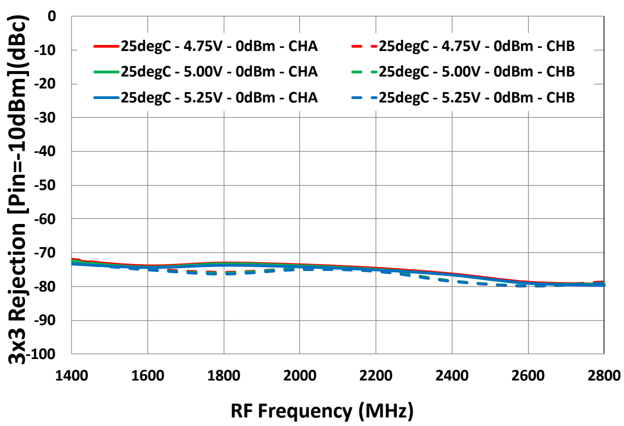
3x3 Rejection vs. T_{case} [$3x3_{MXR}$, HS rejection]



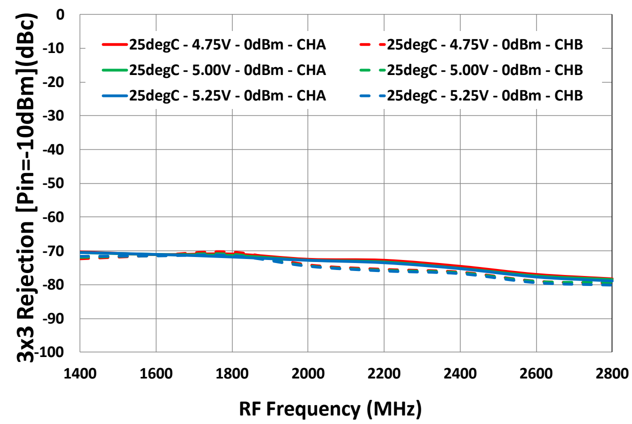
3x3 Rejection vs. T_{case} [$3x3_{MXR}$, LS rejection]



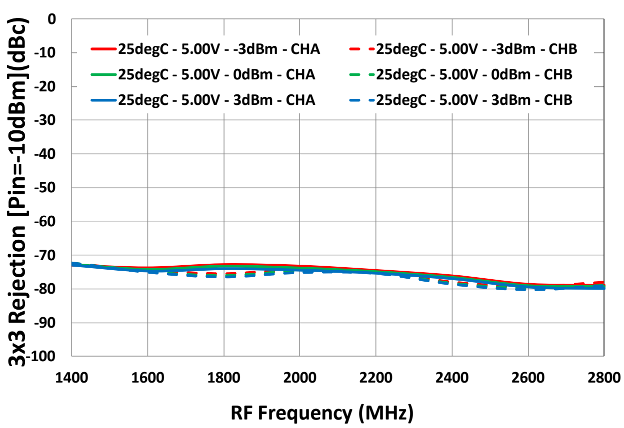
3x3 Rejection vs. V_{cc} [$3x3_{MXR}$, HS rejection]



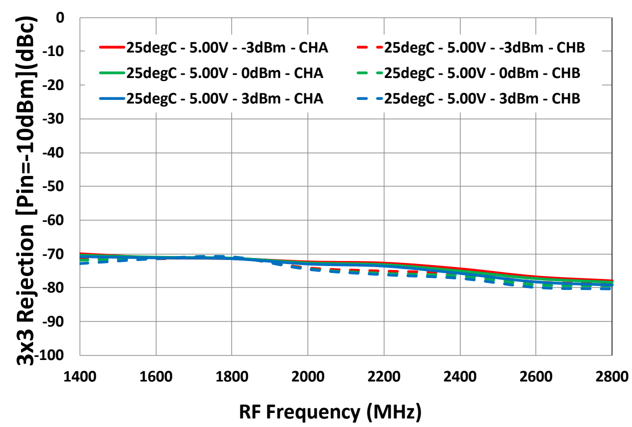
3x3 Rejection vs. V_{cc} [$3x3_{MXR}$, LS rejection]



3x3 Rejection vs. LO Power [$3x3_{MXR}$, HS rejection]

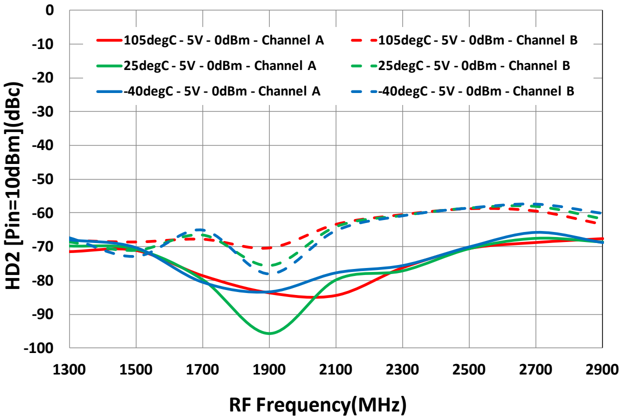


3x3 Rejection vs. LO Power [$3x3_{MXR}$, LS rejection]

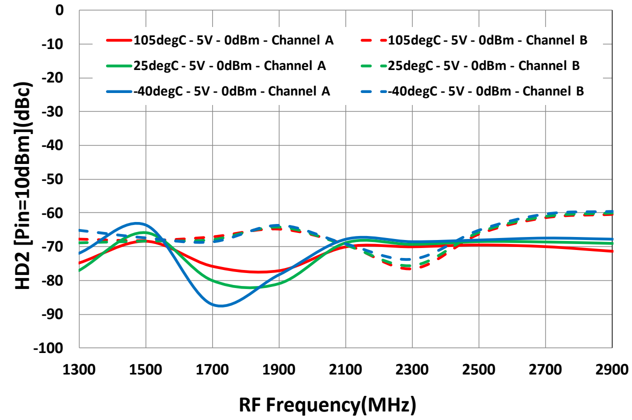


MIXER: TYPICAL OPERATING CONDITIONS (- 15 -)

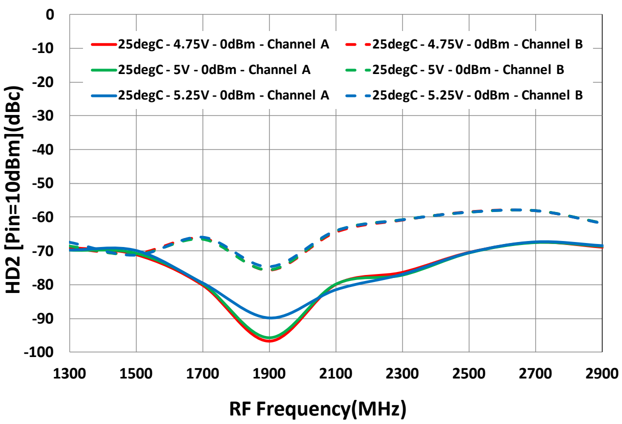
HD2 vs. T_{case} [$HD2_{MXR}$, HS injection]



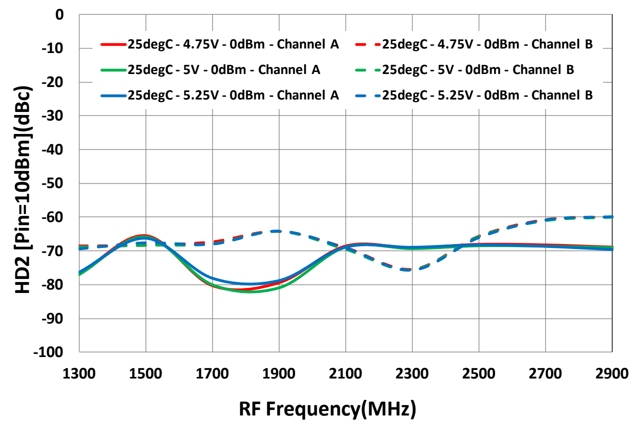
HD2 vs. T_{case} [$HD2_{MXR}$, LS injection]



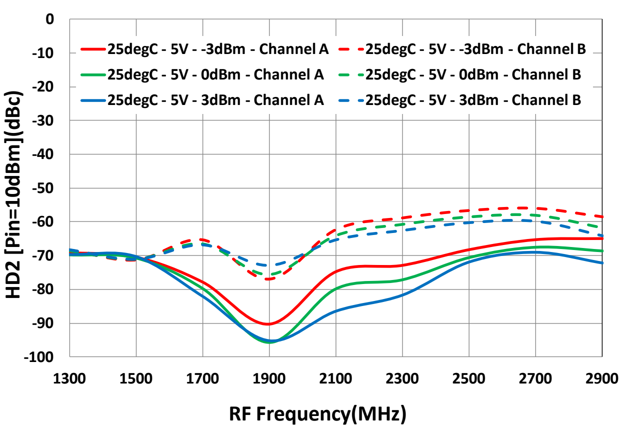
HD2 vs. V_{cc} [$HD2_{MXR}$, HS injection]



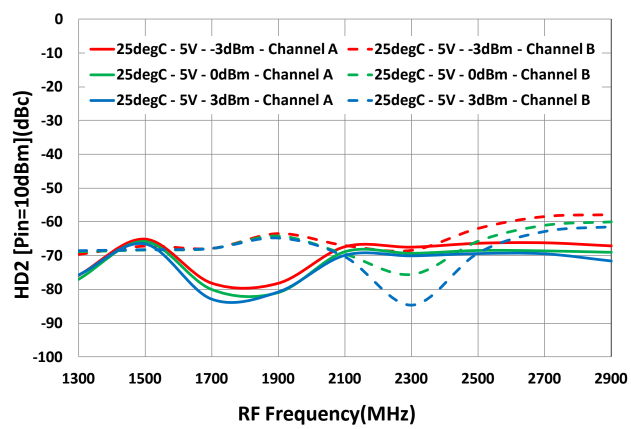
HD2 vs. V_{cc} [$HD2_{MXR}$, LS injection]



HD2 vs. LO Power [$HD2_{MXR}$, HS injection]

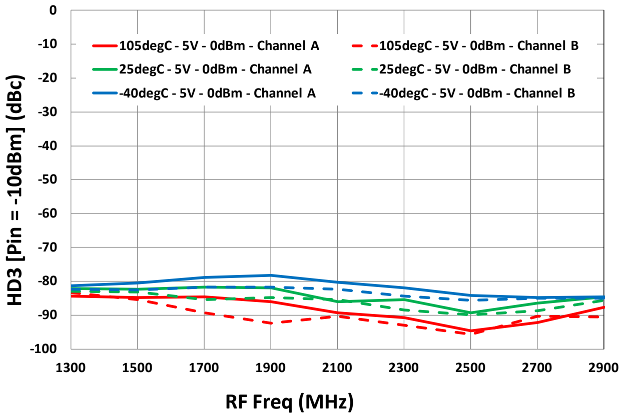


HD2 vs. LO Power [$HD2_{MXR}$, LS injection]

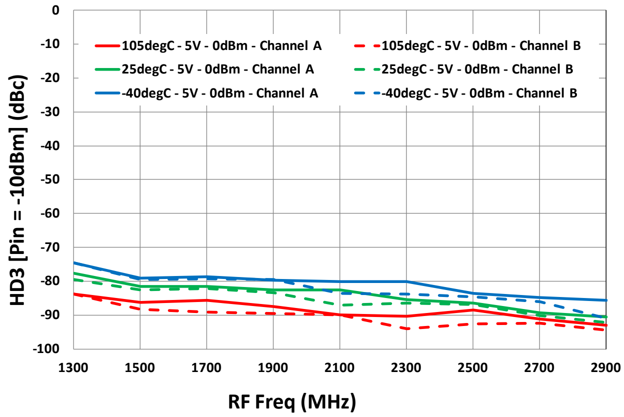


MIXER: TYPICAL OPERATING CONDITIONS (- 16 -)

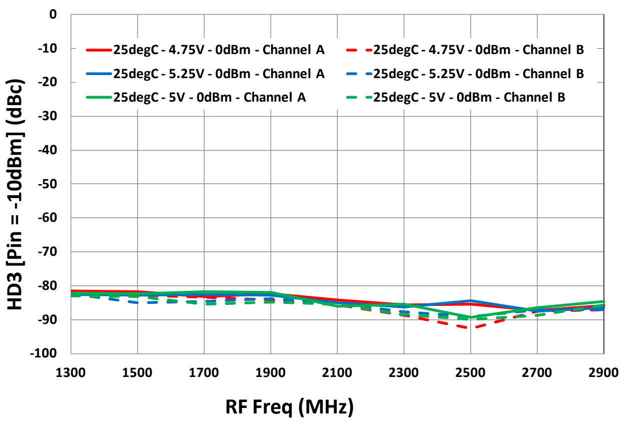
HD3 vs. T_{case} [$HD3_{MXR}$, HS injection]



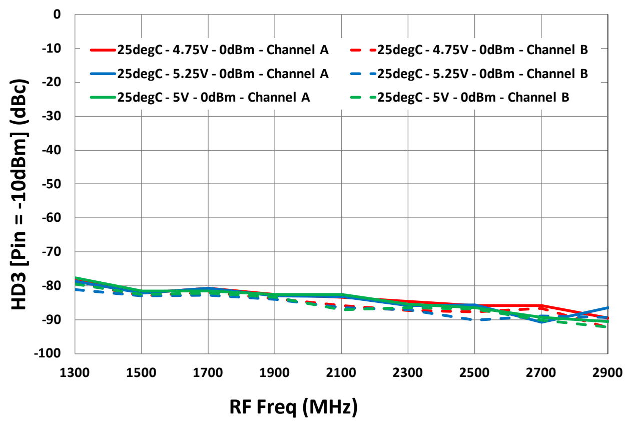
HD3 vs. T_{case} [$HD3_{MXR}$, LS injection]



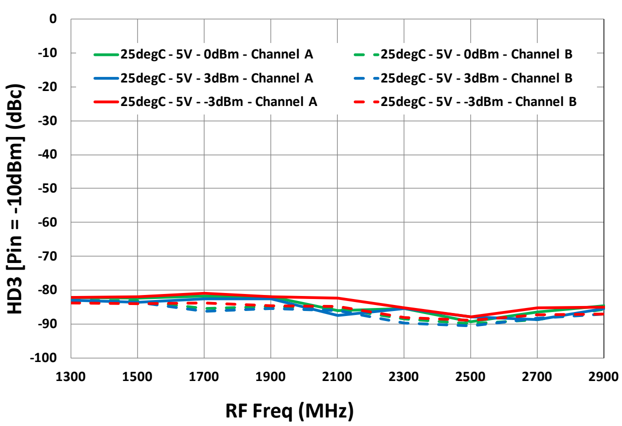
HD3 vs. V_{cc} [$HD3_{MXR}$, HS injection]



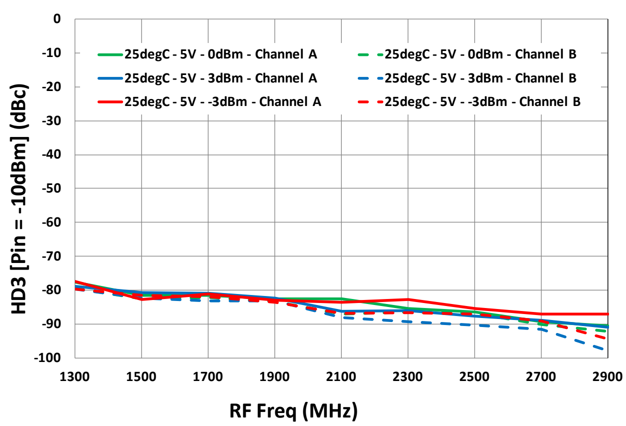
HD3 vs. V_{cc} [$HD3_{MXR}$, LS injection]



HD3 vs. LO Power [$HD3_{MXR}$, HS injection]

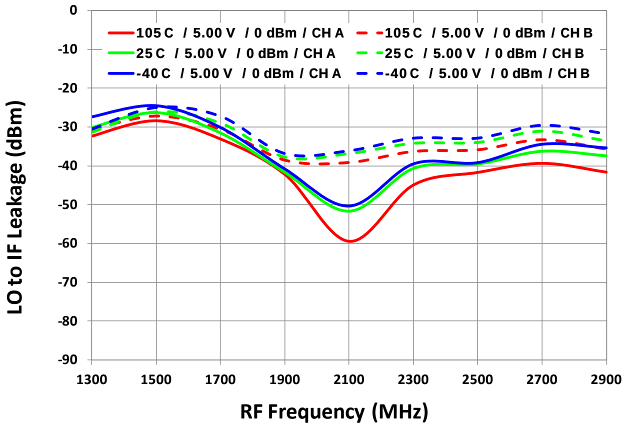


HD3 vs. LO Power [$HD3_{MXR}$, LS injection]

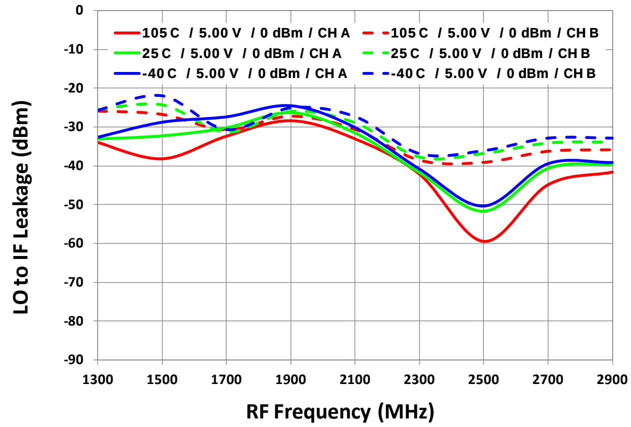


MIXER: TYPICAL OPERATING CONDITIONS (- 17 -)

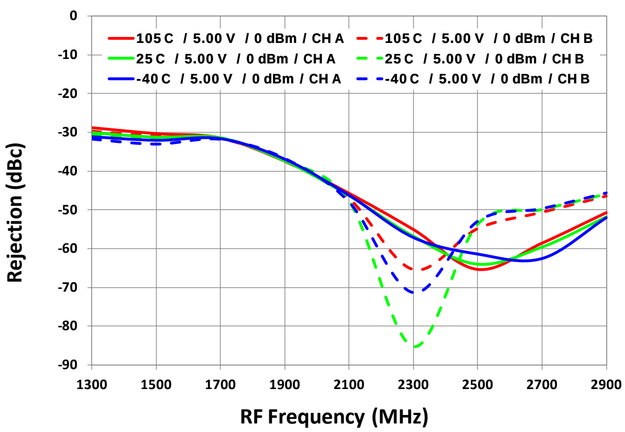
LO to IF Leakage vs. T_{case} [ISO_{LI}, HS injection]



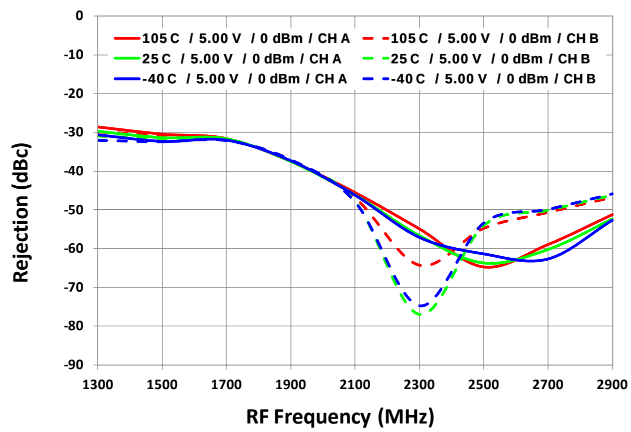
LO to IF Leakage vs. T_{case} [ISO_{LI}, LS injection]



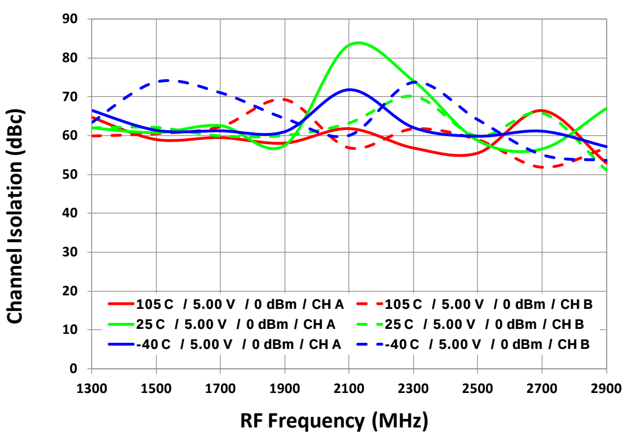
RF to IF Rejection vs. T_{case} [ISO_{RI}, HS injection]



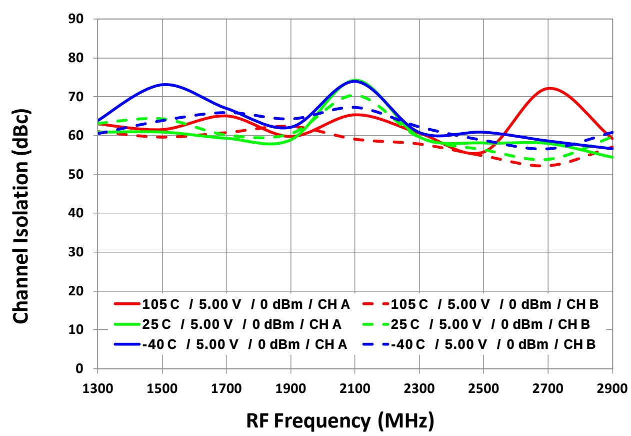
RF to IF Rejection vs. T_{case} [ISO_{RI}, LS injection]



Channel Isolation vs. T_{case} [ISO_{IF}, HS injection]

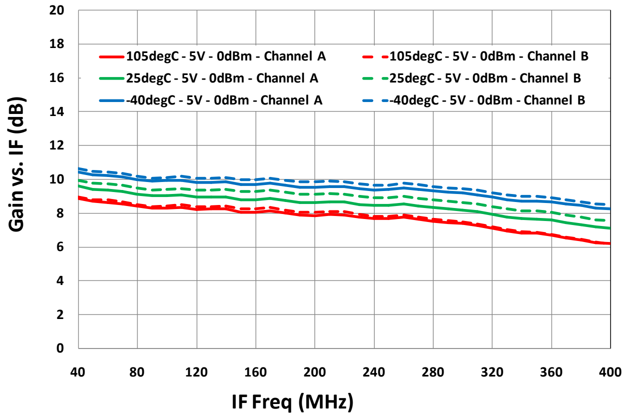


Channel Isolation vs. T_{case} [ISO_{IF}, LS injection]

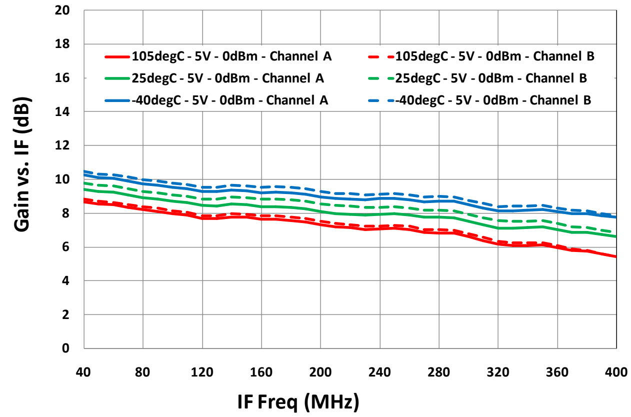


MIXER: TYPICAL OPERATING CONDITIONS (- 18 -)

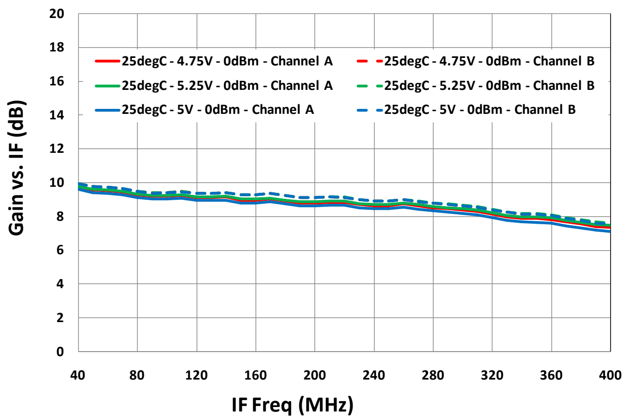
IF Gain flatness vs. T_{case} [G_{MXR_T}, HS injection]



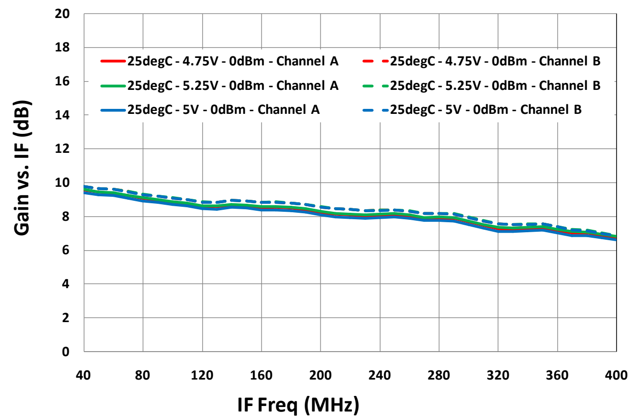
IF Gain flatness vs. T_{case} [G_{MXR_T}, LS injection]



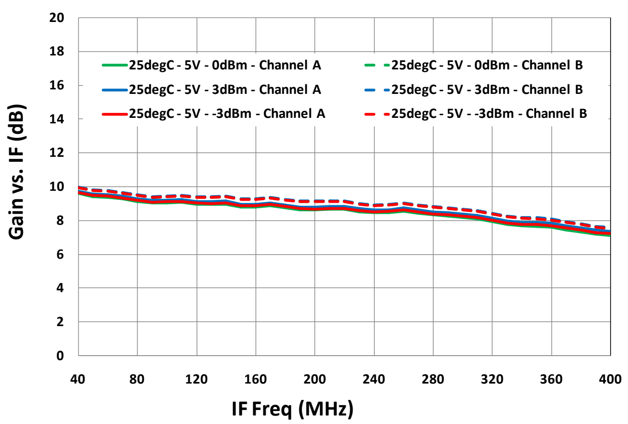
IF Gain flatness vs. V_{cc} [G_{MXR_T}, HS injection]



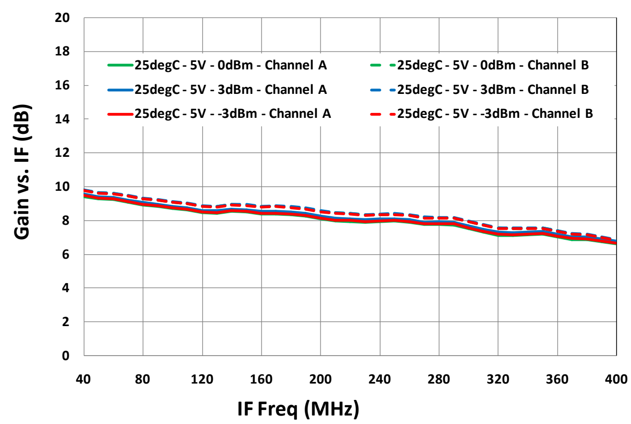
IF Gain flatness vs. V_{cc} [G_{MXR_T}, LS injection]



IF Gain flatness vs. LO Power [G_{MXR_T}, HS injection]

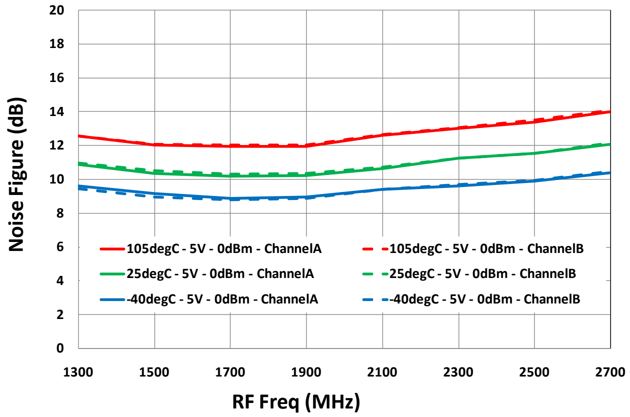


IF Gain flatness vs. LO Power [G_{MXR_T}, LS injection]

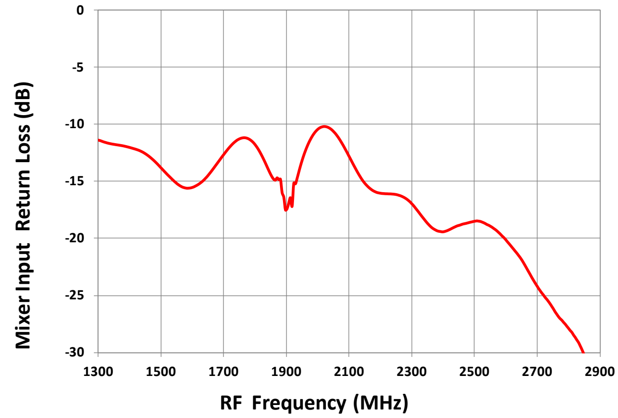


MIXER: TYPICAL OPERATING CONDITIONS (- 19 -)

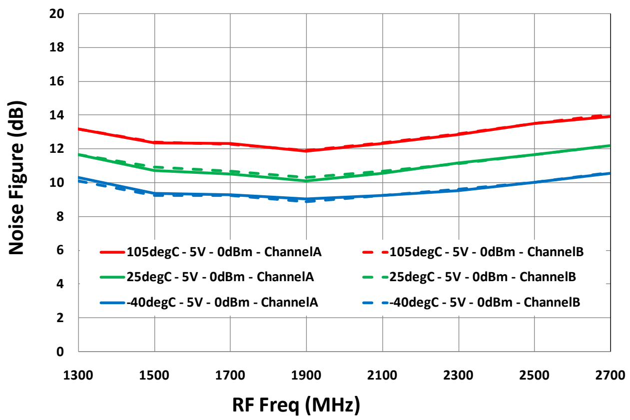
Noise Figure vs.T_{case} [NF_{MXR}, HS Injection]



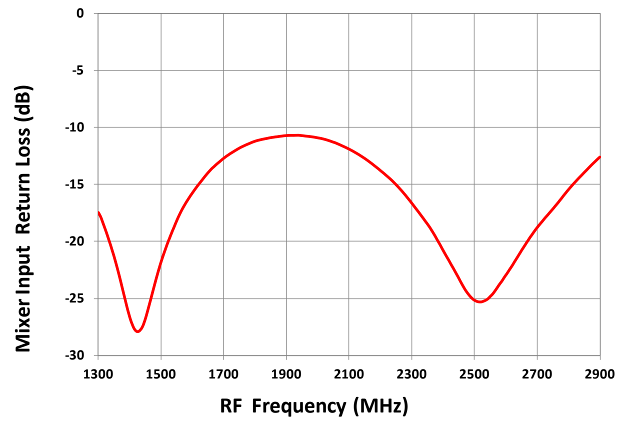
Mixer RF Input Return Loss [$S11_{MXR\_RF}$]



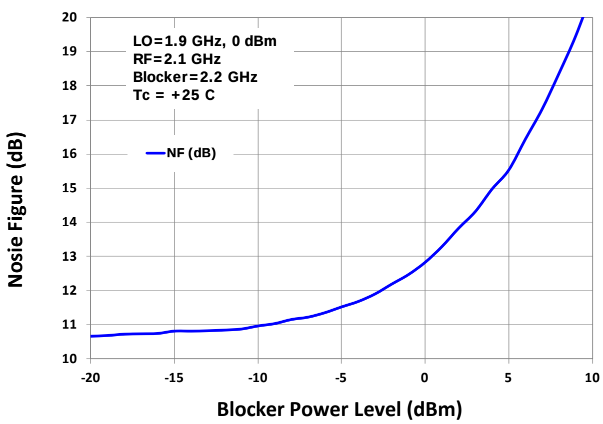
Noise Figure vs.T_{case} [NF_{MXR} LS, Injection]



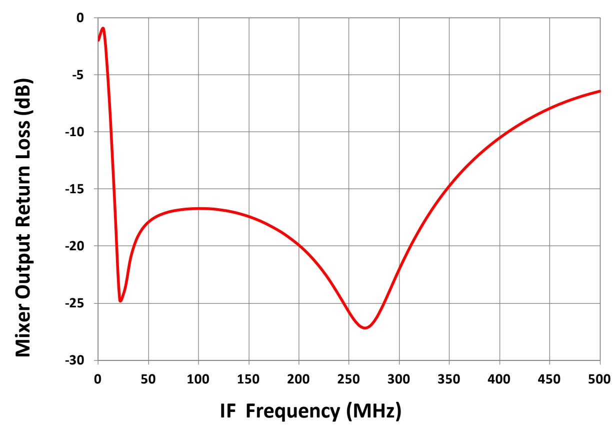
Mixer LO Port Return Loss [$S11_{MXR\_LO}$]



Noise Figure with Blocker [NF_{MXR_BLK}]

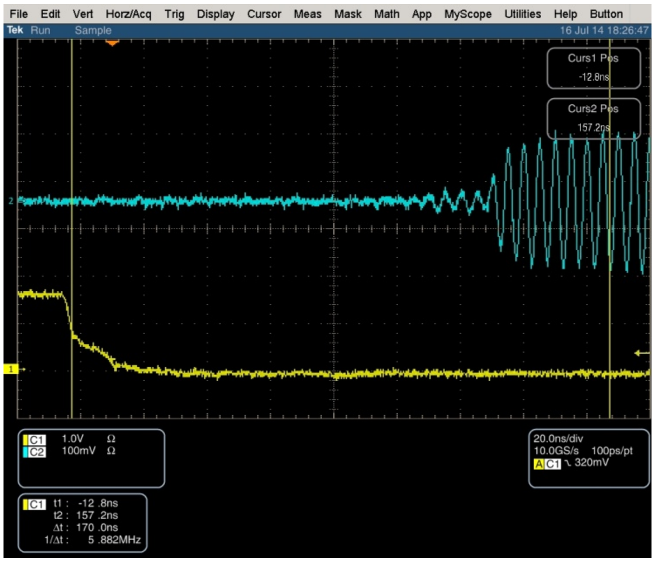


Mixer IF Output Return Loss [$S22_{MXR\_IF}$]

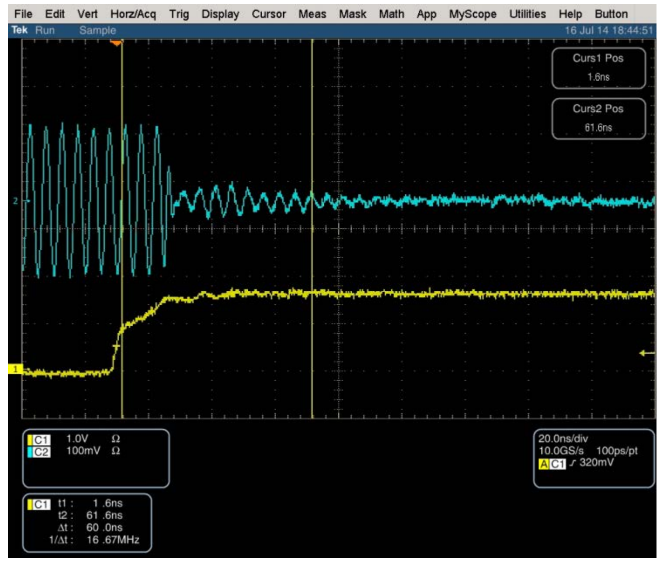


MIXER: TYPICAL OPERATING CONDITIONS (- 20 -)

Mixer STBY ON time [Min to Max, τ_{MXR_SET}]

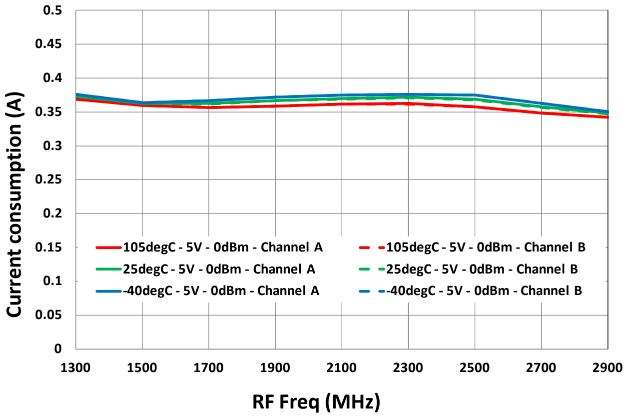


Mixer STBY OFF time [Max to Min, τ_{MXR_SET}]

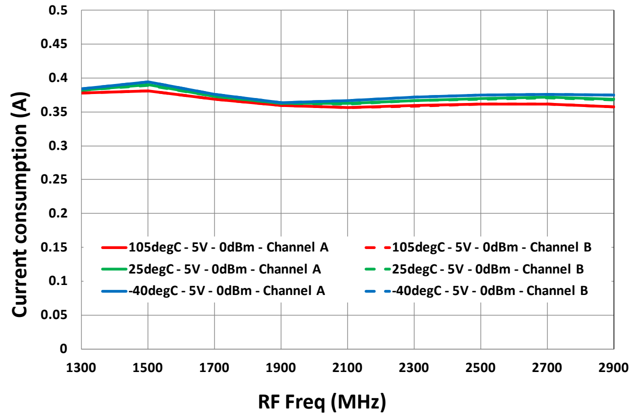


VGA & MIXER: TYPICAL OPERATING CONDITIONS (- 21 -)

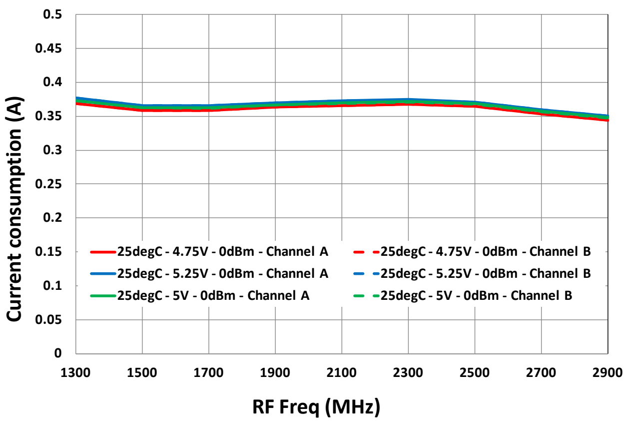
Current Consumption vs. T_{case} [HS injection]



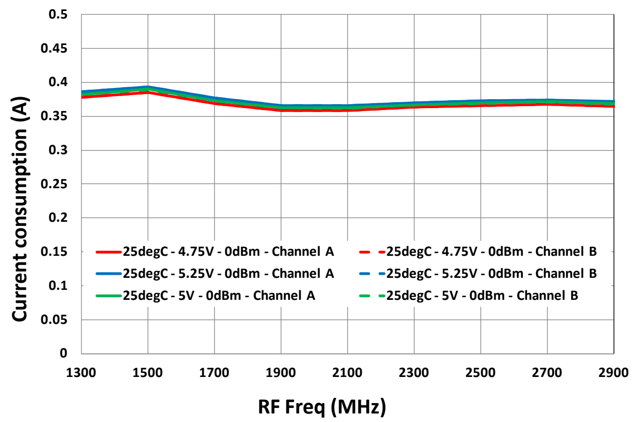
Current consumption vs. T_{case} [LS injection]



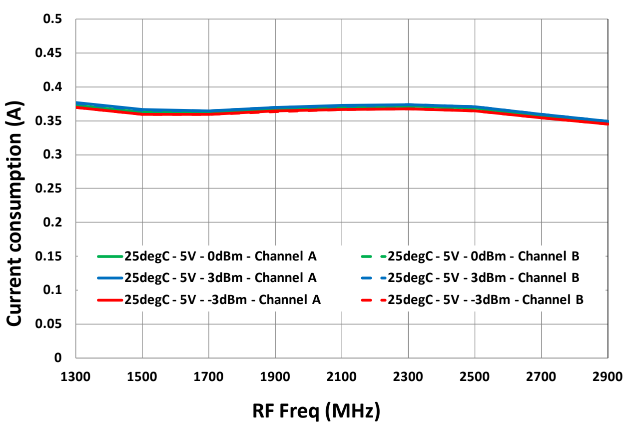
Current consumption vs. V_{cc} [HS injection]



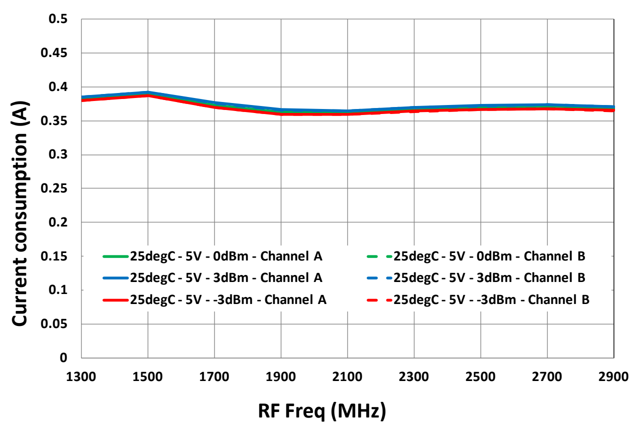
Current consumption vs. V_{cc} [LS injection]



Current consumption vs. LO Power [HS injection]

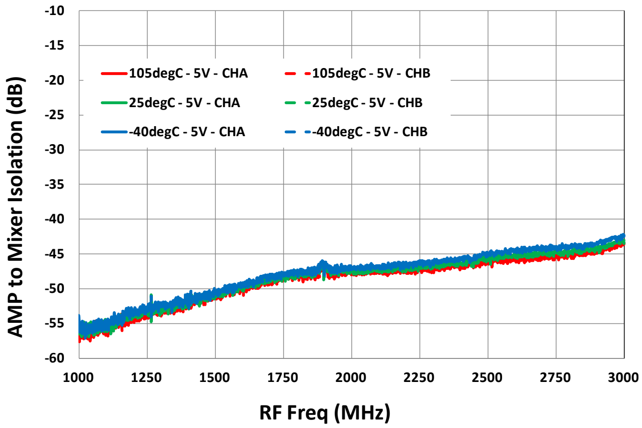


Current consumption vs. LO Power [LS injection]



VGA & MIXER: TYPICAL OPERATING CONDITIONS (- 22 -)

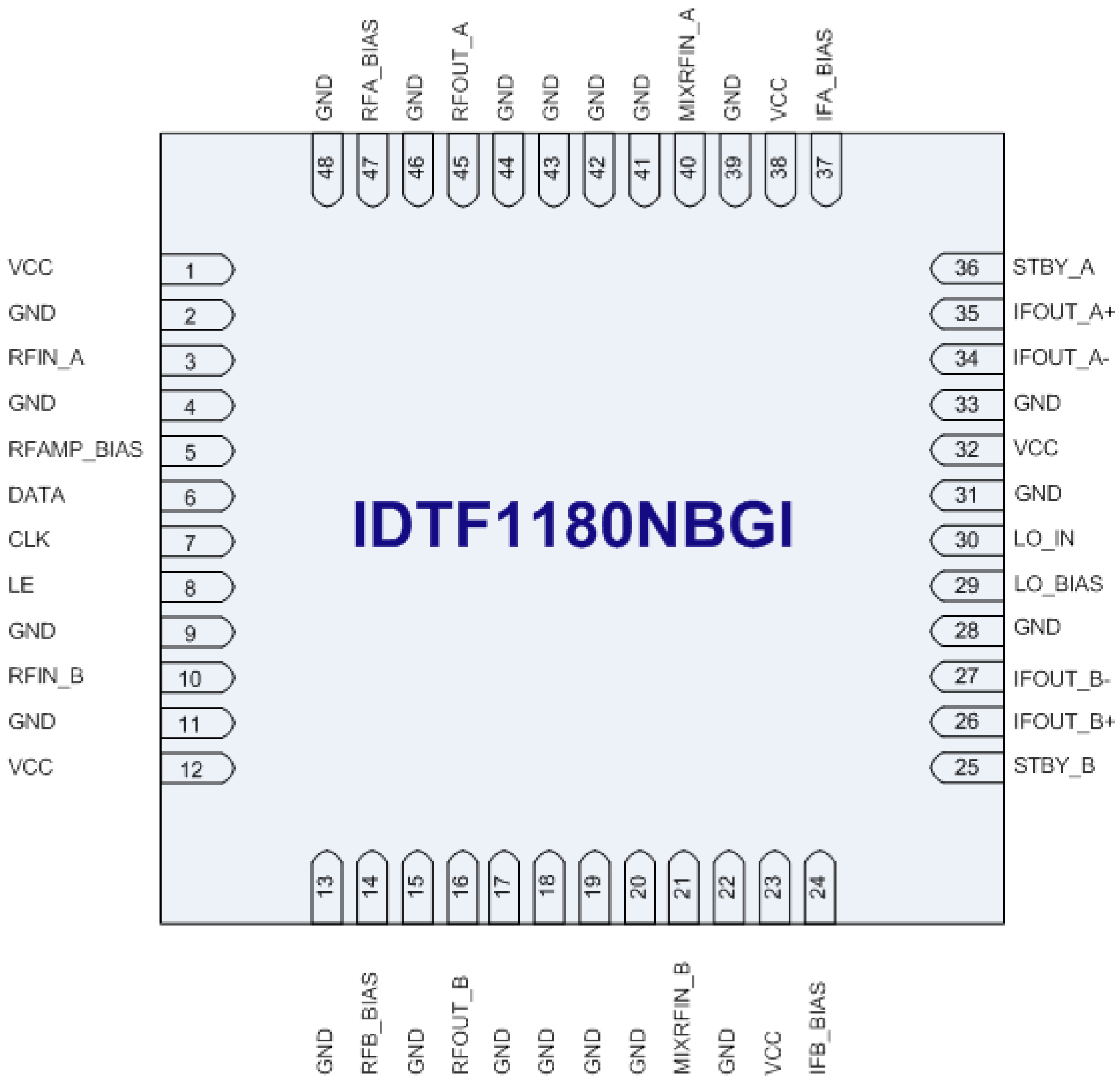
RF Amplifier to Mixer Isolation



PACKAGE OUTLINE DRAWINGS

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

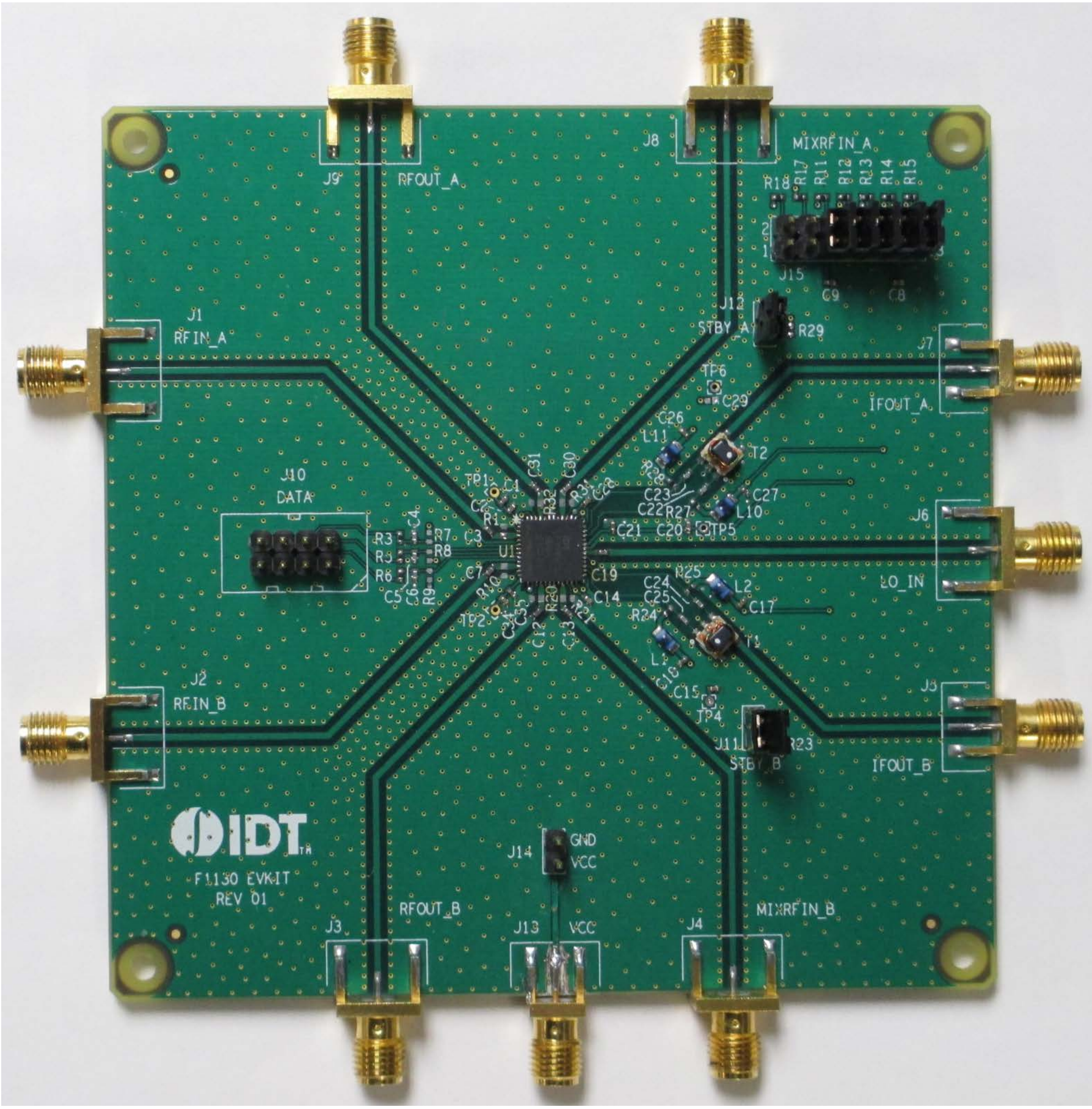
PIN DIAGRAM



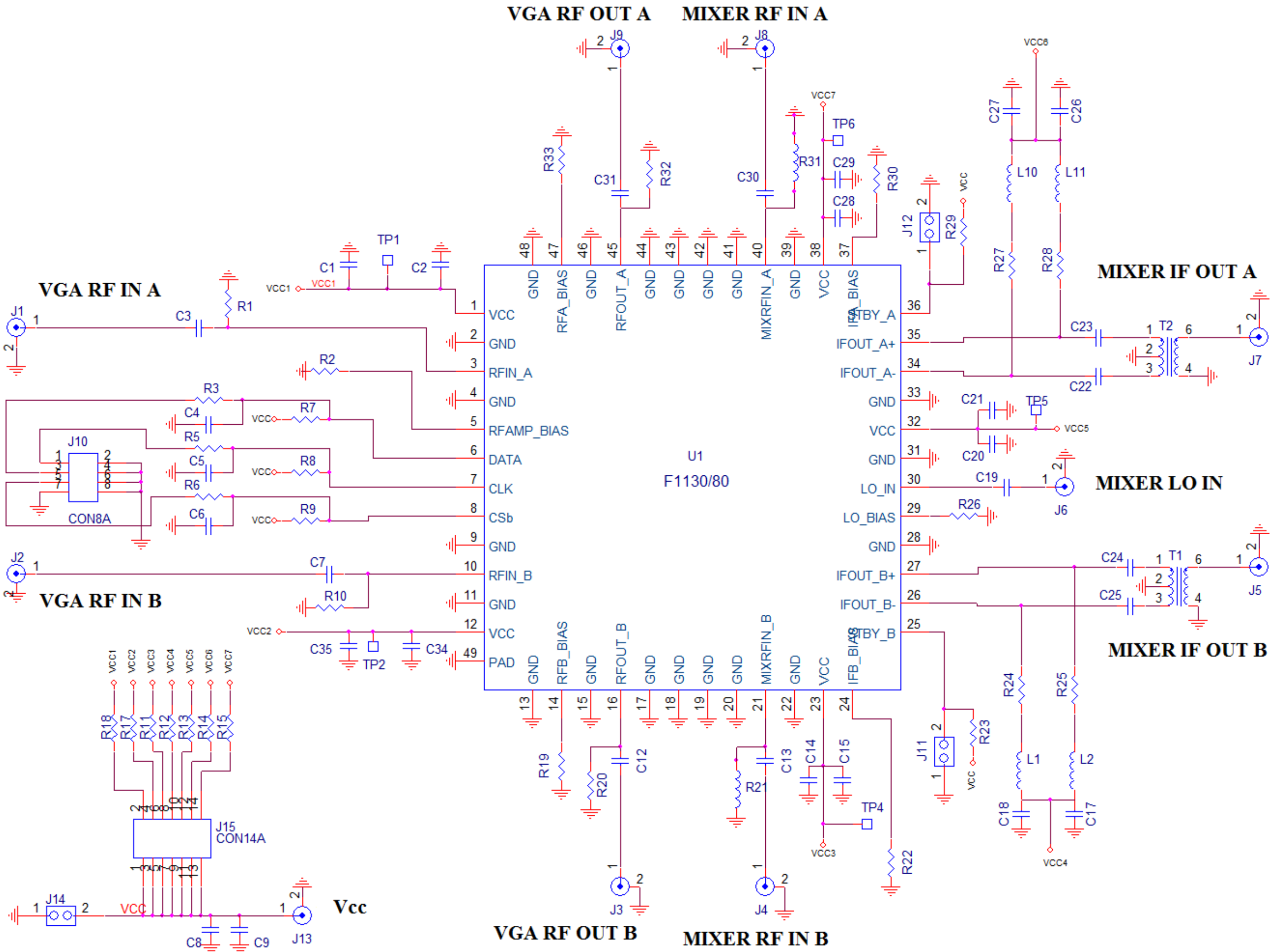
PIN DESCRIPTION

Pin	Name	Function
1, 12, 23, 32, 38	VCC	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
2, 4, 9, 11, 13, 15, 17, 18, 19, 20, 22, 28, 31, 33, 39, 41, 42, 43, 44, 46, 48	GND	Ground these pins.
3	RFIN_A	Channel-A VGA RF Input. Internally matched to 50Ω. AC coupled. DO NOT apply DC to this pin. Place coupling capacitor as close to the pin as possible.
5	RFAMP_BIAS	Connect a resistor to GND (refer to BOM)
6	SPI Data	Data: 1.8V CMOS compatible.
7	SPI CLK	Clock: 1.8V CMOS compatible.
8	SPI LE	Latch Enable: 1.8V CMOS compatible. See Serial Interface Section for pin description.
10	RFIN_B	Channel-B VGA RF Input. Internally matched to 50Ω. AC coupled. DO NOT apply DC to this pin. Place coupling capacitor as close to the pin as possible.
14	RFB_BIAS	Connect a resistor to GND (refer to BOM).
16	RFOUT_B	Channel-B VGA RF Output. Internally matched to 50Ω. AC coupled. DO NOT apply DC to this pin. Place coupling capacitor as close to the pin as possible.
21	MIXRFIN_B	Channel-B Mixer RF Input. Internally matched to 50Ω. DO NOT apply DC to this pin.
24	IFB_BIAS	Connect a resistor to GND (refer to BOM).
25	STBY_B	Standby Diversity Channel (Low = device power ON, High = device power OFF with SPI still powered ON)
26	IFOUT_B+	Channel-B Mixer Differential IF- Output. Connect pullup inductor from this pin to VCC.
27	IFOUT_B-	Channel-B Mixer Differential IF+ Output. Connect pullup inductor from this pin to VCC.
29	LO_BIAS	Connect a resistor to GND (refer to BOM).
30	LO_IN	Mixer Local Oscillator Input. Connect the LO to this port through the recommended coupling capacitor.
34	IFOUT_A-	Channel-A Mixer Differential IF- Output. Connect pullup inductor from this pin to VCC.
35	IFOUT_A+	Channe-Al Mixer Differential IF+ Output. Connect pullup inductor from this pin to VCC.
36	STBY_A	Standby Main Channel (Low = device power ON, High = device power OFF with SPI still powered ON).
37	IFA_BIAS	Connect a resistor to GND (refer to BOM).
40	MIXRFIN_A	Channel-A Mixer RF Input. Internally matched to 50Ω. DO NOT apply DC to this pin.
45	RFOUT_A	Channel-A RF VGA Output. Internally matched to 50Ω. AC coupled. DO NOT apply DC to this pin. Place coupling capacitor as close to the pin as possible.
47	RFA_BIAS	Connect a resistor to GND (refer to BOM).
	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance.

EVKIT PICTURE



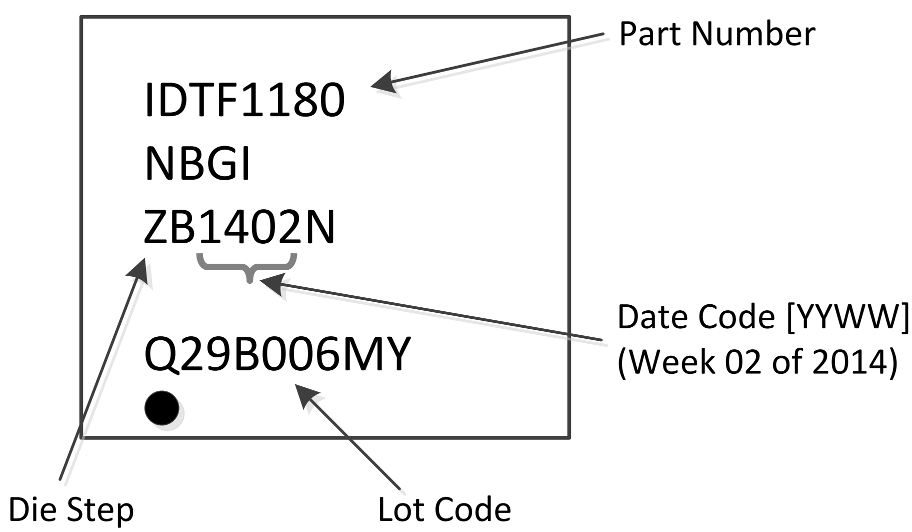
EVKIT / APPLICATIONS CIRCUIT



EVKit BOM

Item #	Part Reference	QTY	Description	Mfr. Part #	Mfr.
1	C2, 8, 14, 17, 20, 26, 28, 34	8	CAP CER 10000PF 16V 10% X7R 0402	GRM155R71C103KA01D	Murata
2	C1, 9, 15, 18, 21, 27, 29, 35	8	CAP CER 0.1UF 16V 10% X7R 0402	GRM155R71C104KA88D	Murata
3	C3, 7, 12, 13, 19, 30, 31	7	CAP CER 39PF 50V 5% C0G 0402	GRM1555C1H390JZ010	Murata
4	C22-25	4	CAP CER 1000PF 50V C0G 0402	GRM1555C1H102JA01D	Murata
5	R2	1	RES 12.4K OHM 1/10W 1% 0402 SMD	ERJ-2RKF1242X	Panasonic
6	R3, 5, 6, 26	4	RES 3.00K OHM 1/10W 1% 0402 SMD	ERJ-2RKF3001X	Panasonic
7	R19, 33	2	RES 3.83K OHM 1/10W 1% 0402 SMD	ERJ-2RKF3831X	Panasonic
8	R22, 30	2	RES 62.0 OHM 1/10W 1% 0402 SMD	ERJ-2RKF62R0X	Panasonic
9	R11-15, 17, 18, 24, 25, 27, 28	11	RES 0.0 OHM 1/10W 0402 SMD	ERJ-2GE0R00X	Panasonic
10	L1, 2, 10, 11	4	0805LS (2012) Ceramic Chip Inductor	0805LS-102XJLB	COILCRAFT
11	T1, 2	2	4:1 Center Tap Balun	TC4-1TG2+	Mini Circuits
12	J11, 12, 14	3	CONN HEADER VERT SGL 2POS GOLD	961102-6404-AR	3M
13	J10	1	CONN HEADER VERT DBL 4POS GOLD	67997-108HLF	FCI
14	J15	1	CONN HEADER VERT DBL 7POS GOLD	67996-114HLF	FCI
15	J1-4, 6, 8, 9	7	SMA_END_LAUNCH (Big)	142-0701-851	Emerson Johnson
16	J5, 7, 13	3	SMA_END_LAUNCH (Small)	142-0711-821	Emerson Johnson
17	U1	1	Dual Path RF Receiver 400-1100MHz	AV650B00_6ZNA	Renesas
18		1	Printed Cicuit Board	F1130 EVKIT REV 01	
19			Bill Of Material	0	
20	C4-6, R1, 7-10, 20, 21, 23, 29, 31, 32	0	Do not populate	N/A	N/A

Top Markings



APPLICATIONS INFORMATION

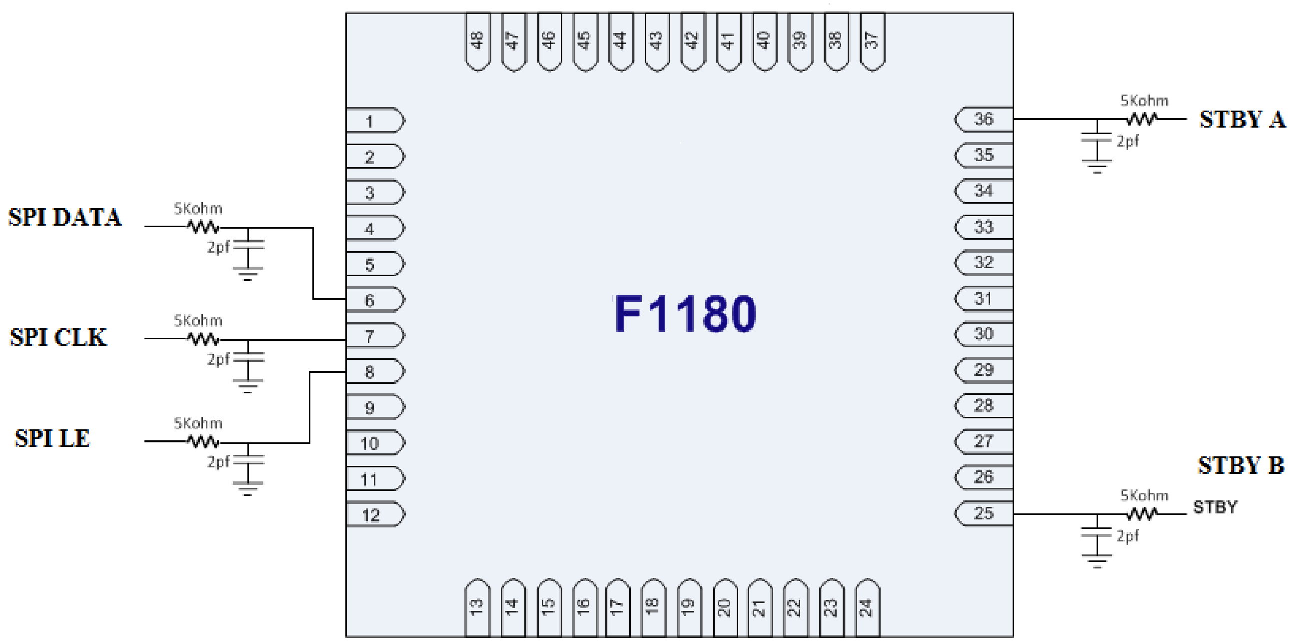
F1180 has been optimized for use in high performance RF applications from 1400MHz to 2700MHz.

Power Supplies

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µs. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to SPI and control pins 6, 7, 8, 25, and 36 as shown below. Note the recommended resistor and capacitor values do not necessarily match the EV kit BOM for the case of poor control signal integrity. For multiple devices driven by a single control line, the component values will need to be adjusted accordingly so as not to overload the control line.



F1180 Digital Pin Voltage & Resistance Values (pins not connected)

The following table list the resitance between various pins and ground when no DC power is applied. When the device is powered up with +5 Volts DC these same pins to should have the measured voltage to ground.

Pin	Name	DC Voltage (volts)	Resistance (ohms)
6	DATA	5	57K
7	CLK	5	57K
8	LE	5	57K
25	STBY_B	5	57K
36	STBY_A	5	57K

Ordering Information

Part Number	Package Description	Carrier Type	Temperature Range
F1180NBGI	48-VFQFPN, 7 × 7 mm	Tape and Reel	-40°C to +85°C
F1180NBGI8		Tray	

Revision History

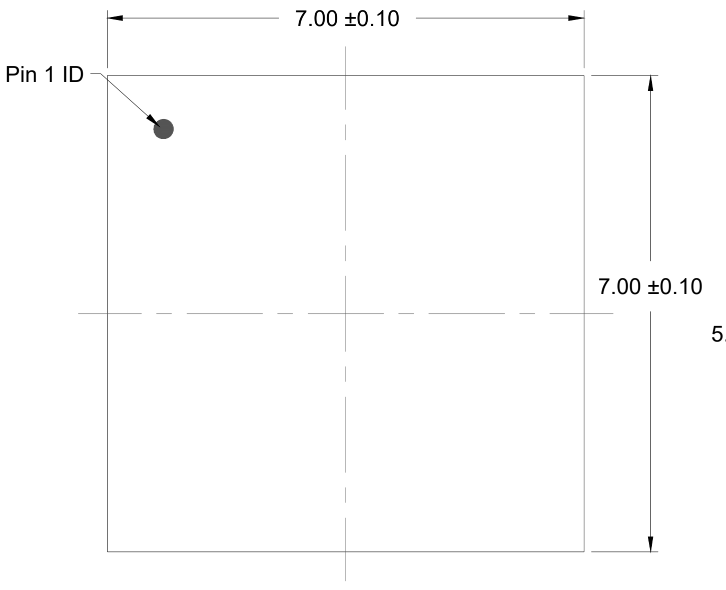
Revision Date	Description
February 8, 2022	Rebranded to Renesas.
July 20, 2016	Initial release.

Package Outline Drawing

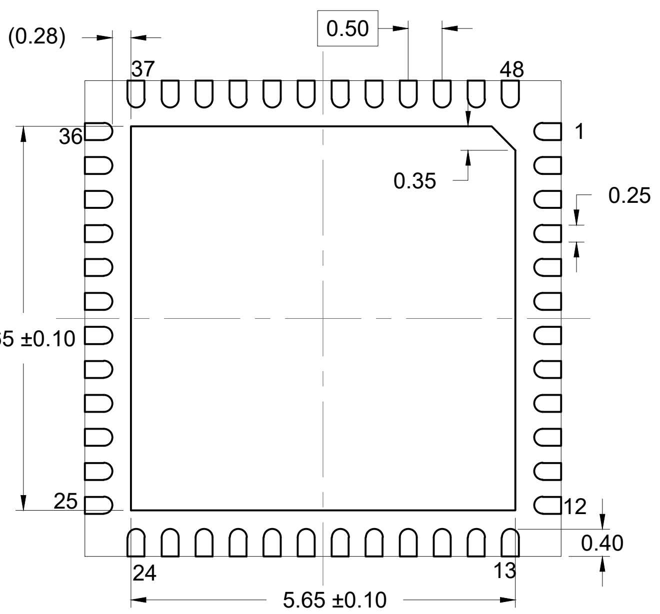
Package Code: NBG48P1

48-VFQFPN 7.0 x 7.0 x 0.75 mm Body, 0.5mm Pitch

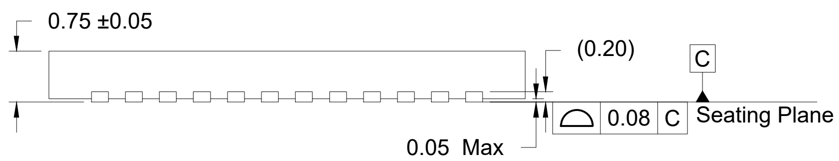
PSC-4228-01, Revision: 03, Date Created: Jun 10, 2024



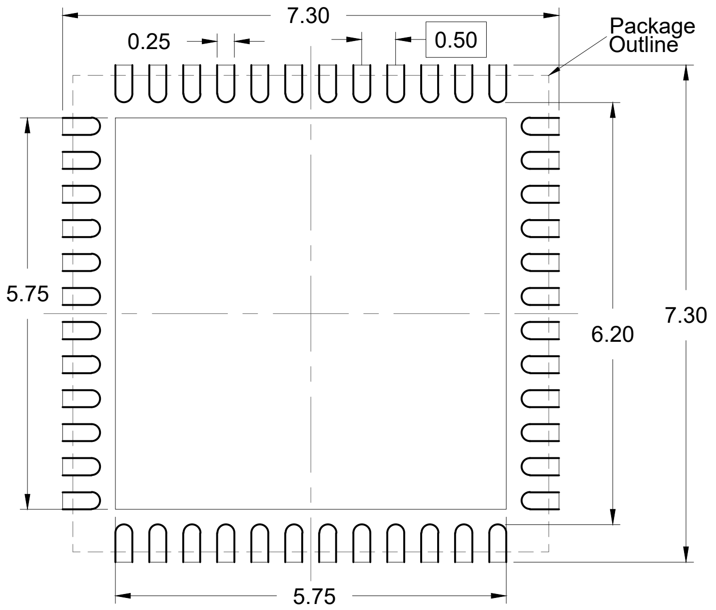
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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