AT25QF641B

64-Mbit SPI Serial Flash Memory with Dual I/O and Quad I/O Support

Features

- Single 2.7 V - 3.6 V Single Supply Voltage
- 64-Mbit (16 x 4 Mbit) Flash Memory
- Serial Peripheral Interface (SPI) Compatible
  - Supports SPI modes 0 and 3 (1,1,1)
  - Supports dual input and dual output operation (1,1,2)
  - Supports quad input and quad output operation (1,1,4)
  - Supports quad XiP (continuous read mode) operation (1,4,4 and 0,4,4)
- 133 MHz Maximum Operating Frequency
- Erase Size and Duration
  - Uniform 4-kbyte Block Erase (65 ms typical)
  - Uniform 32-kbyte Block Erase (150 ms typical)
  - Uniform 64-kbyte Block Erase (240 ms typical)
  - Full Chip Erase (30 seconds typical)
- Default Operating Mode is SPI Quad I/O
- Serial Flash Discoverable Parameters (SFDP, JDES216B) support
- OTP Memory
  - Three Protected Programmable Security Register Pages (Page size: 256 bytes)
  - 64-bit factory programmable UID register
- Hardware Write Protection ($\overline{WP}$ pin)
- Software Write protection (Programmable non-volatile control registers)
- Program and Erase Suspend and Resume
- Byte programming size: up to 256 bytes
- Low Power Dissipation
  - Standby Current (14 µA typical)
  - Deep Power-Down Current (1 µA typical)
- Endurance: 100,000 Program and Erase Cycles
- Data Retention: 20 Years
- Industrial Temperature Range (-40 °C to 85 °C)
- Industry Standard Green (Pb/Halide-free/RoHS Compliant) Package Options
  - 8-lead W-SOIC (208-mil)
  - 8-pad DFN (5 x 6 x 0.6 mm)
  - Die Wafer Form
  - Other Package Options (contact Renesas Electronics)

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1. Product Overview

The AT25QF641B is a serial interface Flash memory device designed for use in a wide variety of high-volume consumer based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the AT25QF641B also is ideal for data storage, eliminating the need for additional data storage devices.

The AT25QF641B erase block sizes are optimized to meet the needs of today's code and data storage applications. This means memory space can be used much more efficiently. Because certain code modules and data storage segments must reside in their own erase regions, the wasted and unused memory space that occurs with large block erase Flash memory devices can be greatly reduced. This increased memory space allows additional code routines and data storage segments to be added, while maintaining the same overall device density. This device also contains three pages of Security Register that can be used for unique device serialization, system-level Electronic Serial Number (ESN) storage, locked key storage, etc. These Security Register pages can be locked individually.

The physical block size of this device is 4 Mbit.

2. Pin Descriptions and Package Pinouts

Table 1. Pin Descriptions

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**CHIP SELECT** Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device is deselected and normally be placed in standby mode. A high-to-low transition on the $\overline{CS}$ pin is required to start an operation; a low-to-high transition is required to end an operation. When ending an internally self-timed operation, such as a program or erase cycle, the device does not enter the standby mode until the operation is complete. To ensure correct power-up sequencing, it is recommended to add a 10k Ohm pull-up resistor from $\overline{CS}$ to V_{CC}. This ensures $\overline{CS}$ ramps together with V_{CC} during power-up.	Low	Input
SCK	**SERIAL CLOCK** This pin provides a clock to the device. Command, address, and input data present on the SI pin is latched in on the rising edge of SCK, while output data on the SO pin is clocked out on the falling edge of SCK.	-	Input
SI (I/O_0)	**SERIAL INPUT** The SI pin is used to shift data into the device. The SI pin is used for all data input, including command and address sequences. Data on the SI pin is always latched in on the rising edge of SCK. With the Dual-Output and Quad-Output Read commands, the SI pin becomes an output pin (I/O_0) in conjunction with other pins to allow two or four bits of data (on I/O_{3-0}) to be clocked in on every falling edge of SCK. Data present on the SI pin is ignored whenever the device is deselected ($\overline{CS}$ is deasserted).	-	Input/Output
SO (I/O_1)	**SERIAL OUTPUT** Data on the SO pin is clocked out on the falling edge of SCK. With the Dual-Output Read commands, the SO pin remains an output pin (I/O_0) in conjunction with other pins to allow two bits of data (on I/O_{1-0}) to be clocked in on every falling edge of SCK. The SO pin is in a high-impedance state whenever the device is deselected ($\overline{CS}$ is deasserted).	-	Input/Output
$\overline{WP}$ (I/O_2)	**WRITE PROTECT** This pin is used either for write-protection, in which case it is referred to as $\overline{WP}$, or as one of the quad-SPI I/O pins, in which case it is referred to as IO_2. When the Quad Enable (QE) bit of Status Register 2 is 0, and the SRP1 and SRP0 bits are 0 and 1, respectively, the pin can be used for write-protection. It then can be asserted (driven low) to protect the Status Registers from modification. When the QE bit of Status Register 2 is 1, quad-SPI communication is enabled, and the pin is used as I/O pin IO_2 in any command that makes use of quad-SPI. In this setting, do not use the pin for write-protection. The $\overline{WP}$ pin is internally pulled high and can be left floating if not used.	-	Input/Output

Table 1. Pin Descriptions*(continued)*

Symbol	Name and Function	Asserted State	Type
$\overline{HOLD}$ (I/O_3)	**HOLD** This pin is used either for pausing communication, in which case it is referred to as $\overline{HOLD}$, or as one of the quad-SPI I/O pins, in which case it is referred to as IO_3. When the Quad Enable (QE) bit of Status Register 2 is 0, this pin is used as a $\overline{HOLD}$ pin. When the QE bit of Status Register 2 is 1, quad-SPI communication is enabled, and the pin is used as I/O pin IO_3 in any command that makes use of quad-SPI. In this setting, do not use the pin for pausing communication. The $\overline{HOLD}$ pin is used to pause a SPI sequence without resetting the clocking sequence. To enable the HOLD mode, $\overline{CS}$ must be low. The HOLD mode effect is on with the falling edge of the $\overline{HOLD}$ signal with SCK being low. The HOLD mode ends on the rising edge of the $\overline{HOLD}$ signal with SCK being low. The $\overline{HOLD}/IO_3$ pin is internally pulled high and can be left floating if not used.	-	Input/Output
V_{CC}	**DEVICE POWER SUPPLY** The V_{CC} pin is used to supply the source voltage to the device.	-	Power
GND	**GROUND** The ground reference for the power supply. Connect GND to the system ground.	-	Power

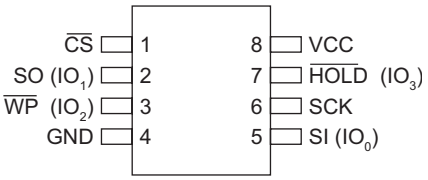


Figure 1. 8-SOIC (208-mil) — Top View

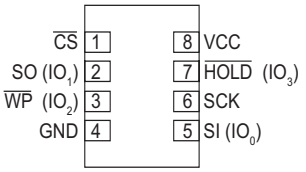
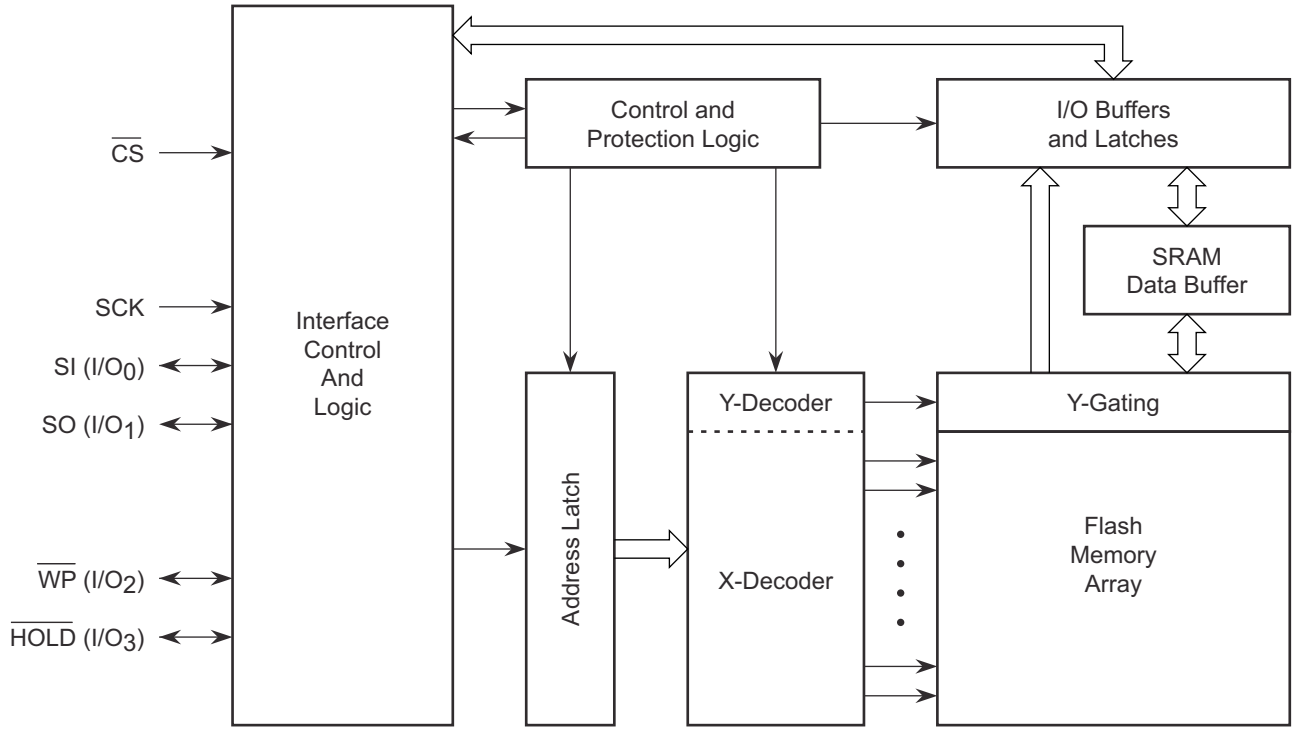


Figure 2. 8-UDFN — Top View

3. Block Diagram



Note: I/O_{3-0} pin naming convention is used for Dual-I/O and Quad-I/O commands.

Figure 3. Block Diagram

4. Memory Array

To provide the greatest flexibility, the memory array of the AT25QF641B can be erased in four levels of granularity, including a full-chip erase. The size of the erase blocks is optimized for both code and data storage applications, allowing both code and data segments to reside in their own erase regions. The Memory Architecture Diagram illustrates each erase level.

Table 2. Memory Architecture Diagram: Block Erase Detail

64 kbyte Block Erase (D8h)	32 kbyte Block Erase (52h)	4 kbyte Block Erase (20h)	Block Address Range
64 kbytes (block 127)	32 kbytes (block 255)	4 kbytes (Block2047)	7FF000h - 7FFFFFh
		4 kbytes (B2046)	7FE000h - 7FEFFFh
		4 kbytes (B2045)	7FD000h - 7FDFFFh
		4 kbytes (B2044)	7FC000h - 7FCFFFh
		4 kbytes (B2043)	7FB000h - 7FBFFFh
		4 kbytes (B2042)	7FA000h - 7FAFFFh
		4 kbytes (B2041)	7F9000h - 7F9FFFh
		4 kbytes (B2040)	7F8000h - 7F8FFFh
	32 kbytes (block 254)	4 kbytes (B2039)	7F7000h - 7F7FFFh
		4 kbytes (B2038)	7F6000h - 7F6FFFh
		4 kbytes (B2037)	7F5000h - 7F5FFFh
		4 kbytes (B2036)	7F4000h - 7F4FFFh
		4 kbytes (B2035)	7F3000h - 7F3FFFh
		4 kbytes (B2034)	7F2000h - 7F2FFFh
		4 kbytes (B2033)	7F1000h - 7F1FFFh
		4 kbytes (B2032)	7F0000h - 7F0FFFh
64 kbytes (block 126) to 64 kbytes (block 1)	32 kbytes (block 253) to 32 kbytes (block 2)	4 kbytes (B2031) to 4 kbytes (B16)	7EF000h - 7EFFFh to 010000h - 010FFFh
64 kbytes (block 0)	32 kbytes (block 1)	4 kbytes (B15)	00F000h - 00FFFFh
		4 kbytes (B14)	00E000h - 00EFFFh
		4 kbytes (B13)	00D000h - 00DFFFh
		4 kbytes (B12)	00C000h - 00CFFFh
		4 kbytes (B11)	00B000h - 00BFFFh
		4 kbytes (B10)	00A000h - 00AFFFh
		4 kbytes (B9)	009000h - 009FFFh
		4 kbytes (B8)	008000h - 008FFFh
	32 kbytes (block 0)	4 kbytes (B7)	007000h - 007FFFh
		4 kbytes (B6)	006000h - 006FFFh
		4 kbytes (B5)	005000h - 005FFFh
		4 kbytes (B4)	004000h - 004FFFh
		4 kbytes (B3)	003000h - 003FFFh
		4 kbytes (B2)	002000h - 002FFFh
		4 kbytes (B1)	001000h - 001FFFh
		4 kbytes (B0)	000000h - 000FFFh

Table 3. AT25QF641B Device Block Memory Map — Page Program

4 kbyte Blocks	256 Byte Page	1 - 256 Byte Page Program
4 kbytes (B2047)	256 Bytes	7FFF00h - 7FFFFFh
4 kbytes (B2046)	256 Bytes	7FFE00h - 7FFEFFh
4 kbytes (B2045)	256 Bytes	7FFD00h - 7FFDFFh
4 kbytes (B2044)	256 Bytes	7FFC00h - 7FFCFFh
4 kbytes (B2043)	256 Bytes	7FFB00h - 7FFBFFh
4 kbytes (B2042)	256 Bytes	7FFA00h - 7FFAFFh
4 kbytes (B2041)	256 Bytes	7FF900h - 7FF9FFh
4 kbytes (B2040)	256 Bytes	7FF800h - 7FF8FFh
4 kbytes (B2039)	256 Bytes	7FF700h - 7FF7FFh
4 kbytes (B2038)	256 Bytes	7FF600h - 7F6FFFh
4 kbytes (B2037)	256 Bytes	7FF500h - 7FF5FFh
4 kbytes (B2036)	256 Bytes	7FF400h - 7FF4FFh
4 kbytes (B2035)	256 Bytes	7FF300h - 7FF3FFh
4 kbytes (B2034)	256 Bytes	7FF200h - 7FF2FFh
4 kbytes (B2033)	256 Bytes	7FF100h - 7FF1FFh
4 kbytes (B2032)	256 Bytes	7FF000h - 7FF0FFh
4 kbytes (B2031) to 4 kbytes (B16)	. . .	. . .
4 kbytes (B15)	256 Bytes	000F00h - 000FFFh
4 kbytes (B14)	256 Bytes	000E00h - 000EFFh
4 kbytes (B13)	256 Bytes	000D00h - 000DFFh
4 kbytes (B12)	256 Bytes	000C00h - 000CFFh
4 kbytes (B11)	256 Bytes	000B00h - 000BFFh
4 kbytes (B10)	256 Bytes	000A00h - 000AFFh
4 kbytes (B9)	256 Bytes	000900h - 0009FFh
4 kbytes (B8)	256 Bytes	000800h - 0008FFh
4 kbytes (B7)	256 Bytes	000700h - 0007FFh
4 kbytes (B6)	256 Bytes	000600h - 0006FFh
4 kbytes (B5)	256 Bytes	000500h - 0005FFh
4 kbytes (B4)	256 Bytes	000400h - 0004FFh
4 kbytes (B3)	256 Bytes	000300h - 0003FFh
4 kbytes (B2)	256 Bytes	000200h - 0002FFh
4 kbytes (B1)	256 Bytes	000100h - 0001FFh
4 kbytes (B0)	256 Bytes	000000h - 0000FFh

5. Device Operation

The AT25QF641B is controlled by a set of commands sent from a host controller, SPI Master. The SPI Master communicates with the AT25QF641B through the SPI bus, which consists of four pins: Chip Select ($\overline{CS}$), Serial Clock (SCK), Serial Input (SI), and Serial Output (SO).

The SPI protocol defines a total of four modes of operation (mode 0, 1, 2, or 3). The AT25QF641B supports the two most common modes, SPI modes 0 and 3. For both SPI modes 0 and 3, data is latched in on the rising edge of SCK and output on the falling edge of SCK.

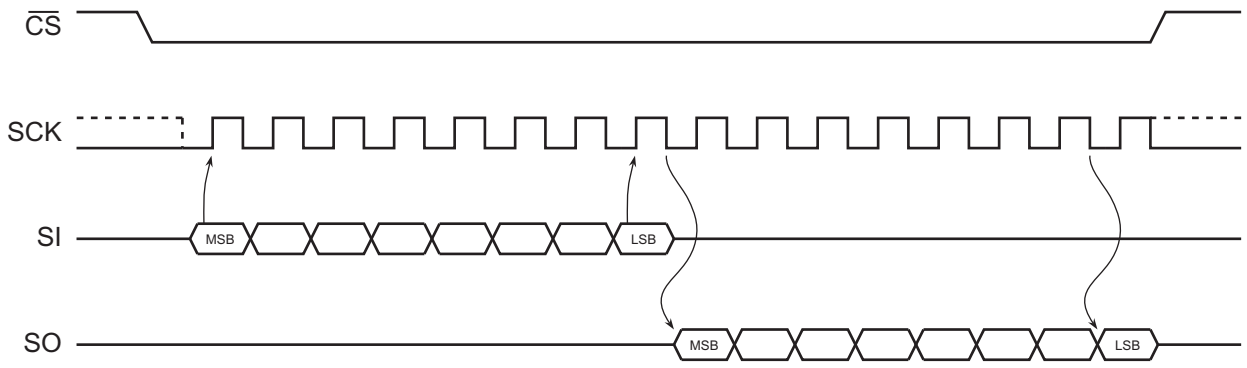


Figure 4. SPI Mode 0 and 3

5.1 Dual Output Read (1-1-2)

The AT25QF641B features a Dual-Output Read mode that allows two bits of data to be clocked out of the device every clock cycle to improve throughput. To do this, both the SI and SO pins are used as outputs for the transfer of data bytes. With the Dual-Output Read Array command, the SI pin becomes an output along with the SO pin.

5.2 Dual I/O Read (1-2-2)

The AT25QF641B supports Dual I/O (1-2-2) transfers, which enhance throughput over the standard SPI mode. This mode transfers the command on the SI pin, but the address and data are transferred on the SI and SO pins. This means that only half the number of clocks are required to transfer the address and data.

5.3 Quad Output Read (1-1-4)

The AT25QF641B features a Quad-Output Read mode that allows four bits of data to be clocked out of the device every clock cycle to improve throughput. To do this, the SI, SO, $\overline{WP}$, and $\overline{HOLD}$ pins are used as outputs for the transfer of data bytes. With the Quad-Output Read Array command, the SI, $\overline{WP}$, and $\overline{HOLD}$ pins become outputs along with the SO pin.

5.4 Quad I/O Read (1-4-4)

The AT25QF641B supports Quad I/O (1-4-4) transfers, which enhance throughput over the standard SPI mode. This mode transfers the command on the SI pin, but the address and data are transferred on the SI, SO, $\overline{WP}$, and $\overline{HOLD}$ pins. This means that only a quarter of the number of clocks are required to transfer the address and data. With the Quad I/O Read Array command, the SI, $\overline{WP}$, and $\overline{HOLD}$ and SO pins become inputs during the address transfer, and switch to outputs during the data transfer.

6. Commands and Addressing

A valid command or operation must be started by first asserting the $\overline{CS}$ pin. After the $\overline{CS}$ pin has been asserted, the host controller must clock out a valid 8-bit opcode on the SPI bus. Following the opcode, command-dependent information, such as address and data bytes, can be clocked out by the host controller. All opcode, address, and data bytes are transferred with the most-significant bit (MSB) first. An operation is ended by deasserting the $\overline{CS}$ pin.

Opcodes not supported by the AT25QF641B are ignored by the device, and no operation is started. The device continues to ignore any data presented on the SI pin until the start of the next operation ($\overline{CS}$ pin being deasserted and then reasserted). Also, if the $\overline{CS}$ pin is deasserted before complete opcode and address information is sent to the device, no operation is performed, and the device simply returns to the idle state and waits for the next operation.

Addressing of the device requires three bytes of information to be sent, representing address bits A23-A0. Since the upper address limit of the AT25QF641B memory array is 7FFFFFh, address bit A23 is always ignored by the device.

Table 4. AT25QF641B Command Table

Command Name	Command Opcode	Bus Transfer Type (OP-AD-DA)[1]	Mode Bit Present	Mode Bit Clocks	Wait Cycle Dummy Clocks	Number of Data Bytes
System Commands						
Enable Reset	66h	1-0-0	N	0	0	0
Reset Device	99h	1-0-0	N	0	0	0
Deep Power-down	B9h	1-0-0	N	0	0	0
Release Power-down	ABh	1-0-0	N	0	0	0
Read Commands						
Normal Read Data	03h	1-1-1	N	0	0	1+
Fast Read	0Bh	1-1-1	N	0	8	1+
Dual Output Fast read	3Bh	1-1-2	N	0	8	1+
Dual-I/O Fast read	BBh	1-2-2	Y	4	0	1+
Dual-I/O Fast read (Continuous Mode)	BBh	0-2-2	Y	4	0	1+
Quad Output Fast read	6Bh	1-1-4	N	0	8	1+
Quad-I/O Fast read	EBh	1-4-4	Y	2	4	1+
Quad-I/O Fast read (Continuous Mode)	EBh	0-4-4	Y	2	4	1+
Word Read Quad-I/O	E7h	1-4-4	Y	2	2	1+
Word Read Quad-I/O (Continuous	E7h	0-4-4	Y	2	2	1+
Set Burst With Wrap	77h	1-0-4	N	0	6	1, D[6:4]
Write Commands						
Write Enable	06h	1-0-0	N	0	0	0
Volatile SR Write Enable	50h	1-0-0	N	0	0	0
Write Disable	04h	1-0-0	N	0	0	0
Program Commands						
Page Program	02h	1-1-1	N	0	0	1+
Quad Page Program	32h	1-1-4	N	0	0	1+

Table 4. AT25QF641B Command Table *(continued)*

Command Name	Command Opcode	Bus Transfer Type (OP-AD-DA)[1]	Mode Bit Present	Mode Bit Clocks	Wait Cycle Dummy Clocks	Number of Data Bytes
Erase Commands						
Block Erase (4 kbytes)	20h	1-1-0	N	0	0	0
Block Erase (32 kbytes)	52h	1-1-0	N	0	0	0
Block Erase (64 kbytes)	D8h	1-1-0	N	0	0	0
Chip Erase	C7h/60h	1-0-0	N	0	0	0
Suspend/Resume Commands						
Program/Erase Suspend	75h	1-0-0	N	0	0	0
Program/Erase Resume	7Ah	1-0-0	N	0	0	0
Status Register Commands						
Read Status Register 1	05h	1-0-1	N	0	0	1
Read Status Register 2	35h	1-0-1	N	0	0	1
Read Status Register 3	15h	1-0-1	N	0	0	1
Write Status Register 1	01h	1-0-1	N	0	0	1
Write Status Register 2	31h	1-0-1	N	0	0	1
Write Status Register 3	11h	1-0-1	N	0	0	1
Device Information Commands						
Manufacturer/Device ID	90h	1-1-1	N	0	0	2
Mfgr./Device ID Dual-I/O	92h	1-2-2	N	0	4	2
Mfgr./Device ID Quad-I/O	94h	1-4-4	N	0	4	2
Read JEDEC ID	9Fh	1-0-1	N	0	0	3
Read Serial Flash Discoverable	5Ah	1-1-1	N	0	8	1+
OTP Commands						
Erase Security Registers	44h	1-1-0	N	0	0	0
Program Security Registers	42h	1-1-1	N	0	0	1+
Read Security Registers	48h	1-1-1	N	0	8	1+
Read Unique ID Number	4Bh	1-0-1	N	0	32	1+

1. OP = Opcode (command number), AD = Address. DA = Data. 0 indicates the corresponding transfer does not occur in that command. 1 indicates the transfer does occur. For example, 1-0-0 indicates a command transfer occurs, but no address or data transfers occur.

   Op: Opcode or Commands (8-bits): 0 => No Opcode [continuous Read], 1 => 8 clocks for Opcode, 2 => 4 clocks for Opcode, 4 => 2 clocks for opcode.

   AD: Address (24-bits) Only: 0 => No address, Opcode only operation, 1 => 24 clocks for Address, 2 => 12 clocks for address, 4 => 6 clocks for address.

   AD: Address (24-bits) + Mode (8-bits): 2 => 12 clocks for address, 4 clocks for mode [BBh only], 4 => 6 clocks for address, 2 clocks for mode [EBh and E7h].

   DA: Data (8-bits): 1 => 8 clocks for Byte, 2 => 4 clocks for Byte, 4 => 2 clocks for Byte

7. Read Commands

7.1 Read Array (0Bh and 03h)

The Read Array command can be used to sequentially read a continuous stream of data from the device by providing the clock pin once the initial starting address is specified. The device incorporates an internal address counter that automatically increments every clock cycle.

To perform the Read Array operation, the $\overline{CS}$ pin first must be asserted, and the appropriate opcode (0Bh or 03h) must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the starting address location of the first byte to read within the memory array. If the 0Bh opcode is used for the Read Array operation, an additional dummy byte must be clocked into the device after the three address bytes.

After the three address bytes (and the dummy byte, if using opcode 0Bh) have been clocked in, additional clock cycles result in data being output on the SO pin. The data is always output with the MSB of a byte first. When the last byte (7FFFFFh) of the memory array has been read, the device continues reading back at the beginning of the array (000000h). No delays are incurred when wrapping around from the end of the array to the beginning of the array.

Deasserting the $\overline{CS}$ pin terminates the read operation and puts the SO pin into high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require a full byte of data be read.

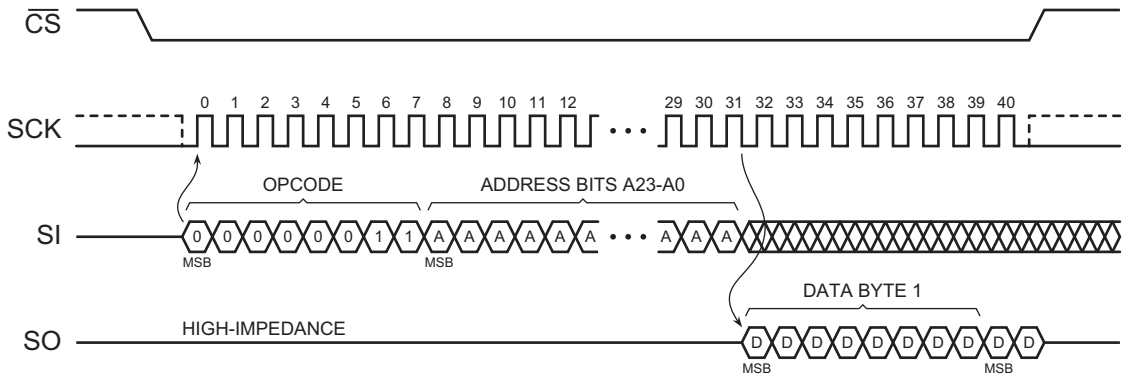


Figure 5. Read Array - 03h Opcode

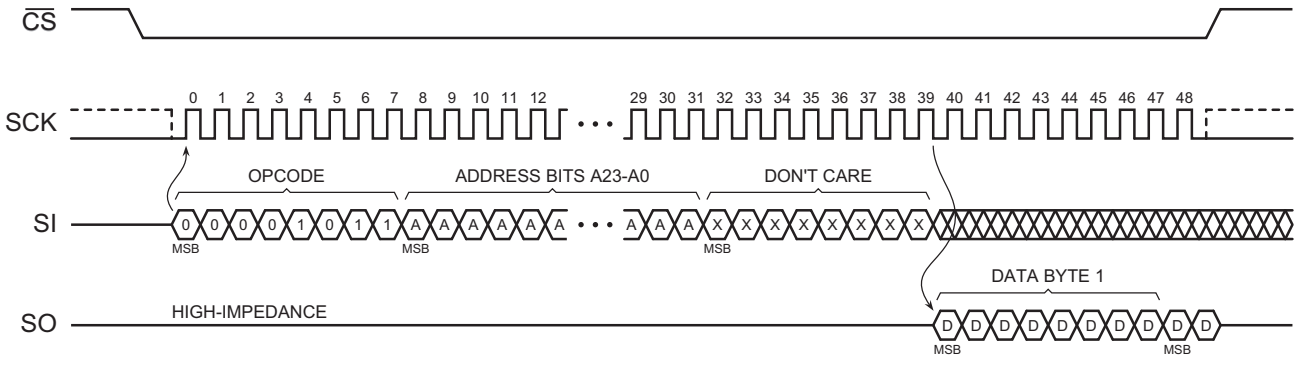


Figure 6. Read Array - 0Bh Opcode

7.2 Dual-Output Fast Read Array (3Bh)

The Dual-Output Read Array command is similar to the standard Read Array command and can be used to sequentially read a continuous stream of data from the device by simply providing the clock pin once the initial starting address has been specified. Unlike the standard Read Array command, the Dual-Output Fast Read Array command allows two bits of data to be clocked out of the device on every clock cycle, rather than just one.

To perform the Dual-Output Fast Read Array operation, the $\overline{CS}$ pin must first be asserted; then, the opcode 3Bh must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the location of the first byte to read within the memory array. Following the three address bytes, a single dummy byte must also be clocked into the device.

After the three address bytes and the dummy byte have been clocked in, additional clock cycles output data on both the SO and SI pins. The data is output with the MSB of a byte first, and the MSB is output on the SO pin. During the first clock cycle, bit seven of the first data byte is output on the SO pin, while bit six of the same data byte is output on the SI pin. During the next clock cycle, bits five and four of the first data byte are output on the SO and SI pins, respectively. The sequence continues with each byte of data being output after every four clock cycles. When the last byte (7FFFFFh) of the memory array has been read, the device continues reading from the beginning of the array (000000h). No delays are incurred when wrapping around from the end of the array to the beginning of the array.Deasserting the $\overline{CS}$ pin terminates the read operation and puts the SO and SI pins into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

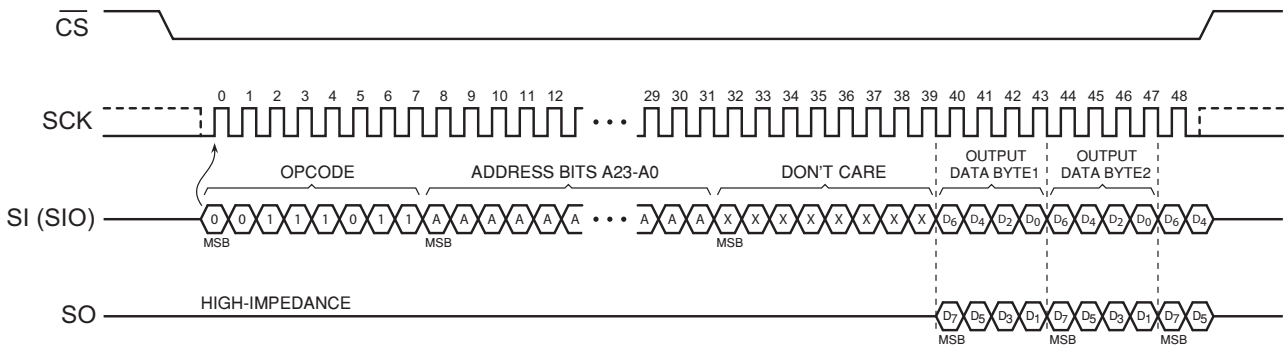


Figure 7. Dual-Output Fast Read Array

7.3 Dual-I/O Read Array (BBh)

The Dual-I/O Read Array command is similar to the Dual-Output Read Array command and can be used to sequentially read a continuous stream of data from the device by providing the clock pin once the initial starting address with two bits of address on each clock and two bits of data on every clock cycle.

To perform the Dual-I/O Read Array operation, the $\overline{CS}$ pin must first be asserted; then, the opcode BBh must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the location of the first byte to read within the memory array. Following the three address bytes, a single mode byte must also be clocked into the device.

After the three address bytes and the mode byte have been clocked in, additional clock cycles output data on both the SO and SI pins. The data is always output with the MSB of a byte first, and the MSB is always output on the SO pin. During the first clock cycle, bit seven of the first data byte is output on the SO pin, while bit six of the same data byte is output on the SI pin. During the next clock cycle, bits five and four of the first data byte are output on the SO and SI pins, respectively. The sequence continues with each byte of data being output after every four clock cycles. When the last byte (7FFFFFh) of the memory array has been read, the device continues reading from the beginning of the array (000000h). No delays are incurred when wrapping around from the end of the array to the beginning of the array. Deasserting the $\overline{CS}$ pin terminates the read operation and puts the SO and SI pins into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

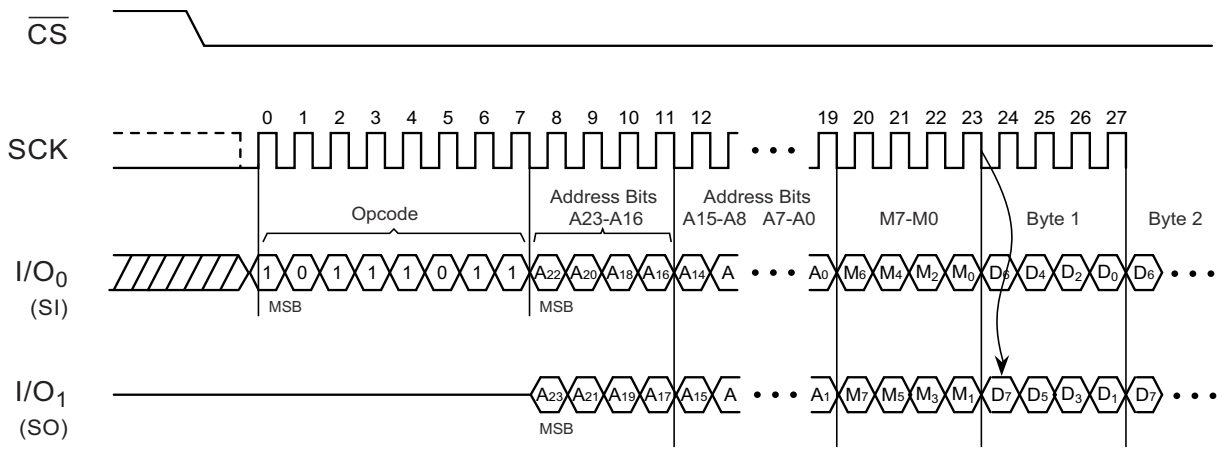


Figure 8. Dual-I/O Read Array (Initial command or previous M5, M4 ≠ 1,0)

7.3.1 Dual-I/O Read Array (BBh) with Continuous Read Mode

The Fast Read Dual-I/O command can further reduce command overhead through setting the Continuous Read Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 9. The upper nibble of M7-4 controls the length of the next Fast Read Dual-I/O command through the inclusion, or exclusion, of the first byte command code. The lower nibble bits of M3-0 are don't care (x). However, the I/O pins must be high-impedance prior to the falling edge of the first data out clock. If the Continuous Read Mode" bits M5-4 = (1,0), the next Fast Read Dual-I/O command (after $\overline{CS}$ is raised and then lowered) does not require the BBh command code. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after $\overline{CS}$ is asserted low. If the Continuous Read Mode bits M5-4 do not equal to (1,0), the next command (after $\overline{CS}$ is raised and then lowered) requires the first byte command code, thus returning to normal operation. A Continuous Read Mode Reset command can also be used to reset M7-0 before issuing normal commands.

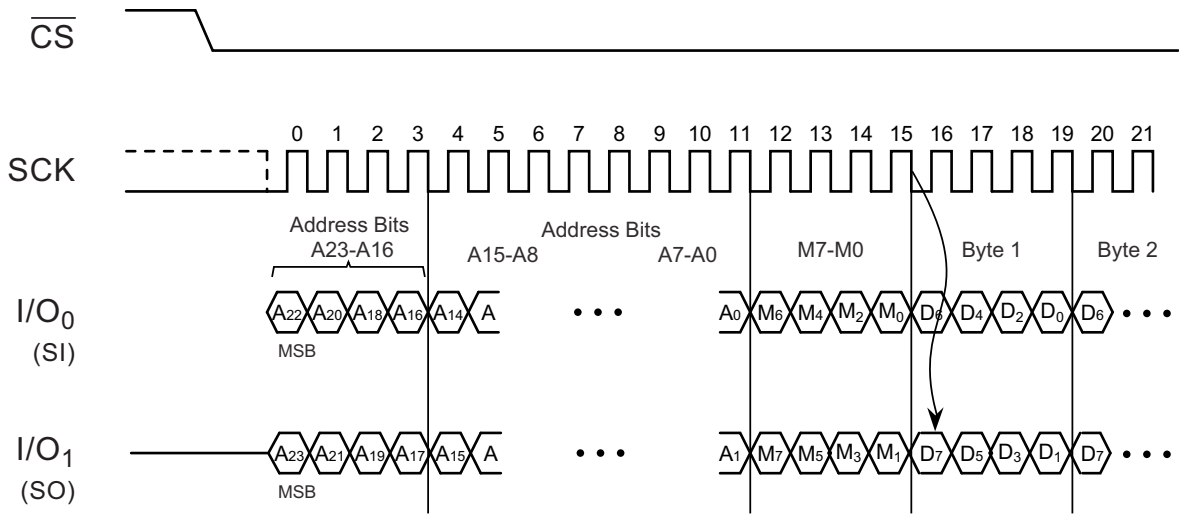


Figure 9. Dual-I/O Read Array (Previous command set M5, M4 = 1,0)

7.4 Quad Output Fast Read Array (6Bh)

The Quad-Output Fast Read Array command is followed by a three-byte address (A23 - A0) and one dummy byte, each bit being latched in during the rising edge of SCK; then, the memory contents are shifted out four bits per clock cycle from I/O_3, I/O_2, I/O_1, and I/O_0. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out.

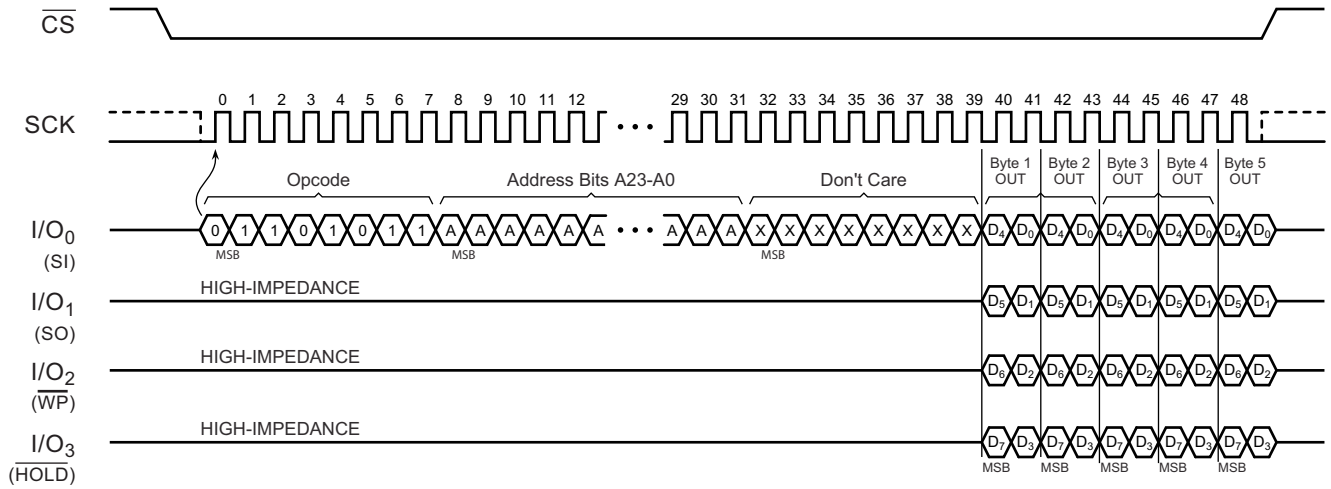


Figure 10. Quad-Output Fast Read Array

7.5 Quad-I/O Read Array (EBh)

The Quad-I/O Read Array command is similar to the Quad-Output Read Array command. It allows four bits of address to be clocked into the device on every clock cycle, rather than just one.

To perform the Quad-I/O Read Array operation, the $\overline{CS}$ pin must first be asserted; then, the opcode EBh must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the location of the first byte to read within the memory array. Following the three address bytes, a single mode byte must also be clocked into the device.

After the three address bytes, the mode byte and two dummy bytes have been clocked in, additional clock cycles output data on the I/O_{3-0} pins. The data is output with the MSB of a byte first, and the MSB is output on the I/O_3 pin. During the first clock cycle, bit 7 of the first data byte is output on the I/O_3 pin while bits 6, 5, and 4 of the same data byte are output on the I/O_2, I/O_1 and I/O_0 pins, respectively. During the next clock cycle, bits 3, 2, 1, and 0 of the first data byte are output on the I/O_3, I/O_2, I/O_1 and I/O_0 pins, respectively. The sequence continues with each byte of data being output after every two clock cycles.

When the last byte (7FFFFFh) of the memory array has been read, the device continues reading from the beginning of the array (000000h). No delays are incurred when wrapping around from the end of the array to the beginning of the array. Deasserting the $\overline{CS}$ pin terminates the read operation and puts the I/O_3, I/O_2, I/O_1 and I/O_0 pins into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.The Quad Enable (QE) bit of the Status Register must be set to enable for the Quad-I/O Read Array command. This is the default setting at power-on.

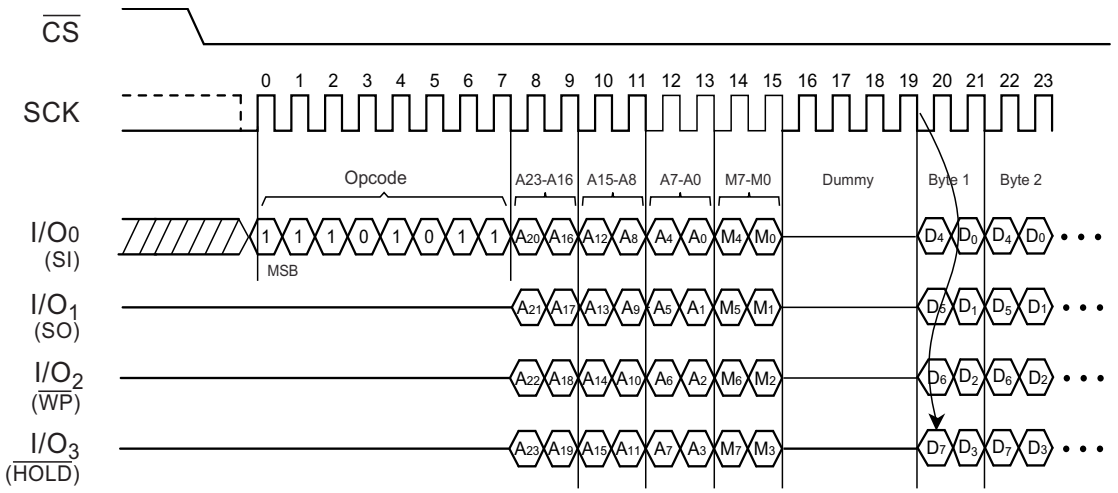


Figure 11. Quad-I/O Read Array (Initial command or previous M5, M4 ≠ 1,0)

7.5.1 Quad-I/O Read Array (EBh) with Continuous Read Mode

The Fast Read Quad-I/O command can further reduce command overhead through setting the Continuous Read Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 11. The upper nibble (M7-4) of the Continuous Read Mode bits controls the length of the next Fast Read Quad-I/O command through the inclusion, or exclusion, of the first byte command code. The lower nibble bits (M3-0) of the Continuous Read Mode bits are don't care. However, the IO pins must be high-impedance prior to the falling edge of the first data out clock. If the Continuous Read Mode bits M5-4 = (1,0), the next Quad-I/O Read Array command (after $\overline{CS}$ is raised and then lowered) does not require the EBh command code, as shown in Figure 12. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after $\overline{CS}$ is asserted low. If the *Continuous Read Mode* bits M5-4 do not equal to (1,0), the next command (after $\overline{CS}$ is raised and then lowered) requires the first byte command code, thus returning to normal operation. A Continuous Read Mode Reset command can also be used to reset M7-0 before issuing normal commands.

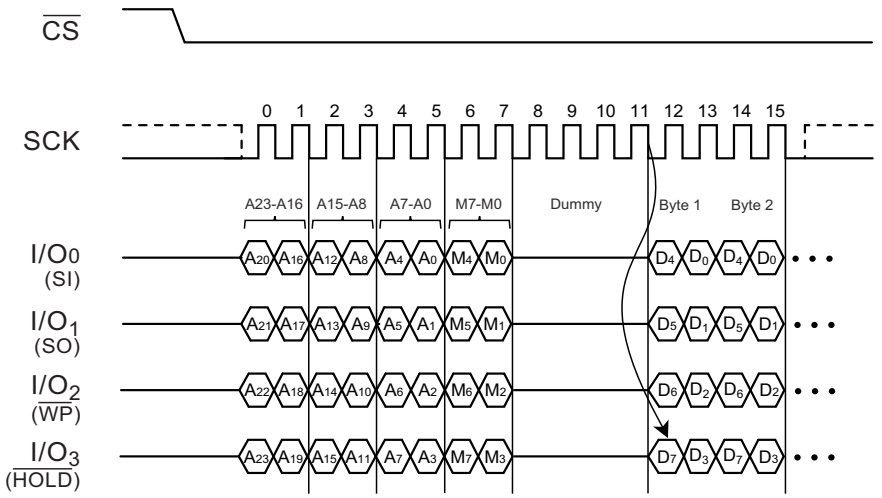


Figure 12. Quad-I/O Read Array with Continuous Read Mode (Previous Command Set M5-4 =1,0)

7.5.2 Set Burst with Wrap (77h)

The Set Burst with Wrap command is used in conjunction with the Quad I/O Fast Read and Quad I/O Word Fast Read command to access a fixed length (8-, 16-, 32-, or 64-byte) section within a 256-byte page in standard SPI mode (see Table 5 and Figure 13).

Table 5. Set Burst with Wrap Command Functions

W6, W5	W4 = 0		W4 = 1 (Default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8 bytes	No	N/A
0 1	Yes	16 bytes	No	N/A
1 0	Yes	32 bytes	No	N/A
1 1	Yes	64 bytes	No	N/A

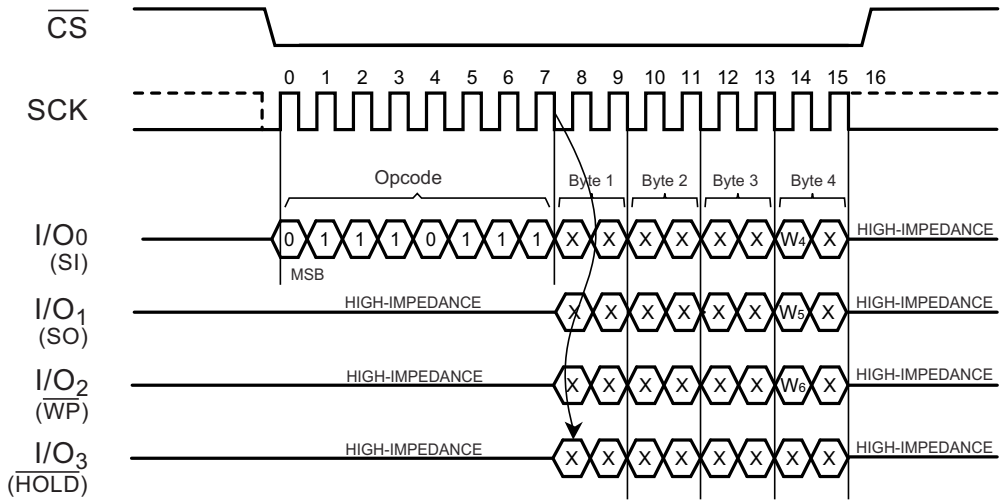


Figure 13. Set Burst with Wrap Timing (SPI Mode)

The Set Burst with Wrap command sequence is: $\overline{CS}$ goes low → Send Set Burst with Wrap command → Send 24 Dummy bits → Send 8 Wrap bits → $\overline{CS}$ goes high.

If W6-4 is set by a Set Burst with Wrap command, all the following Fast Read Quad I/O and Word Read Quad I/O commands use the W6-4 setting to access the 8-, 16-, 32-, or 64-byte section within any page. To exit the Wrap Around function and return to normal read operation, issue another Set Burst with Wrap command to set W4=1. The default value of W4 at power-on is 1.

7.6 Quad-I/O Word Fast Read (E7h)

The Quad-I/O Word Fast Read command is similar to the Quad Fast Read command, except that the lowest address bit (A0) must equal 0 and have two dummy clock cycles. Figure 14 shows the command sequence; the first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of the Status Register (S9) must be set to enable. This is the default setting on power-on.

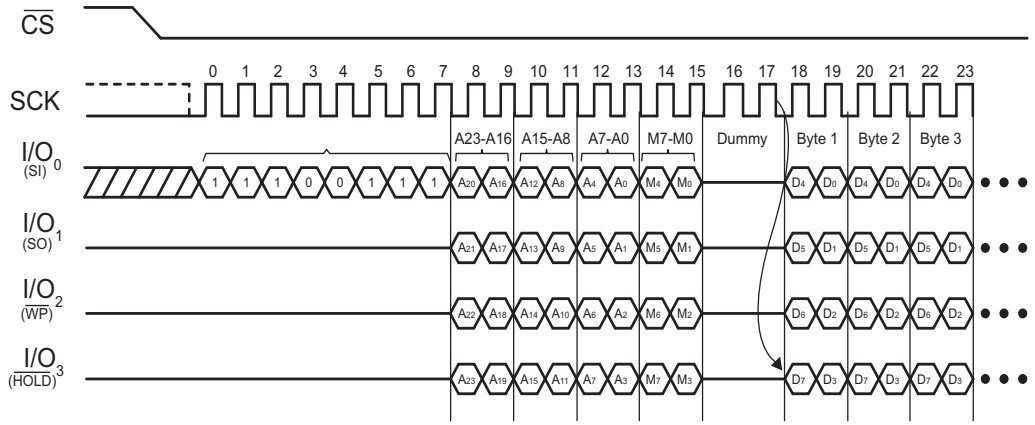


Figure 14. Quad-I/O Word Fast Read Timing (Initial Command Set M5, M4 ≠ 1,0) SPI Mode

7.6.1 Quad-I/O Word Fast Read with Continuous Read Mode

The Quad-I/O Word Fast Read command can further reduce command overhead by setting the Continuous Read Mode bits (M7-0) after input of the Address bits (A23-0). If the Continuous Read Mode bits (M5-4) = (1, 0), the next Quad-I/O Fast Read command (after $\overline{CS}$ is raised and then lowered) does not require the E7h command code. Figure 15 shows the command sequence. If the Continuous Read Mode bits M5-4 do not equal to (1,0), the next command requires the first E7h command code, thus returning to normal operation. A Continuous Read Mode Reset command also can be used to reset (M5-4) before issuing normal command.

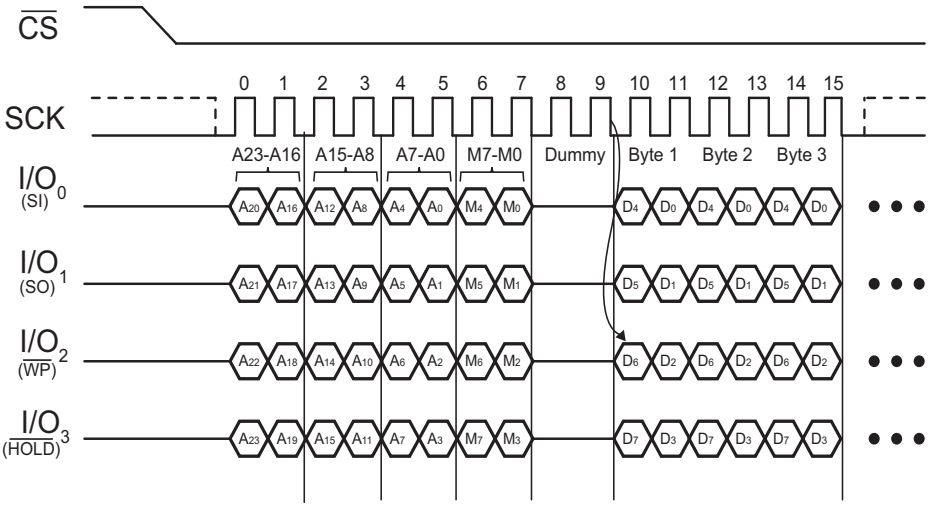


Figure 15. Quad-I/O Word Fast Read Timing (Previous Command Set M5, M4 = 1,0) SPI Mode

7.6.2 Quad-I/O Word Fast Read with 8-, 16-, 32-, 64-Byte Wrap Around in Standard SPI Mode

The Quad-I/O Fast Read command also can be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) command prior to E7h. The Set Burst with Wrap (77h) command can enable or disable the Wrap Around feature for the following E7h commands. When enabled, the data accessed can be limited to an 8-, 16-, 32-, or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the command when it reaches the ending boundary of the 8-, 16-, 32-, or 64-byte section. The output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8-, 16-, 32-, or 64-bytes) of data without issuing multiple read commands.

The Set Burst with Wrap command allows three Wrap Bits (W6-4) to be set. W4 enables or disables the wrap around operation; W5 specifies the length of the wrap around section within a page.

7.7 Read Serial Flash Discoverable Parameter (5Ah)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial Flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. SFDP is a JEDEC Standard, JESD216B. For more detailed SFDP values, contact Renesas Electronics.

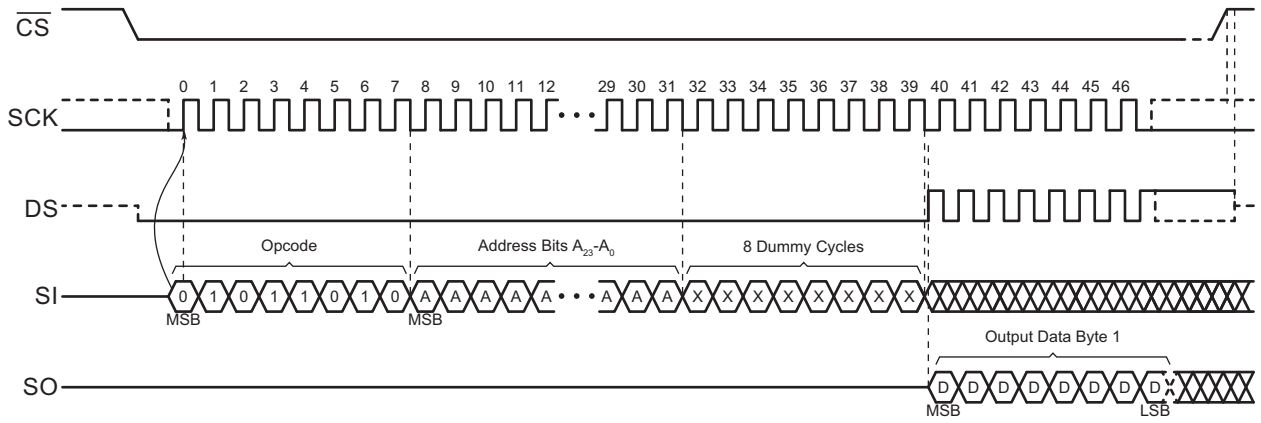


Figure 16. Read Serial Flash Discoverable Parameter Command Sequence Diagram

8. Program and Erase Commands

8.1 Byte/Page Program (02h)

The Byte/Page Program command allows one to 256 bytes of data to be programmed into previously erased memory locations. An erased memory location is one that has all eight bits set to the logical 1 state (a byte value of FFh). Before a Byte/Page Program command can be started, the Write Enable command must have been issued to the device (see Section 9.1) to set the Write Enable Latch (WEL) bit of the Status Register to a logical 1 state.

To perform a Byte/Page Program command, an opcode of 02h must be clocked into the device, followed by the three address bytes denoting the first byte location of the memory array to begin programming at. After the address bytes have been clocked in, data can then be clocked into the device and is stored in an internal buffer.

If the starting memory address denoted by A23-A0 does not fall on an even 256-byte page boundary (A7-A0 are not all 0), special circumstances regarding which memory locations to be programmed apply. In this situation, any data that is sent to the device that goes beyond the end of the page wraps around back to the beginning of the same page. For example, if the starting address denoted by A23-A0 is 0000FEh, and three bytes of data are sent to the device, then the first two bytes of data are programmed at addresses 0000FEh and 0000FFh, and the last byte of data is programmed at address 000000h. The remaining bytes in the page (addresses 000001h through 0000FDh) are not programmed and remain in the erased state (FFh). Furthermore, if more than 256 bytes of data are sent to the device, only the last 256 bytes sent are latched into the internal buffer.

When the $\overline{CS}$ pin is deasserted, the device takes the data stored in the internal buffer and programs it into the appropriate memory array locations based on the starting address specified by A23-A0 and the number of data bytes sent to the device. If fewer than 256 bytes of data were sent to the device, the remaining bytes within the page are not programmed and remain in the erased state (FFh). The programming of the data bytes is internally self-timed and, if only programming a single byte, must take place in a time of t_{PP} or t_{BP}.

The three address bytes and at least one complete data byte must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on even byte boundaries (multiples of eight bits); otherwise, the device aborts the operation and no data is programmed into the memory array. Also, if the memory is in the protected state, the Byte/Page Program command is not executed, and the device returns to the idle state once the $\overline{CS}$ pin has been deasserted. The WEL bit in the Status Register is reset to the logical 0 state if: the program cycle aborts due to an incomplete address being sent, an incomplete byte of data is sent, the $\overline{CS}$ pin is deasserted on uneven byte boundaries, or the memory location to be programmed is protected.

While the device is programming, the Status Register can be read and indicates that the device is busy. For faster throughput, it is recommended that the Status Register be polled, rather than waiting the t_{BP} or t_{PP} time to determine if the data bytes have finished programming. At some point before the program cycle completes, the WEL bit in the Status Register is reset to the logical 0 state.

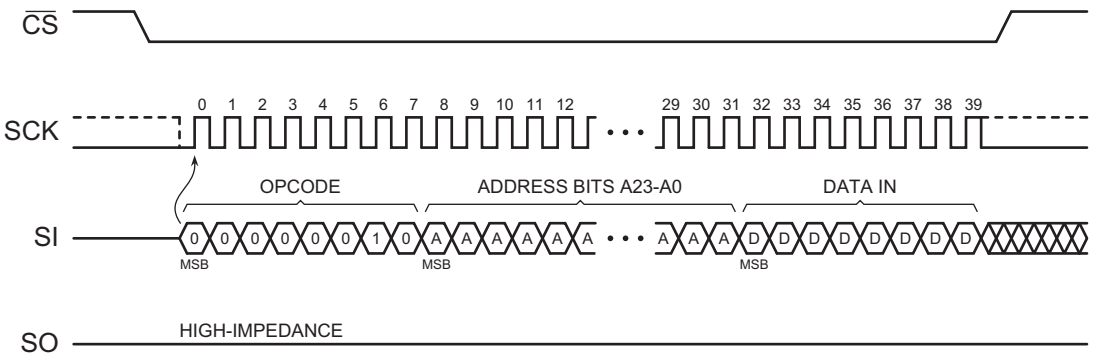


Figure 17. Byte Program

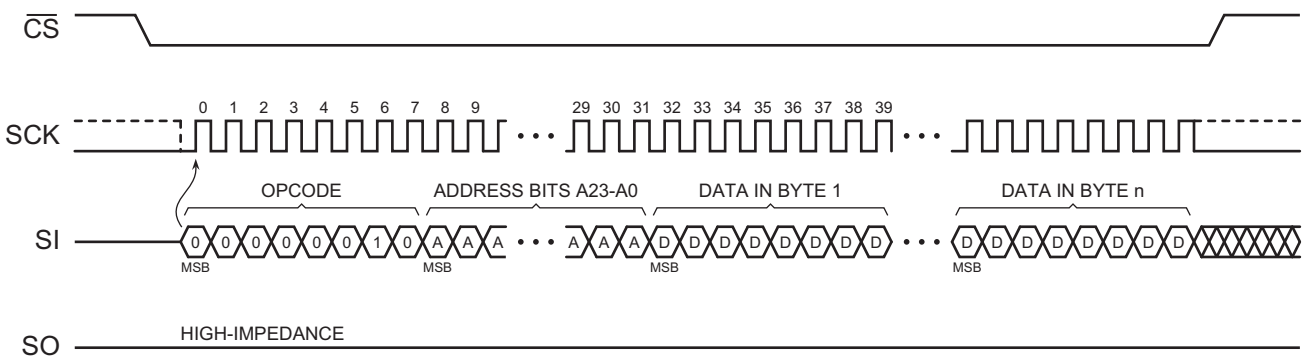


Figure 18. Page Program

8.2 Quad Page Program (32h)

This command is for programming the memory using pins: IO0, IO1, IO2, and IO3. To use this command, the Quad enable (bit 9 in Status Register) must be set (QE=1). Note that this is the default at power-on. A Write Enable command must previously have been executed to set the Write Enable Latch bit before sending the Page Program command. The Quad Page Program command is entered by driving $\overline{CS}$ low, followed by the command code (32H), three address bytes, and at least one data byte on I/O pins.

Figure 19 shows the command sequence. If more than 256 bytes are sent to the device, previously latched data are discarded, and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If fewer than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without affecting other bytes of the same page. $\overline{CS}$ must be driven high after the eighth bit of the last data byte has been latched in; otherwise, the Quad Page Program command is not executed.

As soon as $\overline{CS}$ is driven high, the self-timed Quad Page Program cycle (whose duration is t_{PP}) is initiated. While the Quad Page Program cycle is in progress, the Status Register can be read to check the value of the Write in Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle; it is 0 when done. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table 6 and Table 7) is not executed.

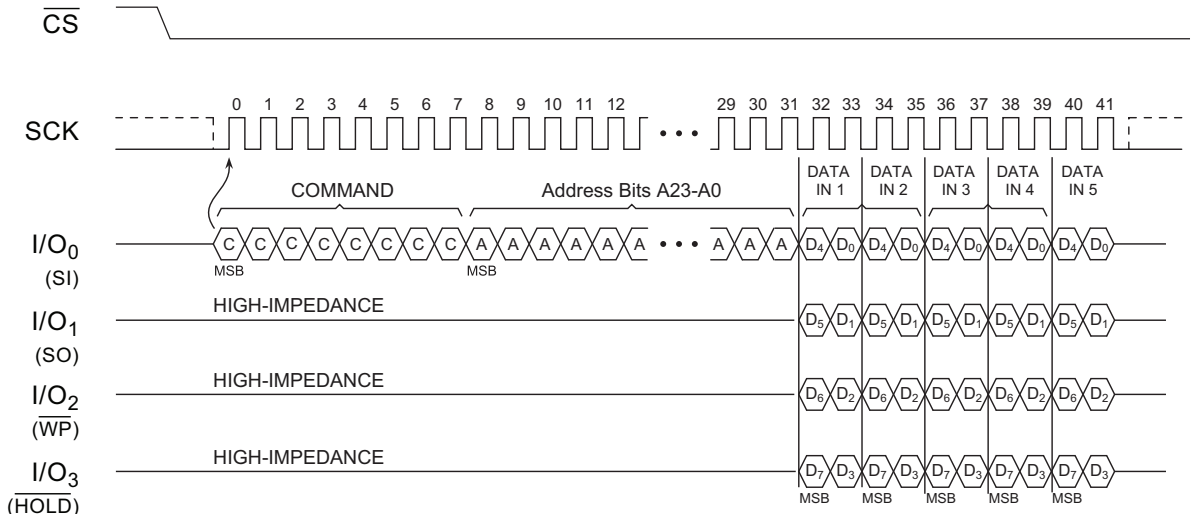


Figure 19. Quad Page Program (32h) Timing

8.3 Block Erase (20h, 52h, or D8h)

A block of 4, 32, or 64 kbytes can be erased (all bits set to the logical 1 state) in a single operation by using one of three different opcodes for the Block Erase command. An opcode of 20h is used for a 4-kbyte erase, an opcode of 52h is used for a 32-kbyte erase, and D8h is used for a 64-kbyte erase. Before a Block Erase command can be started, the Write Enable command must have been previously issued to the device to set the WEL bit of the Status Register to a logical 1 state.

To perform a Block Erase, the $\overline{CS}$ pin must first be asserted and the appropriate opcode (20h, 52h, or D8h) must be clocked into the device. After the opcode has been clocked in, the three address bytes specifying an address within the 4- or 32- or 64-kbyte block to be erased must be clocked in. Any additional data clocked into the device is ignored. When the $\overline{CS}$ pin is deasserted, the device erases the appropriate block. The erasing of the block is internally self-timed and takes place in a time of t_{BLKE}.

Since the Block Erase command erases a region of bytes, the lower order address bits do not need to be decoded by the device. Therefore, for a 4-kbyte erase, address bits A11-A0 are ignored by the device, and their values can be either a logical 1 or 0. For a 32-kbyte erase, address bits A14-A0 are ignored by the device. For a 64-kbyte erase, address bits A15-A0 are ignored by the device. Despite the lower-order address bits not being decoded by the device, the complete three address bytes must still be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, the device aborts the operation, and no erase operation is performed.

If the memory is in the protected state, the Block Erase command is not executed, and the device returns to the idle state once the $\overline{CS}$ pin has been deasserted.

The WEL bit in the Status Register is reset to the logical 0 state if: the erase cycle aborts due to an incomplete address being sent, the $\overline{CS}$ pin is deasserted on uneven byte boundaries, or because a memory location within the region to be erased is protected.

While the device is executing a successful erase cycle, the Status Register can be read and indicates that the device is busy. For faster throughput, it is recommended that the Status Register be polled to determine if the device has finished erasing. At some point before the erase cycle completes, the WEL bit in the Status Register is reset to the logical 0 state.

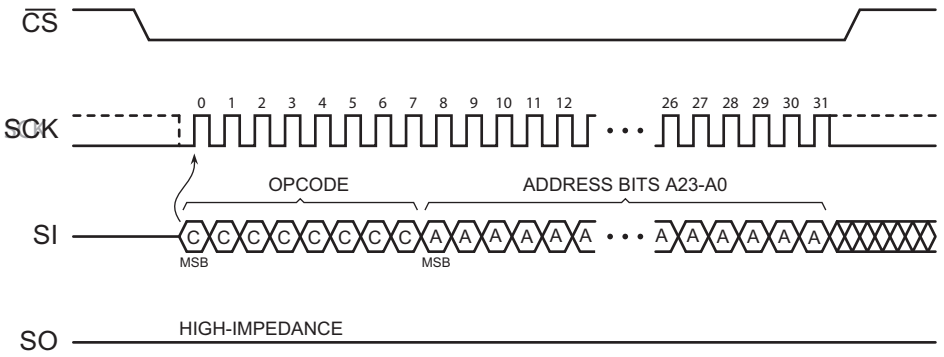


Figure 20. Block Erase

8.4 Chip Erase (60h or C7h)

The entire memory array can be erased in a single operation by using the Chip Erase command. Before a Chip Erase command can be started, the Write Enable command must have been previously issued to the device to set the WEL bit of the Status Register to a logical 1 state.

Two opcodes (60h and C7h) can be used for the Chip Erase command. There is no difference in device functionality when using the two opcodes; thus, they can be used interchangeably. To perform a Chip Erase, one of the two opcodes must be clocked into the device. Since the entire memory array is to be erased, no address bytes need to be clocked into the device, and any data clocked in after the opcode is ignored. When the $\overline{CS}$ pin is deasserted, the device erases the entire memory array. The erasing of the device is internally self-timed and takes place in a time of t_{CHPE}.

The complete opcode must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on an byte boundary (multiples of eight bits); otherwise, no erase is performed. Also, if the memory array is in the protected state, the Chip Erase command is not executed, and the device returns to the idle state once the $\overline{CS}$ pin has been deasserted. The WEL bit in the Status Register is reset to the logical 0 state if the $\overline{CS}$ pin is deasserted on uneven byte boundaries, or if the memory is in the protected state.

While the device is executing a successful erase cycle, the Status Register can be read and indicates that the device is busy. For faster throughput, it is recommended that the Status Register be polled to determine if the device has finished erasing. At some point before the erase cycle completes, the WEL bit in the Status Register is reset to the logical 0 state.

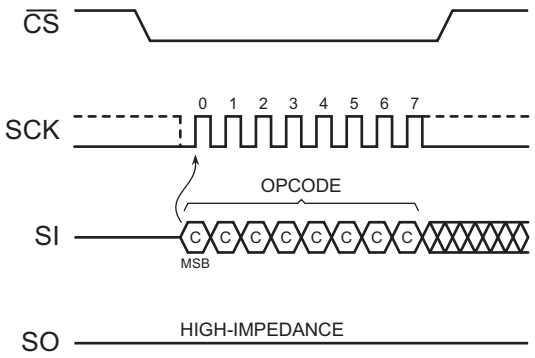


Figure 21. Chip Erase Sequence Diagram

8.5 Program/Erase Suspend (75h)

The Program/Erase Suspend command allows an in-progress program or erase operation to be suspended so that other device operations can be performed. For example, by suspending an erase operation to a particular block, the system can perform functions such as a program or read to a different block.

Chip Erase cannot be suspended. The Program/Erase Suspend command is ignored if it is issued during a Chip Erase.A program operation can be performed while an erase operation is suspended, but the program operation cannot be suspended while an erase operation is currently suspended.

Other device operations, such as a Read Status Register, can also be performed while a program or erase operation is suspended.

Since the need to suspend a program or erase operation is immediate, the Write Enable command does not need to be issued prior to the Program/Erase Suspend command being issued. Thus, the Program/Erase Suspend command operates independently of the state of the WEL bit in the Status Register.

To perform a Program/Erase Suspend, the $\overline{CS}$ pin must first be asserted, and the opcode of 75h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode is ignored. When the $\overline{CS}$ pin is deasserted, the program or erase operation currently in progress is suspended. The Suspend (E_SUS or P_SUS) bits in the Write Status Register then are set to the logical 1 state. In addition, the $\overline{RDY}$/BSY bit in the Status Register indicates that the device is ready for another operation. The complete opcode must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, no suspend operation is performed.

A program operation is not allowed to a block that has been erase suspended. If a program operation is attempted to an erase suspended block, the program operation stops, and the WEL bit in the Status Register is reset to 0. Likewise, an erase operation is not allowed to a block that included the page that has been program suspended. If attempted, the erase operation stops, and the WEL bit in the Status Register is reset to 0.

If an attempt is made to perform an operation that is not allowed during a program or erase suspend, such as a Write Status Register operation, the device ignores the opcode, and no operation is performed. The state of the WEL bit in the Status Register is not affected.

Note: Repeated suspend/resume sequences might significantly impact progress of the erase or program operation. To ensure timely completion of the erase or program operation, limit the number of suspend/resume sequences during the same erase or program operation, or, alternatively, provide sufficient time (up to 3.5 ms for a 4 kB erase; up to 55 ms for a 64 kB erase) after a resume operation to allow the erase or program operation to complete.

Note: A read operation from a physical block that includes a suspended area might provide unreliable data. For the definition of the physical block and for the techniques to ensure high data integrity, see *Application Note AN-500*.

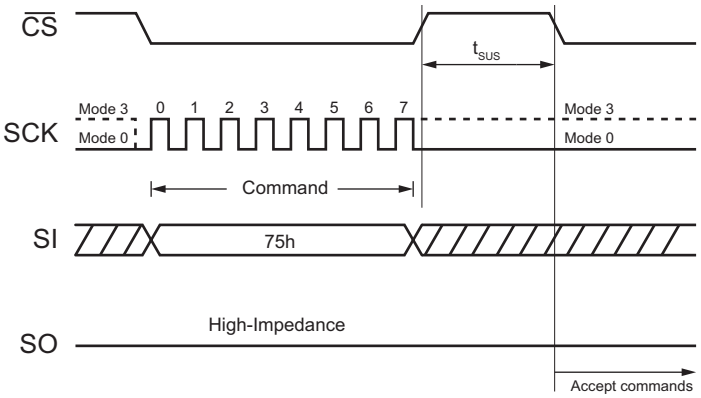


Figure 22. Erase/Program Suspend Command Sequence

8.6 Program/Erase Resume (7Ah)

The Program/Erase Resume command allows a suspended program or erase operation to be resumed and continue programming a Flash page or erasing a Flash memory block where it left off. The Program/Erase Resume command is accepted by the device only if the SUS bit in the Write Status Register equals 1 and the RDY/BSY bit equals 0. If the SUS bit equals 0, or the RDY/BSY bit equals to 1, the Program/Erase Resume command is1 ignored by the device. As with the Program/Erase Suspend command, the Write Enable command does not need to be issued prior to the Program/Erase Resume command being issued. Thus, the Program/Erase Resume command operates independently of the state of the WEL bit in the Status Register.

To perform Program/Erase Resume, the CS pin must first be asserted, and opcode 7Ah must be clocked into the device.

No address bytes need to be clocked into the device, and any data clocked in after the opcode is ignored. When the CS pin is deasserted, the program or erase operation currently suspended resumes. The E_SUS or P_SUS bit in the Status Register is reset back to the logical 0 state to indicate the program or erase operation is no longer suspended. Also, the RDY/BSY bit in the Status Register indicates that the device is busy performing a program or erase operation. The complete opcode must be clocked into the device before the CS pin is deasserted, and the CS pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, no resume operation is performed.

During a simultaneous Erase Suspend/Program Suspend condition, issuing the Program/Erase Resume command results in the program operation resuming first. After the program operation has been completed, the Program/Erase Resume command must be issued again for the erase operation to be resumed.

While the device is busy resuming a program or erase operation, any attempts at issuing the Program/Erase Suspend command are ignored. Thus, if a resumed program or erase operation needs to be subsequently suspended again, the system must either wait before issuing the Program/Erase Suspend command, or it must check the status of the RDY/BSY bit or the E_SUS or P_SUS bit in the Status Register to determine if the previously suspended program or erase operation has resumed.

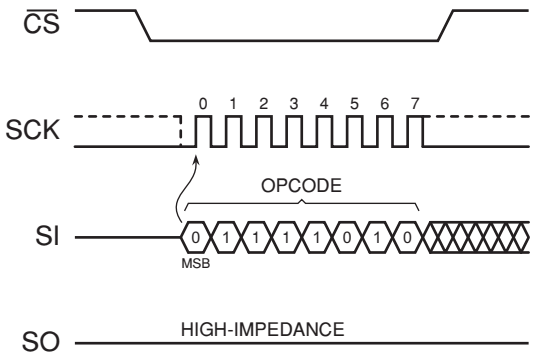


Figure 23. Erase/Program Resume Command Sequence

9. Protection Commands and Features

9.1 Write Enable (06h)

The Write Enable command is used to set the Write Enable Latch (WEL) bit in the Status Register to a logical 1 state. The WEL bit must be set before a Byte/Page Program, Erase, Program Security Register Pages, Erase Security Register Pages or Write Status Register command can be executed. This makes the issuance of these commands a two step process, thus reducing the chances of a command being accidentally or erroneously executed. If the WEL bit in the Status Register is not set prior to the issuance of one of these commands, the command is not executed.

To issue the Write Enable command, the $\overline{CS}$ pin must first be asserted, and the opcode of 06h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode is ignored. When the $\overline{CS}$ pin is deasserted, the WEL bit in the Status Register is set to a logical 1. The complete opcode must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on an byte boundary (multiples of eight bits); otherwise, the device aborts the operation, and the WEL bit state does not change.

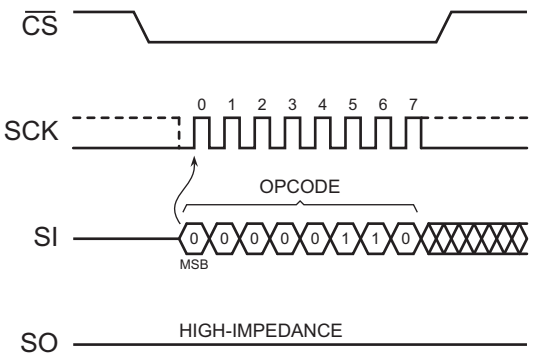


Figure 24. Write Enable Sequence Diagram

9.2 Write Disable (04h)

The Write Disable command is used to reset the Write Enable Latch (WEL) bit in the Status Register to the logical 0 state. With the WEL bit reset, all Byte/Page Program, Erase, Program Security Register Page, and Write Status Register commands are not executed. Other conditions can also cause the WEL bit to be reset; for more details, see the WEL bit section of the Status Register description (Section 9.1).

To issue the Write Disable command, the $\overline{CS}$ pin must be asserted first, and the opcode of 04h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode is ignored. When the $\overline{CS}$ pin is deasserted, the WEL bit in the Status Register is reset to a logical 0. The complete opcode must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on an byte boundary (multiples of eight bits); otherwise, the device aborts the operation, and the WEL bit state does not change.

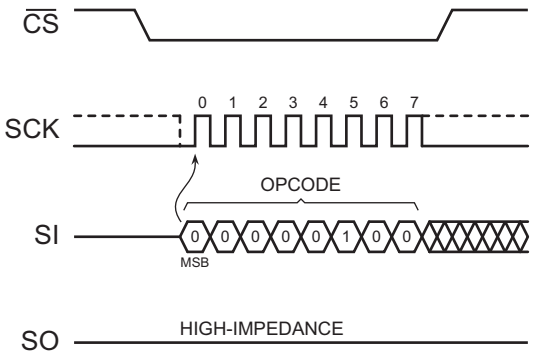


Figure 25. Write Disable Sequence Diagram

9.3 Non-Volatile Protection

The device can be software-protected against erroneous or malicious program or erase operations by using the Non-Volatile Protection feature. Non-Volatile Protection can be enabled or disabled by using the Write Status Register command to change the value of the Protection (CMP, SEC, TB, BP2, BP1, BP0) bits in the Status Register. Table 6 outlines the states of the Protection bits and the associated protection area.

Table 6. Memory Array with CMP = 0

Protection Bits					Memory Content	
SEC	TB	BP2	BP1	BP0	Address Range	Portion
X	X	0	0	0	None	None
0	0	0	0	1	7E0000h - 7FFFFFh	Upper 1/64
0	0	0	1	0	7C0000h - 7FFFFFh	Upper 1/32
0	0	0	1	1	780000h - 7FFFFFh	Upper 1/16
0	0	1	0	0	700000h - 7FFFFFh	Upper 1/8
0	0	1	0	1	600000h - 7FFFFFh	Upper 1/4
0	0	1	1	0	400000h - 7FFFFFh	Upper 1/2
0	1	0	0	1	000000h - 1FFFFFh	Lower 1/64
0	1	0	1	0	000000h - 03FFFFh	Lower 1/32
0	1	0	1	1	000000h - 07FFFFh	Lower 1/16
0	1	1	0	0	000000h - 0FFFFFh	Lower 1/8
0	1	1	0	1	000000h - 1FFFFFh	Lower 1/4
0	1	1	1	0	000000h - 3FFFFFh	Lower 1/2
X	X	1	1	1	000000h - 7FFFFFh	ALL
1	0	0	0	1	7FF000h - 7FFFFFh	Upper 1/2048
1	0	0	1	0	7FE000h - 7FFFFFh	Upper 1/1024
1	0	0	1	1	7FC000h - 7FFFFFh	Upper 1/512
1	0	1	0	X	7F8000h - 7FFFFFh	Upper 1/256
1	1	0	0	1	000000h - 000FFFh	Lower 1/2048
1	1	0	1	0	000000h - 001FFFh	Lower 1/1024
1	1	0	1	1	000000h - 003FFFh	Lower 1/512
1	1	1	0	X	000000h - 007FFFh	Lower 1/256

Table 7. Memory Array Protection with CMP = 1

Protection Bits					Memory Content	
SEC	TB	BP2	BP1	BP0	Address Range	Portion
X	X	0	0	0	000000h - 7FFFFFh	All
0	0	0	0	1	000000h - 7DFFFFh	Lower 63/64
0	0	0	1	0	000000h - 7BFFFFh	Lower 31/32
0	0	0	1	1	000000h - 77FFFFh	Lower 15/16
0	0	1	0	0	000000h - 6FFFFFh	Lower 7/8
0	0	1	0	1	000000h - 5FFFFFh	Lower 3/4
0	0	1	1	0	000000h - 3FFFFFh	Lower 1/2
0	1	0	0	1	020000h - 7FFFFFh	Upper 63/64
0	1	0	1	0	040000h - 7FFFFFh	Upper 31/32
0	1	0	1	1	080000h - 7FFFFFh	Upper 15/16
0	1	1	0	0	100000h - 7FFFFFh	Upper 7/8
0	1	1	0	1	200000h - 7FFFFFh	Upper 3/4
0	1	1	1	0	400000h - 7FFFFFh	Upper 1/2
X	X	1	1	1	NONE	NONE
1	0	0	0	1	000000h - 7FEFFFh	Lower 2047/2048
1	0	0	1	0	000000h - 7FDFFFh	Lower 1023/1024
1	0	0	1	1	000000h - 7FBFFFh	Lower 511/512
1	0	1	0	X	000000h - 7F7FFFh	Lower 255/256
1	1	0	0	1	001000h - 7FFFFFh	Upper 2047/2048
1	1	0	1	0	002000h - 7FFFFFh	Upper 1023/1024
1	1	0	1	1	004000h - 7FFFFFh	Upper 511/512
1	1	1	0	X	008000h - 7FFFFFh	Upper 255/256

As a safeguard against accidental or erroneous protecting or unprotecting of the memory array, the Protection can be locked from updates by using the $\overline{WP}$ pin (see Section 9.4, for more details).

9.4 Protected States and the Write Protect Pin

The $\overline{WP}$ pin is not linked to the memory array itself and has no direct effect on the protection status of the memory array. Instead, the $\overline{WP}$ pin, is used to control the hardware locking mechanism of the device.

If the $\overline{WP}$ pin is permanently connected to GND, then the protection bits cannot be changed.

9.5 Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the AT25QF641B provides a software Reset command instead of a dedicated RESET pin. Once the software Reset command is accepted, any on-going internal operations are terminated, and the device returns to its default power-on state and loses all the current volatile settings, including the Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting (M7-M0), and Wrap Bit setting (W6-W4).

To avoid accidental reset, the Enable Reset and Reset Device commands must be issued in sequence. Any other commands other than Reset (99h) after the Enable Reset (66h) command disables the Reset Enable state. A new sequence of Enable Reset and Reset Device is needed to reset the device. Once the Reset command is accepted by the device, the device takes approximately 30 µs to reset. During this period, no command is accepted.

The Enable Reset and Reset Device command sequence are shown in Figure 26.

Data corruption can happen if there is an on-going or suspended internal Erase or Program operation when the Reset command sequence is accepted by the device. Check the BUSY bit and the SUS bit in the Status Register before issuing the Reset command sequence.

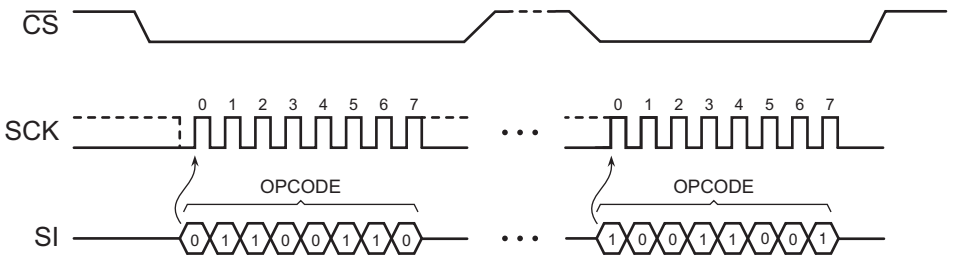


Figure 26. Enable Reset (66h) and Reset Device (99h) Command Timing (SPI Mode)

10. Security Register Commands

The device contains three extra pages, called Security Registers, that can be used for unique device serialization, system-level Electronic Serial Number (ESN) storage, locked key storage, etc. The Security Registers are independent of the main Flash memory.

Each page of the Security Register can be erased and programmed independently. Each page can also be independently locked to prevent further changes.

10.1 Read Unique ID Number (4Bh)

The Read Unique ID Number command accesses a factory-set, read-only 64-bit number that is unique to each AT25QF641B device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 4Bh, followed by four dummy byte clock cycles. After this, the 64-bit ID is shifted out on the falling edge of SCK, as shown in Figure 27.

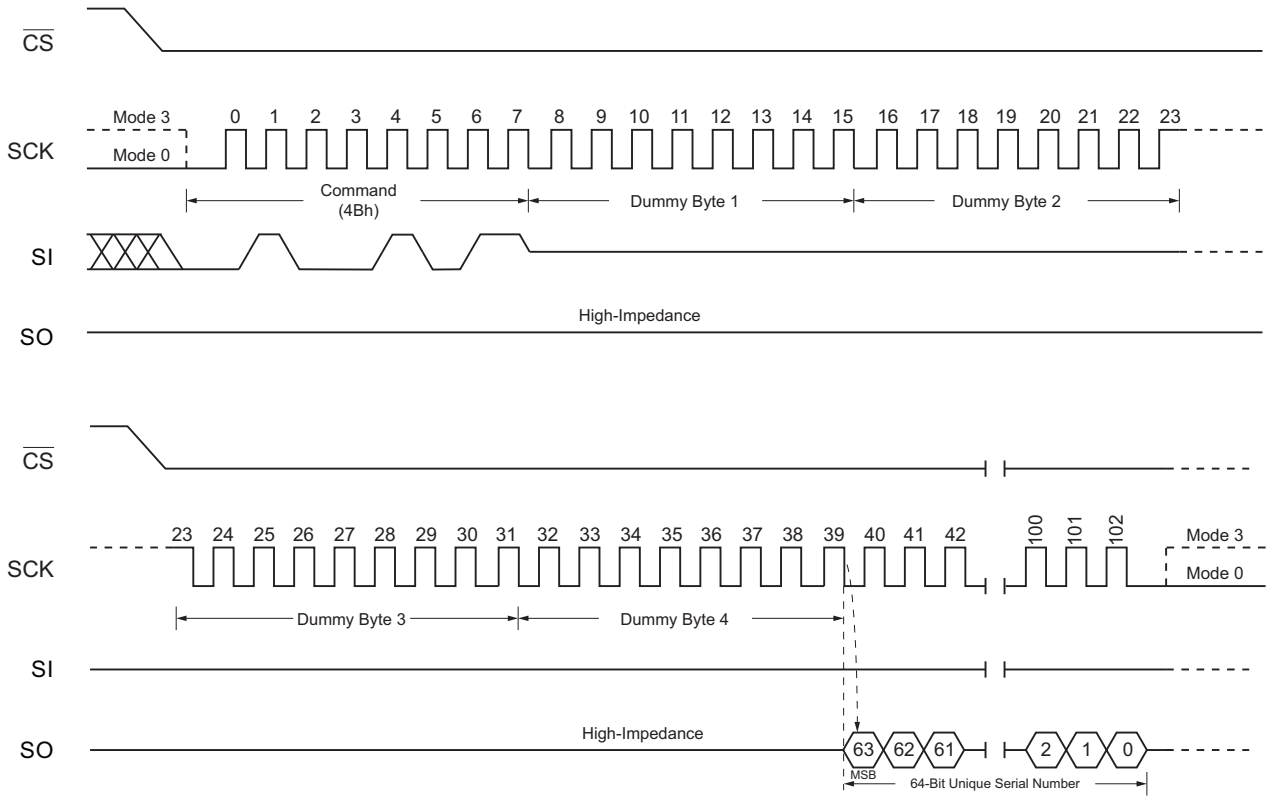


Figure 27. Read Unique ID Timing (SPI Mode)

10.2 Erase Security Registers (44h)

Before an erase Security Register Page command can be started, the Write Enable command must have been previously issued to the device to set the WEL bit of the Status Register to a logical 1 state.

To perform an Erase Security Register Page command, the $\overline{CS}$ pin must first be asserted and the opcode 44h must be clocked into the device. After the opcode has been clocked in, the three address bytes specifying the Security Register Page to be erased must be clocked in. When the $\overline{CS}$ pin is deasserted, the device erases the appropriate page. The erasing of the page is internally self-timed and takes place in a time of t_{PP}.

Since the Erase Security Register Page command erases a region of bytes, the lower-order address bits do not need to be decoded by the device. Thus, address bits A7-A0 are ignored by the device. Despite the lower-order address bits not being decoded by the device, the complete three address bytes must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted right after the last address bit (A0); otherwise, the device aborts the operation, and no erase operation is performed.

While the device is executing a successful erase cycle, the Status Register can be read and indicates that the device is busy. For faster throughput, it is recommended that the Status Register be polled (rather than waiting the t_{PP} time to determine if the device has finished erasing). At some point before the erase cycle completes, the $\overline{RDY}$/BSY bit in the Status Register is reset to the logical 0 state.

The WEL bit in the Status Register is reset to the logical 0 state if: the erase cycle aborts due to an incomplete address being sent, the $\overline{CS}$ pin being deasserted on uneven byte boundaries, or because a memory location within the region to be erased is protected.

The Security Registers Lock Bits (LB3 - LB1) in the Status Register can be used to OTP protect the security registers. Once a Lock Bit is set to 1, the corresponding Security Register is permanently locked. The Erase Security Register Page command is ignored for Security Registers with their Lock Bit set.

Table 8. Security Register Addresses for Erase Security Register Page Command

Address	A23-A16	A15-A12	A11-A8	A7-A0
Security Register 1	00h	1h	0h	Don’t Care
Security Register 2	00h	2h	0h	Don’t Care
Security Register 3	00h	3h	0h	Don’t Care

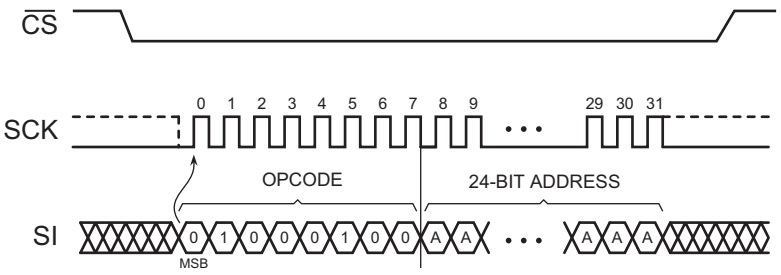


Figure 28. Erase Security Register Page

10.3 Program Security Registers (42h)

The Program Security Registers command uses the internal 256-byte buffer for processing. Thus, the contents of the buffer are altered from their previous state when this command is issued.

The Security Registers can be programmed in a similar fashion to the Program Array operation up to the maximum clock frequency specified by f_{CLK}. Before a Program Security Registers command can be started, the Write Enable command must have been previously issued to the device (see Section 9.1) to set the Write Enable Latch (WEL) bit of the Status Register to a logical 1 state. To program the Security Registers, the $\overline{CS}$ pin must first be asserted, and the opcode of 42h must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the starting address location of the first byte to program within the Security Register.

Table 9. Security Register Addresses for Program Security Registers Command

Address	A23-A16	A15-A12	A11-A8	A7-A0
Security Register 1	00h	1h	0h	Byte Address
Security Register 2	00h	2h	0h	Byte Address
Security Register 3	00h	3h	0h	Byte Address

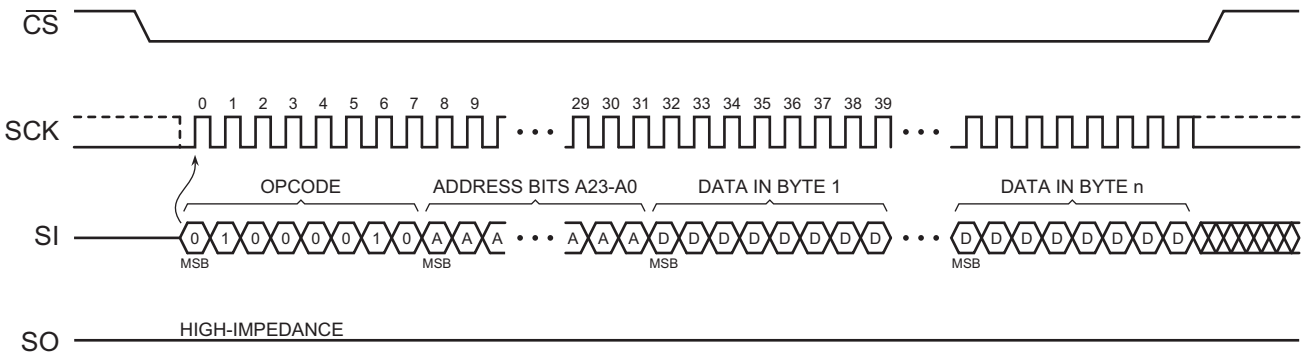


Figure 29. Program Security Registers

10.4 Read Security Registers (48h)

The Security Register can be sequentially read in a similar fashion to the Read Array operation up to the maximum clock frequency specified by f_{CLK}. To read the Security Register, the $\overline{CS}$ pin must first be asserted and the opcode of 48h must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the starting address location of the first byte to read within the Security Register. Following the three address bytes, one dummy byte must be clocked into the device before data can be output.

After the three address bytes and the dummy byte have been clocked in, additional clock cycles result in the Security Register data being output on the SO pin. When the last byte (0003FFh) of the Security Register has been read, the device continues reading back at the beginning of the register (000000h). No delays are incurred when wrapping around from the end of the register to the beginning of the register.

Deasserting the $\overline{CS}$ pin terminates the read operation and puts the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

Table 10. Security Register Addresses for Read Security Registers Command

Address	A23-A16	A15-A12	A11-A8	A7-A0
Security Register 1	00h	1h	0h	Byte Address
Security Register 2	00h	2h	0h	Byte Address
Security Register 3	00h	3h	0h	Byte Address

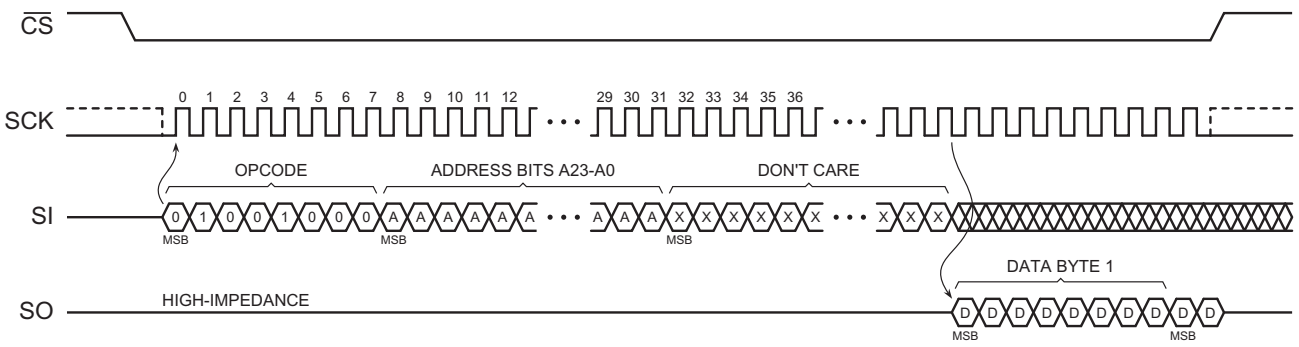


Figure 30. Read Security Registers

11. Status Register Commands

11.1 Read Status Register (05h, 35h, and 15h)

The Status Register can be read to determine the device's ready/busy status, as well as the status of many other functions, such as Block Protection. The Status Register can be read at any time, including during an internally self-timed program or erase operation.

To read Status Register 1, the $\overline{CS}$ pin must first be asserted and the opcode of 05h must be clocked into the device. After the opcode has been clocked in, the device begins outputting Status Register 1 data on the SO pin during every subsequent clock cycle. After the last bit (0) of Status Register 1 has been clocked out, the sequence repeats itself, starting again with bit 7, as long as the $\overline{CS}$ pin remains asserted and the clock pin is being pulsed. The data in the Status Register is constantly being updated, so each repeating sequence outputs new data. Deasserting the $\overline{CS}$ pin terminates the Read Status Register operation and puts the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

To read Status Register 2, the $\overline{CS}$ pin must first be asserted, and the opcode of 35h must be clocked into the device. After the opcode has been clocked in, the device begins outputting Status Register 2 data on the SO pin during every subsequent clock cycle. After the last bit (0) of Status Register 2 has been clocked out, the sequence repeats itself starting again with bit 7 as long as the $\overline{CS}$ pin remains asserted and the clock pin is being pulsed. The data in the Status Register is constantly being updated, so each repeating sequence outputs new data. Deasserting the $\overline{CS}$ pin terminates the Read Status Register operation and puts the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

Table 11. Status Register 1 Bit Assignments

Bit(1)	Mnemonic	Name	Type	Description	
7	SRP0	Status Register Protection bit 0	R/W		See Table 14 on Status Register Protection.
6	SEC	Block Protection	R/W		See Table 6 and Table 7 on Non-Volatile Protection.
5	TB	Top or Bottom Protection	R/W		
4	BP2	Block Protection bit 2	R/W		
3	BP1	Block Protection bit 1	R/W		
2	BP0	Block Protection bit 0	R/W		
1	WEL	Write Enable Latch Status	R	0	Device is not Write Enabled (default).
				1	Device is Write Enabled.
0	$\overline{RDY}$/BSY	Ready/Busy Status	R	0	Device is ready.
				1	Device is busy with an internal operation.

1. Only R/W bits can be modified when using the Write Status Register command.
2. R/W = Readable and writable; R = Readable only.

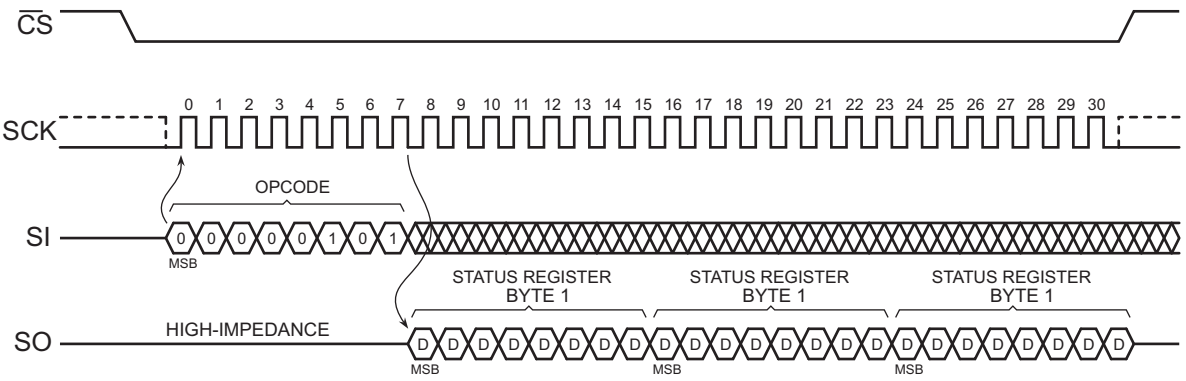


Figure 31. Read Status Register 1

Table 12. Status Register 2 Bit Assignments

Bit[1]	Name		Type	Description	
7	E_SUS	Erase Suspend Status	R	0	Erase operation is not suspended (default).
				1	Erase operation is suspended.
6	CMP	Complement Block Protection	R/W	0	See Table 6 and Table 7 on Block Protection.
5	LB3	Lock Security Register 3	R/W	0	Security Register page-3 is not locked (default).
				1	Security Register page-3 cannot be erased/programmed.
4	LB2	Lock Security Register 2	R/W	0	Security Register page-2 is not locked (default).
				1	Security Register page-2 cannot be erased/programmed.
3	LB1	Lock Security Register 1	R/W	0	Security Register page-1 is not locked (default).
				1	Security Register page-1 cannot be erased/programmed.
2	P_SUS	Program Suspend Status	R	0	Program operation is not suspended (default).
				1	Program operation is suspended.
1	QE	Quad Enable	R/W	0	$\overline{HOLD}$ and $\overline{WP}$ function normally.
				1	$\overline{HOLD}$ and $\overline{WP}$ are I/O pins (default).
0	SRP1	Status Register Protect bit 1	R/W		See Table 14 on Status Register Protection.

1. Only R/W bits can be modified when using the Write Status Register command.
2. R/W = Readable and writable; R = Readable only.

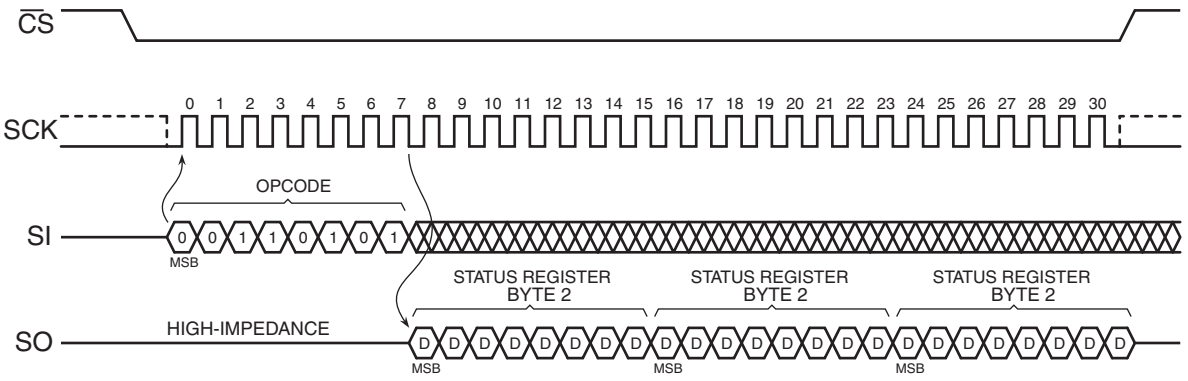


Figure 32. Read Status Register 2

Table 13 shows the bit assignments for Status Register 3. This register can be read using the Status Register 3 Read command (15h), and written using the Status Register 3 Write command (11h).

Table 13. Status Register 3 Bit Assignments

Bit[1]	Mnemonic	Name	Type[2]	Description	
7	Res	Reserved	R	0	Reserved bit.
6:5	DRV[1:0]	Drive Strength	R/W	11	Drive level. The DRV1 and DRV0 bits are used to determine the output driver strength during read operations. A setting of 2'b11 allows the drive strength to be set by hardware based on the VCC level. Four drive settings are supported. This field is encoded as follows: 11: Auto (7 pF based on VCC level) 10: 50% (15 pF) 01: 75% (22 pF) 00: 100% (30 pF)
4:0	Res	Reserved	R	0	Reserved bit.

1. Only R/W bits can be modified when using the Write Status Register command.
2. R/W = Readable and writable. R = Readable only.

11.1.1 SRP1, SRP0 Bits

The SRP1 and SRP0 bits determine if the Status Register can be modified. The state of the $\overline{WP}$ pin, along with the values of the SRP1 and SRP0, determine if the device is software-protected, hardware-protected, or power supply lock-down, as shown in Table 14.

Table 14. Status Register Protection Table

SRP1	SRP0	$\overline{WP}$	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL = 1.(Factory Default)
0	1	0	Hardware Protected	$\overline{WP}$ = 0, the Status Register is locked and cannot be written.
0	1	1	Hardware Unprotected	$\overline{WP}$ = 1, the Status Register is unlocked and can be written to after a Write Enable command, WEL = 1.
1	0	X	Power Supply Lock-Down[1]	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.

1. When SRP1, SRP0 = (1, 0), a Power-Down, Power-Up cycle changes SRP1, SRP0 to the (0, 0) state.

11.1.2 CMP, SEC, TB, BP2, BP1, BP0 Bits

The CMP, SEC, TB, BP2, BP1, and BP0 bits control which portions of the array are protected from erase and program operations (see Table 6 and Table 7).

The CMP bit complements the effect of the other bits.

The SEC bit selects between large and small block size protection.

The TB bit selects between top of the array or bottom of the array protection.

The BP2, BP1, and BP0 bits determine how much of the array is protected.

11.1.3 WEL Bit

The WEL bit indicates the current status of the internal Write Enable Latch. When the WEL bit is in the logical 0 state, the device does not accept any Byte/Page Program, erase, Program Security Register, Erase Security Register, or Write Status Register commands. The WEL bit defaults to the logical 0 state after a device power-up or reset operation. Also, the WEL bit is reset to the logical 0 state automatically under the following conditions:

- Write Disable operation completes successfully
- Write Status Register operation completes successfully or aborts

- Program Security Register operation completes successfully or aborts
- Erase Security Register operation completes successfully or aborts
- Byte/Page Program operation completes successfully or aborts
- Block Erase operation completes successfully or aborts
- Chip Erase operation completes successfully or aborts

If the WEL bit is in the logical 1 state, it is not reset to a logical 0 if an operation aborts due to an incomplete or unrecognized opcode being clocked into the device before the $\overline{CS}$ pin is deasserted. For the WEL bit to be reset when an operation aborts prematurely, the entire opcode for a Byte/Page Program, erase, Program Security Register, Erase Security Register, or Write Status Register command must have been clocked into the device.

11.1.4 $\overline{RDY}$/BSY Bit

The $\overline{RDY}$/BSY bit is used to determine whether or not an internal operation, such as a program or erase, is in progress. To poll the $\overline{RDY}$/BSY bit to detect the completion of a program or erase cycle, new Status Register data must be continually clocked out of the device until the state of the $\overline{RDY}$/BSY bit changes from a logical 1 to a logical 0.

11.1.5 LB3, LB2, LB1 Bits

The LB3, LB2, and LB1 bits are used to determine if any of the three Security Register pages are locked.

The LB3 bit is in the logical 1 state if Security Register page-2 is locked and cannot be erased or programmed.

The LB2 bit is in the logical 1 state if Security Register page-1 is locked and cannot be erased or programmed.

The LB1 bit is in the logical 1 state if Security Register page-0 is locked and cannot be erased or programmed.

11.1.6 E_SUS Bit

This bit is set and cleared by hardware and indicates the status of an erase operation. This bit is encoded as follows:

0: Erase operation is not suspended (default)
1: Erase operation is suspended

Hardware clears this bit once the condition that caused the erase suspend operation has been removed. Hardware typically sets this bit when a Program/Erase Suspend (75h) command is executed, and clears the bit when a Program/Erase Resume (7Ah) command is executed.

11.1.7 P_SUS Bit

This bit is set and cleared by hardware and indicates the status of an program operation. This bit is encoded as follows:

0: Program operation is not suspended (default)
1: Program operation is suspended

Hardware clears this bit once the condition that caused the program suspend operation has been removed. Hardware typically sets this bit when a Program/Erase Suspend (75h) command is executed, and clears the bit when a Program/Erase Resume (7Ah) command is executed.

11.1.8 QE Bit

The QE bit is used to determine if the device is in the Quad Enabled mode. If the QE bit is in the logical 1 state, then the $\overline{HOLD}$ and $\overline{WP}$ pins functions as input/output pins similar to the SI and SO. If the QE bit is in the logical 0 state, then the $\overline{HOLD}$ pin functions as an input only and the $\overline{WP}$ pin functions as an input only. The QE bit is set to 1 at power-on.

11.2 Write Status Register (01h, 31h, and 11h)

The Write Status Register command is used to modify the Block Protection, Security Register Lock-down, Quad Enable, and Status Register Protection. Before the Write Status Register command can be issued, the Write Enable command must have been previously issued to set the WEL bit in the Status Register to a logical 1.

The $\overline{CS}$ pin must be driven high after the eighth bit of the data byte has been latched in. If not, the Write Status Register command is not executed. As soon as the $\overline{CS}$ pin is driven high, the self-timed Write Status Register cycle is initiated.

While the Write Status Register cycle is in progress, the Status Register can be read to check the value of the Write in Progress (WIP) bit. The WIP bit is 1 during the self-timed Write Status Register cycle, and 0 when it is completed. When the cycle is completed, the Write Enable Latch is reset.

The Write Status Register command allows the user to change the values of the Block Protect (SEC, TB, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only. The Write Status Register command also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect ($\overline{WP}$) pin.

The Status Register Protect (SRP1 and SRP0) bits and Write Protect (/WP) pin allow the device to be put in the hardware protected mode. The Write Status Register command is not executed once the hardware protected mode is entered.

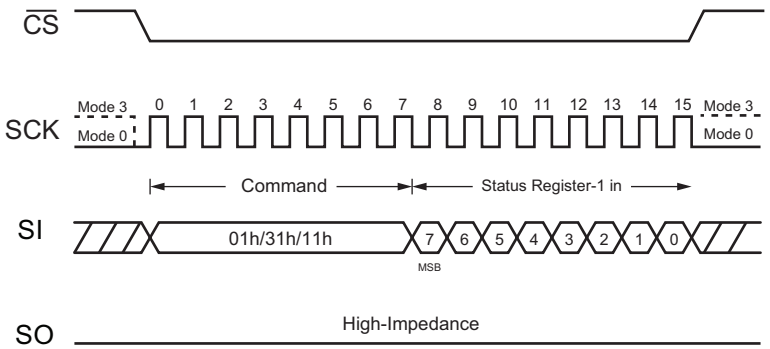


Figure 33. Write Status Register

.

Table 15. Write Status Register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRPO	SEC	TB	BP2	BP1	BP0	WEL	$\overline{RDY}$/BSY

Table 0-1.Write Status Register 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E_SUS	CMP	LB3	LB2	LB1	P_SUS	QE	SRP1

Table 0-2.Write Status Register 3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	DRV1	DRV0	Reserved	Reserved	Reserved	Reserved	Reserved

11.3 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits can also be written to as volatile bits. During power up reset, the non-volatile Status Register bits are copied to a volatile version of the Status Register that is used during device operation. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits.

To write the volatile version of the Status Register bits, the Write Enable for Volatile Status Register (50h) command must be issued prior to each Write Status Registers (01h) command. The Write Enable for Volatile Status Register command does not set the Write Enable Latch bit. It is valid only for the next Write Status Registers command, to change the volatile Status Register bit values.

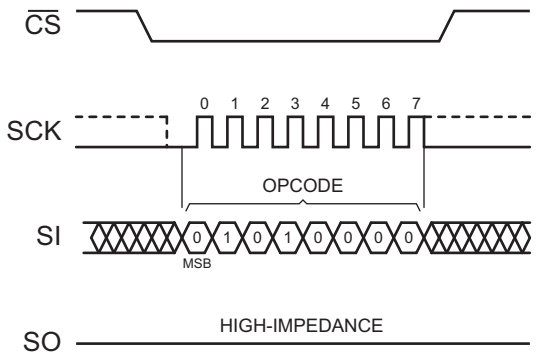


Figure 34. Write Enable for Volatile Status Register

12. Other Commands and Functions

The AT25QF641B supports three different commands to access device identification that indicates the manufacturer, device type, and memory density. The returned data bytes provide information as shown in Table 16.

Table 16. Manufacturer and Device ID Information

Command	Opcode	Dummy Bytes	Manufacturer ID (Byte #1)	Device ID (Byte #2)	Device ID (Byte #3)
Read Manufacturer and Device ID	9Fh	0	1Fh	88h	01h
Read ID (Legacy Command)	90h	3	1Fh		16h
Read ID (Dual-I/O)	92h	3	1Fh		16h
Read ID (Quad-I/O)	94h	3	1Fh		16h
Resume from Deep Power-Down and Read Device ID	ABh	3			16h

12.1 Read Manufacturer and Device ID (9Fh)

Identification information can be read from the device to enable systems to electronically query and identify the device.

Since not all Flash devices are capable of operating at very high clock frequencies, design applications to read the identification information from the devices at a reasonably low clock frequency to ensure all devices used in the application can be identified properly. Once the identification process is complete, the application can increase the clock frequency to accommodate specific Flash devices that are capable of operating at the higher clock frequencies.

To read the identification information, the $\overline{CS}$ pin must first be asserted and the opcode of 9Fh must be clocked into the device. After the opcode has been clocked in, the device begins outputting the identification data on the SO pin during the subsequent clock cycles. The first byte output is the Manufacturer ID, followed by two bytes of Device ID information. Deasserting the $\overline{CS}$ pin terminates the Manufacturer and Device ID read operation and puts the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

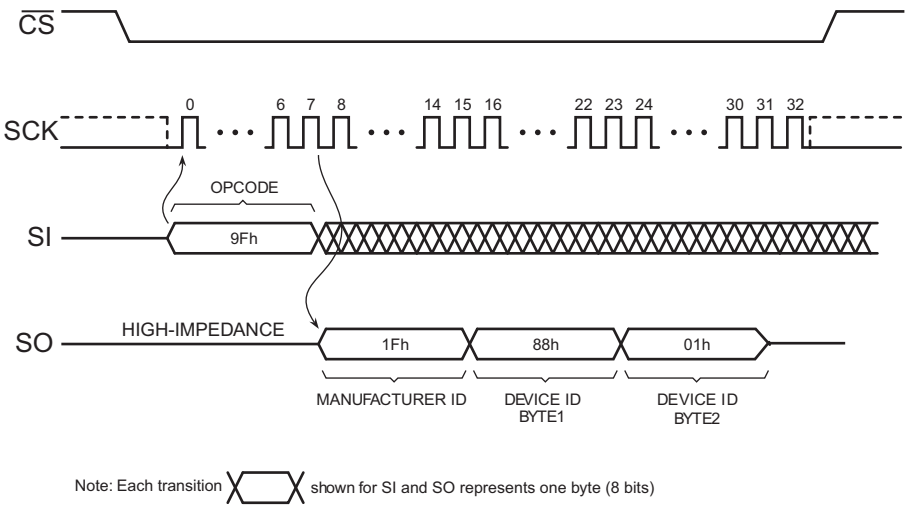


Figure 35. Read Manufacturer and Device ID

12.2 Read ID (Legacy Command) (90h)

Identification information can be read from the device to enable systems to electronically query and identify the device. The JEDEC standard method, described in Section 12.1, is preferred; however, the legacy Read ID command is supported on the AT25QF641B to enable backwards compatibility to previous generation devices.

To read the identification information, the $\overline{CS}$ pin must first be asserted, and the opcode 90h must be clocked into the device, followed by three dummy bytes. After the opcode and three dummy bytes are entered, the device begins outputting the identification data on the SO pin during the subsequent clock cycles. The first byte output is the Manufacturer ID of 1Fh, followed by a single byte of data representing a device code 16h. After the device code is output, the sequence of bytes repeats.

Deasserting the $\overline{CS}$ pin terminates the Read ID operation and puts the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data read.

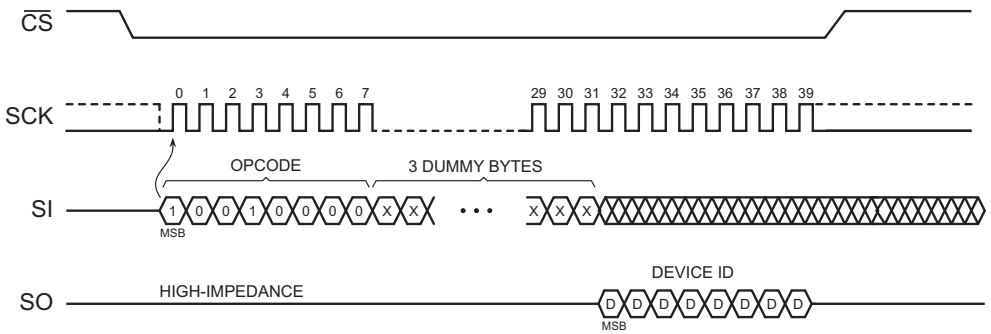


Figure 36. Read Manufacturer ID and Device ID (Legacy Command)

12.3 Dual-I/O Read Manufacture ID/ Device ID (92h)

The Dual-I/O Read Manufacturer/Device ID command is an alternative to the Release from Power-Down/Device ID command that provides both the JEDEC-assigned Manufacturer ID and the specific Device ID by Dual-I/O.

The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 92h, followed by a 24-bit address (A23 - A0) of 000000h. If the 24-bit address is initially set to 000001h, the Device ID is read first.

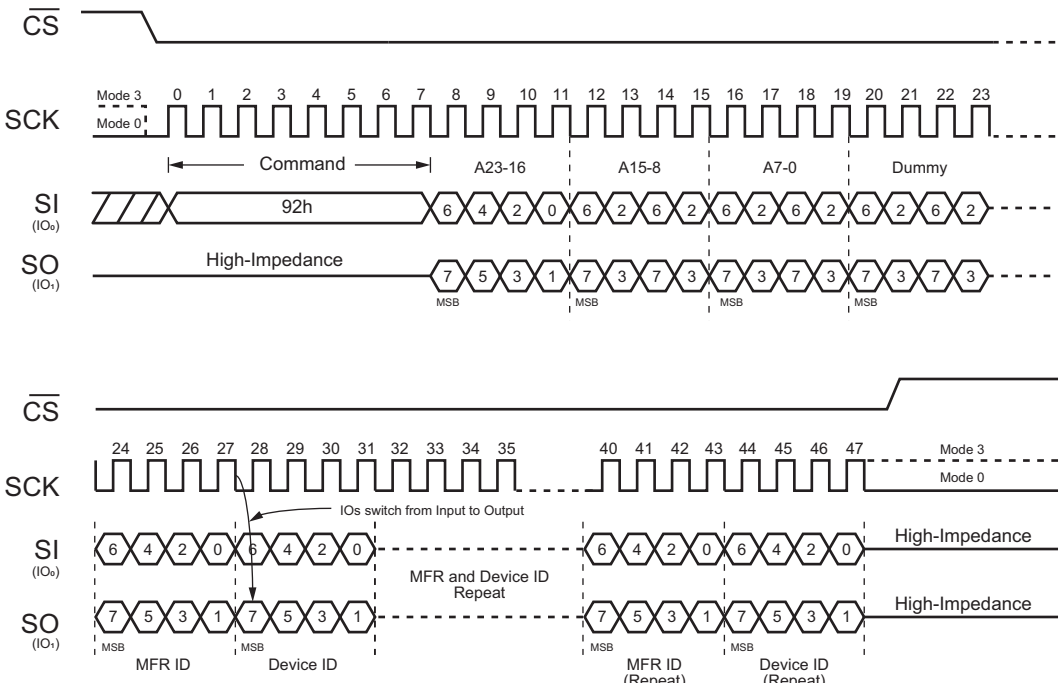


Figure 37. Dual-I/O Read Manufacture ID/ Device ID Sequence Diagram

12.4 Quad-I/O Read Manufacture ID / Device ID (94h)

The Quad-I/O Read Manufacturer/Device ID command is an alternative to the Release from Power-Down/Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O.

The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 94h, followed by a 24-bit address (A23 - A0) of 000000h and four dummy clocks. If the 24-bit address is initially set to 000001h, the Device ID is read out first.

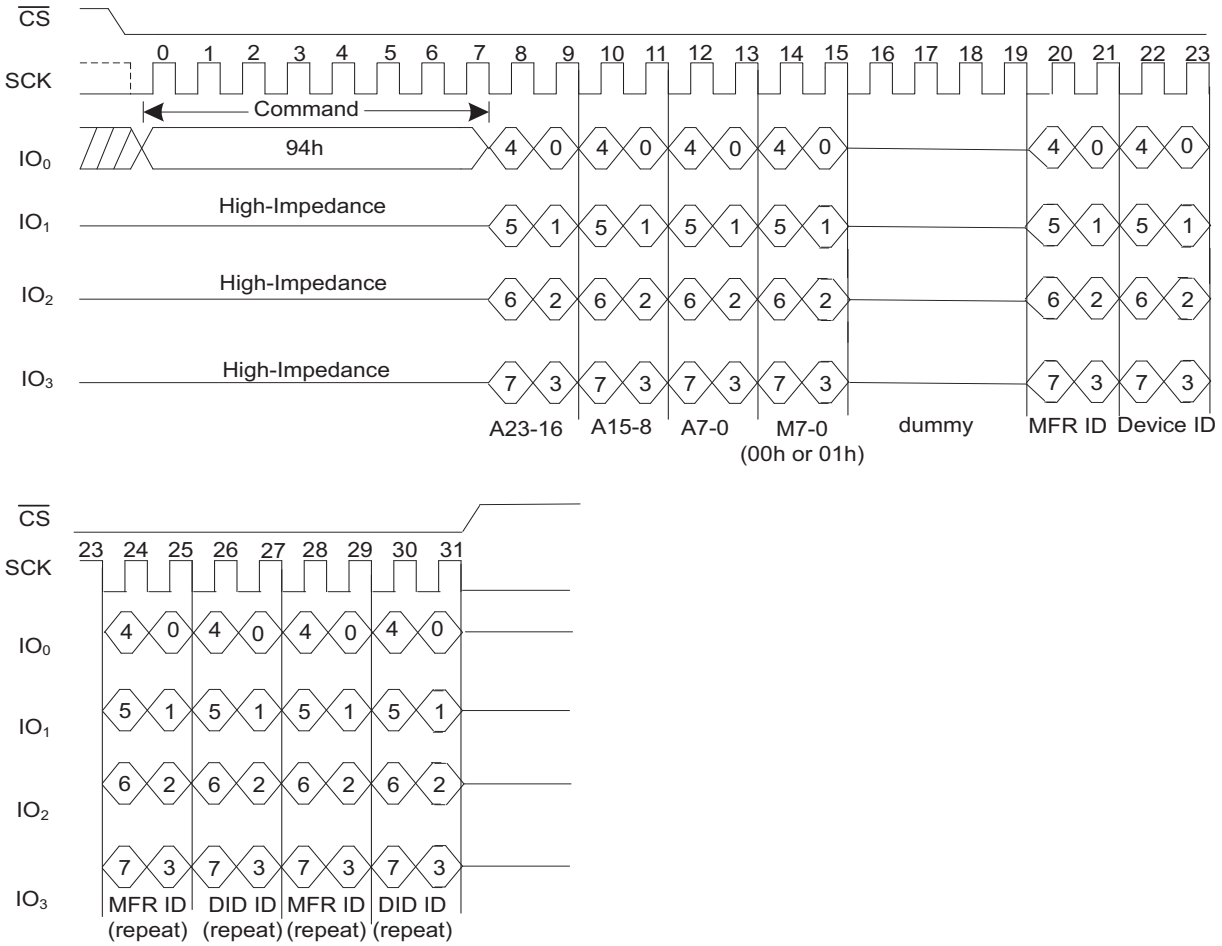


Figure 38. Quad-I/O Read Manufacture ID / Device ID Sequence Diagram

12.5 Deep Power-Down (B9h)

During normal operation, the device is placed in Standby Mode to consume less power as long as the $\overline{CS}$ pin remains deasserted and no internal operation is in progress. The Deep Power-Down command offers the ability to place the device into an even lower-power consumption state called the Deep Power-Down mode.

When the device is in the Deep Power-Down mode, all commands, including the Read Status Register command, are ignored, with the exception of the Resume from Deep Power-Down command. Since all commands are ignored, the mode can be used as an extra protection mechanism against program and erase operations.

Entering the Deep Power-Down mode is done by asserting the $\overline{CS}$ pin, clocking in the opcode of B9h, and then deasserting the $\overline{CS}$ pin. Any additional data clocked into the device after the opcode is ignored. When the $\overline{CS}$ pin is deasserted, the device enters the Deep Power-Down mode.

The complete opcode must be clocked in before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on an byte boundary (multiples of eight bits); otherwise, the device aborts the operation and returns to the Standby Mode once the $\overline{CS}$ pin is deasserted. Also, the device defaults to the Standby Mode after a power-cycle.

The Deep Power-Down command is ignored if an internally self-timed operation, such as a program or erase cycle, is in progress. The Deep Power-Down command must be reissued after the internally self-timed operation has been completed in order for the device to enter the Deep Power-Down mode.

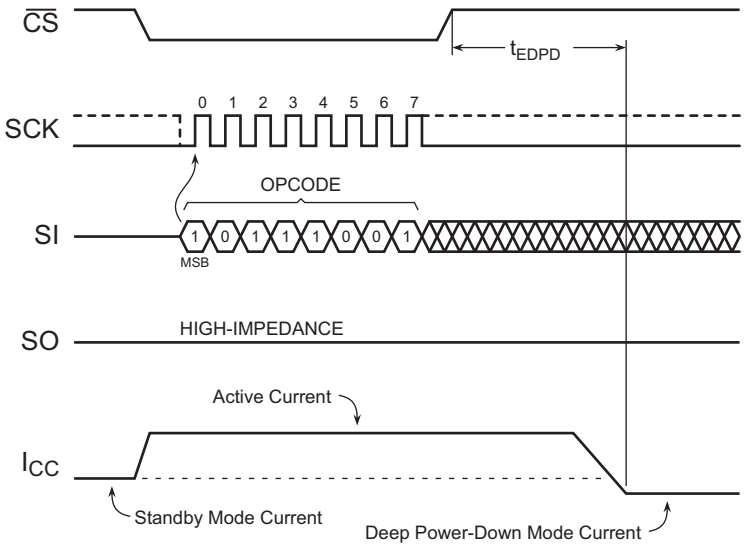


Figure 39. Deep Power-Down

12.6 Resume from Deep Power-Down (ABh)

To exit the Deep Power-Down mode and resume normal device operation, issue the Resume from Deep Power-Down command. This is the only command the device recognizes while in the Deep Power-Down mode.

To resume from the Deep Power-Down mode, the $\overline{CS}$ pin must be asserted first, and the opcode of ABh must be clocked into the device. Any additional data clocked into the device after the opcode is ignored. When the $\overline{CS}$ pin is deasserted, the device exits the Deep Power-Down mode and returns to the Standby Mode. After the device has returned to the Standby Mode, normal command operations, such as Read Array, can be resumed.

If the complete opcode is not clocked in before the $\overline{CS}$ pin is deasserted, or if the $\overline{CS}$ pin is not deasserted on an byte boundary (multiples of eight bits), the device aborts the operation and returns to the Deep Power-Down mode.

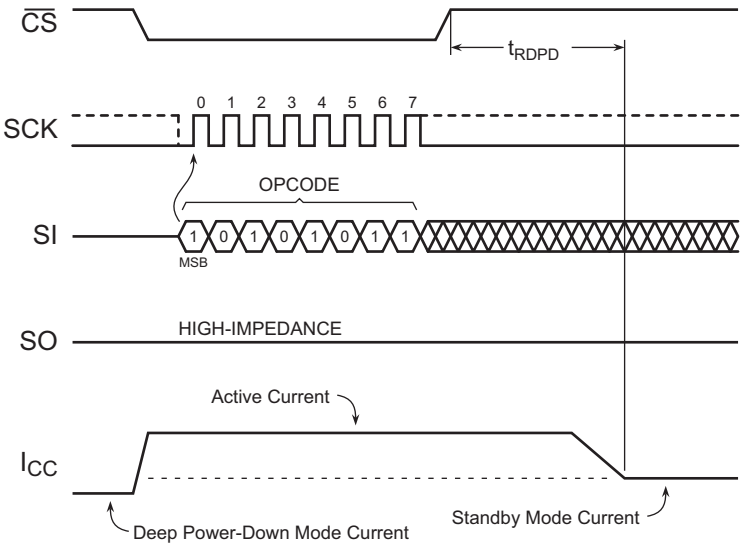


Figure 40. Resume from Deep Power-Down

12.6.1 Resume from Deep Power-Down and Read Device ID (ABh)

The Resume from Deep Power-Down command can also be used to read the Device ID. When used to release the device from the Power-Down state and obtain the Device ID, the $\overline{CS}$ pin must first be asserted and opcode ABh must be clocked into the device, followed by three dummy bytes. The Device ID bits are then shifted out on the falling edge of SCK with the most significant bit (MSB) first, as shown in Figure 41. This command only outputs a single byte Device ID. The Device ID value for the AT25QF641B is listed in Table 16.

After the last bit (0) of the Device ID has been clocked out, the sequence repeats itself, starting again with bit 7, as long as the $\overline{CS}$ pin remains asserted and the SCK pin is being pulsed. After $\overline{CS}$ is deasserted, it must remain high until new commands can be received.

The same command can be used to read the device ID when not in power down mode. In that case, $\overline{CS}$ does not have to remain high remain after it is deasserted.

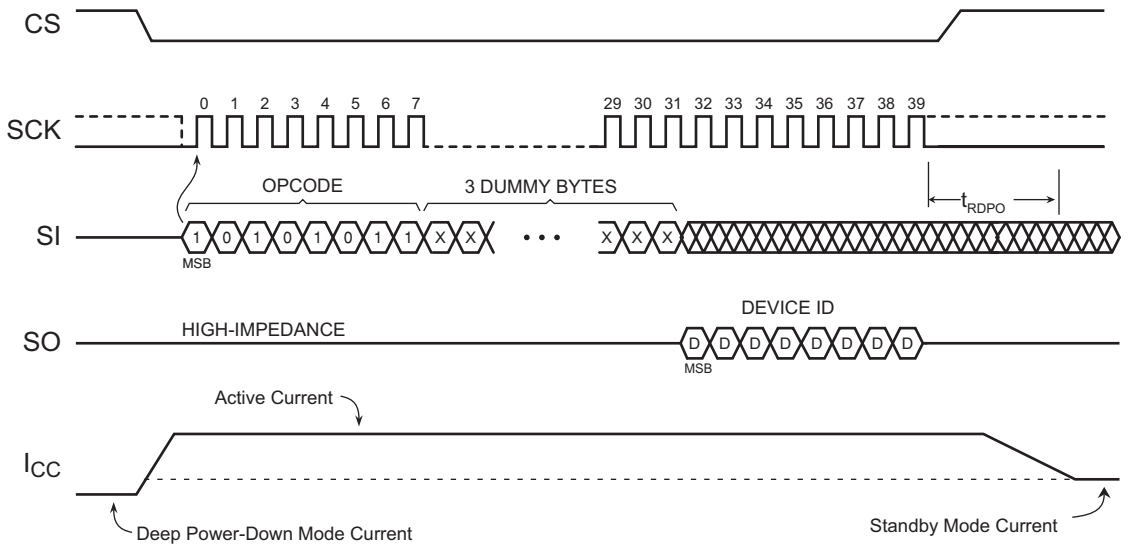


Figure 41. Resume from Deep Power-Down and Read Device ID

12.7 Hold Function

The $\overline{HOLD}$ pin is used to pause the serial communication with the device without having to stop or reset the clock sequence. The Hold mode, however, does not affect any internally self-timed operations, such as a program or erase cycle. Thus, if an erase cycle is in progress, asserting the $\overline{HOLD}$ pin does not pause the operation, and the erase cycle continues until it is finished.

If the QE bit value in the Status Register has been set to logical 1, the $\overline{HOLD}$ pin does not function as a control pin, but as an output for Quad-Output Read and input/output for Quad-I/O Read. The QE bit is set to 1 on power-on.

The Hold mode can only be entered while the $\overline{CS}$ pin is asserted. It is activated by asserting the $\overline{HOLD}$ pin during the SCK low pulse. If the $\overline{HOLD}$ pin is asserted during the SCK high pulse, the Hold mode is not started until the beginning of the next SCK low pulse. The device remains in the Hold mode as long as the $\overline{HOLD}$ pin and $\overline{CS}$ pin are asserted. While in the Hold mode, the SO pin is in a high-impedance state. Also, both the SI pin and the SCK pin are ignored. The $\overline{WP}$ pin, however, can still be asserted or deasserted while in the Hold mode.

To end the Hold mode and resume serial communication, the $\overline{HOLD}$ pin must be deasserted during the SCK low pulse. If the $\overline{HOLD}$ pin is deasserted during the SCK high pulse, the Hold mode does not end until the beginning of the next SCK low pulse.

If the $\overline{CS}$ pin is deasserted while the $\overline{HOLD}$ pin is asserted, any operation that have been started are aborted, and the device resets the WEL bit in the Status Register to the logical 0 state.

13. Electrical Specifications

13.1 Absolute Maximum Ratings*

Temperature under Bias . . . . . -55 °C to +125 °C
Storage Temperature. . . . . -65 °C to +150 °C
All Input Voltages (including NC Pins) with Respect to Ground. . . . . .-0.5 V to +4.0 V
All Output Voltages with Respect to Ground. . . . . .-0.5 V to V_{CC} + 4.0 V

*Notice: Stresses beyond those listed here can cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

13.2 DC and AC Operating Range

Parameter	Condition	Value
Operating Temperature (Case)	Industrial	-40 °C to 85 °C
V_{CC} Power Supply		2.7 V to 3.6 V

13.3 DC Characteristics

Symbol	Parameter	Condition	2.7 V to 3.6 V			Units
			Min	Typ[1]	Max	
I_{DPD}	Deep Power-Down Current	$\overline{CS}$, $\overline{HOLD}$, $\overline{WP}$ = V_{IH} All inputs at CMOS levels		1	5	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{HOLD}$, $\overline{WP}$ = V_{IH} All inputs at CMOS levels		14	25	µA
I_{CC1}	Active Current, Read (03h, 0Bh) Operation	f = 20 MHz; I_{OUT} = 0		3	5	mA
		f = 50 MHz; I_{OUT} = 0		4	6	mA
		f = 85 MHz; I_{OUT} = 0		5	7.5	mA
I_{CC2}	Active Current,(3Bh, BBh Read Operation (Dual)	f = 50 MHz; I_{OUT} = 0		5	7	mA
		f = 85 MHz and 104 MHz; I_{OUT} = 0		7	10	mA
I_{CC3}	Active Current,(6Bh, EBh Read Operation (Quad)	f = 50 MHz; I_{OUT} = 0		6	9	mA
		f = 85 MHz and 104 MHz; I_{OUT} = 0		9	13	mA
I_{CC4}	Active Current, Program Operation	$\overline{CS}$ = V_{CC}			19	mA
I_{CC5}	Active Current, Erase Operation	$\overline{CS}$ = V_{CC}			15	mA
I_{LI}	Input Load Current	All inputs at CMOS levels			±2	µA
I_{LO}	Output Leakage Current	All inputs at CMOS levels			±2	µA
V_{IL}	Input Low Voltage		-0.5		V_{CC} x 0.2	V
V_{IH}	Input High Voltage		V_{CC} x 0.8		V_{CC} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2			V

1. Typical Values measured at 3.0 V at 25 °C.

13.4 AC Characteristics - Maximum Clock Frequencies

Symbol	Parameter	2.7 V to 3.6 V			3.0 V to 3.6 V			Units
		Min	Typ	Max	Min	Typ	Max	
f_{CLK}	Maximum Clock Frequency for all opcodes except 03h, 3Bh, 0Bh, 6Bh, EBh, and E7h			104			133	MHz
	Maximum Clock Frequency for opcode EBh			104			133	MHz
	Maximum Clock Frequency for opcode 0Bh, 3Bh, 6Bh, and E7h			85			104	MHz
	Maximum Clock Frequency for 03h opcode			55			55	MHz

13.5 AC Characteristics - All Other Parameters

Symbol [1]	Parameter	2.7 V to 3.6 V			Units
		Min	Typ	Max	
t_{CLKH}	Clock High Time	4			ns
t_{CLKL}	Clock Low Time	4			ns
t_{CLKR}	Clock Rise Time, Peak-to-Peak (Slew Rate)	0.1			V/ns
t_{CLKF}	Clock Fall Time, Peak-to-Peak (Slew Rate)	0.1			V/ns
t_{CSH}	$\overline{CS}$ High Time	20			ns
t_{CSLS}	$\overline{CS}$ Low Setup Time (relative to Clock)	5			ns
t_{CSLH}	$\overline{CS}$ Low Hold Time (relative to Clock)	5			ns
t_{CSHS}	$\overline{CS}$ High Setup Time (relative to Clock)	5			ns
t_{CSHH}	$\overline{CS}$ High Hold Time (relative to Clock)	5			ns
t_{DS}	Data In Setup Time	2			ns
t_{DH}	Data In Hold Time	2			ns
t_{DIS}	Output Disable Time			6	ns
t_V	Output Valid Time			7	ns
t_{OH}	Output Hold Time	0			ns
t_{HLS}	$\overline{HOLD}$ Low Setup Time (relative to Clock)	5			ns
t_{HLH}	$\overline{HOLD}$ Low Hold Time (relative to Clock)	5			ns
t_{HHS}	$\overline{HOLD}$ High Setup Time (relative to Clock)	5			ns
t_{HHH}	$\overline{HOLD}$ High Hold Time (relative to Clock)	5			ns
t_{HLQZ}	$\overline{HOLD}$ Low to Output High-Z			6	ns
t_{HHQZ}	$\overline{HOLD}$ High to Output High-Z			6	ns
t_{RES1}	$\overline{CS}$ High to Standby Mode Without Electronic Signature Read			20	µs
t_{RES2}	$\overline{CS}$ High to Standby Mode With Electronic Signature Read			20	µs
t_{SUS}	$\overline{CS}$ High to Next Command After Suspend			20	µs
t_{WPS}	Write Protect Setup Time	20			ns
t_{WPH}	Write Protect Hold Time	100			ns
t_{EDPD}	$\overline{CS}$ High to Deep Power-Down			20	µs
t_{RDPD}	$\overline{CS}$ High to Standby Mode			20	µs
t_{RDPO}	Resume Deep Power-Down, $\overline{CS}$ High to ID			20	µs

1. Not 100% tested (value guaranteed by design and characterization).

13.6 Program and Erase Characteristics

Symbol	Parameter	Condition	2.7 V to 3.6 V			
			Min	Typ[1]	Max[2]	Units
t_{PP}	Page Program Time (256 Bytes)			0.4	3.0	ms
t_{BP1}	First Byte Program Time			30	50	µs
t_{BP2}	Second Byte Program Time			2.5	12	µs
t_{BLKE}	Block Erase Time	4 kbytes		65	250	ms
		32 kbytes		150	500	
		64 kbytes		240	900	
t_{CHPE} [3]	Chip Erase Time			30	40	sec
t_{WRSR}	Write Status Register Time			5	30	ms

1. Typical value is measured at 3.0 V, 25 °C.
2. Unless specified otherwise, maximum is worst case measurement at cycling conditions after 100k cycles.
3. Under worst condition: 85 °C, 2.7 V.

13.7 Power-Up Conditions

Symbol	Parameter	Min	Max	Units
t_{VSL}	Minimum V_{CC} to $\overline{CS}$ Low Time	70		µs

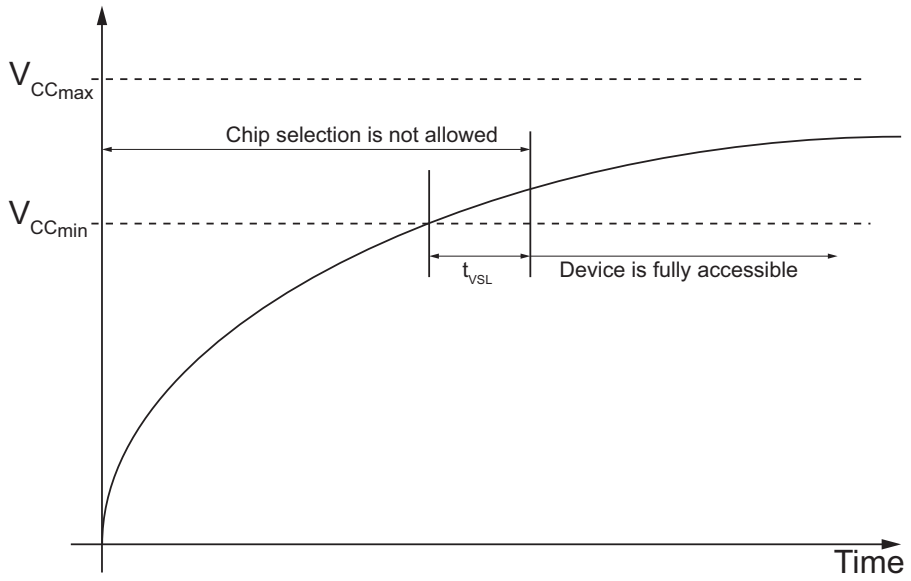
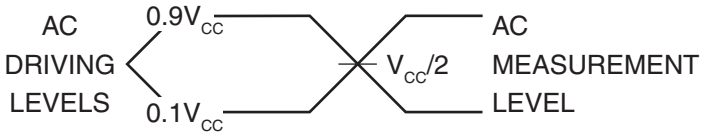
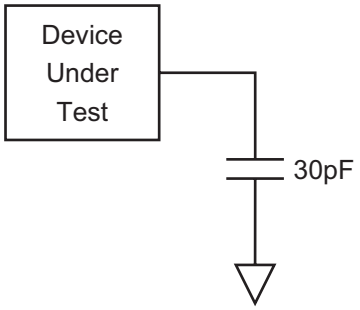


Figure 42. Power-Up Timing and Voltage Levels

13.8 Input Test Waveforms and Measurement Levels



13.9 Output Test Load



14. AC Waveforms

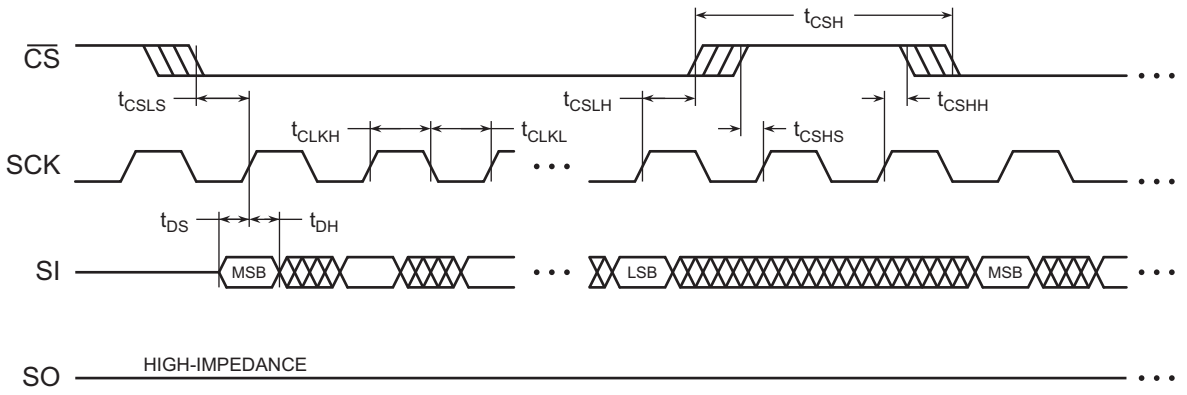


Figure 43. Serial Input Timing

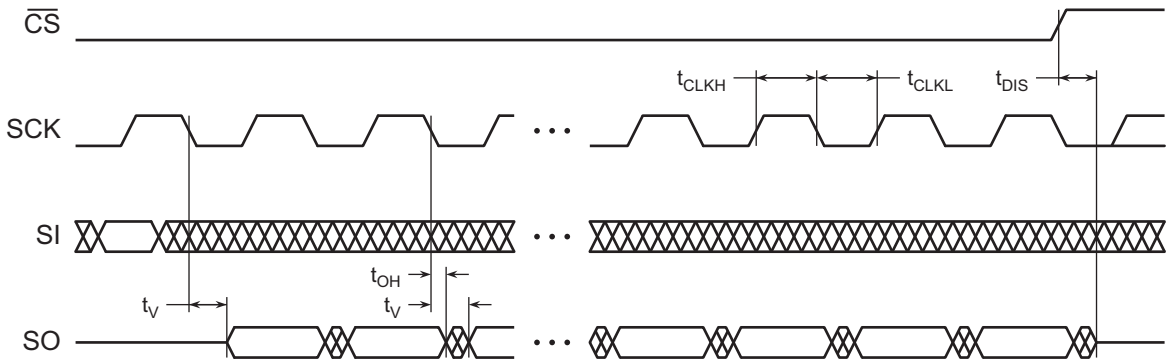


Figure 44. Serial Output Timing

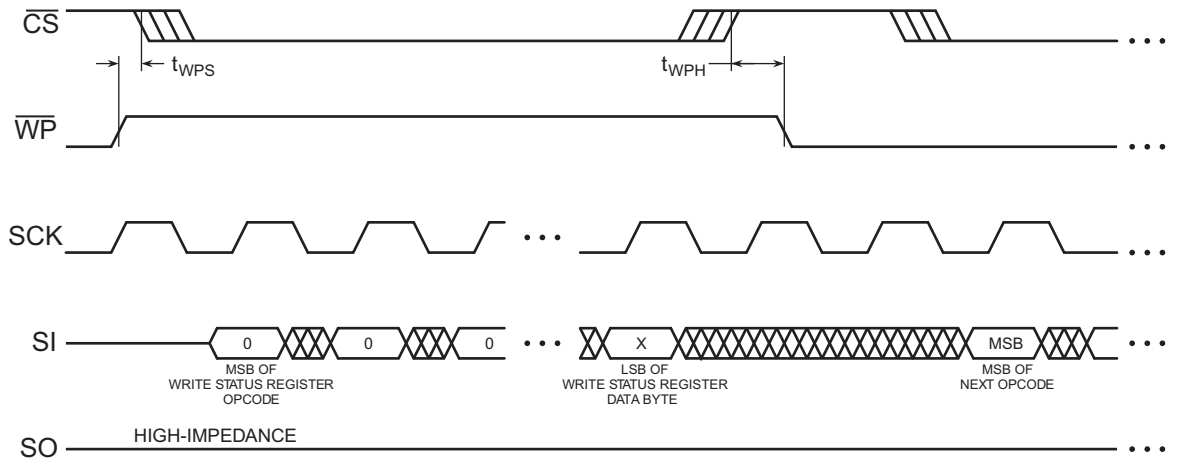


Figure 45. $\overline{WP}$ Timing for Write Status Register Command When BPL = 1

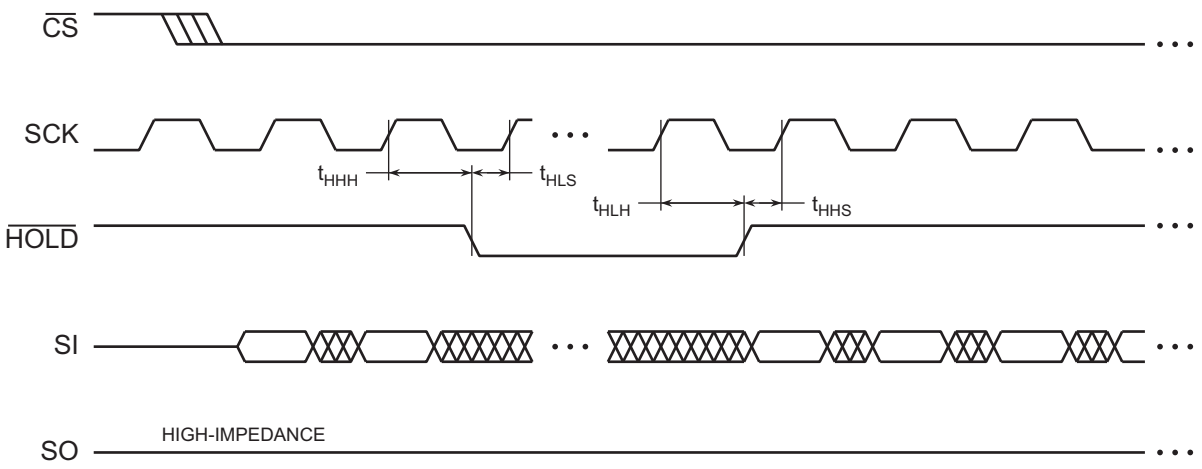


Figure 46. $\overline{HOLD}$ Timing – Serial Input

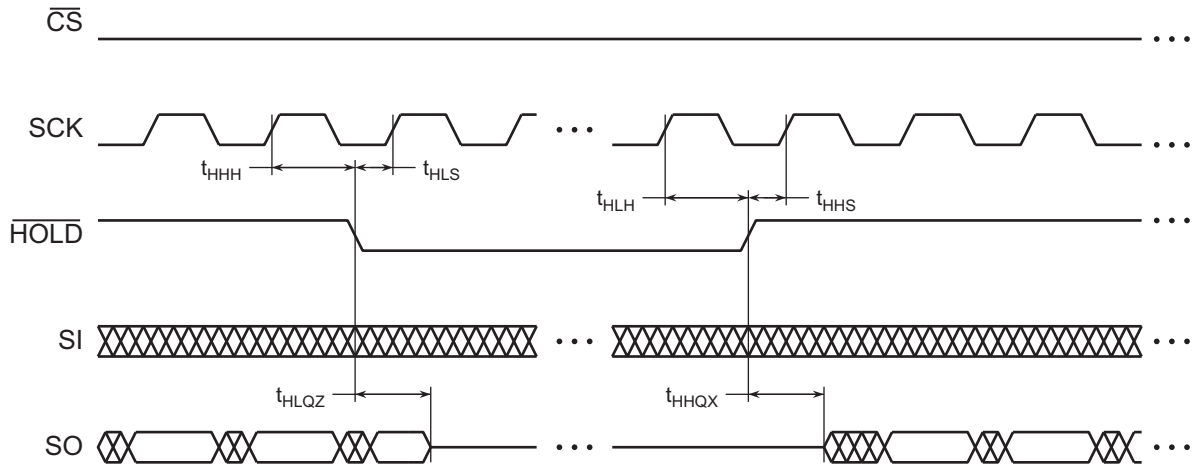
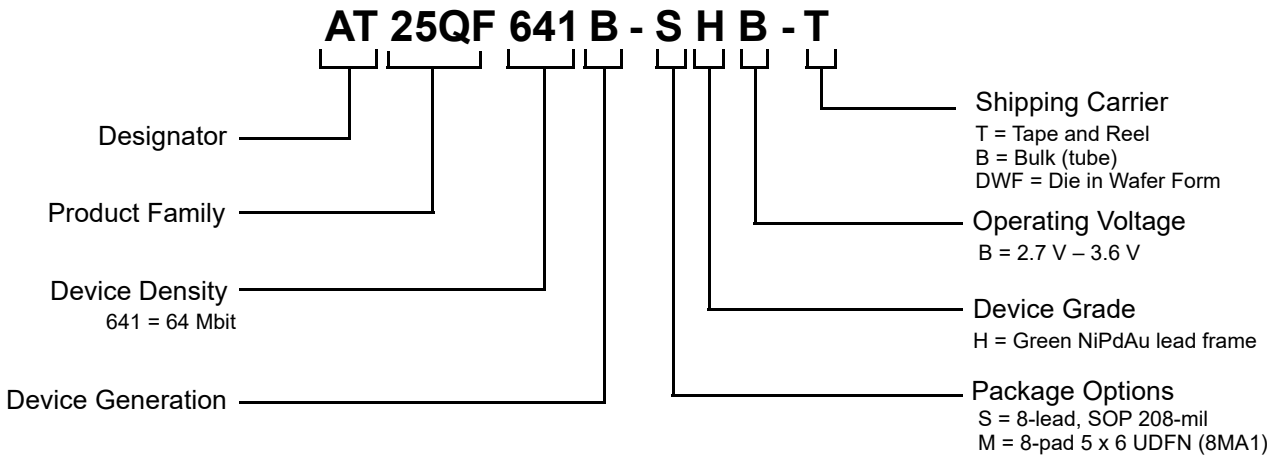


Figure 47. $\overline{HOLD}$ Timing – Serial Output

15. Ordering Information

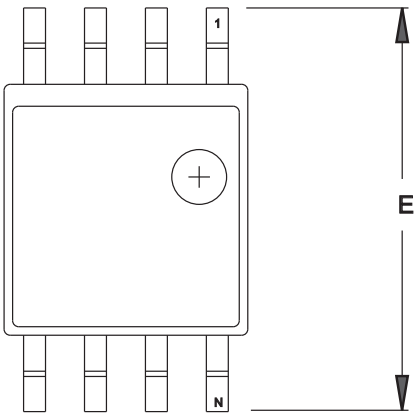


Ordering Code	Package	Operating Voltage	Maximum Frequency (MHz)	Operation Range
AT25QF641B-SHB-B	8-lead, 208-mil Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)	2.7 V to 3.6 V	133 MHz [1]	Industrial (-40 °C to +85 °C)
AT25QF641B-SHB-T				
AT25QF641B-SPB-T				
AT25QF641B-MHB-T	8-pad (5 x 6 x 0.6 mm body), Thermally Enhanced Plastic Ultra-thin Dual Flat No-lead (UDFN)			
AT25QF641B-DWF[2]	Die in Waver Form			

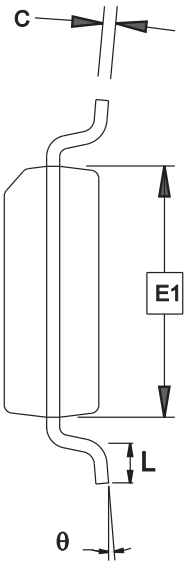
1. Only for the EBh command with 3.0V - 3.6 V power supply.
2. Contact Renesas Electronics for detailed information.

16. Packaging Information

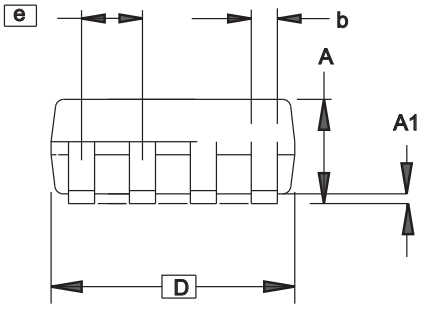
16.1 8-lead, 208-mil Wide EIAJ SOIC



TOP VIEW



END VIEW



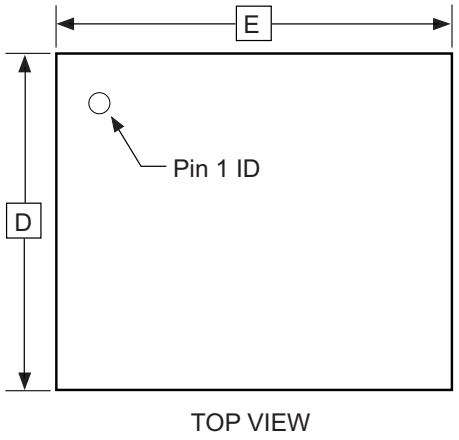
SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

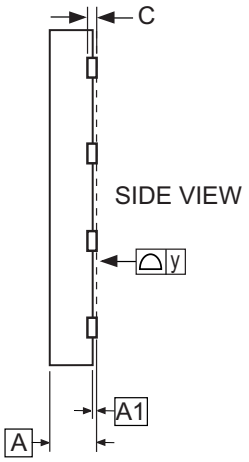
SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	4
C	0.15		0.35	4
D	5.13		5.38	
E1	5.18		5.40	2
E	7.70		8.26	
L	0.51		0.85	
θ	0°		8°	
e	1.27 BSC			3

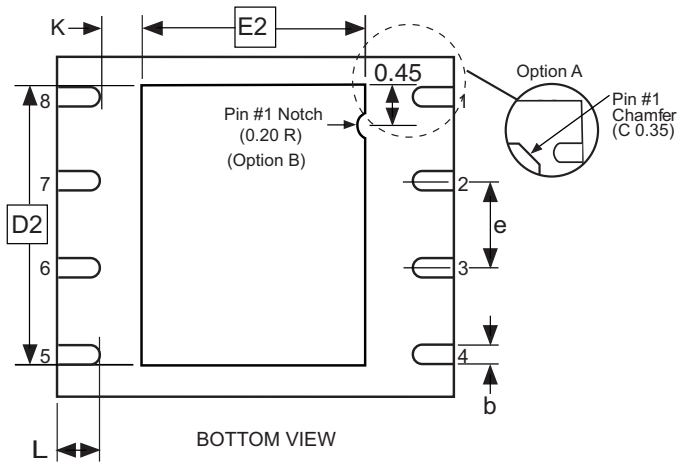
Notes: 1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs aren't included.
3. Determines the true geometric position.
4. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

16.2 8-Pad 5 x 6 x 0.6 mm UDFN



TOP VIEW





BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.45	0.55	0.60	
A1	0.00	0.02	0.05	
b	0.35	0.40	0.48	
C		0.152 REF		
D	4.90	5.00	5.10	
D2	3.80	4.00	4.20	
E	5.90	6.00	6.10	
E2	3.20	3.40	3.60	
e		1.27		
L	0.50	0.60	0.75	
y	0.00	–	0.08	
K	0.20	–	–	

Notes: 1. This package conforms to JEDEC reference MO-229, Saw Singulation.
2. The terminal #1 ID is a Laser-marked Feature.

17. Revision History

Revision Number	Date	Tasks
A	02/2020	Initial release of AT25QF641B data sheet.
B	06/2020	Replaced some diagrams with higher-quality ones (no change in content). Replaced all instances of Status Register Byte with Status Register. Added timing diagrams to the descriptions of opcodes 60h/C7h, 75h, 7Ah, 06h, and 04h. Updated erase times at the end of Section 8.5. Changed resume/suspend numbers in Section 8.5: 2 ms → 3.5 ms, and 18 ms → 55 ms.
C	12/2020	Updated numbers in Tables 13.3 and 13.6 based on latest characterization. Removed “Preliminary” from title page.
D	05/2022	Applied new corporate template to document. Added physical block size information to Section 1, Product Overview. Added the following note to the end of the description for opcode 75h: “Note: A read operation from a physical block that includes a suspended area might provide unreliable data. For the definition of the physical block and for the techniques to ensure high data integrity, see *Application Note AN-500*.” Changed t_{VCSL} to t_{VSL} in Section 13.7. Added the following to the end of the $\overline{CS}$ description in Table 1: “To ensure correct power-up sequencing, it is recommended to add a 10k Ohm pull-up resistor from $\overline{CS}$ to V_{CC}. This ensures $\overline{CS}$ ramps together with V_{CC} during power-up.” Changed the description of $\overline{WP}$ and $\overline{HOLD}/IO_3$ in Table 1.
E	07/2023	Added 133 MHz max frequency in Feature List, Section 13.4 and Section 15.

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