Four Output Low Power Differential Fanout Buffer for PCI Express Gen1, Gen2, Gen3, and QPI

9DBL411B

General Description:

The ICS9DBL411B is a 4 output lower power differential buffer. Each output has its own OE# pin. It has a maximum operating frequency of 150 MHz.

Recommended Application:

PCI-Express Gen 1/2/3 or QPI fanout buffer

Output Features:

- 4 - low power differential output pairs
- Individual OE# control of each output pair

Key Specifications:

- Output cycle-cycle jitter < 15ps additive
- Output to output skew: < 50ps

Features/Benefits:

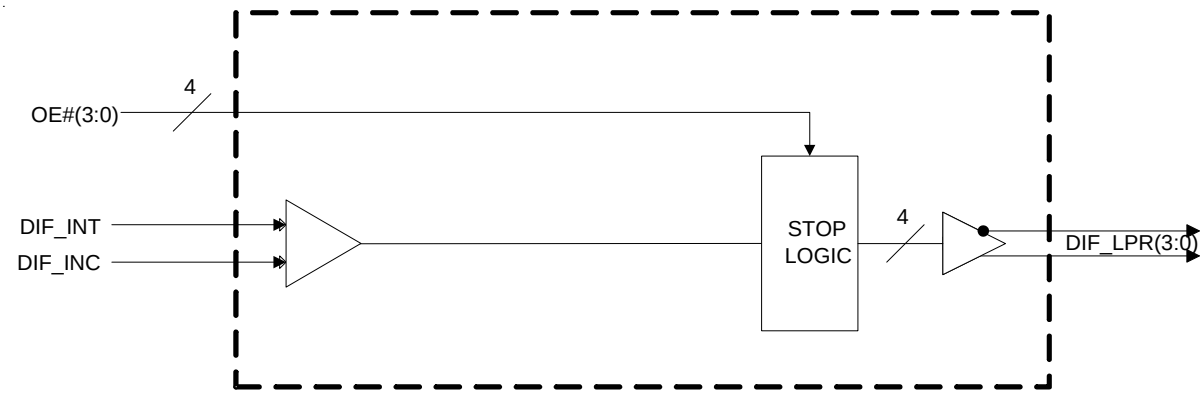
- Low power differential outputs for PCI-Express and QPI clocks
- Power down mode when all OE# are high
- Available in I-temp
- 20-pin MLF or TSSOP packaging

Power Groups

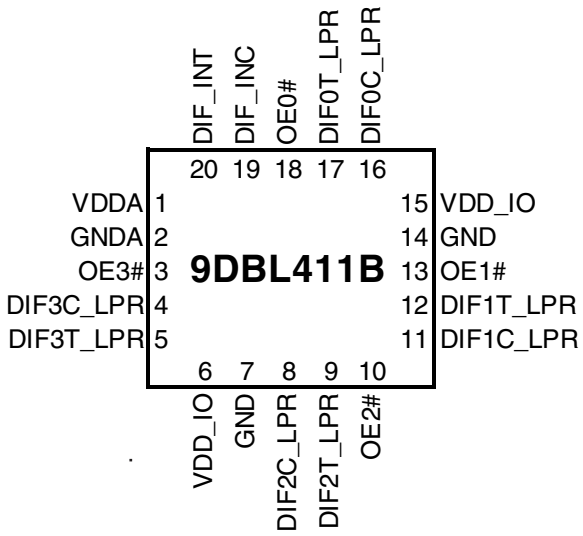
Pin Number (TSSOP)		Description
VDD	GND	
9,18	10,17	VDD_IO for DIF(3:0)
4	5	3.3V Analog VDD & GND

Pin Number (MLF)		Description
VDD	GND	
6,15	7,14	VDD_IO for DIF(3:0)
1	2	3.3V Analog VDD & GND

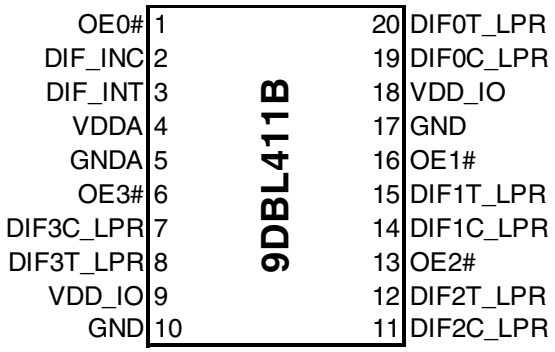
Functional Block Diagram



Pin Configurations

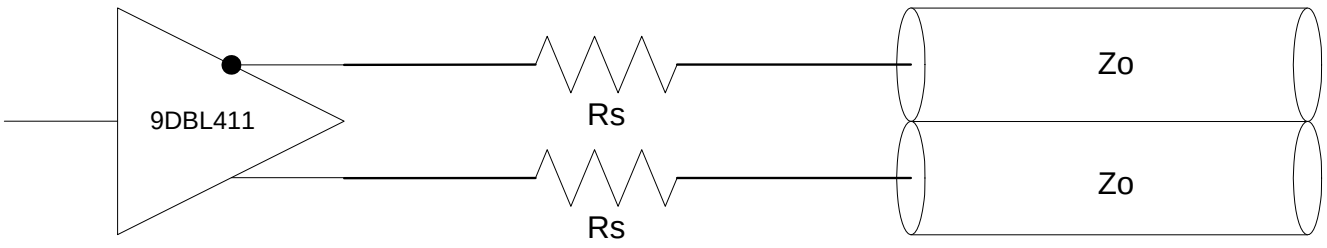


20-pin MLF



20-pin TSSOP

Terminations



Zo – 17 = Rs (ohms), where Zo is the single-ended intrinsic impedance of the board transmission line. Single-ended intrinsic impedance is ½ that of the differential impedance.

Single Ended Impedance (Zo)	Rs 5% tolerance	Rs 2% tolerance	Notes
50	33	33.2	In general, 5% resistors may be used. All values are in ohms.
45	27	27.4	
42.5	24 or 27	24.9	

TSSOP Pin Description

PIN # (TSSOP)	PIN NAME	PIN TYPE	DESCRIPTION
1	OE0#	IN	Output Enable for DIF0 output. Control is as follows: 0 = enabled, 1 = Low-Low
2	DIF_INC	IN	Complement side of differential input clock
3	DIF_INT	IN	True side of differential input clock
4	VDDA	PWR	3.3V Power for the Analog Core
5	GNDA	GND	Ground for the Analog Core
6	OE3#	IN	Output Enable for DIF3 output. Control is as follows: 0 = enabled, 1 = Low-Low
7	DIF3C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
8	DIF3T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
9	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
10	GND	GND	Ground pin
11	DIF2C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
12	DIF2T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
13	OE2#	IN	Output Enable for DIF2 output. Control is as follows: 0 = enabled, 1 = Low-Low
14	DIF1C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
15	DIF1T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
16	OE1#	IN	Output Enable for DIF1 output. Control is as follows: 0 = enabled, 1 = Low-Low
17	GND	GND	Ground pin
18	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
19	DIF0C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
20	DIF0T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)

MLF Pin Description

PIN # (MLF)	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDA	PWR	3.3V Power for the Analog Core
2	GNDA	GND	Ground for the Analog Core
3	OE3#	IN	Output Enable for DIF3 output. Control is as follows: 0 = enabled, 1 = Low-Low
4	DIF3C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
5	DIF3T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
6	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
7	GND	GND	Ground pin
8	DIF2C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
9	DIF2T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
10	OE2#	IN	Output Enable for DIF2 output. Control is as follows: 0 = enabled, 1 = Low-Low
11	DIF1C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
12	DIF1T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
13	OE1#	IN	Output Enable for DIF1 output. Control is as follows: 0 = enabled, 1 = Low-Low
14	GND	GND	Ground pin
15	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
16	DIF0C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
17	DIF0T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
18	OE0#	IN	Output Enable for DIF0 output. Control is as follows: 0 = enabled, 1 = Low-Low
19	DIF_INC	IN	Complement side of differential input clock
20	DIF_INT	IN	True side of differential input clock

Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Maximum Supply Voltage	VDDA	Core Supply Voltage		4.6	V	1,7
Maximum Supply Voltage	VDD_IO	Low-Voltage Differential I/O	0.99	3.8	V	1,7
Maximum Input Voltage	V_{IH}	3.3V LVCMOS Inputs		4.6	V	1,7,8
Minimum Input Voltage	V_{IL}	Any Input	Vss - 0.5		V	1,7
Ambient Operating Temp	TambCOM	Commercial Range	0	70	°C	1
	TambIND	Industrial Range	-40	85	°C	1
Storage Temperature	Ts	-	-65	150	°C	1,7
Input ESD protection	ESD prot	Human Body Model	2000		V	1,7

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Supply Voltage	VDDA	Supply Voltage	3.000	3.600	V	1
Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply	0.99	3.600	V	1
Input High Voltage	V_{IHSE}	Single-ended inputs	2	V_{DD} + 0.3	V	1
Input Low Voltage	V_{ILSE}	Single-ended inputs	V_{SS} - 0.3	0.8	V	1
Differential Input High Voltage	V_{IHDIF}	Differential inputs (single-ended measurement)	600	1.15	V	1
Differential Input Low Voltage	V_{ILDIF}	Differential inputs (single-ended measurement)	V_{SS} - 0.3	300	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4	8	V/ns	2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5	5	uA	1
Operating Supply Current	$I_{DD\_3.3V}$	VDDA supply current		20	mA	1
	$I_{DD\_IO\_133M}$	VDD_IO supply @ fOP = 133MHz		20	mA	1
Power Down Current (All OE# pins High)	$I_{DD\_SB\_3.3V}$	VDDA supply current, Input stopped, OE# pins all high		750	uA	1
	I_{DD_SBIO}	VDD_IO supply, Input stopped, OE# pins all high		150	uA	1
Input Frequency	F_i	V_{DD} = 3.3 V	15	150	MHz	2
Pin Inductance	L_{pin}			7	nH	1
Input Capacitance	C_{IN}	Logic Inputs	1.5	5	pF	1
	C_{OUT}	Output pin capacitance		6	pF	1
OE# latency (at least one OE# is low)	$T_{OE\#LAT}$	Number of clocks to enable or disable output from assertion/deassertion of OE#	1	3	periods	1
Clock stabilization time (from all OE# high to first OE# low).	T_{STAB}	Delay from assertion of first OE# to first clock out (assumes input clock running and device in power down state))		150	ns	1
Tdrive_OE#	$T_{DROE\#}$	Output enable after OE# de-assertion		10	ns	1
Tfall_OE#	T_{FALL}	Fall/rise time of OE# inputs		5	ns	1
Trise_OE#	T_{RISE}			5	ns	1

AC Electrical Characteristics - DIF Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	1.5	4	V/ns	1,2
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	1.5	4	V/ns	1,2
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement		20	%	1
Maximum Output Voltage	V_{HIGH}	Includes overshoot		1150	mV	1
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300		mV	1
Differential Voltage Swing	V_{SWING}	Differential Measurement	1200		mV	1
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300	550	mV	1,3,4
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		140	mV	1,3,5
Duty Cycle Distortion	$D_{CYCDIS0}$	Differential Measurement, fIN<=133.33MHz		3	%	1,6
Additive Cycle to Cycle Jitter	$DIFJ_{C2CADD}$	Differential Measurement, **Additive**		15	ps	1
DIF[3:0] Skew	DIF_{SKEW}	Differential Measurement		50	ps	1
Propagation Delay	t_{PD}	Input to output Delay	2.5	3.5	ns	1
Additive Phase Jitter - PCIe Gen1	$t_{phase\_add\ PCIG1}$	1.5MHz < 22MHz		6	ps Pk-Pk	1,9
Additive Phase Jitter - PCIe Gen2 High Band	$t_{phase\_add\ PCIG2HI}$	High Band is 1.5MHz to Nyquist (50MHz)		0.16	ps rms	1,9
Additive Phase Jitter PCIe Gen2 Low Band	$t_{phase\_add\ PCIG2LO}$	Low Band is 10KHz to 1.5MHz		0.07	ps rms	1,9
Additive Phase Jitter PCIe Gen3	$t_{phase\_add\ PCIG2LO}$	2M-4M, 2M-5M filter		0.2	ps rms	1,9
Additive Phase Jitter QPI133 (6.4GBs, 12 UI)	$t_{phase\_add\ QPI6G4}$	11MHz to 33MHz		0.04	ps rms	1,9

Notes on Electrical Characteristics (all measurements use 9LRS3187B as clock source and R_S=33ohms/C_L=2pF test load):

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

[3] Vxabs is defined as the voltage where CLK = CLK#

[4] Only applies to the differential rising edge (CLK rising and CLK# falling)

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

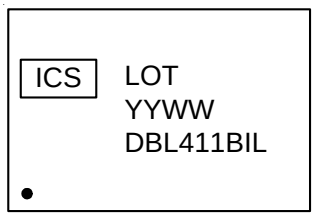
[6] This figure refers to the maximum distortion of the input wave form.

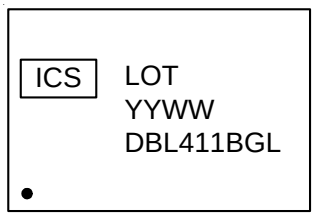
[7] Operation under these conditions is neither implied, nor guaranteed.

[8] Maximum input voltage is not to exceed maximum VDD

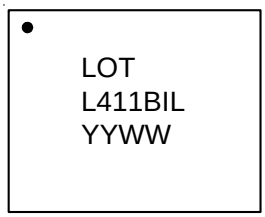
[9] The 9DBL411B has no PLL, so the part itself contributes very little jitter to the input clock. But this also means that the 9DBL411 cannot 'de-jitter' a noisy input clock. Values calculated per PCI SIG and per Intel Clock Jitter tool version 1.5

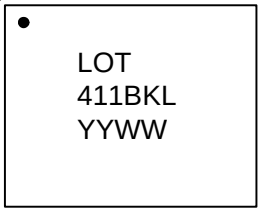
20-pin TSSOP Marking Diagrams



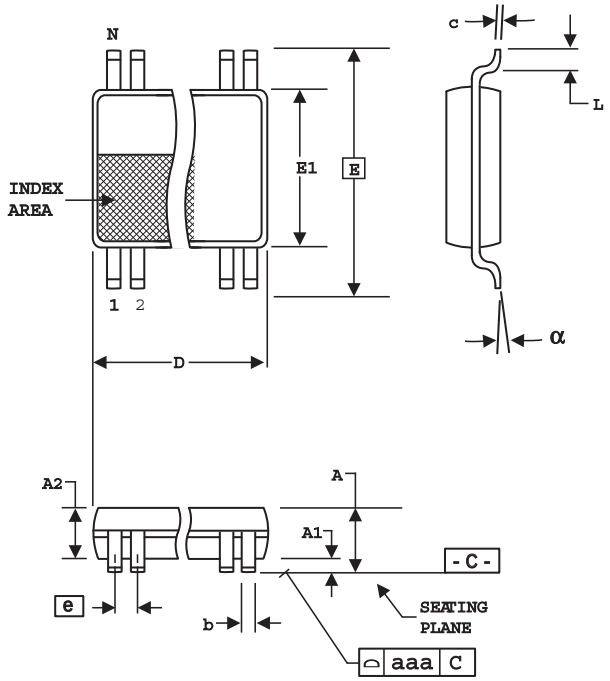


20-pin MLF Marking Diagrams





20-pin TSSOP Package Drawing and Dimensions



20-Lead, 4.40 mm. Body, 0.65 mm. Pitch TSSOP
(173 mil) (25.6 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

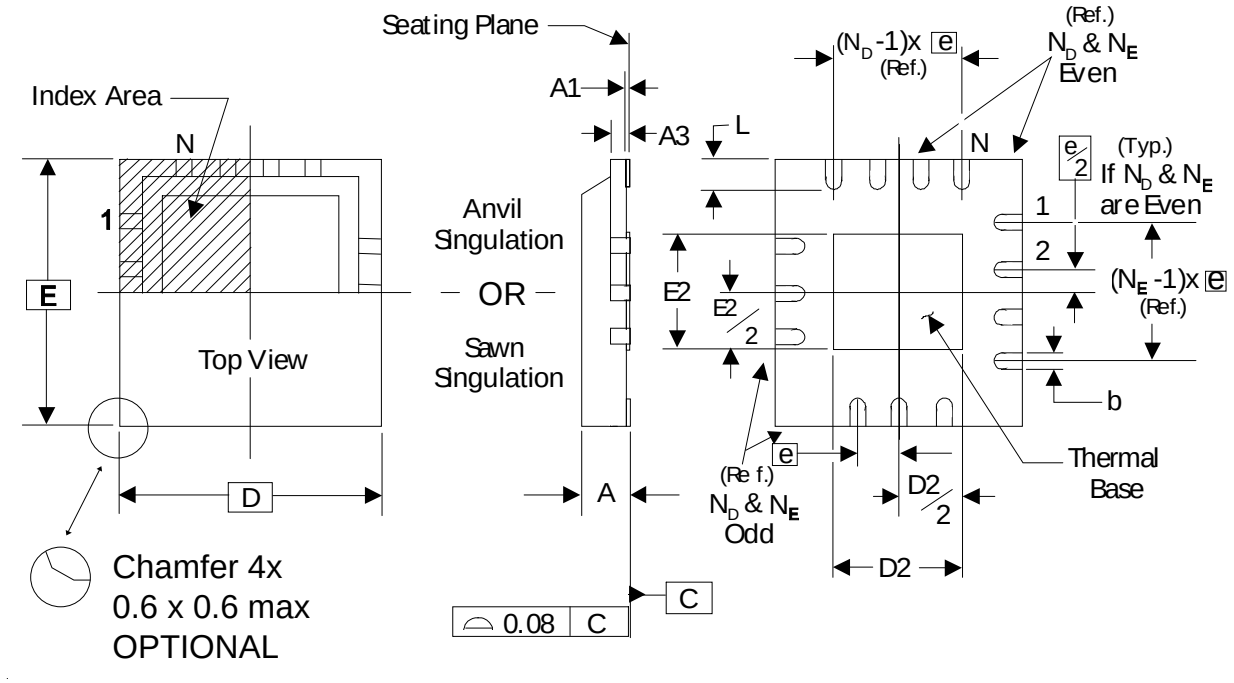
VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
20	6.40	6.60	.252	.260

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

20-pin MLF Package Drawing and Dimensions



THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.20 Reference	
b	0.18	0.3
e	0.50 BASIC	

DIMENSIONS

SYMBOL	ICS 20L TOLERANCE
N	20
N_D	5
N_E	5
D x E BASIC	4.00 x 4.00
D2 MIN. / MAX.	2.00 / 2.25
E2 MIN. / MAX.	2.00 / 2.25
L MIN. / MAX.	0.45 / 0.65

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9DBL411BKLF	Tubes	20-pin MLF	0 to +70°C
9DBL411BKLFT	Tape and Reel	20-pin MLF	0 to +70°C
9DBL411BGLF	Tubes	20-pin TSSOP	0 to +70°C
9DBL411BGLFT	Tape and Reel	20-pin TSSOP	0 to +70°C
9DBL411BKILF	Tubes	20-pin MLF	-40 to +85°C
9DBL411BKILFT	Tape and Reel	20-pin MLF	-40 to +85°C
9DBL411BGILF	Tubes	20-pin TSSOP	-40 to +85°C
9DBL411BGILFT	Tape and Reel	20-pin TSSOP	-40 to +85°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
"B" is the device revision designator (will not correlate to the datasheet revision).

Revision History

Rev.	Issue Date	Description	Page #
0.1	1/8/2010	Initial Release. Compared with A rev the following have changed: 1. Added I-temp version 2. Updated electrical tables for I-temp 3. Revised Phase Jitter specs and added QPI.	
A	1/8/2010	Released to final.	
B	4/23/2010	Changed Input Frequency from 33 min to 15 MHz min	5
C	10/18/2010	Updated Supply Voltage min/max ratings.	5
D	3/22/2012	Updated phase jitter table for PCIe Gen3.	
E	6/28/2012	Typo in "Differential Input Low Voltage" units; changed "V" to "mV"	
F	8/16/2013	Correct typo on top-side marking for MLF (commercial temp.) from "L411BKL" to "411BKL".	
G	9/25/2018	Replaced "Trays" with "Tubes" in Ordering Information.	

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