# Lower Power 3.3V CMOS Fast SRAM 256K (32K x 8-Bit)

**71V256SA**

## Features

- **Ideal for high-performance processor secondary cache**
- **Commercial (0°C to +70°C) and Industrial (–40°C to +85°C) temperature range options**
- **Fast access times:**
  - *Commercial and Industrial: 12/15/20ns*
- **Low standby current (maximum):**
  - *2mA full standby*
- **Small packages for space-efficient layouts:**
  - *28-pin 300 mil SOJ*
  - *28-pin TSOP Type I*
- **Produced with advanced high-performance CMOS technology**
- **Inputs and outputs are LVTTL-compatible**
- **Single 3.3V(±0.3V) power supply**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**
- **Green parts available, see ordering information**

## Description

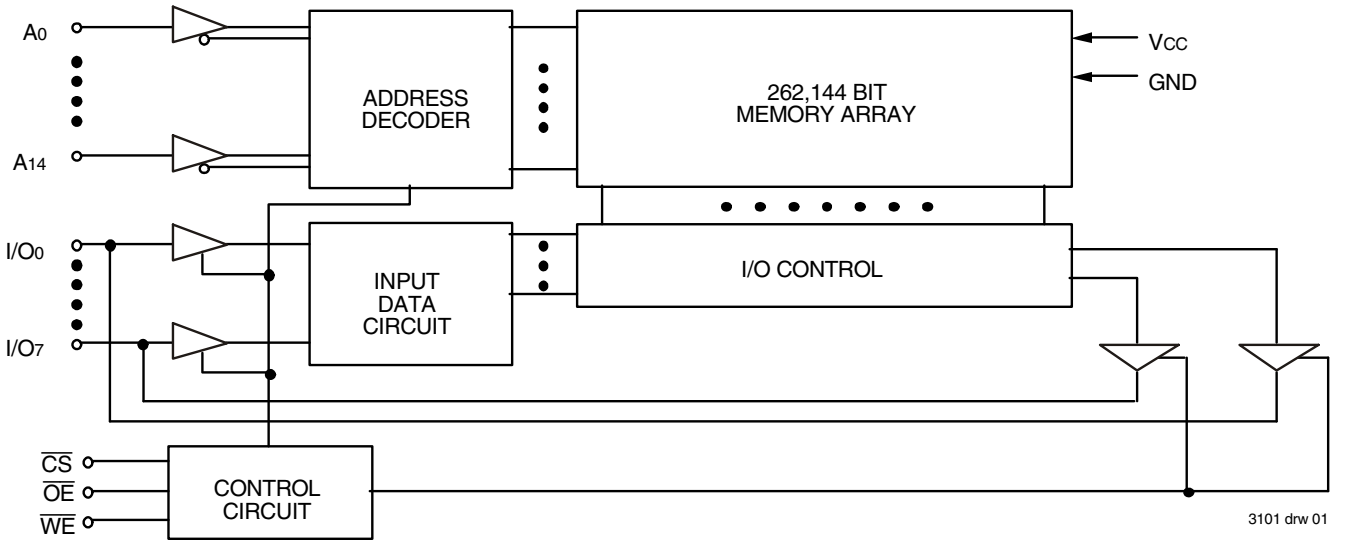
The IDT71V256SA is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using a high-performance, high-reliability CMOS technology.

The IDT71V256SA has outstanding low power characteristics while at the same time maintaining very high performance. Address access times of as fast as 12ns are ideal for 3.3V secondary cache in 3.3V desktop designs.

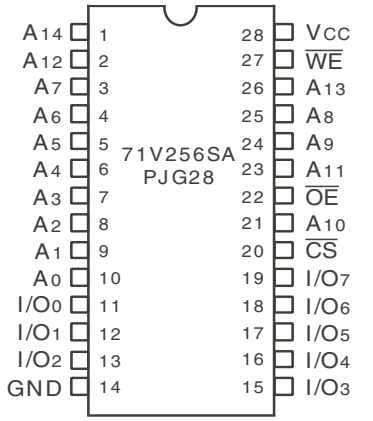
When power management logic puts the IDT71V256SA in standby mode, its very low power characteristics contribute to extended battery life. By taking $\overline{CS}$ HIGH, the SRAM will automatically go to a low power standby mode and will remain in standby as long as $\overline{CS}$ remains HIGH. Furthermore, under full standby mode ($\overline{CS}$ at CMOS level, f=0), power consumption is guaranteed to always be less than 6.6mW and typically will be much smaller.

The IDT71V256SA is packaged in a 28-pin 300 mil SOJ and a 28-pin 300 mil TSOP Type I.

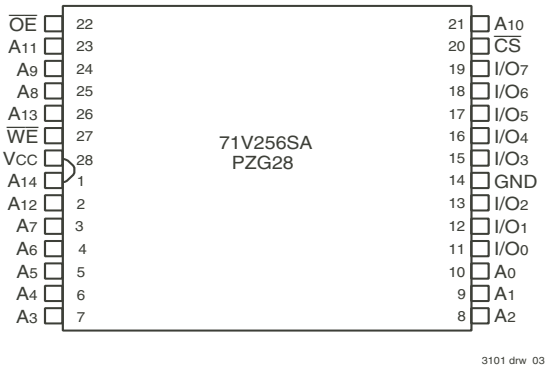
## Functional Block Diagram



## Pin Configurations(1)




DIP/SOJ
Top View




TSOP
Top View

**NOTE:**
1. This text does not indicate orientation of actual part-marking.

## Pin Descriptions

| Name | Description |
|---|---|
| $A_0$ - $A_{14}$ | Addresses |
| $I/O_0$ - $I/O_7$ | Data Input/Output |
| $\overline{CS}$ | Chip Select |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| GND | Ground |
| $V_{CC}$ | Power |

3101 tbl 01

## Truth Table(1)

| $\overline{WE}$ | $\overline{CS}$ | $\overline{OE}$ | I/O | Function |
|---|---|---|---|---|
| X | H | X | High-Z | Standby ($I_{SB}$) |
| X | $V_{HC}$ | X | High-Z | Standby ($I_{SB1}$) |
| H | L | H | High-Z | Output Disable |
| H | L | L | $D_{OUT}$ | Read |
| L | L | X | $D_{IN}$ | Write |

3101 tbl 02

**NOTE:**
1. H = $V_{IH}$, L = $V_{IL}$, X = Don't Care

## Absolute Maximum Ratings(1)

| Symbol | Rating | Com'l | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage Relative to GND | -0.5 to +4.6 | V |
| $V_{TERM}$(2) | Terminal Voltage Relative to GND | -0.5 to $V_{CC}$+0.5 | V |
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | -55 to +125 | °C |
| $P_T$ | Power Dissipation | 1.0 | W |
| $I_{OUT}$ | DC Output Current | 50 | mA |

3101 tbl 03

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input, Output, and I/O terminals; 4.6V maximum.

## Capacitance
($T_A$ = +25°C, f = 1.0MHz, SOJ package)

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 3dV | 7 | pF |

3101 tbl 04

**NOTE:**
1. This parameter is determined by device characterization, but is not production tested.

## Recommended Operating Temperature and Supply Voltage

| Grade | Temperature | GND | Vcc |
|---|---|---|---|
| Commercial | 0°C to +70°C | 0V | 3.3V ± 0.3V |
| Industrial | -40°C to +85°C | 0V | 3.3V ± 0.3V |

3101 tbl 05

## Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| GND | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage - Inputs | 2.0 | — | $V_{CC}$ +0.3 | V |
| $V_{IH}$ | Input High Voltage - I/O | 2.0 | — | $V_{CC}$ +0.3 | V |
| $V_{IL}$ | Input Low Voltage | -0.3[1] | — | 0.8 | V |

3101 tbl 06

**NOTE:**
1. $V_{IL}$ (min.) = –2.0V for pulse width less than 5ns, once per cycle.

## DC Electrical Characteristics[1]

($V_{CC}$ = 3.3V ± 0.3V, $V_{LC}$ = 0.2V, $V_{HC}$ = $V_{CC}$ - 0.2V, Commercial and Industrial Temperature Ranges)

| Symbol | Parameter | 71V256SA12 | 71V256SA15 | 71V256SA20 | Unit |
|---|---|---|---|---|---|
| $I_{CC}$ | Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, $V_{CC}$ = Max., f = $f_{MAX}$[2] | 90 | 85 | 85 | mA |
| $I_{SB}$ | Standby Power Supply Current (TTL Level) $\overline{CS}$ = $V_{IH}$, $V_{CC}$ = Max., Outputs Open, f = $f_{MAX}$[2] | 20 | 20 | 20 | mA |
| $I_{SB1}$ | Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, $V_{CC}$ = Max., Outputs Open, f = 0[2], $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$ | 2 | 2 | 2 | mA |

3101 tbl 07

**NOTES:**
1. All values are maximum guaranteed values.
2. $f_{MAX}$ = 1/$t_{RC}$, only address inputs cycling at $f_{MAX}$; f = 0 means that no inputs are cycling.

## DC Electrical Characteristics

($V_{CC}$ = 3.3V± 0.3V)

| Symbol | Parameter | Test Conditions | IDT71V256SA | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $\|I_{LI}\|$ | Input Leakage Current | $V_{CC}$ = Max., $V_{IN}$ = GND to $V_{CC}$ | — | — | 2 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $V_{CC}$ = Max., $\overline{CS}$ = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | — | — | 2 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8mA, $V_{CC}$ = Min. | — | — | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4mA, $V_{CC}$ = Min. | 2.4 | — | — | V |

3101 tbl 08

## AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 3ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| AC Test Load | See Figures 1 and 2 |

3101 tbl 09

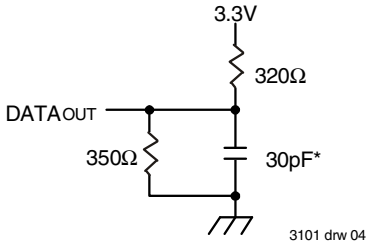



**Figure 1. AC Test Load**

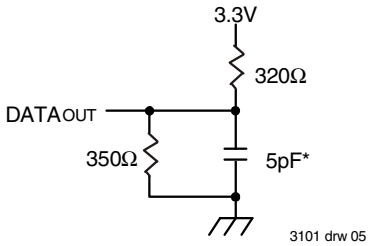



**Figure 2. AC Test Load (for $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{OW}$, $t_{WHZ}$)**

*Includes scope and jig capacitances

## AC Electrical Characteristics

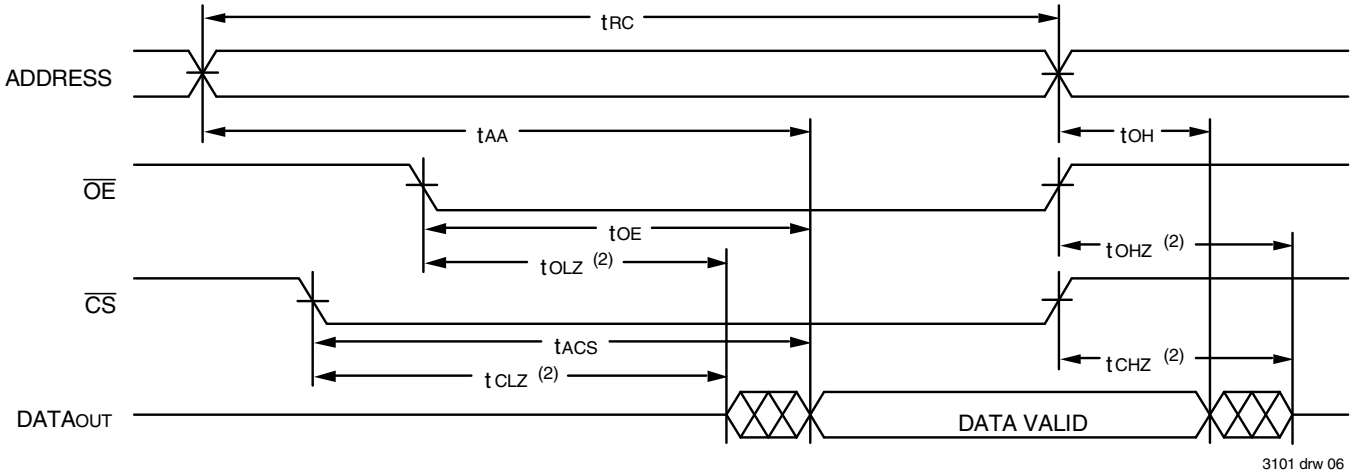
($V_{CC}$ = 3.3V ± 0.3V, Commercial and Industrial Temperature Ranges)

| Symbol | Parameter | 71V256SA12 | | 71V256SA15 | | 71V256SA20 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Read Cycle** | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 12 | — | 15 | — | 20 | — | ns |
| $t_{AA}$ | Address Access Time | — | 12 | — | 15 | — | 20 | ns |
| $t_{ACS}$ | Chip Select Access Time | — | 12 | — | 15 | — | 20 | ns |
| $t_{CLZ}$(1) | Chip Select to Output in Low-Z | 5 | — | 5 | — | 5 | — | ns |
| $t_{CHZ}$(1) | Chip Select to Output in High-Z | 0 | 8 | 0 | 9 | 0 | 10 | ns |
| $t_{OE}$ | Output Enable to Output Valid | — | 6 | — | 7 | — | 8 | ns |
| $t_{OLZ}$(1) | Output Enable to Output in Low-Z | 3 | — | 0 | — | 0 | — | ns |
| $t_{OHZ}$(1) | Output Disable to Output in High-Z | 2 | 6 | 0 | 7 | 0 | 8 | ns |
| $t_{OH}$ | Output Hold from Address Change | 3 | — | 3 | — | 3 | — | ns |
| **Write Cycle** | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 12 | — | 15 | — | 20 | — | ns |
| $t_{AW}$ | Address Valid to End-of-Write | 9 | — | 10 | — | 15 | — | ns |
| $t_{CW}$ | Chip Select to End-of-Write | 9 | — | 10 | — | 15 | — | ns |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width | 9 | — | 10 | — | 15 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{DW}$ | Data to Write Time Overlap | 6 | — | 7 | — | 8 | — | ns |
| $t_{DH}$ | Data Hold from Write Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{OW}$(1) | Output Active from End-of-Write | 4 | — | 4 | — | 4 | — | ns |
| $t_{WHZ}$(1) | Write Enable to Output in High-Z | 1 | 8 | 1 | 9 | 1 | 10 | ns |

3101 tbl 10

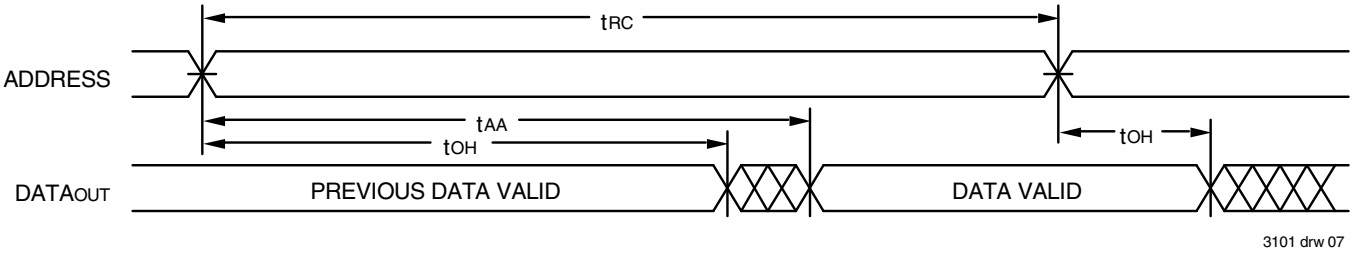
**NOTE:**
1. This parameter guaranteed with the AC test load (Figure 2) by device characterization, but is not production tested.

## Timing Waveform of Read Cycle No. 1(1)

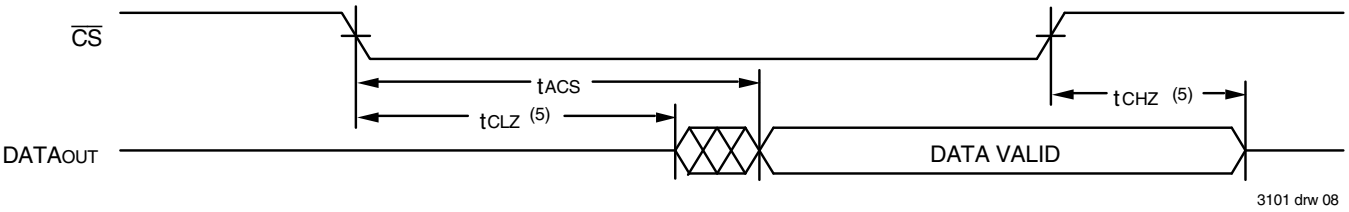



**NOTES:**
1. $\overline{WE}$ is HIGH for Read cycle.
2. Transition is measured ±200mV from steady state.

## Timing Waveform of Read Cycle No. 2(1,2,4)

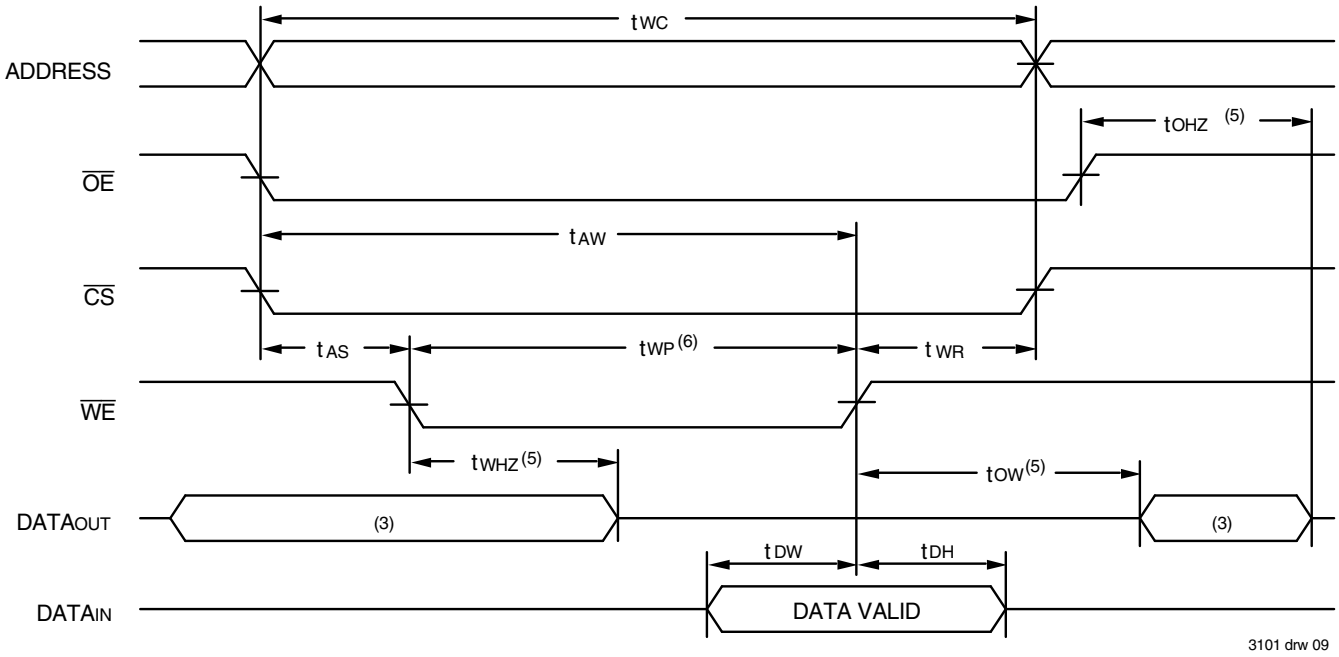



## Timing Waveform of Read Cycle No. 3(1,3,4)



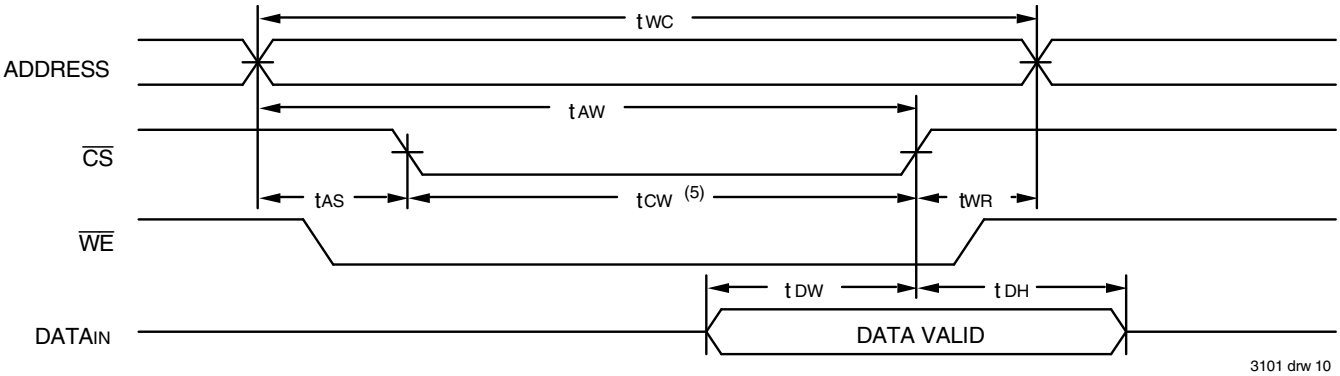

**NOTES:**
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

## Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1,2,4,6)



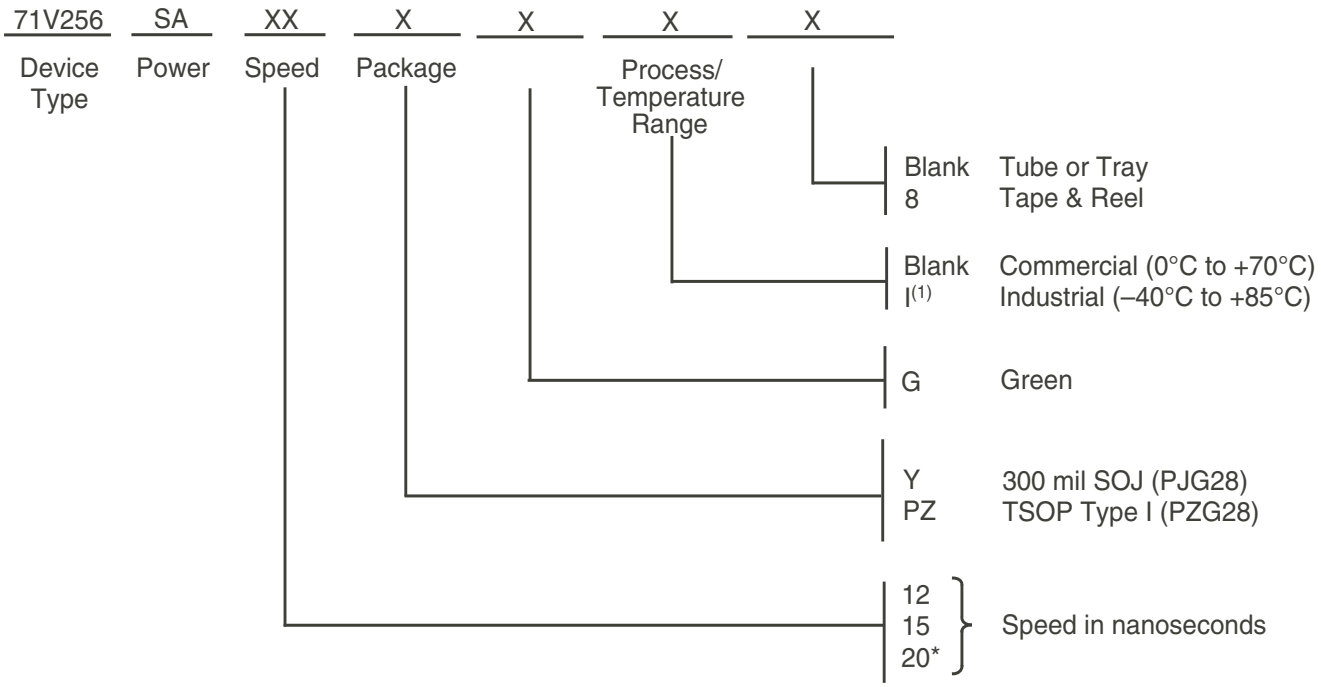

**NOTES:**
1. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
2. $t_{WR}$ is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
3. During this period, I/O pins are in the output state so that the input signals must not be applied.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured ±200mV from steady state.
6. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of $t_{WP}$ or ($t_{WHZ}$ + $t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required $t_{DW}$. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified $t_{WP}$.

## Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1,2,3,4)




**NOTES:**
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $t_{WR}$ is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of $t_{WP}$ or ($t_{WHZ}$ + $t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required $t_{DW}$. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified $t_{WP}$.

## Ordering Information




* Available in TSOP package only.

3101 drw 11

**NOTE:**
1. Contact your local sales office for industrial temp. range for other speeds, packages and powers.

## Orderable Part Information

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|---|---|---|---|---|
| 12 | 71V256SA12PZG | PZG28 | TSOP | C |
| | 71V256SA12PZG8 | PZG28 | TSOP | C |
| | 71V256SA12PZGI | PZG28 | TSOP | I |
| | 71V256SA12PZGI8 | PZG28 | TSOP | I |
| | 71V256SA12YG | PJG28 | SOJ | C |
| | 71V256SA12YG8 | PJG28 | SOJ | C |
| | 71V256SA12YGI | PJG28 | SOJ | I |
| | 71V256SA12YGI8 | PJG28 | SOJ | I |
| 15 | 71V256SA15PZG | PZG28 | TSOP | C |
| | 71V256SA15PZG8 | PZG28 | TSOP | C |
| | 71V256SA15PZGI | PZG28 | TSOP | I |
| | 71V256SA15PZGI8 | PZG28 | TSOP | I |
| | 71V256SA15YG | PJG28 | SOJ | C |
| | 71V256SA15YG8 | PJG28 | SOJ | C |
| | 71V256SA15YGI | PJG28 | SOJ | I |
| | 71V256SA15YGI8 | PJG28 | SOJ | I |
| 20 | 71V256SA20PZG | PZG28 | TSOP | C |
| | 71V256SA20PZG8 | PZG28 | TSOP | C |
| | 71V256SA20PZGI | PZG28 | TSOP | I |
| | 71V256SA20PZGI8 | PZG28 | TSOP | I |

# Datasheet Document History

| | | |
|---|---|---|
| 1/7/00 | | Updated to new format |
| | Pg. 1, 3, 4, 7 | Expanded Industrial Temperature offerings |
| | Pg. 1, 2, 7 | Removed 28-pin 300 mil plastic DIP package offering |
| | Pg. 6 | Removed Note No. 1 from Write Cycle No. 1 diagram; renumbered notes and footnotes |
| | Pg. 7 | Revised Ordering Information |
| | Pg. 8 | Added Datasheet Document History |
| 08/09/00 | | Not recommended for new designs |
| 02/01/01 | | Removed "Not recommended for new designs" |
| 06/21/02 | Pg. 7 | Added tape and reel option to the ordering information |
| 01/30/04 | Pg. 7 | Added "restricted hazardous substance device" to order information. |
| 02/20/09 | Pg. 7 | Removed "IDT" from ordering parts |
| 06/11/12 | Pg. 3 | Corrected Recommended DC Operation Conditions Max $V_{IH}$ from 5.0 to Vcc+0.3V |
| | Pg. 7 | Added Green designator to ordering information |
| | Pg. 7 | Corrected footnote in the ordering information from "available in SOJ package only" to "available in TSOP package only" |
| 07/24/14 | Pg.7 | Added tube or tray to the ordering information |
| 08/18/15 | Pg.1 & 7 | Removed commercial 10ns speed offering & added green parts available to features |
| | Pg.2 & 7 | Removed "-X"extensions from all pin configurations SOJ28 & TSOP28 |
| | Pg. 3 & 4 | Removed commercial 10ns speed offering columns from the DC & AC Elec tables |
| | Pg.7 | Updated the Industrial and Green footnotes in the Ordering Information |
| 06/02/20 | Pg.1 - 9 | Rebranded as Renesas datasheet |
| | Pg.2 & 7 | Updated package codes |
| | Pg.7 | Added Orderable Part Information |

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