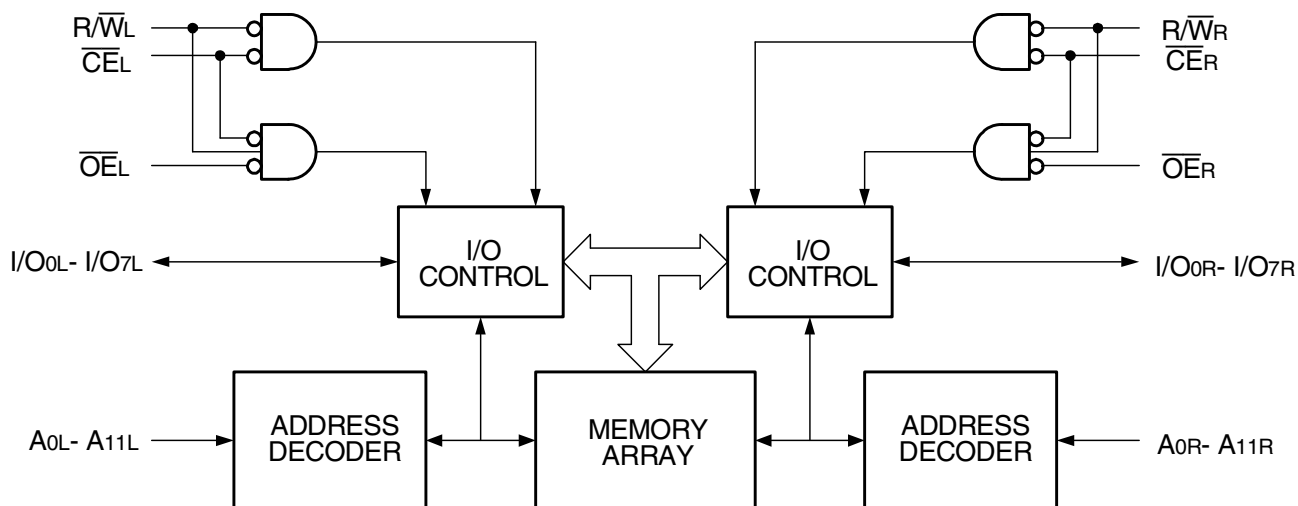


Features

- ◆ **High-speed access**
 - Commercial: 20/55ns (max.)
 - Industrial: 25ns (max.)
 - Military: 35/45/55/70ns (max.)
- ◆ **Low-power operation**
 - IDT7134SA
Active: 700mW (typ.)
Standby: 5mW (typ.)
 - IDT7134LA
Active: 700mW (typ.)
Standby: 1mW (typ.)
- ◆ Fully asynchronous operation from either port
- ◆ Battery backup operation—2V data retention (LA only)
- ◆ TTL-compatible; single 5V (±10%) power supply
- ◆ Available in 48-pin DIP, LCC, Flatpack and 52-pin PLCC
- ◆ Military product compliant to MIL-PRF-38535 QML
- ◆ Industrial temperature range (–40°C to +85°C) is available for selected speeds
- ◆ Green parts available, see ordering information

Functional Block Diagram



2720 drw 01

Description

The IDT7134 is a high-speed 4K x 8 Dual-Port Static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same Dual-Port RAM location.

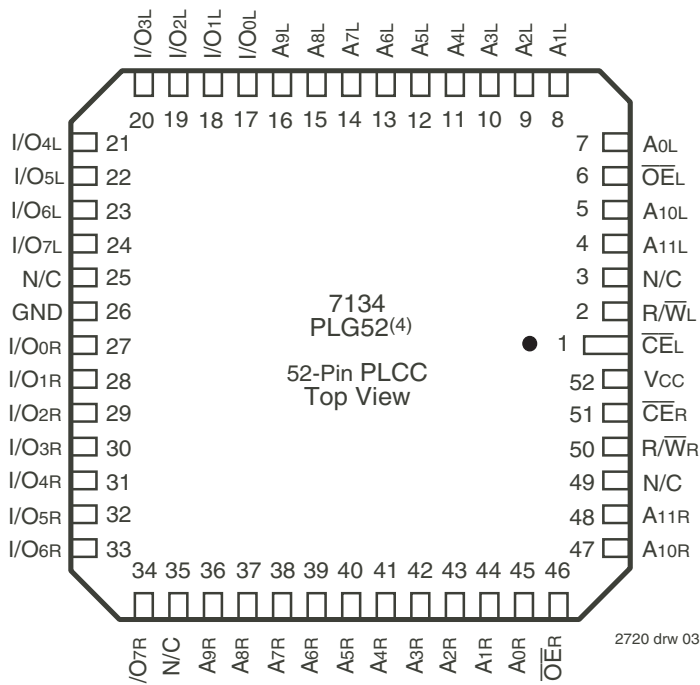
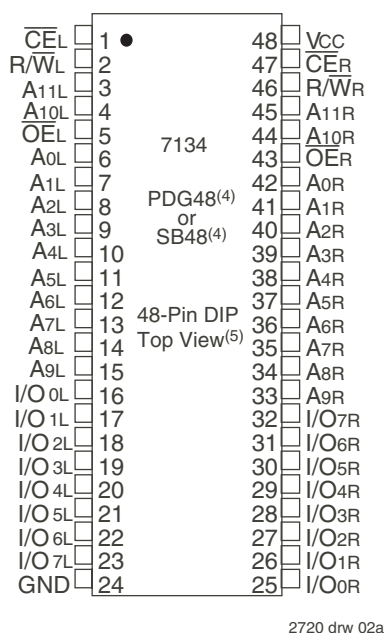
The IDT7134 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature,

controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using CMOS high-performance technology, these Dual-Ports typically operate on only 700mW of power. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200 μ W from a 2V battery.

The IDT7134 is packaged in either a sidebrazed or plastic 48-pin DIP, 48-pin LCC, 52-pin PLCC and 48-pin Flatpack. Military grade product is manufactured in compliance with MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

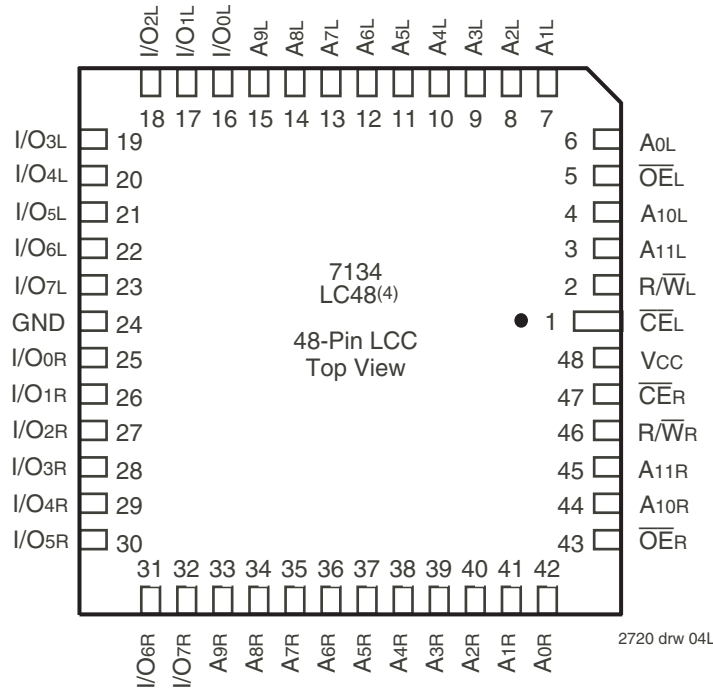
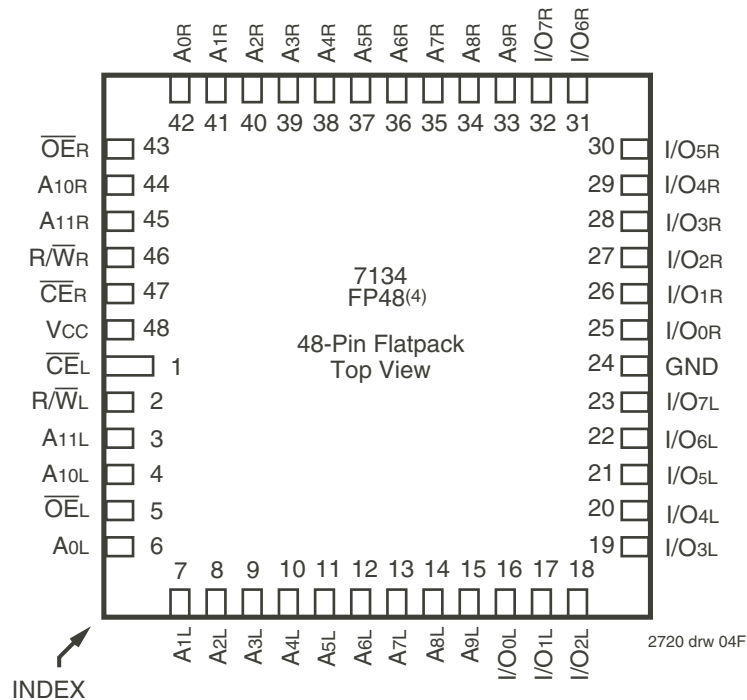
Pin Configurations^(1,2,3)



NOTES:

1. All VCC pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. PDG48 package body is approximately .55 in x 2.43 in x .18 in.
SB48 package body is approximately .62 in x 2.43 in x .15 in.
PLG52 package body is approximately .75 in x .75 in x .17 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of actual part-marking.

Pin Configurations ^(1,2,3)(con't.)



NOTES:

1. All VCC pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. LC48 package body is approximately .57 in x .57 in x .68 in.
FP48 package body is approximately .75 in x .75 in x .11 in.
4. This package code is used to reference the package diagram.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-65 to +150	-65 to +150	°C
P _T ⁽³⁾	Power Dissipation	1.5	1.5	W
I _{OUT}	DC Output Current	50	50	mA

2720 tbl 01

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{CC} + 10% for more than 25% of the cycle time or 10 ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ V_{CC} + 10%.
- V_{TERM} = 5.5V.

Capacitance⁽¹⁾ (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	11	pF
C _{OUT}	Output Capacitance	V _{OUT} = 3dV	11	pF

2720 tbl 02

NOTES:

- This parameter is determined by device characterization but is not production tested.
- 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V and from 3V to 0V.

Recommended Operating Temperature and Supply Voltage^(1,2)

Grade	Ambient Temperature	GND	V _{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

2720 tbl 03

NOTES:

- This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0 ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

2720 tbl 04

NOTES:

- V_{IL} (min.) ≥ -1.5V for pulse width less than 10ns.
- V_{TERM} must not exceed V_{CC} + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Conditions	7134SA		7134LA		Unit
			Min.	Max.	Min.	Max.	
I _{LI}	Input Leakage Current ⁽¹⁾	V _{CC} = 5.5V, V _{IN} = 0V to V _{CC}	—	10	—	5	μA
I _{LO}	Output Leakage Current	$\overline{CE}$ - V _{IH} , V _{OUT} = 0V to V _{CC}	—	10	—	5	μA
V _{OL}	Output Low Voltage	I _{OL} = 6mA	—	0.4	—	0.4	V
		I _{OL} = 8mA	—	0.5	—	0.5	V
V _{OH}	Output High Voltage	I _{OH} = -4mA	2.4	—	2.4	—	V

2720 tbl 05

NOTES:

- At V_{CC} ≤ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(1,2) ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Condition	Version		7134X20 Com'l Only		7134X25 Com'l & Ind		7134X35 Com'l & Military		Unit
					Typ.	Max.	Typ.	Max.	Typ.	Max.	
I _{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$ Outputs Disabled $f = f_{MAX}^{(3)}$	COM'L	SA LA	170 170	280 240	160 160	280 220	150 150	260 210	mA
			MIL & IND	SA LA	— —	— —	160 160	310 260	150 150	300 250	
I _{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(3)}$	COM'L	SA LA	25 25	100 80	25 25	80 50	25 25	75 45	mA
			MIL & IND	SA LA	— —	— —	25 25	100 80	25 25	75 55	
I _{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^{A*} = V_{IL}$ and $\overline{CE}^{B*} = V_{IH}$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$	COM'L	SA LA	105 105	180 150	95 95	180 140	85 85	170 130	mA
			MIL & IND	SA LA	— —	— —	95 95	210 170	85 85	200 160	
I _{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(3)}$	COM'L	SA LA	1.0 0.2	15 4.5	1.0 0.2	15 4.0	1.0 0.2	15 4.0	mA
			MIL & IND	SA LA	— —	— —	1.0 0.2	30 10	1.0 0.2	30 10	
I _{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	One Port $\overline{CE}^{A*}$ or $\overline{CE}^{B*} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$	COM'L	SA LA	105 105	170 130	95 95	170 120	85 85	160 110	mA
			MIL & IND	SA LA	— —	— —	95 95	210 150	85 85	190 130	

2720 tbl 06a

				7134X45 Com'l & Military		7134X55 Com'l, Ind & Military		7134X70 Com'l & Military			
Symbol	Parameter	Test Condition	Version		Typ.	Max.	Typ.	Max.	Typ.	Max.	Unit
I _{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$ Outputs Disabled $f = f_{MAX}^{(3)}$	COM'L	SA	140	240	140	240	140	240	mA
				LA	140	200	140	200	140	200	
			MIL &	SA	140	280	140	270	140	270	
			IND	LA	140	240	140	220	140	220	
I _{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(3)}$	COM'L	SA	25	70	25	70	25	70	mA
				LA	25	40	25	40	25	40	
			MIL &	SA	25	70	25	70	25	70	
			IND	LA	25	50	25	50	25	50	
I _{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^{A*} = V_{IL}$ and $\overline{CE}^{B*} = V_{IH}$ Active Port Outputs Disabled, $f=f_{MAX}^{(3)}$	COM'L	SA	75	160	75	160	75	160	mA
				LA	75	130	75	130	75	130	
			MIL &	SA	75	190	75	180	75	180	
			IND	LA	75	150	75	150	75	150	
I _{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(3)}$	COM'L	SA	1.0	15	1.0	15	1.0	15	mA
				LA	0.2	4.0	0.2	4.0	0.2	4.0	
			MIL &	SA	1.0	30	1.0	30	1.0	30	
			IND	LA	0.2	10	0.2	10	0.2	10	
I _{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	One Port $\overline{CE}^{A*}$ or $\overline{CE}^{B*} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$	COM'L	SA	75	150	75	150	75	150	mA
				LA	75	100	75	100	75	100	
			MIL &	SA	75	180	75	170	75	170	
			IND	LA	75	120	75	120	75	120	

2720 tbl 06b

NOTES:

- 'X' in part number indicates power rating (SA or LA).
- $V_{CC} = 5V$, $T_A = +25^\circ C$ for typical, and parameters are not production tested.
- $f_{MAX} = 1/t_{RC} =$ All inputs cycling at $f = 1/t_{RC}$ (except Output Enable). $f = 0$ means no address or control lines change. Applies only to inputs at CMOS level standby I_{SB3}.

Data Retention Characteristics Over All Temperature Ranges

(LA Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

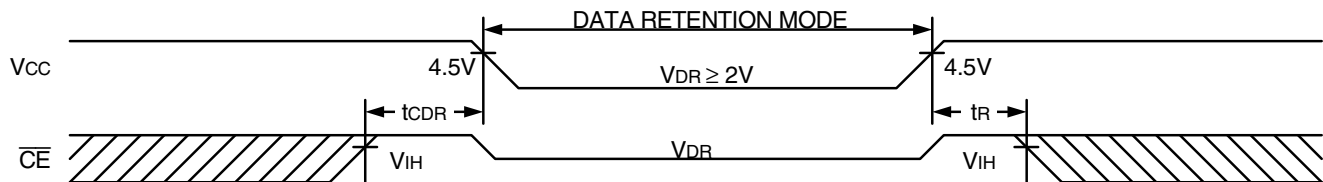
Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	V _{CC} for Data Retention	$V_{CC} = 2V$	2.0	—	—	V
I _{CDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL. & IND. —	100	4000	μA
			COM'L. —	100	1500	
t _{CDR} ⁽³⁾	Chip Deselect to Data Retention Time		0	—	—	ns
t _R ⁽³⁾	Operation Recovery Time		t _{RC} ⁽²⁾	—	—	ns

2720 tbl 07

NOTES:

1. $V_{CC} = 2V$, $T_A = +25^\circ C$, and are not production tested.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but not production tested.

Data Retention Waveform

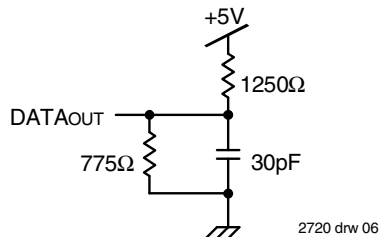


2720 drw 05

AC Test Conditions

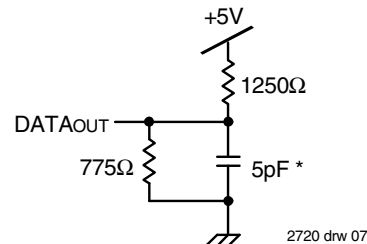
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2720 tbl 08



2720 drw 06

Figure 1. AC Output Test Load



2720 drw 07

Figure 2. Output Test Load
(for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
*Including scope and jig

AC Electrical Characteristics Over the
Operating Temperature and Supply Voltage⁽³⁾

Symbol	Parameter	7134X20 Com'l Only		7134X25 Com'l & Ind		7134X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	20	—	25	—	35	—	ns
tAA	Address Access Time	—	20	—	25	—	35	ns
tACE	Chip Enable Access Time	—	20	—	25	—	35	ns
tAOE	Output Enable Access Time	—	15	—	15	—	20	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	ns
tLZ	Output Low-Z Time ^(1,2)	0	—	0	—	0	—	ns
tHZ	Output High-Z Time ^(1,2)	—	15	—	15	—	20	ns
tPU	Chip Enable to Power Up Time ⁽²⁾	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time ⁽²⁾	—	20	—	25	—	35	ns

2720 tbl 09a

Symbol	Parameter	7134X45 Com'l & Military		7134X55 Com'l, Ind & Military		7134X70 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t _{AA}	Address Access Time	—	45	—	55	—	70	ns
t _{ACE}	Chip Enable Access Time	—	45	—	55	—	70	ns
t _{AOE}	Output Enable Access Time	—	25	—	30	—	40	ns
t _{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t _{LZ}	Output Low-Z Time ^(1,2)	5	—	5	—	5	—	ns
t _{HZ}	Output High-Z Time ^(1,2)	—	20	—	25	—	30	ns
t _{PU}	Chip Enable to Power Up Time ⁽²⁾	0	—	0	—	0	—	ns
t _{PD}	Chip Disable to Power Down Time ⁽²⁾	—	45	—	50	—	50	ns

2720 tbl 09b

NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. 'X' in part number indicates power rating (SA or LA).

Timing diagram for the 2720 device showing ADDRESS and DATAout signals. The diagram illustrates the relationship between the address valid period (t_{rc}), the data output valid period ($t_{AA}^{(5)}$), and the data output delay (t_{oH}).

The ADDRESS signal is shown as a horizontal line. The DATAout signal is shown as a horizontal line. The data output is shown as a signal that becomes valid after the address is valid and remains valid until the address is no longer valid. The data output is shown as a signal that becomes valid after the address is valid and remains valid until the address is no longer valid. The data output is shown as a signal that becomes valid after the address is valid and remains valid until the address is no longer valid.

Labels in the diagram include:

- ADDRESS
- DATAout
- PREVIOUS DATA VALID
- DATA VALID
- t_{rc}
- $t_{AA}^{(5)}$
- t_{oH}

2720 drw 08

The timing diagram shows the following signals and their transitions:

- CE (Chip Enable):** Transitions from high to low at the start of the read cycle and back to high at the end. Setup time t_{ACE} is the time before the falling edge of CE that DATAOUT must be valid. Hold time t_{HCE} is the time after the rising edge of CE that DATAOUT must remain valid.
- OE (Output Enable):** Transitions from high to low to enable the output and back to high to disable it. Setup time $t_{AOE}^{(4)}$ is the time before the falling edge of OE that DATAOUT must be valid. Hold time $t_{HOE}^{(4)}$ is the time after the rising edge of OE that DATAOUT must remain valid.
- DATAOUT:** The data bus output. It shows a period of "VALID DATA⁽⁴⁾" during which the data is stable and valid. The output is in a high-impedance state (indicated by a hatched box) when both CE and OE are high.
- ICC (Supply Current):** Transitions from a low level to a high level when the device is enabled. The transition time is t_{PU} (turn-on time).
- ISB (Standby Current):** Transitions from a high level to a low level when the device is disabled. The transition time is t_{PD} (turn-off time).
- Current Levels:** The high level for ICC is labeled "50%", and the low level for ISB is also labeled "50%".
- Other Timing Parameters:**
 - $t_{LZ}^{(1)}$: Time from the falling edge of CE to the output becoming high-impedance.
 - $t_{LZ}^{(1)}$: Time from the falling edge of OE to the output becoming high-impedance.
 - $t_{HZ}^{(2)}$: Time from the rising edge of OE to the output becoming high-impedance.

2720 drw 09

1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. $R/\overline{W} = V_{IH}$.
4. Start of valid data depends on which timing becomes effective, t_{AOE} , t_{ACE} or t_{AA}
5. t_{AA} for RAM Address Access and t_{sAA} for Semaphore Address Access.

AC Electrical Characteristics Over the
Operating Temperature and Supply Voltage⁽⁵⁾

Symbol	Parameter	7134X20 Com'l Only		7134X25 Com'l & Ind		7134X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	20	—	25	—	35	—	ns
tEW	Chip Enable to End-of-Write	15	—	20	—	30	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	30	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	25	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	15	—	20	—	ns
tHZ	Output High-Z Time ^(1,2)	—	15	—	15	—	20	ns
tDH	Data Hold Time ⁽³⁾	0	—	0	—	3	—	ns
tWZ	Write Enable to Output in High-Z ^(1,2)	—	15	—	15	—	20	ns
tOW	Output Active from End-of-Write ^(1,2,3)	3	—	3	—	3	—	ns
tWDD	Write Pulse to Data Delay ⁽⁴⁾	—	40	—	50	—	60	ns
tDDD	Write Data Valid to Read Data Delay ⁽⁴⁾	—	30	—	30	—	35	ns

2720 tbl 10a

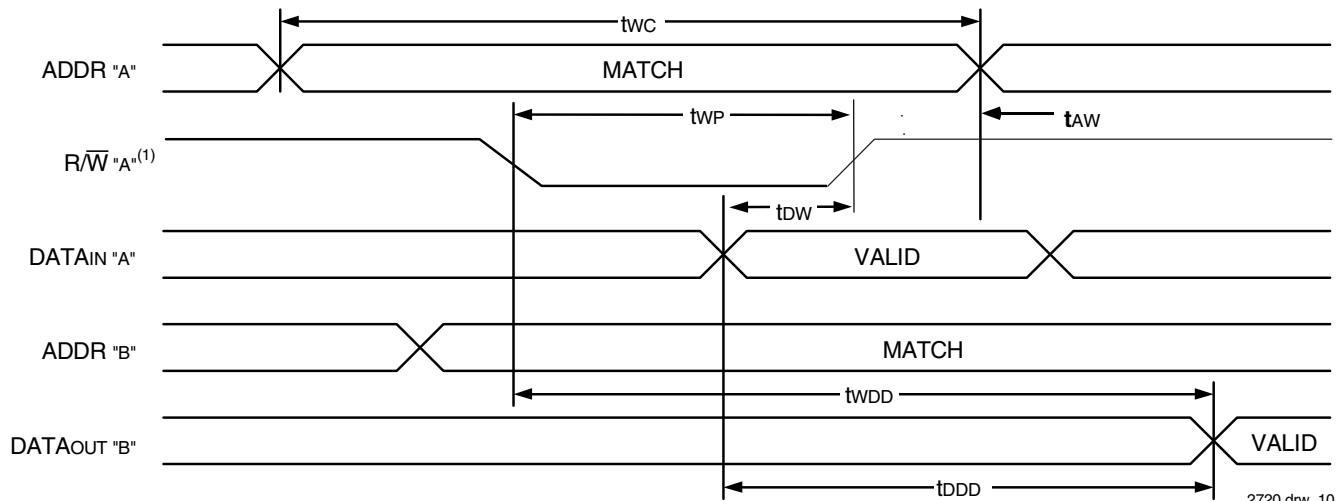
Symbol	Parameter	7134X45 Com'l & Military		7134X55 Com'l, Ind & Military		7134X70 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t _{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t _{EW}	Chip Enable to End-of-Write	40	—	50	—	60	—	ns
t _{AW}	Address Valid to End-of-Write	40	—	50	—	60	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	40	—	50	—	60	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t _{DW}	Data Valid to End-of-Write	20	—	25	—	30	—	ns
t _{HZ}	Output High-Z Time ^(1,2)	—	20	—	25	—	30	ns
t _{DH}	Data Hold Time ⁽³⁾	3	—	3	—	3	—	ns
t _{WZ}	Write Enable to Output in High-Z ^(1,2)	—	20	—	25	—	30	ns
t _{OW}	Output Active from End-of-Write ^(1,2,3)	3	—	3	—	3	—	ns
t _{WDD}	Write Pulse to Data Delay ⁽⁴⁾	—	70	—	80	—	90	ns
t _{DDD}	Write Data Valid to Read Data Delay ⁽⁴⁾	—	45	—	55	—	70	ns

2720 tbl 10b

NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read".
5. 'X' in part number indicates power rating (SA or LA).

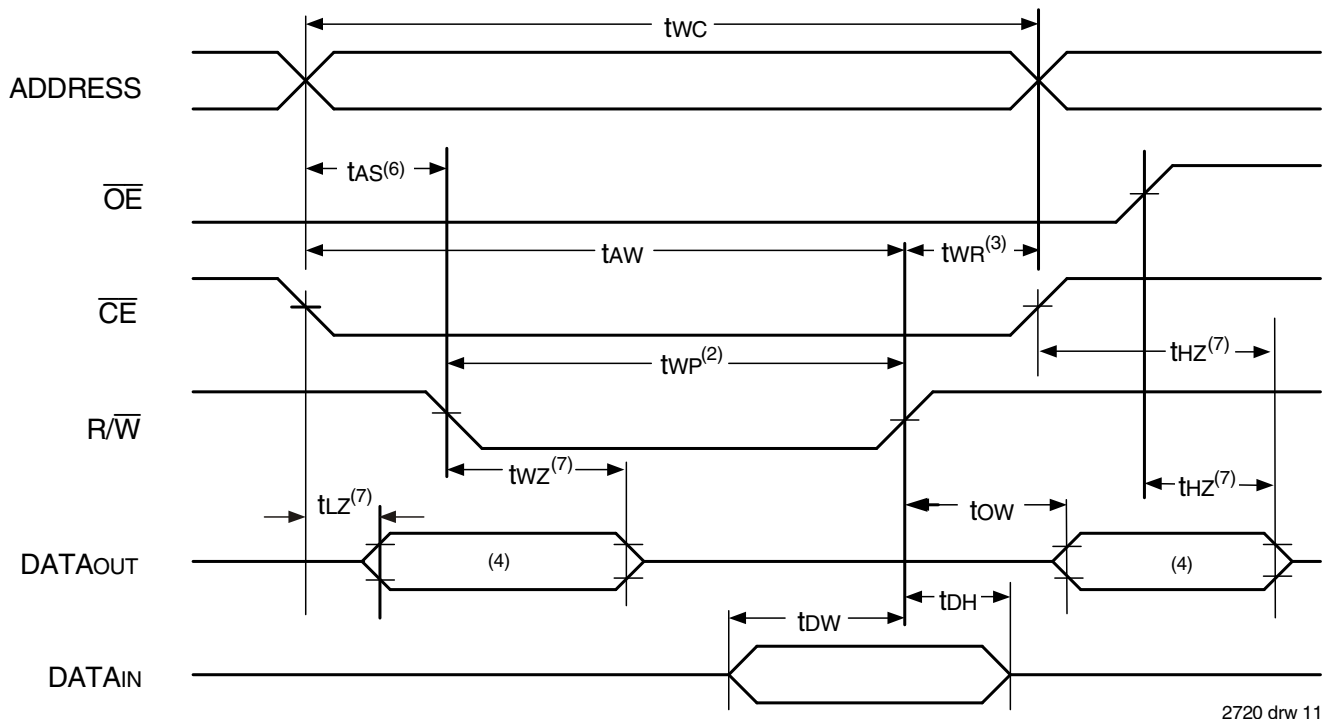
Timing Waveform of Write with Port-to-Port Read^(1,2,3)



NOTES:

1. Write cycle parameters should be adhered to, in order to ensure proper writing.
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$, $\overline{OE}_B = V_{IL}$.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

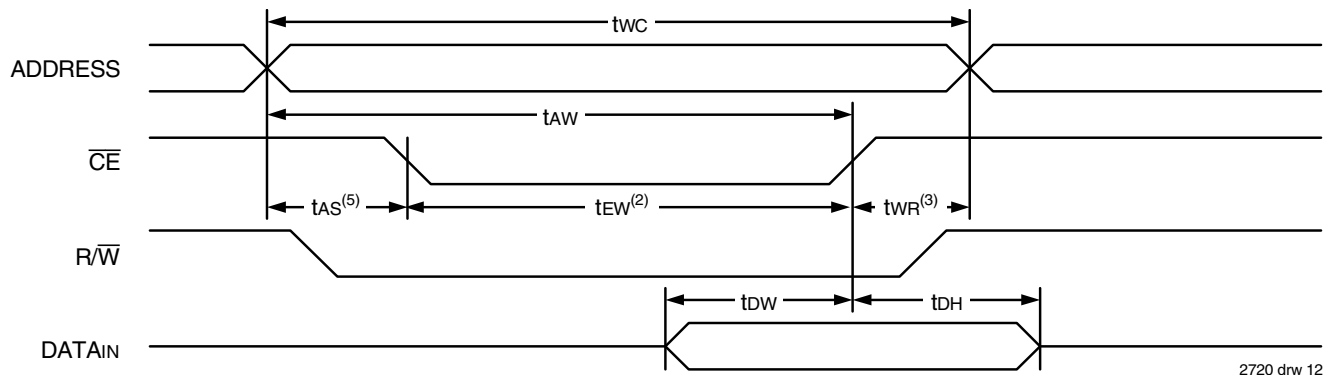
Timing Waveform of Write Cycle No. 1, $R/\overline{W}$ Controlled Timing^(1,5,8)



NOTES:

1. $R/\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE} = V_{IL}$ and $R/\overline{W} = V_{IL}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or $R/\overline{W}$ going to V_{IH} to the end-of-write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE} = V_{IL}$ transition occurs simultaneously with or after the $R/\overline{W} = V_{IL}$ transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or $R/\overline{W}$) is asserted last.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE} = V_{IL}$ during a $R/\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WZ} + t_{OW})$ to allow the I/O drivers to turn off data to be placed on the bus for the required t_{OW} . If $\overline{OE} = V_{IH}$ during an $R/\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

Timing Waveform of Write Cycle No. 2, $\overline{\text{CE}}$ Controlled Timing^(1,4)



2720 drw 12

NOTES:

1. $\overline{\text{R/W}}$ or $\overline{\text{CE}}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{\text{CE}} = \text{V}_{\text{IL}}$ and $\overline{\text{R/W}} = \text{V}_{\text{IL}}$.
3. t_{WR} is measured from the earlier of $\overline{\text{CE}}$ or $\overline{\text{R/W}}$ going HIGH to the end-of-write cycle.
4. If the $\overline{\text{CE}}$ LOW transition occurs simultaneously with or after the $\overline{\text{R/W}}$ LOW transition, the outputs remain in the High-impedance state.
5. Timing depends on which enable signal ($\overline{\text{CE}}$ or $\overline{\text{R/W}}$) is asserted last.

Functional Description

The IDT7134 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{\text{CE}}$. The $\overline{\text{CE}}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{\text{CE}}$ HIGH). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{\text{OE}}$). In the read mode, the port's $\overline{\text{OE}}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Truth Table I.

Truth Table I – Read/Write Control

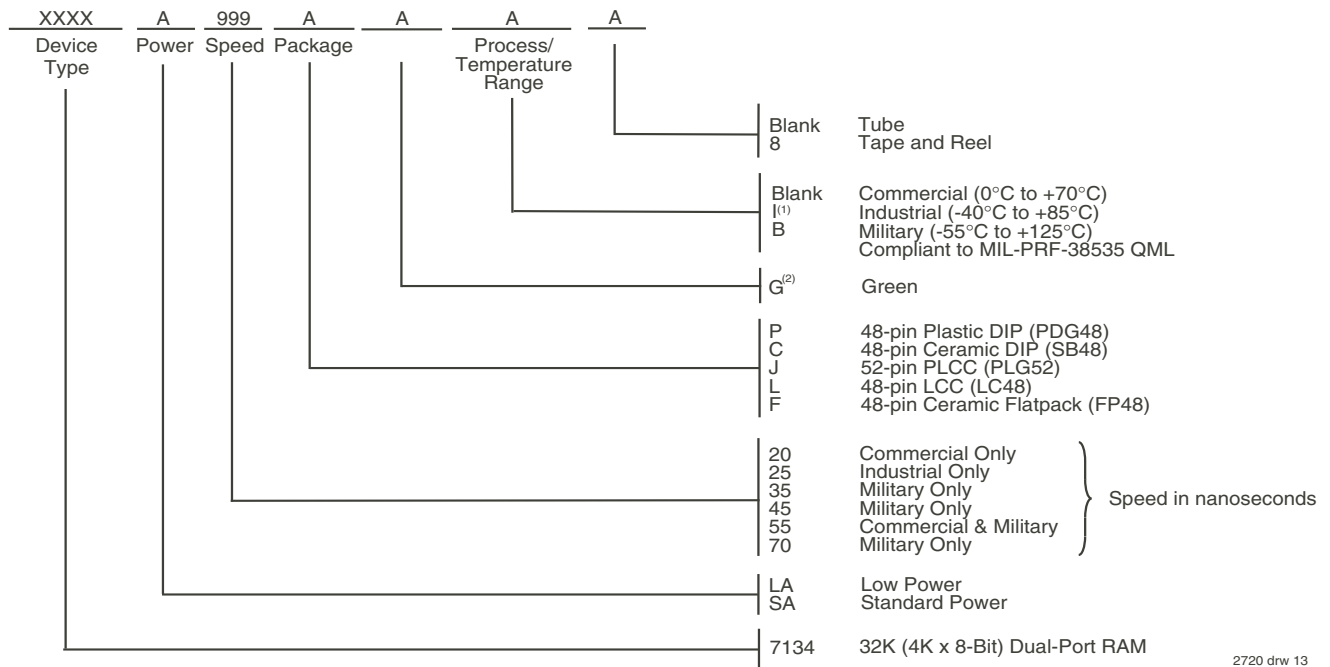
Left or Right Port ⁽¹⁾				
$\overline{\text{R/W}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	D0-7	Function
X	H	X	Z	Port Deselected and in Power-Down Mode, ISB2 or ISB4
X	H	X	Z	$\overline{\text{CE}}_{\text{R}} = \overline{\text{CE}}_{\text{L}} = \text{H}$, Power Down Mode ISB1 or ISB3
L	L	X	DATA _{IN}	Data on port written into memory
H	L	L	DATA _{OUT}	Data in memory output on port
X	X	H	Z	High impedance outputs

2720 tbl 11

NOTE:

1. A0L - A11L $\neq$ A0R - A11R
"H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care, and "Z" = High Impedance

Ordering Information



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NOTES:

- Contact your local sales office for industrial temp. range for other speeds, packages and powers.
 - Green parts available. For specific speeds, packages and powers contact your local sales office.
- LEAD FINISH (SnPb) parts are Obsolete excluding FP48, LC48 & SB48. Product Discontinuation Notice - PDN# SP-17-02
Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
20	7134LA20JG	PLG52	PLCC	C
	7134LA20JG8	PLG52	PLCC	C
	7134LA20PDG	PDG48	PDIP	C
25	7134LA25JGI	PLG52	PLCC	I
	7134LA25JGI8	PLG52	PLCC	I
	7134LA25PDGI	PDG48	PDIP	I
35	7134LA35CB	SB48	SB	M
	7134LA35FB	FP48	FPACK	M
	7134LA35L48B	LC48	LCC	M
45	7134LA45CB	SB48	SB	M
55	7134LA55CB	SB48	SB	M
	7134LA55L48B	LC48	LCC	M
70	7134LA70CB	SB48	SB	M
	7134LA70L48B	LC48	LCC	M

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
35	7134SA35CB	SB48	SB	M
	7134SA35L48B	LC48	LCC	M
45	7134SA45CB	SB48	SB	M
55	7134SA55CB	SB48	SB	M
	7134SA55JG	PLG52	PLCC	C
	7134SA55JG8	PLG52	PLCC	C
	7134SA55L48B	LC48	LCC	M
70	7134SA70CB	SB48	SB	M
	7134SA70L48B	LC48	LCC	M

Datasheet Document History

03/25/99:		Initiated datasheet document history
		Converted to new format
		Cosmetic and typographical corrections
	Pages 2	Added additional notes to pin configurations
06/09/99:		Changed drawing format
10/01/99:		Added Industrial Temperature Ranges and removed corresponding notes
11/10/99:		Replaced IDT logo
12/22/99:	Page 1	Made corrections to drawing
03/03/00:		Corrected block diagram and pin configurations
		Changed $\pm 500\text{mV}$ to 0mV
01/12/00:	Pages 1 2	Moved "Description to page 2 and adjusted page layout
	Page 1	Added "LA only)" to paragraph
	Page 2	Fixed P48-1 package description
	Page 3	Increased storage temperature parameters
		Clarified TA parameter
	Page 4	DC Electrical parameters—changed wording from "open" to "disabled"
	Page 10	Fixed Truth Table specification in "Functional Description" paragraph
01/17/06:	Page 1	Added green availability to features
	Page 11	Added green indicator to ordering information
	Page 1 & 11	Replaced old IDT™ with new IDT™ logo
08/12/08:	Page 11	Corrected typo in the ordering information
10/21/08:	Page 11	Removed "IDT" from orderable part number
01/16/13:	Page 1, 4, 6 & 8	Removed Military 25ns & Industrial 35ns speed grades from Features and corrected the headers of the DC Chars and AC Chars tables to indicate this change
	Page 11	Added T & R indicator to and removed Military 25ns & Industrial 35ns speed grades from the ordering information
10/21/08:	Page 11	Removed "IDT" from orderable part number
02/04/13:	Page 1, 4, 6 & 8	Removed Military 25ns & Industrial 35ns speed grades from Features and corrected the headers of the DC Chars and AC Chars tables to indicate this change
	Page 11	Added T & R indicator to and removed Military 25ns & Industrial 35ns speed grades from the ordering information
	Page 2	Typo/correction
01/11/18:		Product Discontinuation Notice - PDN# SP-17-02
		Last time buy expires June 15, 2018
05/10/21:	Pages 1 - 14	Rebranded as Renesas datasheet
	Page 2 & 3	Rotated LC48 LCC, FP48 Flatpack & PLG52 PLCC to accurately reflect pin 1 orientation
	Page 2, 3 & 12	Updated package codes
	Page 12	Added Orderable Part Information tables

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